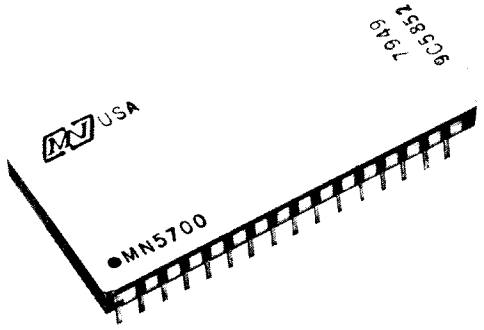
# MN5700

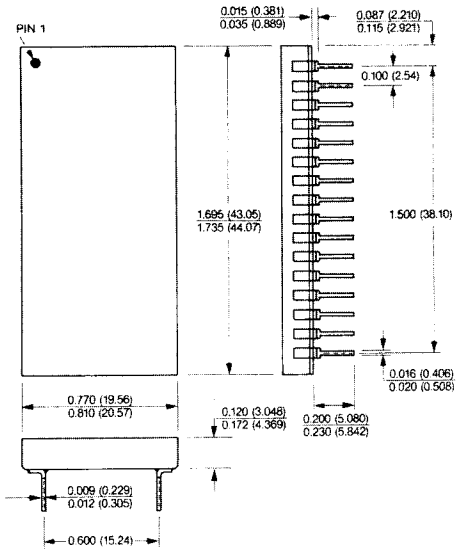
200°C 12 BIT
A/D CONVERTER




## FEATURES

- **−55°C to +200°C Guaranteed Performance**
- **Max Linearity Error ±0.05%FSR at +200°C**
- **Max Accuracy Error ±1%FSR at +200°C**
- **Low Power 311mW**
- **Internal Reference**
- **250 μsec Conversion Time**
- **LPTTL-CMOS Compatible**

**32 PIN DIP**




**Dimensions in inches (millimeters)**

## DESCRIPTION

The MN5700 is a complete, Dual-in-Line packaged, 12 Bit Successive Approximation A/D Converter designed and fully specified for continuous operation at +200°C (ambient). This thin-film hybrid employs a low-power CMOS switching network, a proprietory discrete comparator, Micro Networks ultra-stable thin-film nichrome resistor networks, and a proprietory three-metal interconnect system all selected and designed for +200°C operation. The MN5700's low power consumption and the excellent stability of the comparator, the resistor networks, and the device's internal reference combine to guarantee better than ±0.05%FSR linearity and better than ±1%FSR absolute accuracy at +200°C without the use of external trimming potentiometers.

Other features include 4 user-selectable input ranges (0 to −10V, 0 to −20V, ±5V, and ±10V), 250 μsec conversion time, and 311 mW power consumption.

## APPLICATIONS

The MN5700 is the first extended temperature range A/D designed for down-hole instrumentation systems and the most demanding industrial applications. Its ability to withstand high temperatures makes it well suited for oil well logging, geothermal probing, and jet engine, nuclear reactor, oil refinery, and chemical process monitoring. Transducer outputs can be digitized locally and digitally transmitted without signal degradation. Performance specifications are fully tested and guaranteed at +200°C to assure field interchangeability without the need for readjustment. Highly reliable thin-film hybrid construction assures a product lifetime compatible with that of other presently available 200°C components.

**Micro Networks**
A DIVISION OF UNITRODE CORPORATION
324 Clark Street, Worcester, MA 01606 • Tel: (617) 852-5400

# MN5700 200°C 12 BIT A/D CONVERTER

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Operating Temperature Range | −55°C to +200°C |
| Storage Temperature Range | −65°C to +150°C |
| +15V Supply (+Vcc, Pin 12) | −0.5 to +18 Volts |
| −15V Supply (−Vcc, Pin 21) | +0.5 to −18 Volts |
| +5V Supply (+Vdd, Pin 20) | −0.5 to +16 Volts |
| Analog Input (Pins 10 and 11) | ±25 Volts |
| Digital Inputs (Pins 1, 2) | −0.3 to +Vdd Volts |

**SPECIFICATIONS (TA = +25°C, Supply Voltages ±15V and +5V, unless otherwise specified).**

| | | | | | |
|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | |
| Input Voltage Ranges: | | 0 to −10, −20; ±5, ±10 | | | Volts |
| Input Impedance: 0 to −10V, ±5V | | | 25 | | kΩ |
| 0 to −20V, ±10V | | | 50 | | kΩ |
| **DIGITAL INPUTS (Note 1)** | | | | | |
| Logic Levels (Note 2): Logic "1" | +5V | 3.5 | | | Volts |
| | +10V | 8.0 | | | Volts |
| Logic "0" | +5V | | | 1.5 | Volts |
| | +10V | | | 2.0 | Volts |
| Input Loading: Logic "1" (Vin = 15V) | | | 0.005 | 1.0 | μA |
| Logic "0" (Vin = 0V) | | −1.0 | −0.005 | | μA |
| Input Capacitance: Clock Input | | | 10 | | pF |
| Start Convert Input | | | 5 | | pF |
| Clock Input: Pulse Width (Note 3) | +5V | 250 | | | nsec |
| | +10V | 100 | | | nsec |
| Rise and Fall Times (Note 3) | +5V | | | 15 | μsec |
| | +10V | | | 5 | μsec |
| Frequency (Note 4) | | 34 | 48 | | kHz |
| Start Input: Pulse Width | | 100 | | | nsec |
| Setup Time Start Low to Clock | +5V | 80 | | | nsec |
| | +10V | 30 | | | nsec |
| **TRANSFER CHARACTERISTICS (Note 5)** | | | | | |
| Linearity Error (Notes 5, 6, 7): +25°C | | | ±0.005 | ±0.012 | %FSR |
| −55°C to +200°C | | | ±0.025 | ±0.05 | %FSR |
| Differential Linearity Error | | | ±½ | | LSB |
| No Missing Codes for 12 Bits (Note 8) | | | Guaranteed | | |
| Full Scale Absolute Accuracy Error (Note 9): | | | | | |
| +25°C | | | ±0.05 | ±0.15 | %FSR |
| −55°C to +200°C | | | ±0.5 | ±1.0 | %FSR |
| Zero Error (Note 10): +25°C | | | ±0.05 | ±0.1 | %FSR |
| −55°C to +200°C | | | ±0.3 | ±0.5 | %FSR |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Conversion Time (Note 4) | | | 250 | 350 | μsec |
| Propagation Delay From Clock to Serial Output Valid (Note 11) | +5V | | 180 | 325 | nsec |
| | +10V | | 70 | 125 | nsec |
| Propagation Delay From Resetting Clock Edge to Status High | +5V | | 190 | 350 | nsec |
| | +10V | | 75 | 150 | nsec |
| Propagation Delay From Status Low to LSB Valid | +5V | | | 250 | nsec |
| | +10V | | | 100 | nsec |
| **DIGITAL OUTPUTS** | | | | | |
| Logic Coding (Note 11): Unipolar Ranges | | Complementary Straight Binary | | | |
| Bipolar Ranges | | Complementary Offset Binary | | | |
| Logic Levels: Logic "1" $I_O = -10\mu A$ | +5V | 4.0 | | | Volts |
| $I_O = -10\mu A$ | +10V | 8.5 | | | Volts |
| $I_O = -360\mu A$ | +5V | 2.4 | | | Volts |
| Logic "0" $I_O = 10\mu A$ | +5V | | | 0.5 | Volts |
| $I_O = 10\mu A$ | +10V | | | 1.1 | Volts |
| $I_O = 360\mu A$ | +5V | | | 0.4 | Volts |
| **REFERENCE OUTPUT** | | | | | |
| Internal Reference: Voltage | | | +5.0 | | Volts |
| Initial Accuracy | | | ±1 | | % |
| Drift | | | ±5 | | ppm/°C |
| External Current | | | | 1 | mA |

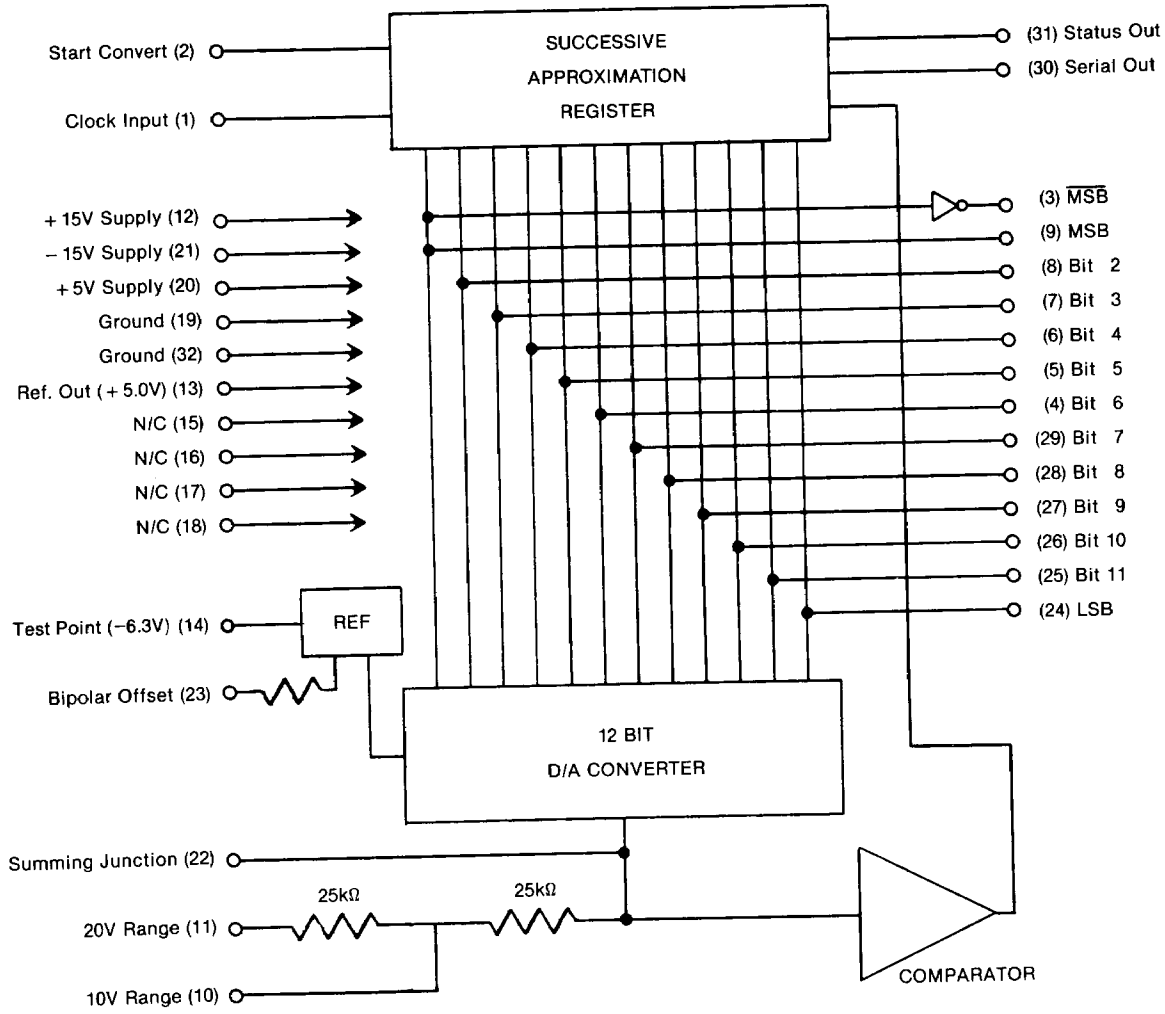
| | | | | |
|---|---|---|---|---|
| Power Supply Range: ± Vcc<br>+ Vdd | ± 14.5<br>+ 4.75 | ± 15.0 | ± 15.5<br>+ 10.0 | Volts<br>Volts |
| Power Supply Rejection: + Vcc<br>− Vcc<br>+ Vdd | | ± 0.01<br>± 0.05<br>± 0.05 | | %FSR/%Vs<br>%FSR/%Vs<br>%FSR/%Vs |
| Current Drain: + Vcc<br>− Vcc<br>+ Vdd | | 8<br>− 12<br>2.2 | 12<br>− 17<br>4 | mA<br>mA<br>mA |
| Power Consumption | | 311 | 455 | mW |

**SPECIFICATION NOTES:**

1. The digital circuitry used in the MN5700 is CMOS, and the standard precautionary measures for handling CMOS should be followed.
2. The + Vdd Logic Supply (Pin 20) can be at any voltage between + 5V (low power TTL compatibility and + 10V (CMOS compatibility).
3. The clock may asymmetrical, and it may ramp up and down as long as it meets minimum pulse width and maximum rise and fall time requirements.
4. Conversion Time is defined as the width of the Status Output pulse. For the MN5700, a 250 μsec conversion time corresponds to a clock frequency of 48 kHz.
5. FSR = Full Scale Range. A unit connected for 0 to − 20V or ± 10V input has a 20 volt FSR. A unit connected for 0 to − 10V or ± 5V input has a 10 volt FSR.
6. Micro Networks tests and guarantees maximum linearity error at room temperature and at the high and low extremes of the specified operating temperature range.
7. For a 12 bit converter, 1 LSB = 0.024%FSR; ±0.012%FSR = ± ½ LSB. ±0.05%FSR = ± ½ LSB in 10 bits.
8. No Missing Codes for 10 bits is graranteed over the entire − 55°C to + 200°C operating temperature range.
9. Full Scale Absolute Accuracy Error applies at negative full scale for the unipolar negative ranges and at both positive and negative full scale for the bipolar ranges.
10. Zero Error applies at both unipolar and bipolar zero volt input points.
11. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.



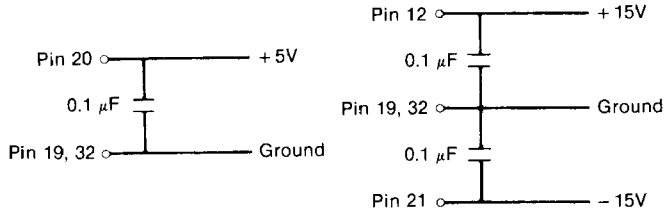
## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

**LAYOUT CONSIDERATIONS**—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5700. The units' two GROUND pins (Pins 19 and 32) are not connected to each other internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01$\mu$F ceramic bypass capacitor should be connected between Pins 19 and 32 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with 0.1$\mu$F high temperature capacitors (KD components #HT14B104K or equivalent) located close to the converters.

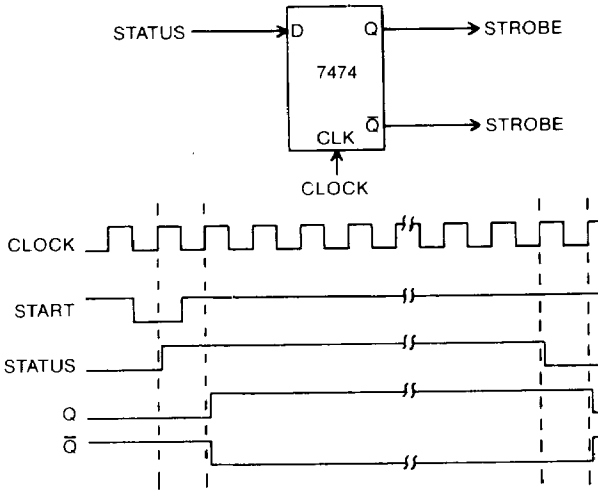



**POWER SUPPLY DECOUPLING**

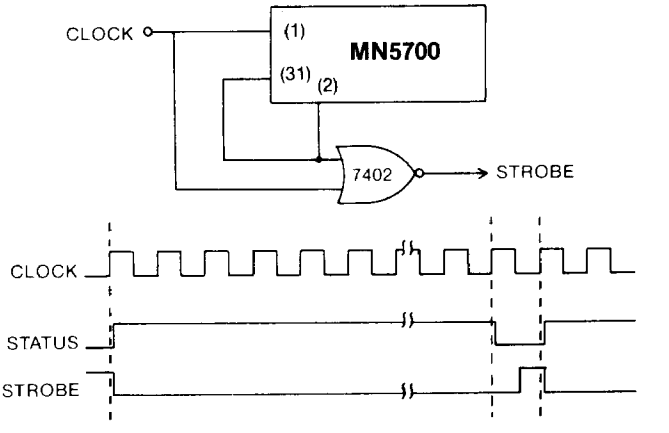
**CONTINUOUS CONVERTING**—The MN5700 can be made to continuously convert by trying the STATUS output (Pin 31) to the START CONVERT input (Pin 2). In this configuration, STATUS (START CONVERT) will go low at the end of conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing STATUS (START CONVERT) high again. The MSB will be set on the next rising clock edge. The result is that the STATUS will go low for approximately one clock period following each conversion. Please read the section describing the Status output. See below for continuous conversions while short cycling.

**SHORT CYCLING AND CONTINUOUS CONVERTING**—A previous section described how continuous converting for 12 bits could be accomplished by simply trying the STATUS output back to the START CONVERT input. To continuously convert at n bits, simply tie the bit (n + 1) output back to the START CONVERT input. The bit (n + 1) output acts like a STATUS when short-cycling at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be avoided by making the START CONVERT input the AND function of bit (n + 1) and the STATUS output.

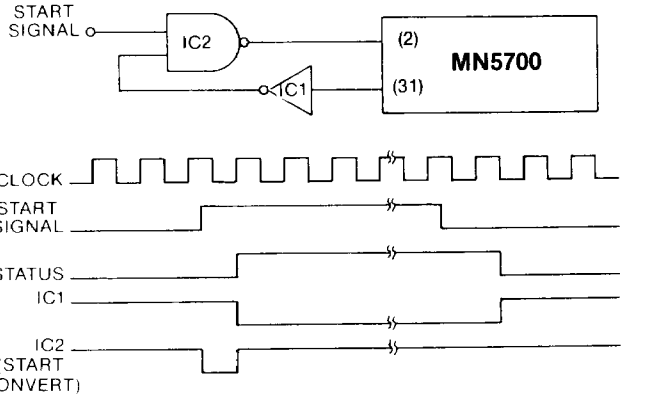
**STATUS OUTPUT**—The STATUS or END OF CONVERSION (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 250nsec after STATUS has returned low. Therefore, an adequate delay must be provided if STATUS is to be used to strobe latches to hold output data. Simple gate delays can be employed or the STATUS can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after STATUS changes.




If continuously converting, the STATUS (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse 1/2 period wide, 1/2 period after the STATUS output has gone low. The rising edge of this pulse can be used to latch data after each conversion.



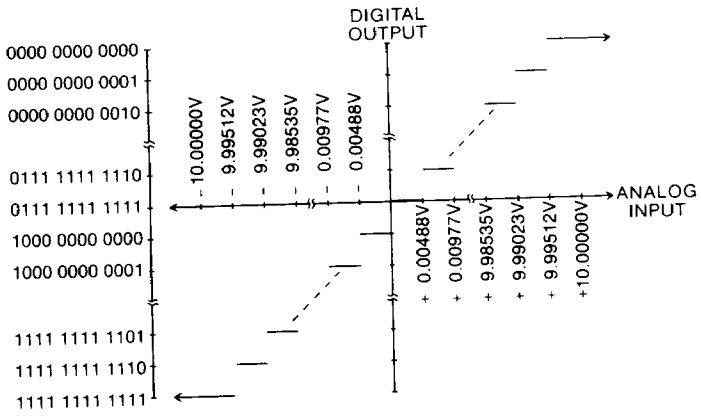

**TRIGGERING WITH A POSITIVE EDGE**—If it is inconvenient to generate a negative going START CONVERT pulse of the proper width, the MN5700 can be made to start converting on a positive going edge by employing the circuit shown below. Assuming the previous conversion is done and the START SIGNAL is low, the STATUS output will be low, the output of IC1 will be high, and the output of IC2 will be high. A rising edge as a START SIGNAL will drive the output of IC2 low. The converter will reset on the next rising clock edge. Resetting brings the STATUS high; IC1 goes low; the START SIGNAL is still high so the output of IC2 goes high allowing the conversion to continue immediately. The START SIGNAL has only to be brought back down before the conversion is completed.



## ABSOLUTE ACCURACY ERROR

A given digital output code is valid for a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated below where portions of the theoretical analog input/digital output transfer function for the −10V to +10V input range are sketched.

Notice that any analog input between +0.00488V (1 LSB = 4.88 mV) and +0.00977V will give a digital output of 0111 1111 1110. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 0111 1111 1110 digital code corresponds to analog inputs of +7.32 mV ±2.44mV which can be written as +7.32 mV ± ½ LSB. The ± ½ LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error and its magnitude can be reduced only by going to higher resolution converters.




**IDEAL INPUT/OUTPUT TRANSFER FUNCTION ±10V RANGE**

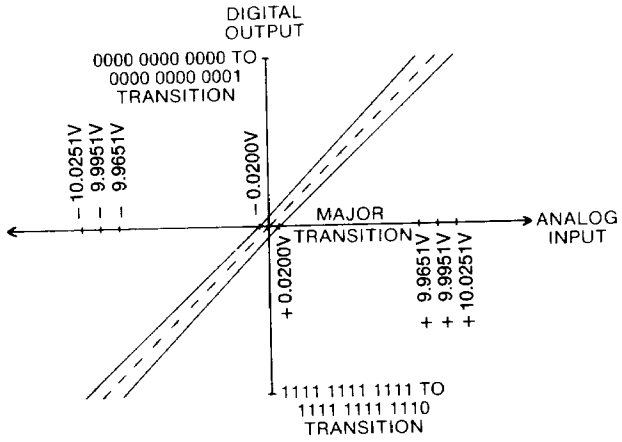
It is difficult and time consuming to measure the center of a quantization level (the +0.00732 volts in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next. The Absolute Accuracy Error of a voltage input A/D converter is the difference between the actual, unadjusted, analog input voltage at which a given digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or % FSR. Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors.

For the MN5700, Micro Networks tests Absolute Accuracy Error at both endpoints of unipolar input ranges and at both endpoints and the midpoint of bipolar input ranges. These tests are performed at room temperature and at both the high and low extremes of the specified operating temperature range. The specifications appear in the table as the Full Scale Absolute Accuracy and Zero Errors.

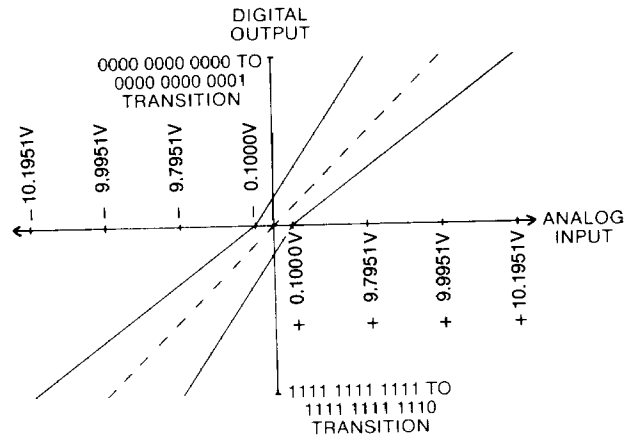
Return to the ideal analog input/digital output transfer function for the ±10V input range sketched above. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from −10V to −9.9951V. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to −9.9951V. This voltage −9.9951V is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9951V. The 1000 0000 0000 to 0111 1111 1111 transition (called the major transition because all the bits change) ideally occurs at the zero volt analog input.

For the MN5700 operating on its ±10V range, Micro Networks 100% tests linearity and the absolute accuracy of the three transition voltages just discussed at −55°C, +25°C, and +200°C. At 25°C, we guarantee that the transfer function will be ±1/2 LSB linear, that the positive and negative full scale transition voltages will occur within ±30 mV (±0.15%FSR) of their ideal values, and that the major transition will occur within ±20 mV (±0.1%FSR) of zero volts. At −55°C and at +200°C, we guarantee that the transfer function will be ±0.05%FSR linear, that the positive and negative full scale LSB transition voltages will occur within ±200 mV (±1%FSR) of their ideal values, and that the major transition will occur within ±100 mV (±0.5%FSR) of zero volts.

These Absolute Accuracy Error specifications are summarized below. In each sketch, the ideal transfer function is represented by the broken line and the absolute accuracy limits by the solid lines.




**ABSOLUTE ACCURACY +25°C**




**ABSOLUTE ACCURACY −55°C to +200°C**

MN5700

## INPUT RANGE SELECTION

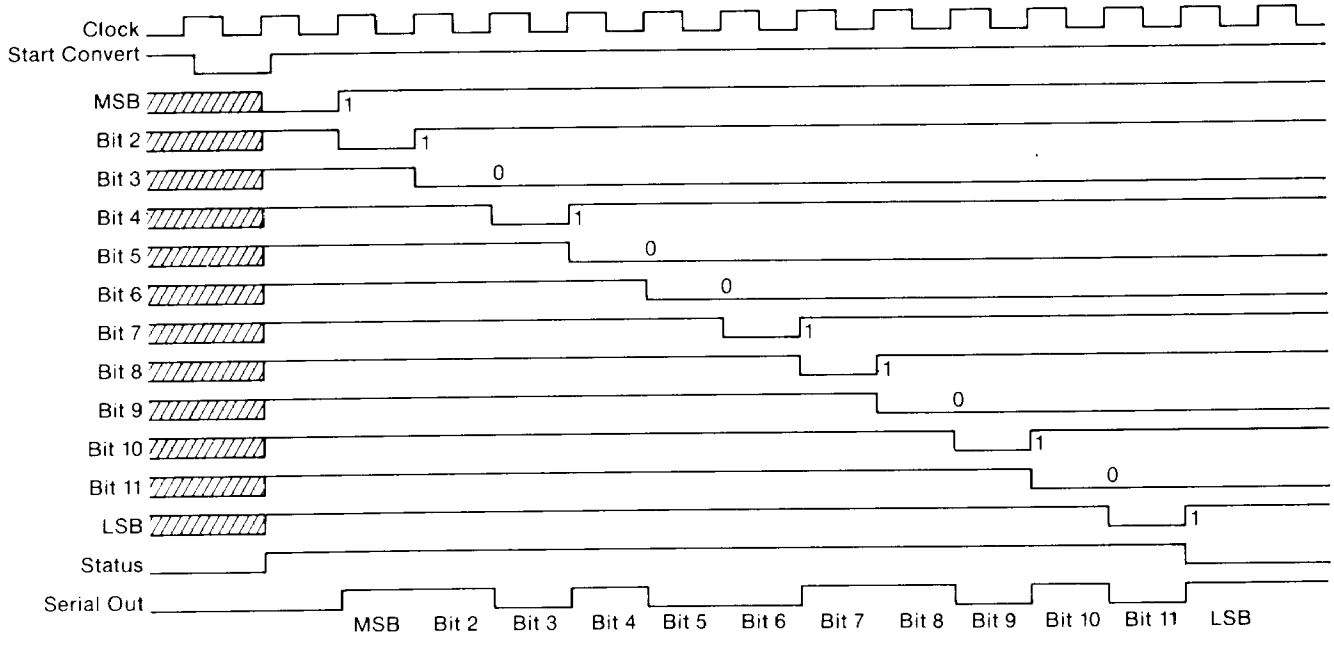
| Range | Analog Input | Connect Pin 23 to |
|---|---|---|
| 0 to −10V | Pin 10 | Ground |
| 0 to −20V | Pin 11 | Ground |
| −5 to +5V | Pin 10 | Pin 22 |
| −10 to +10V | Pin 11 | Pin 22 |

## OUTPUT CODING

| ANALOG INPUT (volts) | | | | DIGITAL OUTPUT |
|---|---|---|---|---|
| 0 to −10V | 0 to −20V | −5V to +5V | −10V to +10V | MSB LSB |
| 0.0000 | 0.0000 | +5.0000 | +10.0000 | 0000 0000 0000 |
| −0.0024 | −0.0049 | +4.9976 | +9.9951 | 0000 0000 000Ø* |
| −4.9976 | −9.9951 | +0.0024 | +0.0049 | 0111 1111 111Ø* |
| −5.0000 | −10.0000 | 0.0000 | 0.0000 | ØØØØ ØØØØ ØØØØ* |
| −5.0024 | −10.0049 | −0.0024 | −0.0049 | 1000 0000 000Ø* |
| −9.9976 | −19.9951 | −4.9976 | −9.9951 | 1111 1111 111Ø* |
| −10.0000 | −20.0000 | −5.0000 | −10.0000 | 1111 1111 1111 |

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explantion of Output Transition Voltages.
EXAMPLE: For the ± 10V analog input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.9951 volts. Subsequently, any input voltage more positive than +9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at −9.9951 volts. An input more negative than −9.9951 volts will give all "1's".

## TIMING DIAGRAM




**TIMING DIGRAM NOTES:**

1. Operation shown is for the digital word 1101 0011 0101 which corresponds to −8.2568V on the 0 to −10V input range.
2. Conversion time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 80nsec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 350 nsec maximum. See specification table.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 250 nsec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated. See specification table.
8. For continuous conversion, connect the STATUS output (Pin 31) to the START CONVERT input (Pin 2). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.