

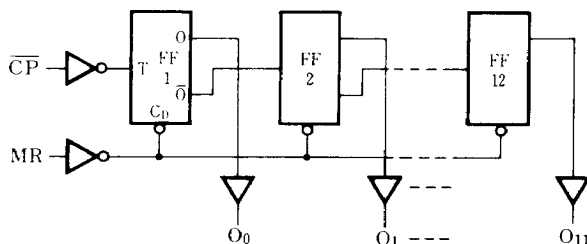
MN4040B / MN4040BS

12-Stage Binary Counters

■ Description

The MN4040B/S are 12-stage binary ripple counters with a clock input. The reset input and outputs are fully buffered. The counter advances on the negative going edge of the clock input. A High on the MR input clears all counter stages and forces all outputs ($O_0 \sim O_{11}$) Low, independent of the clock input. These are suitable for frequency dividers and center-control circuits, and are equivalent to MOTOROLA MC14040B and RCA CD4040B.

■ Logic Diagram



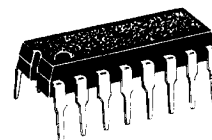
Pin Explanation

$\overline{CP}$: Clock input ($\neg$)

MR : Reset input

$O_0 \sim O_{11}$: Output (12 Bits)

P- 3



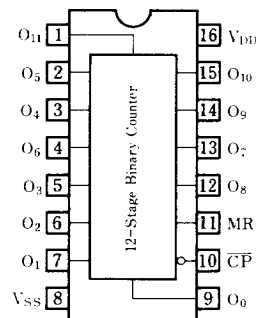
16-Pin • Plastic DIL Package

P- 4



16-Pin • Panafiat Package (SO-16D)

Pin Configuration



■ Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	$-0.5 \sim +18$	V
Input Voltage		V_I	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage		V_O	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input - Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	$T_a = -40 \sim +60^\circ\text{C}$	P_D	max. 400	mW
	$T_a = +60 \sim +85^\circ\text{C}$		Decrease up to 200mW rating at $8\text{mW}/^\circ\text{C}$	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		T_{opr}	$-40 \sim +85$	$^\circ\text{C}$
Storage Temperature		T_{stg}	$-65 \sim +150$	$^\circ\text{C}$

* $V_{DD} + 0.5\text{V}$ should be under 18V

■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} V	Sym- bol	Conditions	$T_a=-40^\circ C$		$T_a=25^\circ C$		$T_a=85^\circ C$		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_i=V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_i=V_{SS}$ or V_{DD} $ I_O < 1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_i=V_{SS}$ or V_{DD} $ I_O < 1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_O < 1\mu A$ $V_O=0.5V$ or $4.5V$ $V_O=1V$ or $9V$ $V_O=1.5V$ or $13.5V$	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_O < 1\mu A$ $V_O=0.5V$ or $4.5V$ $V_O=1V$ or $9V$ $V_O=1.5V$ or $13.5V$	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O=0.4V, V_i=0$ or $5V$	0.52	—	0.44	—	0.36	—	mA
	10		$V_O=0.5V, V_i=0$ or $10V$	1.3	—	1.1	—	0.9	—	
	15		$V_O=1.5V, V_i=0$ or $15V$	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=4.6V, V_i=0$ or $5V$	0.52	—	0.44	—	0.36	—	mA
	10		$V_O=9.5V, V_i=0$ or $10V$	1.3	—	1.1	—	0.9	—	
	15		$V_O=13.5V, V_i=0$ or $15V$	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=2.5V, V_i=0$ or $5V$	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	$V_i=0$ or $15V$	—	0.3	—	0.3	—	1	μA

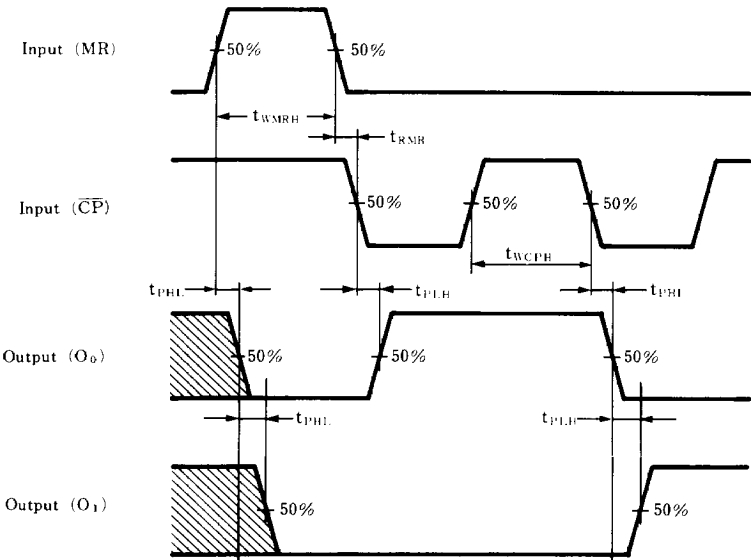
■ Switching Characteristics ($T_a=25^\circ C, V_{SS}=0V, C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP} \rightarrow O_0$ (L $\rightarrow$ H)	5	t_{PLH}	—	105	315	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $\overline{CP} \rightarrow O_0$ (H $\rightarrow$ L)	5	t_{PHL}	—	105	315	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time $O_n \rightarrow O_{n+1}$ (L $\rightarrow$ H)	5	t_{PLH}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time $O_n \rightarrow O_{n+1}$ (H $\rightarrow$ L)	5	t_{PHL}	—	80	240	ns
	10		—	30	90	
	15		—	20	60	

■ Switching Characteristics (Ta=25°C, Vss=0V, CL=50pF)

Item	VDD(V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time MR→On (H→L)	5	tPHL	—	180	540	ns
	10		—	90	270	
	15		—	70	210	
Minimum Clock Pulse Width	5	tWCPH	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	tWMRH	—	65	195	ns
	10		—	50	150	
	15		—	45	135	
Reset Recovery Time	5	tRMR	—	60	180	ns
	10		—	35	105	
	15		—	25	75	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		13	25	—	
	15		18	35	—	
Input Capacitance		CI	—	—	7.5	pF

● Dynamic Signal Waveforms



Waveforms showing propagation delays for MR to O₀ and CP to O₀, minimum MR and CP pulse widths and recovery time for MR