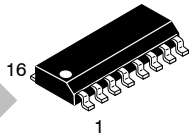
MMPQ6700

Quad Complementary Pair Transistor

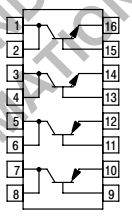
PNP/NPN Silicon

ON Semiconductor®

http://onsemi.com



CASE 751B–05, STYLE 4
SO–16



MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector – Emitter Voltage	V_{CEO}	40		Vdc
Collector – Base Voltage	V_{CB}	40		Vdc
Emitter – Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	200		mAdc
		Each Transistor	**Four Transistors Equal Power**	
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.4 3.2	0.72 6.4	W mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	0.66 5.3	1.92 15.4	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

© Semiconductor Components Industries, LLC, 2006

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage[1] (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	—	Vdc
Collector – Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	—	Vdc
Emitter – Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	50	nAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	50	nAdc
ON CHARACTERISTICS[1]				
DC Current Gain	h_{FE}			—
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)		35	—	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)		50	—	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		70	—	
Collector – Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	—	0.25	Vdc
Base – Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	—	0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current – Gain — Bandwidth Product[1] (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	200	—	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}		4.5	pF
Input Capacitance	C_{ib}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz) PNP		—	10	
NPN		—	8.0	

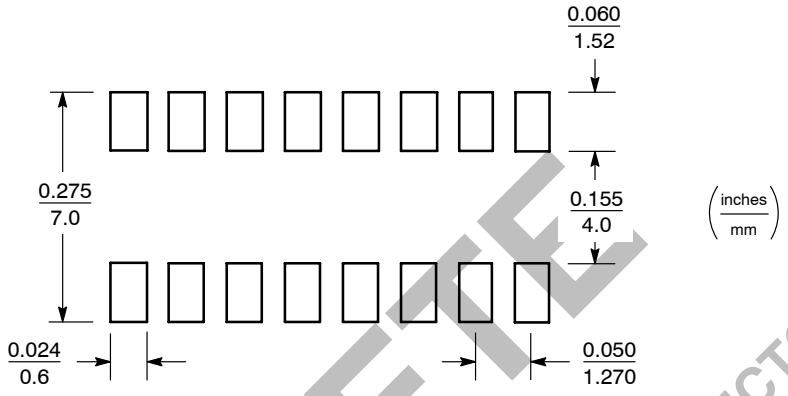
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

INFORMATION FOR USING THE SO−16 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SO−16

SO−16 POWER DISSIPATION

The power dissipation of the SO−16 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SO−16 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 1.0 watt.

$$P_D = \frac{150°C - 25°C}{125°C/W} = 1.0 \text{ watt}$$

The 125°C/W for the SO−16 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.0 watt. There are other alternatives to achieving higher power dissipation from the SO−16 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

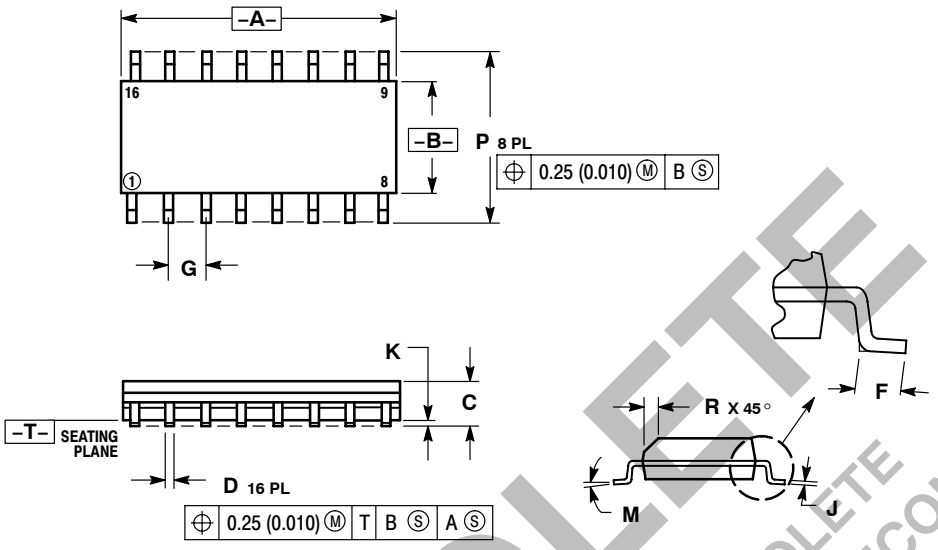
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

PACKAGE DIMENSIONS

CASE 751B–05
SO–16
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

Thermal Clad is a trademark of the Bergquist Company.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5773–3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

MMPQ6700/D