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DUAL COMPLEMENTARY PAIR PLUS INVERTER

GENERAL DESCRIPTION

The MMC 4007 (G and H types) and MMC 4007 (E and F types) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package. The MMC 4007 types are comprised of three n-channel and three p-channel enchancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in typical applications.
More complex functions are possible using multiple packages. Numbers shown in parantheses indicate terminals that are connected together to form the various configuration listed.

FEATURES

- Standardized symmetrical output characteristics
- Medium speed operation t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- Quiescent current specified to 20 V for G and H types
- Input current of 100 nA at 18 V and 25° C for G and H types
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

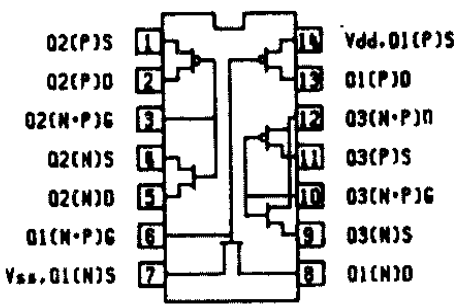
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



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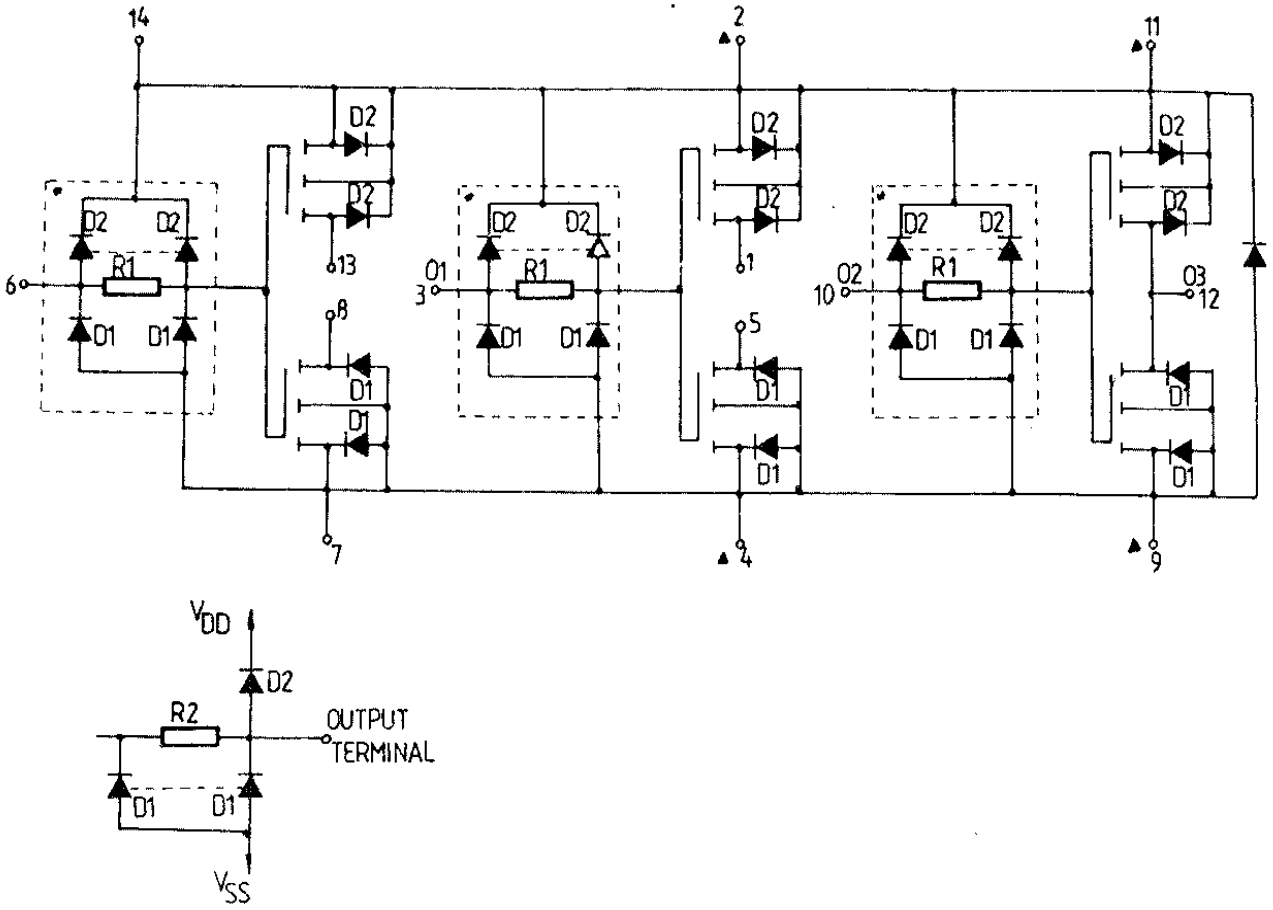
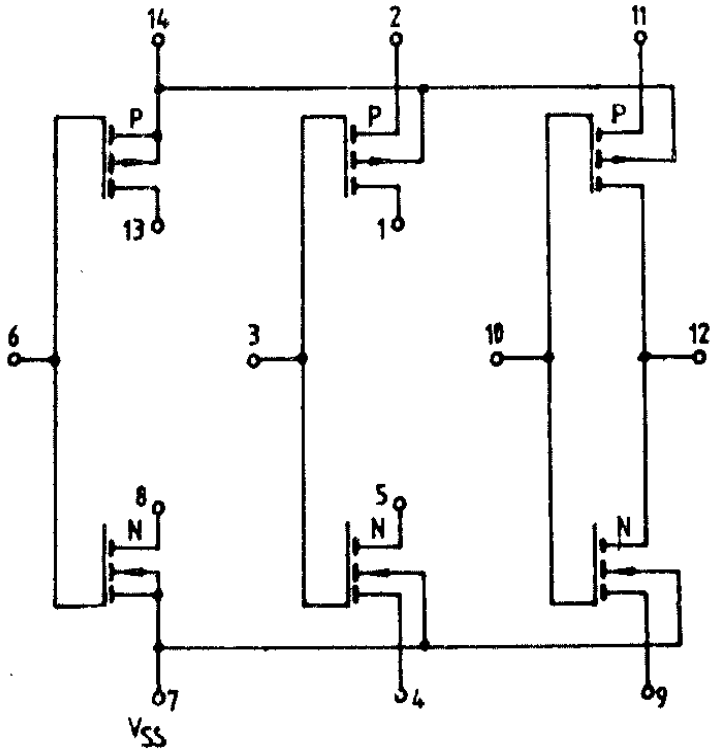
SCHEMATIC DIAGRAM



FUNCTIONAL DIAGRAM



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STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	—Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12		12			12		
V_{IL}	—Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13.5/1.5	< 1	15		2.5			2.5		2.5	
I_{OH}	—Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

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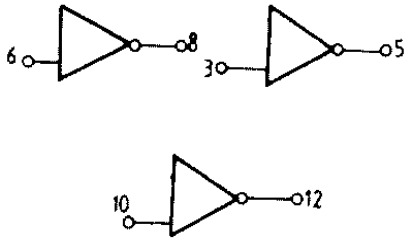
DYNAMIC ELECTRICAL CHARACTERISTICS (T_A = 25° C, C_L = 50 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} values is 0.3/°C, all input rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS	VALUES			Unit
		V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time		5		55	110	ns
		10		30	60	
		15		25	50	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

TYPICAL APPLICATIONS (sample CMOS logic circuit arrangements using type 4007)

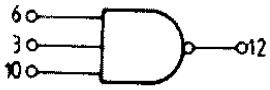
Triple inverters. (14,2,11); (8,13);



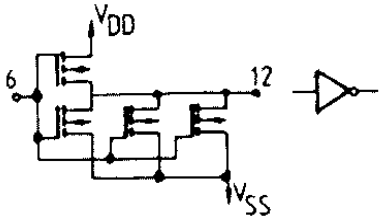
3—input NOR gate (13,2); (1,11); (12,5,8); (7,4,9);



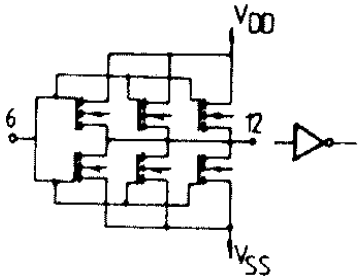
3—input NAND gate (1,12,13); (2,14,11) (4,8); (5,9);



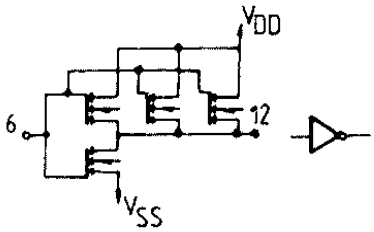
High sink-current driver. (6,3,10); (8,5,12); (11,14); (7,4,9);



High sink-and source-curent driver. (6,3,10); (14,2,11); (7,4,9); (13,8,1,5,12)



High source-curent driver. (6,3,10); (13,1,12); (14,2,11); (7,9);



Dual bi-directional transmission gating. (1,5,12); (2,9); (11,4); (8,13,10); (6,3)

