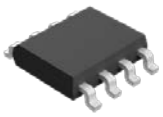
MLX90395 Triaxis® Magnetometer Node

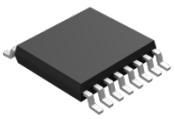
Datasheet

1. Features and Benefits

- Triaxis® Hall Technology
- Automotive Grade (AEC-Q100)
- Micro-power with Programmable Duty Cycle
- Selectable Digital Output
  - 16-bit Magnetic (XYZ)
  - 16-bit Supply Voltage (V)
  - 14-bit Temperature (T)
- At runtime programmable modes
  - Single Measurement
  - Burst Mode up to 2kHz (XYZ)
  - Wake-up On Change (WOC) Mode
- Programmable Measurement Range & extended magnetic sensing range option
- On-chip magnetic calibration data allowing off-chip DSP to achieve maximum accuracy
- 8-bit measurement CRC
- Measurement Counter
- Selectable Bus Protocol – Slave node
  - Up to 10MHz SPI or 1MHz I^2C
- 48-bit unique ID Number
- RoHS Compliant & Green Packages



SOIC-8



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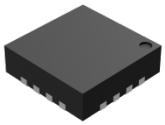
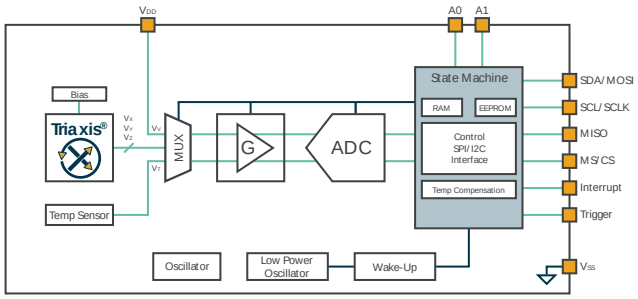


QFN-16



2. Application Examples

- HMI Non-Contacting Potentiometer
  - Joystick with Push
  - Rotary with Push
  - Linear (Long Stroke)
- Top-Column Module
  - Stalk Position/Function Sensor
- Center Stack
  - Shifter Position Sensor
  - Multimedia Rotary/Push Selector
  - Knobs / Levers
- Body Control
  - Door handle & door lock
  - Mirror position

3. Description

The MLX90395 Triaxis® Magnetic Node is a miniature monolithic sensor IC sensitive to the three orthogonal components of the flux density applied to the IC (i.e. B_X, B_Y and B_Z) and to temperature. This allows the MLX90395 with the correct magnetic circuit to decode the absolute position of any moving magnet. It enables the design of novel generation of non-contacting position sensors that are frequently required for both automotive and industrial applications.

The MLX90395 selectable measurement data can be read over I^2C or SPI bus. The sensor is runtime programmable and offers on-chip temperature compensation of the measured units. The selectable measurement duty cycle enables unsurpassed micro-power functionality. In this respect, the MLX90395 is the first true Software Defined Sensor: one IC, any magnetic sensing application. You define the function.

4. Ordering Information

Note: Ordering code BAA-x0x: not recommended for new designs.

Product	Temperature	Package	Option Code	Packing Form	Definition
MLX90395	K	DC	BAA-000	RE	Medium-Field Version (50mT)
MLX90395	K	GO	BAA-000	RE	Medium-Field Version (50mT)
MLX90395	K	LW	BAA-000	RE	Medium-Field Version (50mT)
MLX90395	K	DC	BAA-100	RE	High-Field Version (120mT)
MLX90395	K	GO	BAA-100	RE	High-Field Version (120mT)
MLX90395	K	LW	BAA-100	RE	High-Field Version (120mT)
MLX90395	K	DC	BBA-001	RE	Medium-Field Version (50mT)
MLX90395	K	GO	BBA-001	RE	Medium-Field Version (50mT)
MLX90395	K	LW	BBA-001	RE	Medium-Field Version (50mT)
MLX90395	K	DC	BBA-101	RE	High-Field Version (120mT)
MLX90395	K	GO	BBA-101	RE	High-Field Version (120mT)
MLX90395	K	LW	BBA-101	RE	High-Field Version (120mT)

Legend:

Temperature Code:	K: from -40°C to 125°C
Package Code:	“DC” for SOIC-8 package “GO” for TSSOP-16 package (dual die) “LW” for QFN-16 package (wettable flanks)
Option Code - chip revision:	B**xx**-abc B**AA**: not recommended for new designs B**BA**: standard version
Option Code - application:	Bxx-**abc**: **a**: Magnetic Sensing Range 0: Medium Field Version (50mT) 1: High Field Version (120mT) **b**: N/A **c**: SPI Filter 0: No filter (SPI frequency up to 10MHz) 1: 1MHz filter (SPI frequency up to 1MHz)
Packing Form:	“RE” for Reel “DC”: 3000 pcs/reel “GO”: 4500 pcs/reel “LW”: 5000 pcs/reel
Ordering Example:	“MLX90395KLW-BBA-101-RE” For a 120mT sensing range 3D Magnetic Node in QFN-16 package, delivered in Reel.

Table 1: Ordering information

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5. Functional Diagram

The MLX90395 is sensitive to the three (B_X, B_Y, B_Z) components of the flux density applied to the IC. This allows the MLX90395 with the correct off-chip signal processing to decode the absolute position of any moving magnet (e.g. rotary position from 0 to 360 Degrees, linear displacement, joystick… as shown in Figure 1). The flexibility resides in the runtime selection of measurement data and the application software in the external microcontroller, resulting in a true "Software-Defined Magnetic Sensor".

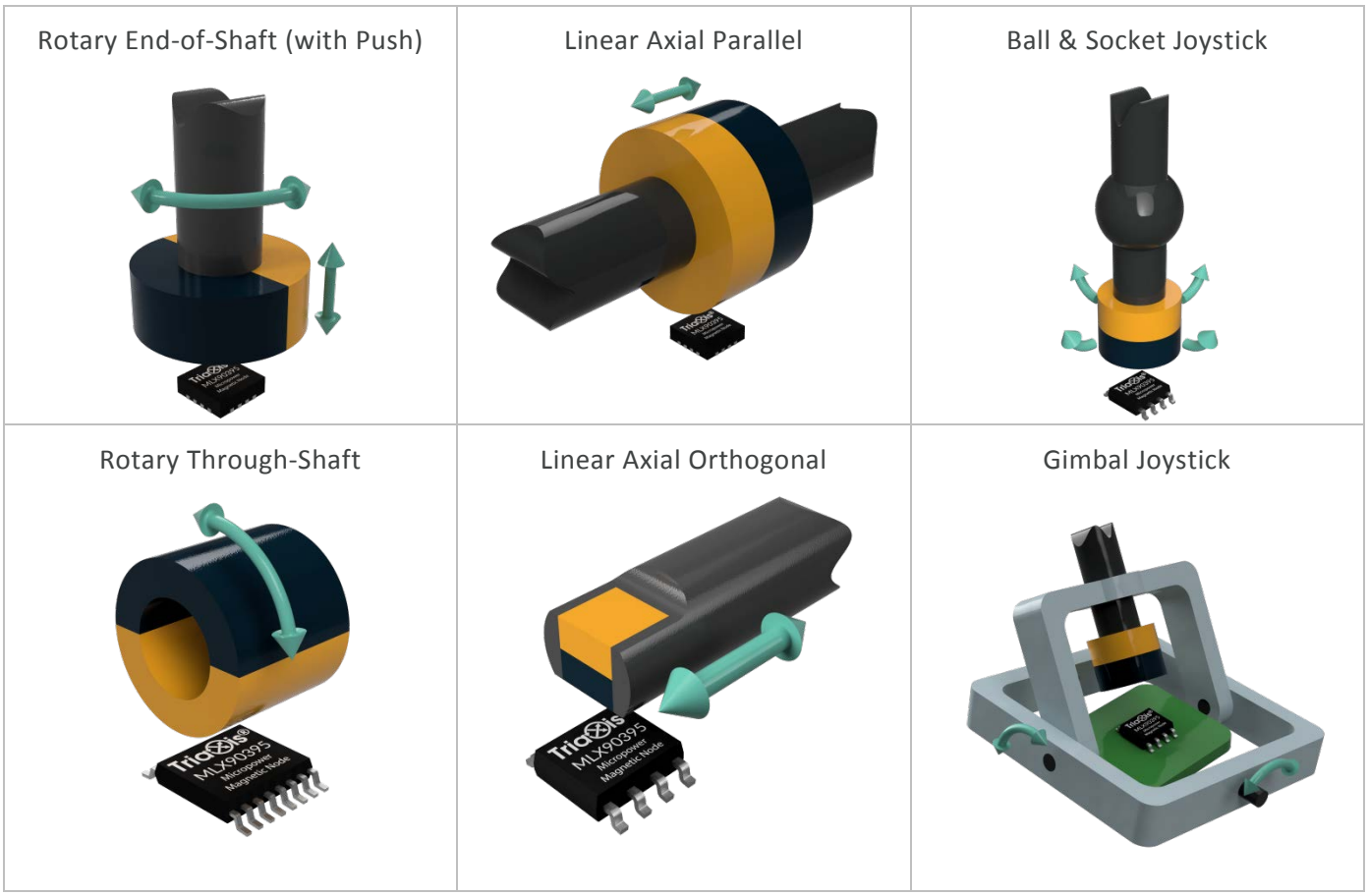


Figure 1: Magnetic Applications

As the MLX90395 has no on-board microcontroller, it lends itself well to applications requiring a concatenation of multiple sensors on the communication bus of a single microcontroller, allowing more cost-efficient and lean designs. Melexis' Applications Engineers can support in the microcontroller computations.

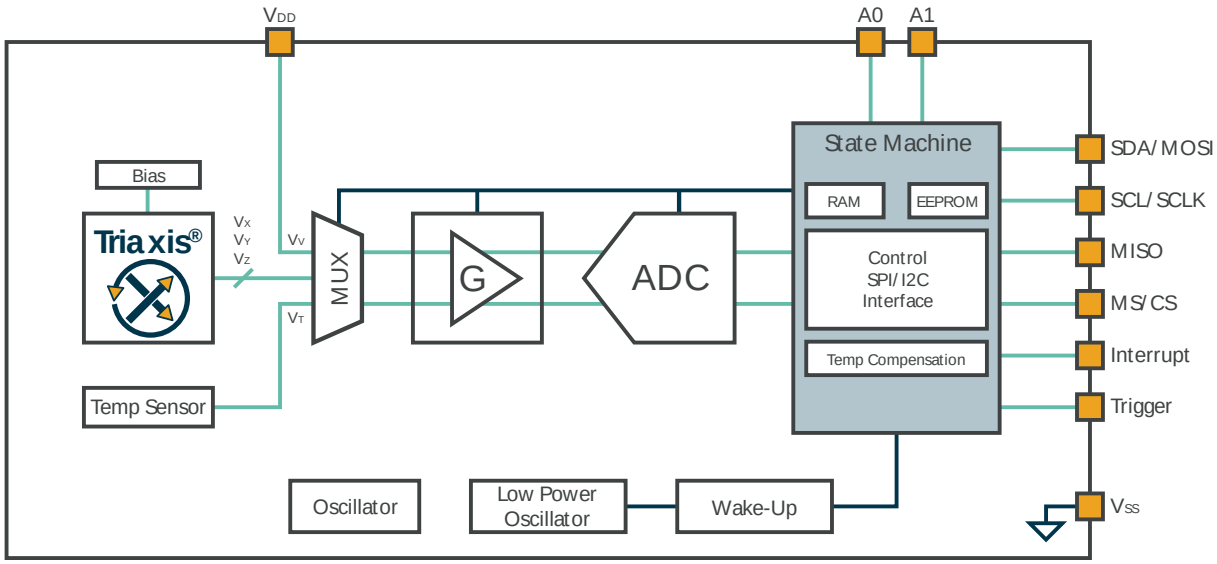


Figure 2: Block Diagram for the QFN-16 package

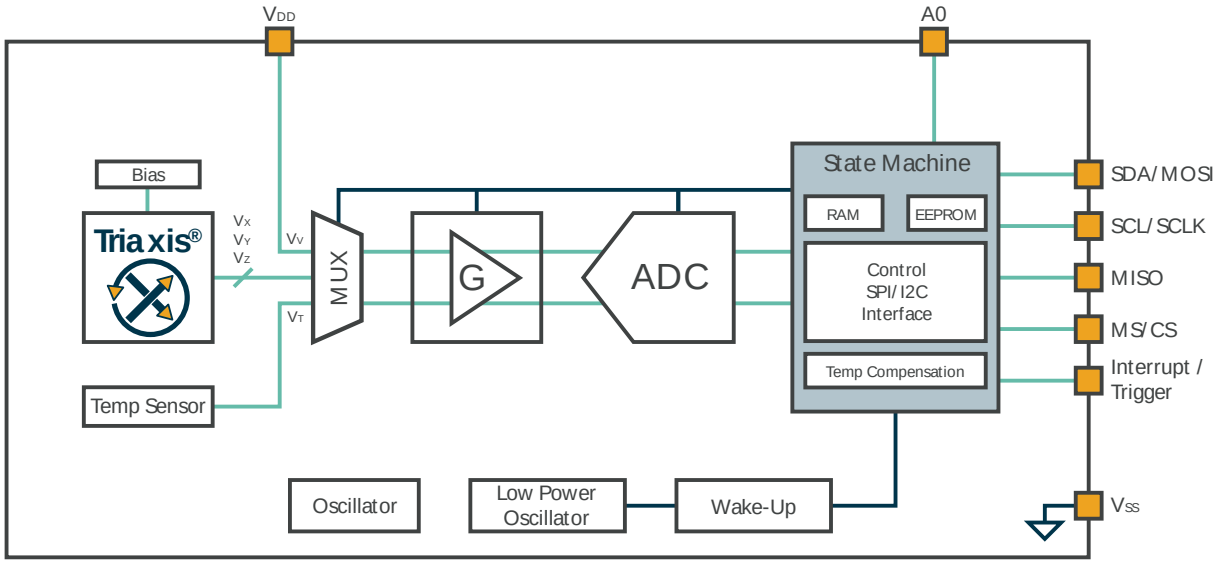


Figure 3: Block diagram for the SOIC-8 (single die) and TSSOP-16 (dual die) package

6. Glossary of Terms

Term	Description	Term	Description
Gauss (G), Tesla (T)	Units for the magnetic flux density: 1mT = 10G	EMC	Electro-Magnetic Compatibility
TC	Temperature Coefficient (in ppm/°C)	FIR	Finite Impulse Response
ADC	Analog-to-Digital Converter	OSR	Over Sampling Rate
DAC	Digital-to-Analog Converter	PWL	Piece Wise Linear
LSB	Least Significant Bit	POR	Power On Reset
MSB	Most Significant Bit	SW	Software
DNL	Differential Non-Linearity	HW	Hardware
INL	Integral Non-Linearity	IMC	Integrated Magnetic Concentrator
ASP	Analog Signal Processing	ROM	Read-only Memory
DSP	Digital Signal Processing	RAM	Random-access Memory
CDM	Charge Device Model	ESD	Electrostatic Discharge
HBM	Human Body Model		

Table 2: Glossary of Terms

7. Pin Definitions

7.1. Pin Definition for SOIC-8 Package

Pin #	Name (I^2C)	Name (SPI)	Description
1	SCL	SCLK	[I] Bus clock
2	SDA	MOSI	[I/O] Bus Data / SPI Master Out Slave In
3	Not Used	MISO	[O] SPI Master In Slave Out
4	INT/TRG	INT/TRG	[O or I] Interrupt / Trigger Pin (Programmable)
5	A0	Not Used	[I] I^2C Address Pin 0
6	VSS	VSS	[S] Ground
7	VDD	VDD	[S] Supply
8	MS	/CS	[I] Mode Select / Chip Select

Table 3: SOIC-8 Pin Definitions and Descriptions

For optimal EMC behaviour connect the unused pins (Not Used) to the Ground (See section 19.1). [I] stands for Input Pin, [O] stands for Output Pin and [S] stands for Supply Pin.

7.2. Pin Definition for TSSOP-16 Package

Pin #	Name (I^2C)	Name (SPI)	Description
1	SCL_1	$SCLK_1$	[I] Bus clock
2	SDA_1	$MOSI_1$	[I/O] I^2C Data / SPI Master Out Slave In
3	Not Used	$MISO_1$	[O] SPI Master In Slave Out
4	INT/TRG_1	INT/TRG_1	[O or I] Interrupt / Trigger Pin (Programmable)
5	$A0_2$	Not Used	[I] I^2C Address Pin 0
6	VSS_2	VSS_2	[S] Ground
7	VDD_2	VDD_2	[S] Supply
8	MS_2	$/CS_2$	[I] Mode Select / Chip Select
9	SCL_2	$SCLK_2$	[I] Bus clock

Pin #	Name (I^2C)	Name (SPI)	Description
10	SDA_2	$MOSI_2$	[I/O] I^2C Data / SPI Master Out Slave In
11	Not Used	$MISO_2$	[O] SPI Master In Slave Out
12	INT/TRG_2	INT/TRG_2	[O or I] Interrupt / Trigger Pin (Programmable)
13	$A0_1$	Not Used	[I] I^2C Address Pin 0
14	VSS_1	VSS_1	[S] Ground
15	VDD_1	VDD_1	[S] Supply
16	MS_1	$/CS_1$	[I] Mode Select / Chip Select

Table 4: TSSOP-16 Pin Definitions and Descriptions

For optimal EMC behaviour connect the unused pins (Not Used) to the Ground (See section 19.1). [I] stands for Input Pin, [O] stands for Output Pin and [S] stands for Supply Pin.

7.3. Pin Definition for QFN-16 Package

Pin #	Name (I^2C)	Name (SPI)	Description
1	INT	INT	[O] Interrupt
2	MS	/CS	[I] Mode Select / Chip Select
3	SCL	SCLK	[I] Bus clock
4	Not Used	Not Used	Not Connected
5	SDA	MOSI	[I/O] I^2C Data / SPI Master Out Slave In
6	Not Used	MISO	[O] SPI Master In Slave Out
7	INT/TRG	INT/TRG	[O or I] Interrupt / Trigger Pin (Programmable)
8	Not Used	Not Used	Not Connected
9	Not Used	Not Used	Not Connected
10	Not Used	Not Used	Not Connected
11	A1	Not Used	[I] I^2C Address Pin 1
12	A0	Not Used	[I] I^2C Address Pin 0
13	VSS	VSS	[S] Ground
14	Not Used	Not Used	Not Connected
15	VDD	VDD	[S] Supply
16	Not Used	Not Used	Not Connected

Table 5: QFN-16 Pin Definitions and Descriptions

For optimal EMC behaviour connect the unused pins (Not Used) to the Ground (See section 19.2). [I] stands for Input Pin, [O] stands for Output Pin and [S] stands for Supply Pin.

8. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	VDD_{MAX}			4	V	<48h
Reverse Voltage Protection	VDD_{REV}	-0.3			V	<48h
Positive Output Voltage	Vout			4	V	<48h Vout<VDD+0.3V
Negative Output Voltage	$Vout_{REV}$	-0.3			V	<48h
Positive Input Voltage [1]	Vin			4	V	<48h Vin<VDD+0.3V
Negative Input Voltage	Vin_{REV}	-0.3			V	<48h
Operating Temperature	T_{AMB}	-40		+125	°C	Refer to the qualification profile
Junction Temperature	T_J			+150	°C	
Storage Temperature	T_{ST}	-40		+150	°C	Refer to the qualification profile
Magnetic Flux Density	B_{MAX}	-1		+1	T	
ESD voltage, HBM	ESD_{HBM}	-2		+2	kV	According AEC-Q100-002 DC and LW package code
ESD voltage, CDM	ESD_{CDM}	-750		+750	V	According AEC-Q100-011 DC and LW package code

Table 6: Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

9. Isolation Specification

Only valid for the package code GO, i.e. TSSOP-16 package (dual die).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Isolation Resistance	R_{ISOL}	4			MΩ	Between dies, measured between Vss_1 and Vss_2 with ±20V bias

Table 7: Isolation Specification

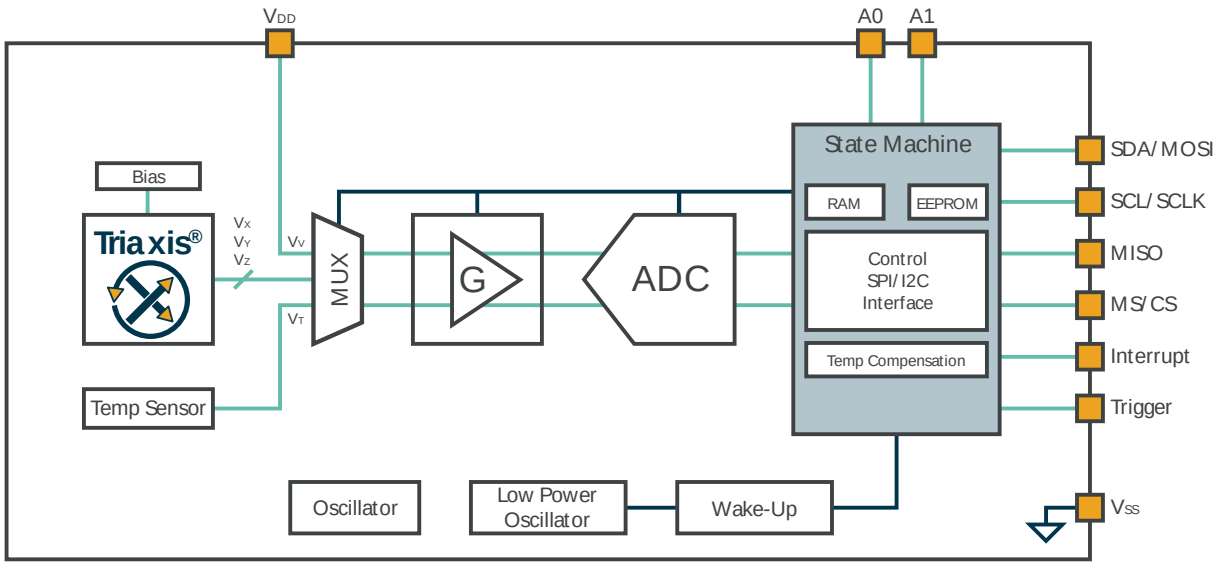
[1] *For shared [I/O] pin, maximum rating for output applies.*

10. General Description

As described on the block diagram the three vector components of the magnetic flux density (B_X, B_Y and B_Z) applied to the IC are sensed through the sensor front-end. The respective Hall signals (V_X, V_Y and V_Z) are generated at the Hall plates and amplified.

The analog front-end is based on a fully differential analog chain featuring the classic offset cancellation technique (Hall plate 4 Phases spinning and chopper-stabilized amplification).

The conditioned analog signals are converted through a sigma-delta ADC (19 bits) and provided to a DSP block for further processing. The DSP stage is a custom finite state machine whose primary function consists of signal conditioning of the raw XYZ signals: offset & sensitivity adjustment and thermal offset & sensitivity drift compensation using the calibrated on-board temperature sensor. The result of these computations are a predetermined transfer characteristic of the sensor for a fixed gain setting.



These 3D linear Hall measurements are made available to the communication bus master for readout. The supported communication protocols are both I^2C and SPI, where the Triaxis® Magnetic Node is a slave on the bus. Upon readback, it is then up to the microcontroller to process the measurement data – either in a vectorial or a scalar way – in order to achieve more complex position sensing functionality required by the application.

When processing data in a vectorial (or angular) way, all signal amplitude variations due to the sensitivity imperfections of the sensor, as well as the flux density degradation of the permanent magnet over temperature are cancelled out. The magnetic vectorial information is intrinsically self-compensated vs. flux density variations. This feature allows therefore an improved thermal accuracy vs. position sensors based on conventional 1D linear Hall sensors.

Another advantage of vectorial versus scalar signal processing is extended absolute position sensing range and higher linearity for Axial Parallel linear stroke position sensing applications.

In addition to the improved thermal accuracy, the realized position sensor features excellent linearity performances taking into account typical manufacturing tolerances (e.g. relative placement between the Hall IC and the magnet).

11. General Electrical Specification

General electrical specifications are valid for temperature range: -40 - 125°C, supply voltage range: 2.6/3.0 - 3.6V unless otherwise noted (condition).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Analog Supply Voltage	VDD	2.6	3.3	3.6	V	$T_A \leq 90°C$
Analog Supply Voltage	VDD	3.0	3.3	3.6	V	$T_A > 90°C$
Supply Current [2]	$Idd.conv_{XY}$		2.3	3	mA	X-/Y-axis measurement
Supply Current [2]	$Idd.conv_Z$		3	4	mA	Z-axis measurement
Supply Current [2]	$Idd.conv_T$		1.6	2	mA	Temperature measurement
Supply Current [2]	$Idd.conv_V$		1.6	2	mA	Voltage measurement
Idle Current [2, 3]	Idd.idle		1.4 1.4	9 [5] 20	µA µA	$T_A \leq 85°C$ T_A within T_{AMB}
Standby Current [2, 4]	Idd.stby		2.4 2.4	10 [5] 21	µA µA	$T_A \leq 85°C$ T_A within T_{AMB}
Surge Current [2, 5]	Isurge		25	250	mA	Startup current, <3µs
Power-On reset (rising)	VporLH		1.45	1.52	V	
Power-On reset (falling)	VporLH	1.3	1.39		V	
Input High Threshold [5]	VIH			75	%VDD	SDA/MOSI, SCL/SCLK
Input Low Threshold [5]	VIL	25			%VDD	SDA/MOSI, SCL/SCLK
Input Level Hysteresis [5]	VIHYST	15	27		%VDD	SDA/MOSI, SCL/SCLK
Input High Threshold [5]	VIH			70	%VDD	INT/TRG, MS/CS
Input Low Threshold [5]	VIL	20			%VDD	INT/TRG, MS/CS
Input Level Hysteresis [5]	VIHYST	17	22		%VDD	INT/TRG, MS/CS
Input Capacitance [5]	Cin		5	30	pF	
Output Level High	VOH	98			%VDD	MISO, INT, INT/TRIG, SDA (Static, 1mA load)
Output Level Low	VOL			2	%VDD	MISO, INT, INT/TRIG, SDA (Static, 1mA load)
ON Resistance [5]	Rds.on	4	6	9	Ω	SDA
ON Resistance [5]	Rds.on	13	20	27	Ω	INT (NMOS and PMOS)
Output High Short Circuit Current [5]	IshortH	-60			mA	Vout forced to 0V
Output Low Short Circuit Current [5]	IshortL			110	mA	Vout forced to VDD

[2] For the dual die version, the supply current is multiplied by 2.

[3] Idle current is the current that is drawn by the IC in the IDLE mode, where it can only receive new commands on the communication bus, but all other blocks are disabled. The analog (excluding the power-on-reset block) is disconnected, only the digital IO part allows clocking of a few vital gates.

[4] Standby current corresponds to the current consumed in the digital, where not the main oscillator is running which is used for analog sequencing, but only the low-power oscillator. This standby current is present in Burst mode or WOC mode; whenever the IC is counting down to start a new conversion.

[5] Not covered by final test, based on characterization data.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Leakage Current (5)	Ileak			20	nA	SDA
				0.1	nA	INT
				25	nA	MISO
				20	nA	SCLK, MS/CS

Table 8: Electrical Specification

12. Timing Specification

Timing conditions include the variations of supply, temperature and aging, unless specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Main Oscillator Frequency	F_{OSC}	0.95	1	1.05	MHz	T_A = 35°C
Main Oscillator Thermal Drift	F_{OSC_TH}	-5		5	%F_{OSC}	T_A within T_{AMB}
Low Power Oscillator Frequency	F_{LPOSC}	48	50	52	kHz	T_A = 35°C
LP Oscillator Thermal Drift	F_{LPOSC_TH}	-6		6	%F_{LPOSC}	T_A within T_{AMB}
Reset Time (POR and RT command) (6)	T_{POR}		1.3	2.4	ms	Time from STARTUP to IDLE
Initialization Time (6)	T_{INIT}		165		µs	Time from IDLE to start of conversion
Voltage Conversion Time (6)	$TCONV_V$	163		259	µs	VDD measurement F_{OSC} = 1MHz
Temperature Conversion Time (6)	$TCONV_T$	163		835(7)	µs	Programmable Signal Integration F_{OSC} = 1MHz
Magnetic Conversion Time (6)	$TCONV_M$	163		33347(8)	µs	Programmable Signal Integration F_{OSC} = 1MHz, single channel
Conversion Time (6)	TCONV	$TCONV_V$ + $TCONV_T$ + $TCONV_M$+11			µs	F_{OSC} = 1MHz
Output Data Rate (6)	ODR_{DC} ODR_{CONT}	1/(TCONV + T_{INIT}) 1/TCONV			µs	Duty Cycled Operation Continuous Operation
Interval Time (6)	T_{INT}	0		1260(9)	ms	Time in between conversion cycles (F_{LPOSC} = 50kHz)
Trigger Pulse Width (6)	T_{TRIG}	0.01		250	µs	Active High
Memory Store time (6)	T_{HS_WAIT}			15	ms	T_A within T_{AMB}

Table 9: General Timing Specification

[6] *Not covered by final test, based on characterization data.*
[7] *$(2^{OSR2}*96)+67$. See section 18.4 for more information about filters.*
[8] *$m*\{[(2+2^{DIGFILT})*2^{OSR}*32]+67\}$, m = selectable 0 to 3 (XYZ) axes. See section 18.4 for more information about filters.*
[9] *BURST_DATA_RATE*20.*

13. Temperature Specification

The MLX90395 allows for measuring of the junction temperature for on-chip thermal compensations as well as off-chip thermal information within the application, provided there is proper modeling of the junction temperature to application temperature.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Temperature Sensor Resolution	T_{RES}		50		LSB_{14}/°C	
Temperature Sensor Output 0°C	T_0		0		LSB_{14}	
Temperature Sensor Output 35°C	T_{35}		1750		LSB_{14}	Calibration Temperature
Temperature Sensor Linearity	T_{LIN}	-2		+2	°C	
Temperature Sensor Accuracy	T_{ACC}	0		+10	°C	$T_A \leq 35$°C
Temperature Sensor Accuracy	T_{ACC}	-1		+7	°C	$T_A > 35$°C

Table 10: Temperature Specification

14. Voltage Specification

The MLX90395 allows for measurement of the supply voltage for ADC plausibility checks as well as for monitoring battery discharge in battery powered applications.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Voltage Resolution	V_{RES}		5500		LSB_{16}/V	
Voltage Output for 3V	V_{3V}		16500		LSB_{16}	
Voltage Output for 2V	V_{2V}		11000		LSB_{16}	
Voltage Linearity	V_{LIN}	-20		20	mV	
Voltage Accuracy	V_{ACC}	-200		200	mV	

Table 11: Voltage Specification

15. Magnetic Field Requirements

This section describes the magnetic field requirements in order to meet the performance described in section 16.

15.1. Medium-Field Variant (-0xx code)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Magnetic Flux Density in X or Y	B_X, B_Y			55[10]	mT	$\sqrt{B_X^2 + B_Y^2}$
Magnetic Flux Density in Z	B_Z			130	mT	
IMC Gain in X and Y	G_{IMC_XY}	1.5		1.8		
IMC Gain in Z	G_{IMC_Z}	1		1.2		
k factor	k	1.3		1.7		G_{IMC_XY} / G_{IMC_Z}

Table 12: Magnetic field requirement for Medium-Field Variant

15.2. High-Field Variant (-1xx code)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Magnetic Flux Density in X or Y	B_X, B_Y			120[10]	mT	$\sqrt{B_X^2 + B_Y^2}$
Magnetic Flux Density in Z	B_Z			130	mT	
IMC Gain in X and Y	G_{IMC_XY}	0.4		0.6		
IMC Gain in Z	G_{IMC_Z}	1.1		1.2		
k factor	k	0.3		0.5		G_{IMC_XY} / G_{IMC_Z}

Table 13: Magnetic field requirement for High-Field Variant

[10] *Above this value, the IMC starts saturating yielding to an increase of the linearity error*

16. Accuracy Specification

16.1. Medium-Field Variant (-0xx code)

Magnetic Specifications (with **Melexis default factory programming**) are valid for temperature range: -40 - 125°C, supply voltage range: 2.6/3.0 - 3.6V unless otherwise noted (condition).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
ADC Internal Resolution	N_{ADCINT}		17.2		bits	
ADC External Resolution	N_{ADCEXT}		16		bits	
Sensing Range	$B_{RANGE50}$		50		mT	
Offset [11]	X_0, Y_0, Z_0	-150		150	LSB_{16}	T_A within T_{AMB}
Sensitivity X- or Y-axis [12]	S_{XX50}, S_{YY50}		2.5 400		$\mu T/LSB_{16}$ LSB_{16}/mT	
Sensitivity Accuracy X- or Y-axis		-8		8	%	T_A = 35°C
Sensitivity Temperature Coefficient X- or Y-axis	T_{CSXY}	-500		500	ppm/°C	T_A within T_{AMB}
Sensitivity Z-axis [13]	S_{ZZ50}		2.5 400		$\mu T/LSB_{16}$ LSB_{16}/mT	
Sensitivity Accuracy Z-axis		-10		10	%	T_A = 35°C
Sensitivity Temperature Coefficient Z-axis	T_{CSZ}	-600		600	ppm/°C	T_A within T_{AMB}
Mismatch on the Raw Signals X, Y and Z [14]	S_{MISMXY} S_{MISMXZ} S_{MISMYZ}	-2 -5 -5		2 5 5	%	T_A = 35°C
Thermal Drift of Sensitivity Mismatch		-3		3	%	T_A within T_{AMB}
Cross-Axis Sensitivity (intrinsic)	S_{XYi}, S_{YXi}, S_{XZi}, S_{ZXi}, S_{YZi}, S_{ZYi}	-5		5	%	T_A = 35°C
Noise				275 350 450	µT rms µT rms µT rms	T_A = 35°C T_A = 85°C T_A = 125°C 0 µT field
Hysteresis				60	LSB_{16}	T_A = 35°C

Table 14: Accuracy Specification for Medium-Field Variant

[11] *The thermal offset drift will be within a +/-30LSB window, by characterization.*

[12] *Sensitivity can be adjusted with the parameter SENSXY, RESX and RESY. See section 18.6 for more details.*

[13] *Sensitivity can be adjusted with the parameter SENSZ and RESZ. See section 18.6 for more details.*

[14] *Die rotation tolerances (tilt die) of +/-2° included.*

16.2. High-Field Variant (-1xx code)

Magnetic Specifications (with **Melexis default factory programming**) are valid for temperature range: -40 - 125°C, supply voltage range: 2.6/3.0 - 3.6V unless otherwise noted (condition).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
ADC Internal Resolution	N_{ADCINT}		17.2		bits	
ADC External Resolution	N_{ADCEXT}		16		bits	
Sensing Range	$B_{RANGE120}$		120		mT	
Offset [15]	X_0, Y_0, Z_0	-150		150	LSB_{16}	T_A within T_{AMB}
Sensitivity X- or Y-axis [16]	S_{XX120}, S_{YY120}		7.14 140		$\mu T/LSB_{16}$ LSB_{16}/mT	
Sensitivity Accuracy X- or Y-axis		-8		8	%	T_A = 35°C
Sensitivity Temperature Coefficient X- or Y-axis	T_{CSXY}	-500		500	ppm/°C	T_A within T_{AMB}
Sensitivity Z-axis [17]	S_{ZZ120}		7.14 140		$\mu T/LSB_{16}$ LSB_{16}/mT	
Sensitivity Accuracy Z-axis		-10		10	%	T_A = 35°C
Sensitivity Temperature Coefficient Z-axis	T_{CSZ}	-600		600	ppm/°C	T_A within T_{AMB}
Mismatch on the Raw Signals X, Y and Z [18]	S_{MISMXY} S_{MISMXZ} S_{MISMYZ}	-2 -5 -5		2 5 5	%	T_A = 35°C
Thermal Drift of Sensitivity Mismatch		-3		3	%	T_A within T_{AMB}
Cross-Axis Sensitivity (intrinsic)	S_{XYi}, S_{YXi}, S_{XZi}, S_{ZXi}, S_{YZi}, S_{ZYi}	-5		5	%	T_A = 35°C
Noise				1080 1250 1650	µT rms µT rms µT rms	T_A = 35°C T_A = 85°C T_A = 125°C 0 µT field
Hysteresis				60	LSB_{16}	T_A = 35°C

Table 15: Accuracy Specification for High-Field Variant

[15] The thermal offset drift will be within a +/-30LSB window, by characterization.

[16] Sensitivity can be adjusted with the parameter SENSXY, RESX and RESY. See section 18.6 for more details.

[17] Sensitivity can be adjusted with the parameter SENSZ and RESZ. See section 18.6 for more details.

[18] Die rotation tolerances (tilt die) of +/-2° included.

17. Functional Description

17.1. Operating Modes

The MLX90395 always acts as slave on the bus. It operates with 3 state machines:

- Measurement State Machine – running off the Main Oscillator
- Low Power State Machine – running off the Low Power Oscillator
- Communication State Machine – running off the bus clock

The three operating modes are controlled and defined by the master. All modes can be enabled and disabled at runtime through the communication protocol. On reset, the device is in idle mode, waiting for commands.

The components (field in X, Y or Z direction, temperature and voltage) which are needed to be measured can be provided when sending the commands. The order of conversion is fixed, and components which are not needed are simply skipped.

It is the user's responsibility to read back the data and ensure that timings are met. The MLX90395 is purely a slave. Even in burst mode, the user is responsible to collect the data from the MLX90395.

Operating Mode	Start of Mode	End of Mode (Return to IDLE)	Measurement Data
Single Measurement	SM command TRG pin rising edge	Measurement finished	Argument of SM command or BURST_SEL register content if empty argument BURST_SEL register if empty argument, provided SM command has been issued once in the past
Burst Mode	SB command	EX command	Argument of SB command or BURST_SEL register content if empty argument
Wake-up On Change (WOC) Mode	SWOC command	EX command	Argument of SWOC command or BURST_SEL register content if empty argument

Table 16: Summary of the operating modes

17.1.1. Single Measurement

In single measurement mode, a single measurement is requested by the master through either the SM command or via a rising edge on the TRG pin. After finishing the measurement, the INT pin will go high and the MLX90395 will go back to idle mode. The measurement can be read out at any time by means of the RM command. This will clear the INT pin.

17.1.2. Burst Mode

In burst mode, the MLX90395 will continuously make measurements. The mode is started with the SB command and can be ended with the EX command. Measurements are read by the RM command and the status byte will indicate the freshness of the data. The rate of measurements is programmable. Each time a measurement is finished, the INT pin will go high. Reading out the data will clear the INT pin. If the measurement is not read on time, it will be overwritten by the next measurement when ready. The INT pin will show again a rising edge when the set of measurements can be read out. As long as the INT pin is high, the data is ensured to be most recent and ready.

In burst mode, the only allowed commands are RM and EX. In case a different command is sent, the status will show a communication error. In case of SPI, this status is sent right after the first byte is received (even for multi byte commands).

17.1.3. Wake-up on Change Mode

In wake-up on change mode, the MLX90395 will continuously make measurements. The mode is started with the SWOC command and can be ended with the EX command. Measurements can be read by the RM command, and the status byte will indicate the freshness of the data. Also here the rate of measurements is programmable. This mode differs from the burst mode in the sense that the INT pin will not go high at each finish of measurements but go high only when a specific condition is met. This condition can be controlled by the user:

- Absolute mode: each measurement is compared with the initial one (first measurement after start of the WOC mode). If the difference is larger than the threshold, then the INT pin goes high. The pin is cleared by the RM command.
- Differential mode: each measurement is compared with the previous one. If the difference is larger than the threshold, then the INT pin goes high. The pin is cleared by the RM command.

Comparisons are done on the 16-bit output data, independent of the resolution programmed.

In WOC mode, the only allowed commands are RM and EX. In case a different command is sent, the status will show a communication error. In case of SPI, this status is sent right after the first byte is received (even for multi byte commands).

17.2. Flow Chart

The flow chart below shows the different states the sensor can be in and how they are related for different measurement types. In case of an exit command, the measurement is first finished, and the loop is ended via the SM path.

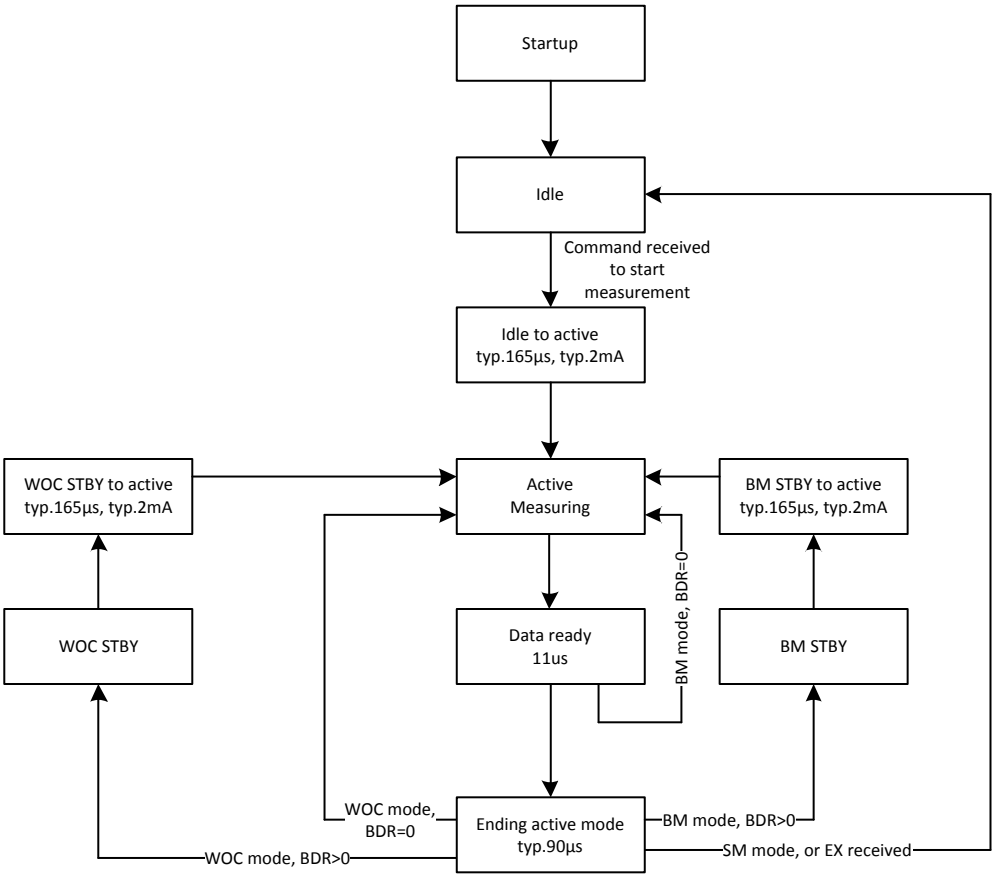


Figure 4: Flow Chart (BDR = BurstDataRate)

17.3. Status Byte

A status byte is provided on nearly each command (RT does not return a status byte). Depending on the operating mode, the interpretation differs.

Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Burst Mode	1	Measurement Counter			CE / DED	OVF	RST	DRDY
WOC Mode	0	1	0	0	CE / DED	OVF	RST	DRDY
SM Mode	0	0	1	0	CE / DED	OVF	RST	DRDY
Idle	0	0	0	0	CE / DED	OVF	RST	DRDY
Memory	0	0	0	0	CE / DED	SEC	RST	DRDY

Table 17: Status Byte

The SB command is always replied with a “Burst Mode” status, the SWOC command by a “WOC Mode” status. When the SM command is successfully received, an “SM Mode” status is given.

For the RM and RV command, the status returned purely depends on the mode in which the IC is operating. For single measurement mode, if the measurement is finished, the “Idle” status byte is given.

An EX command, when successfully received is replied with an “Idle” status byte.

Memory commands (HR, HS, RR and WR) are replied with the “Memory” status byte.

In case of an illegal command (RR in burst mode for example) then the status will be the one of the mode currently in, not necessarily the one associated with the command. The command got rejected, and the CE bit is set.

Melexis recommends verifying that the status byte matches the expected value.

17.3.1. Data Ready - DRDY

This flag is set to 1 to indicate that new data is ready (not yet read), or when it is the first time that this data is being read. This flag is updated after the measurement is done.

In burst mode, there is a 10µs window just before the measurement (and measurement counter) is updated, where the flag is always zero, even if the data has not yet been read.

17.3.2. Reset - RST

The reset flag is set whenever the IC has gone through a power-on reset (cold reset through V_{DD} cycling or warm reset through RT command).

17.3.3. Single Bit Error Corrected - SEC

If set, a single bit error is detected in the NVRAM, and the bit is corrected.

17.3.4. Double Bit Error Detected - DED

If set, a double bit error is detected in the NVRAM. Once this bit is set, it will be latched until the problem is cleared (eg. by a write operation to the inconsistent register).

17.3.5. Overflow - OVF

If set, it indicates that the MSBit of the ADC (bit 18) is set. This situation should not occur, and could indicate a failure in the analog front-end of the IC.

17.3.6. Communication Error - CE

This flag is set in case a communication error is detected. It can be that a wrong command is set (or too early), or a command which was not allowed on a specific operating mode.

17.3.7. Measurement Counter

The 3-bit measurement counter is present in burst mode and is increased on each measurement. This allows the user to know if a measurement is missed when for example the RM commands are not in sync with the measurement rate.

17.4. Measurement CRC

The measured data is protected with a CRC in order to provide a data integrity check at master side. The CRC is implemented as 8-bit CRC-8-CCITT (polynomial 0x07) on the totality of the measured data. The calculation is always done with 10 bytes of data in the order X[15:8], X[7:0], Y[15:8], Y[7:0], Z[15:8], Z[7:0], T[15:8], T[7:0], V[15:8], V[7:0]. Components which are not measured are to be filled out with 0x00.

17.4.1. CRC calculation

The below describes the CRC calculation. Also an example is provided to show the CRC calculation in action.

```
// Code                          // Example
crc = 0x00;                      crc = 0x00;
crc = CRC_TABLE[crc ^ X[15:8]];  0x00 = CRC_TABLE[0x00 ^ 0x00];
crc = CRC_TABLE[crc ^ X[7:0]];   0x00 = CRC_TABLE[0x00 ^ 0x00];
crc = CRC_TABLE[crc ^ Y[15:8]];  0x89 = CRC_TABLE[0x00 ^ 0x80];
crc = CRC_TABLE[crc ^ Y[7:0]];   0xB6 = CRC_TABLE[0x89 ^ 0x00];
crc = CRC_TABLE[crc ^ Z[15:8]];  0x0B = CRC_TABLE[0xB6 ^ 0x00];
crc = CRC_TABLE[crc ^ Z[7:0]];   0x31 = CRC_TABLE[0x0B ^ 0x00];
crc = CRC_TABLE[crc ^ T[15:8]];  0x8C = CRC_TABLE[0x31 ^ 0x05];
crc = CRC_TABLE[crc ^ T[7:0]];   0x5F = CRC_TABLE[0x8C ^ 0x26];
crc = CRC_TABLE[crc ^ V[15:8]];  0x9A = CRC_TABLE[0x5F ^ 0x00];
crc = CRC_TABLE[crc ^ V[7:0]];   0xCF = CRC_TABLE[0x9A ^ 0x00];
```

The CRC table is shown below

```
CRC_TABLE[256] = {
    0x00, 0x07, 0x0E, 0x09, 0x1C, 0x1B, 0x12, 0x15,
    0x38, 0x3F, 0x36, 0x31, 0x24, 0x23, 0x2A, 0x2D,
    0x70, 0x77, 0x7E, 0x79, 0x6C, 0x6B, 0x62, 0x65,
    0x48, 0x4F, 0x46, 0x41, 0x54, 0x53, 0x5A, 0x5D,
    0xE0, 0xE7, 0xEE, 0xE9, 0xFC, 0xFB, 0xF2, 0xF5,
    0xD8, 0xDF, 0xD6, 0xD1, 0xC4, 0xC3, 0xCA, 0xCD,
    0x90, 0x97, 0x9E, 0x99, 0x8C, 0x8B, 0x82, 0x85,
    0xA8, 0xAF, 0xA6, 0xA1, 0xB4, 0xB3, 0xBA, 0xBD,
    0xC7, 0xC0, 0xC9, 0xCE, 0xDB, 0xDC, 0xD5, 0xD2,
    0xFF, 0xF8, 0xF1, 0xF6, 0xE3, 0xE4, 0xED, 0xEA,
    0xB7, 0xB0, 0xB9, 0xBE, 0xAB, 0xAC, 0xA5, 0xA2,
    0x8F, 0x88, 0x81, 0x86, 0x93, 0x94, 0x9D, 0x9A,
    0x27, 0x20, 0x29, 0x2E, 0x3B, 0x3C, 0x35, 0x32,
    0x1F, 0x18, 0x11, 0x16, 0x03, 0x04, 0x0D, 0x0A,
    0x57, 0x50, 0x59, 0x5E, 0x4B, 0x4C, 0x45, 0x42,
    0x6F, 0x68, 0x61, 0x66, 0x73, 0x74, 0x7D, 0x7A,
    0x89, 0x8E, 0x87, 0x80, 0x95, 0x92, 0x9B, 0x9C,
    0xB1, 0xB6, 0xBF, 0xB8, 0xAD, 0xAA, 0xA3, 0xA4,
    0xF9, 0xFE, 0xF7, 0xF0, 0xE5, 0xE2, 0xEB, 0xEC,
    0xC1, 0xC6, 0xCF, 0xC8, 0xDD, 0xDA, 0xD3, 0xD4,
    0x69, 0x6E, 0x67, 0x60, 0x75, 0x72, 0x7B, 0x7C,
    0x51, 0x56, 0x5F, 0x58, 0x4D, 0x4A, 0x43, 0x44,
    0x19, 0x1E, 0x17, 0x10, 0x05, 0x02, 0x0B, 0x0C,
    0x21, 0x26, 0x2F, 0x28, 0x3D, 0x3A, 0x33, 0x34,
    0x4E, 0x49, 0x40, 0x47, 0x52, 0x55, 0x5C, 0x5B,
    0x76, 0x71, 0x78, 0x7F, 0x6A, 0x6D, 0x64, 0x63,
    0x3E, 0x39, 0x30, 0x37, 0x22, 0x25, 0x2C, 0x2B,
    0x06, 0x01, 0x08, 0x0F, 0x1A, 0x1D, 0x14, 0x13,
    0xAE, 0xA9, 0xA0, 0xA7, 0xB2, 0xB5, 0xBC, 0xBB,
    0x96, 0x91, 0x98, 0x9F, 0x8A, 0x8D, 0x84, 0x83,
    0xDE, 0xD9, 0xD0, 0xD7, 0xC2, 0xC5, 0xCC, 0xCB,
    0xE6, 0xE1, 0xE8, 0xEF, 0xFA, 0xFD, 0xF4, 0xF3
};
```

17.5. Commands

In the commands with zyxt in their first byte, the zyxt is used to select which components need to be measured (set corresponding bit to 1). zyxt = 0x0 results in all components being measured according the settings of VmeasEn and BurstSel (X, Y, Z, T and V). Else, the components of the zyxt argument are measured. With temperature compensation enabled, the temperature will always be measured. However depending on the argument zyxt, it can be read out or not (for CRC calculation it will be 0x0). Recommended is to do the measurement and the read command with the same zyxt argument.

It is not allowed to use the Reset command (RT) during any mode (Single Measurement Mode, Burst Mode, WOC Mode). The Exit Mode command (EX) has to be used to end a mode. The Reset command can be applied at least 1ms following the Exit command, if required.

Name	Symbol	#	CMD Byte #1	CMD Byte #2	CMD Byte #3	CMD Byte #4
Start Burst Mode	SB	1	0b0001 zyxt	N/A	N/A	N/A
Start WOC Mode	SWOC	2	0b0010 zyxt	N/A	N/A	N/A
Start Single Measurement Mode	SM	3	0b0011 zyxt	N/A	N/A	N/A
Read Measurement (SPI)	RM	4	0b0100 zyxt	N/A	N/A	N/A
Read Register (SPI)	RR	5	0b0101 dddd [19]	REG[5:0] << 2	N/A	N/A
Write Register (SPI)	WR	6	0b0110 dddd [19]	DATA[15:8]	DATA[7:0]	REG[5:0] << 2
Exit Mode	EX	8	0b1000 0000	N/A	N/A	N/A
Read Voltage	RV	C	0b1100 dddd [19]	N/A	N/A	N/A
Memory Recall	HR	D	0b1101 dddd [19]	N/A	N/A	N/A
Memory Store	HS	E	0b1110 dddd [19]	N/A	N/A	N/A
Reset	RT	F	0b1111 0000	N/A	N/A	N/A

Table 18: Command overview

Register access is always done per word (=2 bytes).

In SPI commands, the register equals the word-address, and is shifted by two bits to the left. To access register 0x01, the corresponding command byte becomes 0x04.

For I^2C, the RR and WR commands do not exist, but direct register access is available through the I^2C protocol. More information is found in section 17.7.

17.6. SPI Communication

The SPI protocol is of mode 3, which means that data is clocked on rising edge of the clock and the clock is at a high level in idle (CPOL=1, CPHA=1). MSbits are sent first. CS must be high after command completion and whenever the IC is not communicated with. With CS low the IC will wait for communication to occur.

Note that MISO and MOSI can be shorted together to allow for 3-wire SPI (mind the increased capacitance). This implies that the SPI output of MLX90395 is half-duplex. There is one danger, in case of an illegal command with more than 1 command byte, the IC immediately sends out the status byte after receiving the

[19] *d stands for "don't care". These bits are not checked and can be both 0 and 1.*

first byte. This leads to a collision on the bus. Illegal commands like this are RR and WR in burst or WOC mode. Always allow the current measurement to be finished too after sending the EX command, before sending other commands.

17.6.1. Command implementation

For the examples give, the below convention is used.



Figure 5: SPI convention

17.6.1.1. SB, SWOC, SM, EX, HR, HS

All the commands follow the structure below. The reply from the MLX90395 is only the status byte. The example below is for a start of a burst mode with X and Y being measured.

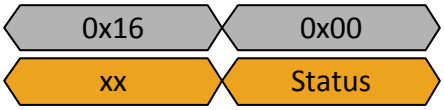


Figure 6: SB command, XY

After the HS command, wait at least 15ms before sending the next command to allow the IC to update the NVRAM correctly.

17.6.1.2. RT

This command will (warm-)reset the IC. The status byte of the command following will indicate the reset event.

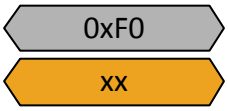


Figure 7: RT command

17.6.1.3. RM

This command differs depending on the value for zyxt. In case it is different than 0, the data is returned in the order Status-T-X-Y-Z-CRC, where the components which are set to zero are skipped. In case zyxt is 0, the returned order is Status-CRC-X-Y-Z-T-V (none skipped, unmeasured data is set to 0). The below three examples show this.

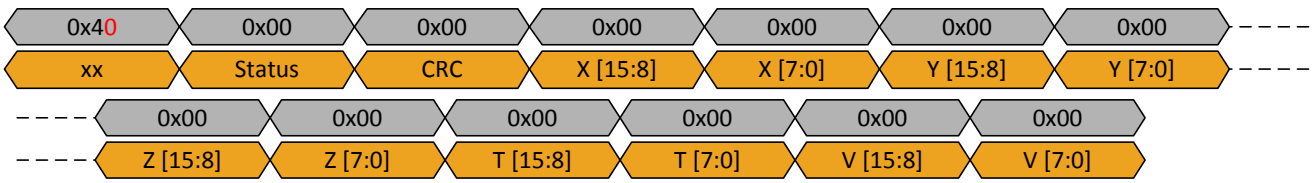


Figure 8: RM command, XYZTV

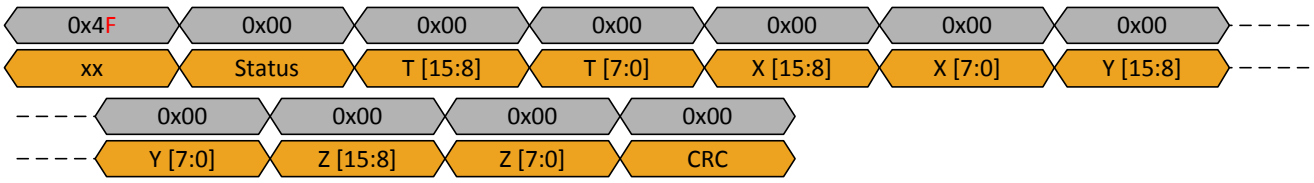


Figure 9: RM command, XYZT

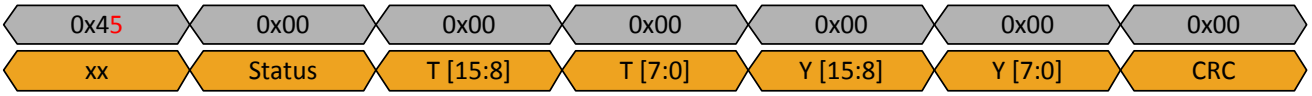


Figure 10: RM command, YT

17.6.1.4. RR

Important in this command is that the register address to be read needs to be shifted left by two bits. To read register 0x12 for example, the MOSI byte becomes 0x48.

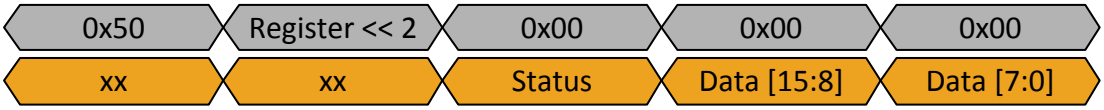


Figure 11: RR command

17.6.1.5. WR

Important in this command is that the register address to be read needs to be shifted left by two bits. To read register 0x12 for example, the MOSI byte becomes 0x48.

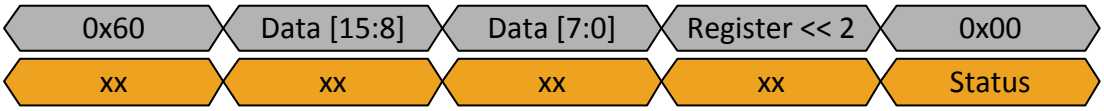


Figure 12: WR command

17.6.1.6. RV

In case RM with 0 as zyxt is done, V can be returned. To get the data faster without the X, Y, Z and T (all zero) also being clocked out, the RV command can be used.

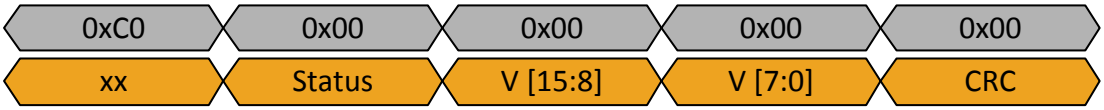


Figure 13: RV command

17.6.2. SPI Timing Specification

All timings are referred to the levels found in Table 8.

Electrical Parameter	Symbol	Min.	Max.	Unit
SPI Clock Cycle	t_c (SPC)	100		ns
SPI Clock Cycle	t_c (SPC)		10	MHz
CS Setup Time	t_{su} (CS)	5		ns
CS Hold Time	t_h (CS)	10		ns
SDI Input Setup Time	t_{su} (SI)	5		ns
SDI Input Hold Time	t_h (SI)	15		ns
SDO Valid Output Time	t_v (SO)		50	ns
SDO Output Hold Time	t_h (SO)	5		ns
SDO Output Disable Time	t_{dis} (SO)		50	ns

Table 19: General SPI Timing Specification

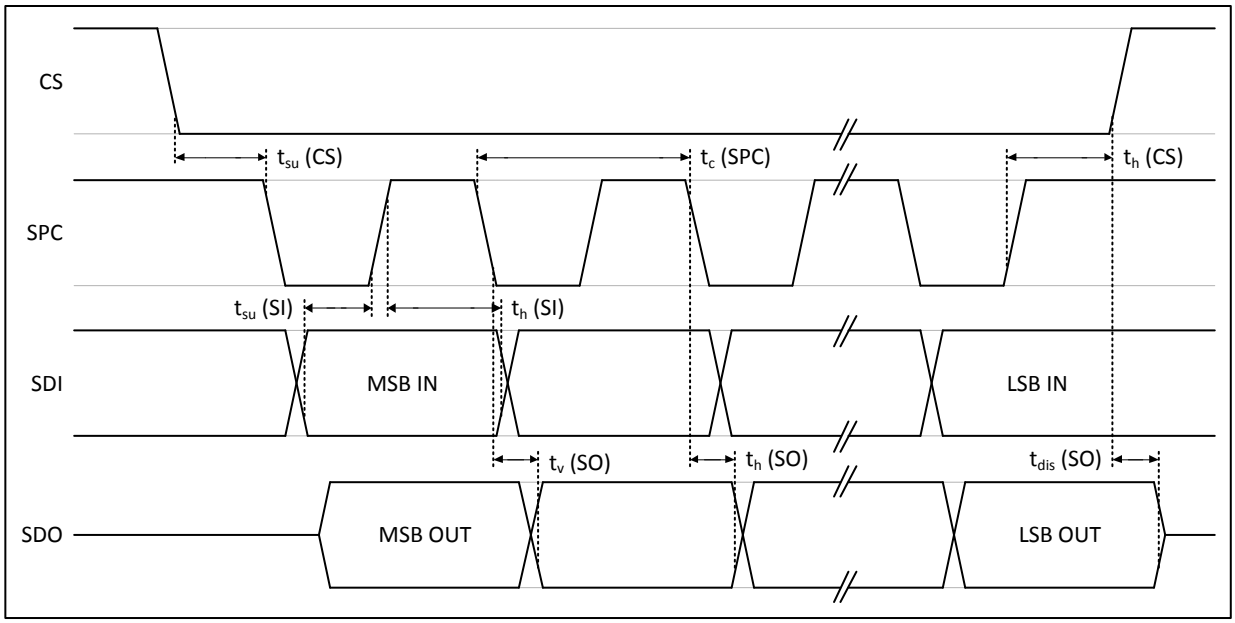


Figure 14: SPI Timing Diagram

17.6.3. EMC filter (not re-programmable) - Not available in BAA version

An RC filter is enabled on the SPI communication input lines. The impact of this filter is that 1MHz is the maximum SPI clock frequency that the IC accepts. For other filter configurations, please contact Melexis.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SCLK RC Filter Bandwidth	BW_{1MHz}	2		4	MHz	
CS RC Filter Bandwidth	BW_{CS}	3.6		9.5	MHz	
MOSI RC Filter Bandwidth	BW_{MOSI}	4.75		9.15	MHz	

Table 20: SPI RC Filter Specifications

This feature is **not available in the BAA** version.

17.7. I²C Communication

The I²C protocol is implemented such that the command is written to a specific register (0x80) in the RAM, and the status and measurement data are read back from this RAM. The commands themselves are the same as for SPI (section 17.5) except for the read measurement commands and the memory read/write commands. For memory read/write commands, register access is provided directly through the I²C protocol. Note that memory read/write commands are required to be word-wise, so always in multiples of 2 bytes. The I2C protocol uses the byte address instead of the word address. Because a word contains 2 bytes, the byte address is double that of the word address or register. Hence in the I²C, the corresponding command byte becomes the register shifted by 1 bit to the left.

Read measurement is the same as a memory read, except starting from the status register. MSbits are sent first.

The 7-bit I²C-address is determined by the connection to the A0 and A1 pins. The 5 MSBs are programmed by Melexis in the MLX90395. Please contact Melexis in case other addressing is required.

7-bit I²C address							R/W bit
7	6	5	4	3	2	1	0
0	0	0	1	1	0 if A1 shorted to ground 1 if A1 shorted to supply	0 if A0 shorted to ground 1 if A0 shorted to supply	0 for I²C write 1 for I²C read

17.7.1. Command Implementation

For the examples given, the below convention is used.

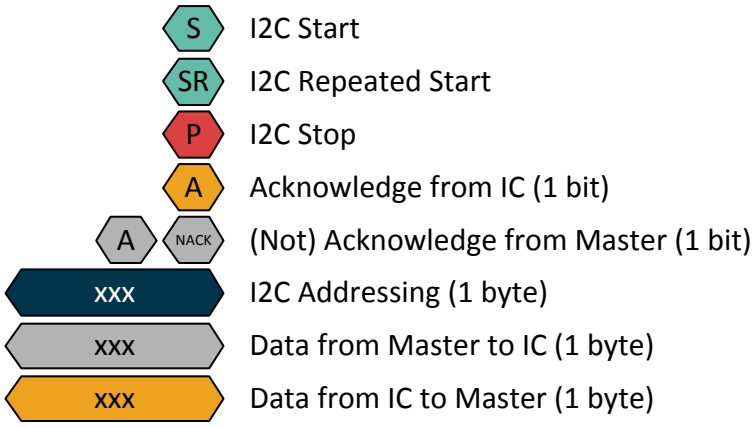


Figure 15: I²C Convention

17.7.1.1. SB, SWOC, SM, EX, HR, HS

All the commands follow the structure below. The reply from the MLX90395 is only the status byte. The example below is for a start of a burst mode with X and Y being measured.



Figure 16: SB command, XY

After the HS command, wait at least 15ms before sending the next command to allow the IC to update the NVRAM correctly.

17.7.1.2. RT

This command will (warm-)reset the IC. The status byte of the command following will indicate the reset event.

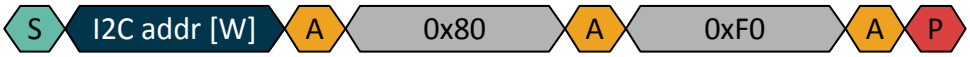


Figure 17: RT command

17.7.1.3. RM

All values which are not measured are 0x00.

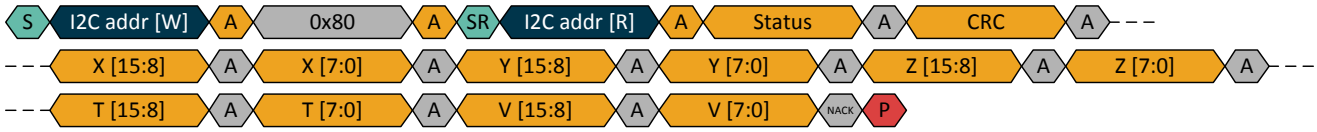


Figure 18: RM command

17.7.1.4. RR

Important in this command is that the register address to be read needs to be shifted left by one bit. To read register 0x12 for example, the SDA byte becomes 0x24.



Figure 19: RR command

17.7.1.5. WR

Important in this command is that the register address to be written needs to be shifted left by one bit. To write register 0x12 for example, the SDA byte becomes 0x24.



Figure 20: WR command

17.7.1.6. RV

In case RR with 0 as zyxt is done, only V will be returned. To get the data faster without the X, Y, Z and T (all zero) also being clocked out, the RV command can be used.



Figure 21: RV command

17.7.2. I²C Timing Specification

All timings are referred to the levels found in Table 8.

Electrical Parameter	Symbol	I²C Standard Mode		I²C Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f (SCL)		100		1000	kHz
SCL Clock Low Time	t_w (SCLL)	4.7		0.5		µs
SCL Clock High Time	t_w (SCLH)	4		0.26		µs
SDA Setup Time	t_{su} (SDA)	250		50		ns
SDA Data Hold Time	t_h (SDA)		3.45	0	0.45	µs
SDA and SCL Rise Time	t_r (SDA) t_r (SCL)		1000	20+0.1*C_b [20]	120	ns
SDA and SCL Fall Time	t_r (SDA) t_r (SCL)		300	20+0.1*C_b [20]	120	ns
START Condition Hold Time	t_h (ST)	4		0.26		µs
REPEATED START Condition Setup Time	t_{su} (SR)	4.7		0.26		µs
STOP Condition Setup Time	t_{su} (SP)	4		0.26		µs
Bus Free Time Between STOP and START Condition	t_w (SP:ST)	4.7		0.5		µs

Table 21: General I²C Timing Specification

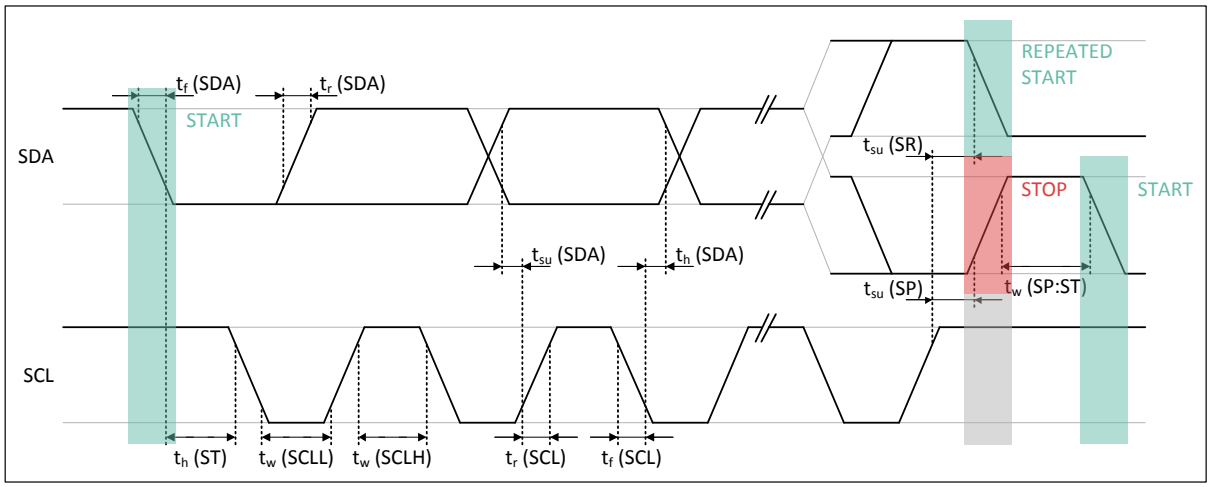


Figure 22: I²C Timing Diagram

[20] *Where C_b is the total bus capacitance (in pF).*

18. Memory Structure and End-User Programmable Items

18.1. NVRAM Endurance

The NVRAM is qualified to guarantee an endurance of minimum 1000 write cycles (store operations) at 125°C (for engineering/calibration purpose).

If operated above 90°C with less than 3.0V supply, the performance of the NVRAM is not guaranteed.

18.2. Memory Structure

The MLX90395 has 1kbit of non-volatile memory, and the same amount of volatile memory. Each memory consists out of 64 addresses containing 16-bit words. The non-volatile memory has automatic 2-bit error detection and 1-bit error correction capabilities per address. The handling of such corrections & detections is explained in Section 17.3.

The memory is split in 2 areas:

- Customer area [address 0x00 to 0x1F]
- Melexis area [address 0x20 to 0x3F]

The RR and WR commands impact the volatile memory only, there no direct access possible to the non-volatile memory. The customer area of the volatile memory is fully accessible (read and write) to the customer; the Melexis area is write-protected and contains the 48-bit unique identification. Only modifications in the customer area are allowed with the WR command. The adjustments in the customer area can be stored in the permanent non-volatile memory with the store command HS, which copies the entire volatile memory to the non-volatile memory. With the HR command the non-volatile memory content can be recalled to the volatile memory, which can restore any modifications due to prior WR commands. The HR step is performed automatically at start-up of the IC, either through cold reset or warm reset with the RT command.

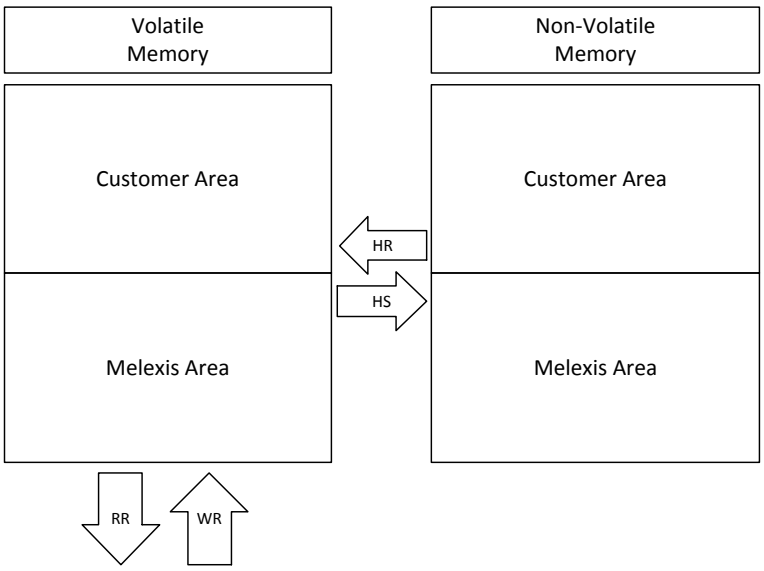


Figure 23: MLX90395 Memory Structure

18.3. Register Map

The table below gives an overview of the customer area in the MLX90395's NVRAM.

In the register map, the 16-bit words are split into 2 bytes for the sake of readability. The general format is shown below in the yellow table. [21]

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x..	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
	Bit 15 (MSB)	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	GainSel[3:0]				HallConf[3:0]			
	Lock_HS	Lock_WR	Reserved[21]	TrimDelSDAOut[1:0]		TrimDelSDAIn[1:0]		ZSeries
0x01	BurstSel[1:0]		BurstDataRate[5:0]					
	TrigIntSel	CommMode[1:0]		WOCDiff	ExtTrig	TCmpEn	BurstSel[3:2]	
0x02	ResY[0]	ResX[1:0]		DigFilt[2:0]			OSR[1:0]	
	OSR3	0x0	VMeasEn	OSR2[1:0]		ResZ[1:0]		ResY[1]
0x03	TRef[7:0]							
	-	-	-	-	-[21]	WOCStart	TRef[9:8]	
0x04	SensTCH[7:0]							
	-	-	-	-	-	-	-	SensTCH[8]
0x05	SensTCL[7:0]							
	-	-	-	-	-	-	-	SensTCL[8]
0x06	OffsetX[7:0]							
	OffsetX[15:8]							
0x07	OffsetY[7:0]							
	OffsetY[15:8]							
0x08	OffsetZ[7:0]							
	OffsetZ[15:8]							
0x09	OffsetDriftXL[7:0]							
	OffsetDriftXH[7:0]							
0x0A	OffsetDriftYL[7:0]							
	OffsetDriftYH[7:0]							
0x0B	OffsetDriftZL[7:0]							
	OffsetDriftZH[7:0]							
0x0C	SensXY[7:0]							
	-	-	-	-	-	-	SensXY[9:8]	
0x0D	SensZ[7:0]							
	-	-	-	-	-	-	SensZ[9:8]	
0x0E	WocXYThreshold[7:0]							
	WocXYThreshold[15:8]							

[21] Cells marked with "-" can be overwritten. Reserved cells are not to be changed.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	WocZThreshold[7:0]							
	WocZThreshold[15:8]							
0x10	WocTThreshold[7:0]							
	WocTThreshold[15:8]							
0x11	WocVThreshold[7:0]							
	WocVThreshold[15:8]							
0x12 - 0x1F	Free							
	Free							

For the RM command in I^2C, the register can be accessed byte-wise, with automatic increment. No left shift (as compared to the RR and RM commands in I^2C) is needed to access these registers.

Register I^2C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x80	Command/Status							
0x81	CRC-8-CCITT							
0x82	X[15:8]							
0x83	X[7:0]							
0x84	Y[15:8]							
0x85	Y[7:0]							
0x86	Z[15:8]							
0x87	Z[7:0]							
0x88	T[15:8]							
0x89	T[7:0]							
0x8A	V[15:8]							
0x8B	V[7:0]							

Melexis stores a unique ID in every single IC. This ID is stored in the following registers (Read-Only):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x26	ID1[7:0]							
	ID1[15:8]							
0x27	ID2[7:0]							
	ID2[15:8]							
0x28	ID3[7:0]							
	ID3[15:8]							

18.3.1. Default NVRAM content

Changing the default settings will impact the values in Table 12 and Table 13.

Parameter	Medium Field Version	High Field Version
HallConf	0	0
GainSel	9	8
ZSeries	0	0
TrimSelSDAIn	1	1
TrimSelSDAOut	0	0
Reserved	0 (keep zero) [22]	0 (keep zero) [22]
Lock_WR (not available in BAA)	0	0
Lock_HS (not available in BAA)	0	0
BurstDataRate	0	0
BurstSel	15 (0xF)	15 (0xF)
TCmpEn	1	1
ExtTrig	0	0
WOCDiff	0	0
CommMode	0	0
TrigIntSel	1	1
OSR	0	0
DigFilt	0	0
ResX	1	1
ResY	1	1
ResZ	1	1
OSR2	0	0
VMeasEn	0	0
OSR3	0	0
TRef	Trimmed to 35°C	Trimmed to 35°C
WOCStart **(check paragraph 18.8)**	0	0
SensTCH, SensTCL	Trimmed to 0ppm/°C	Trimmed to 0ppm/°C
OffsetX, OffsetY, OffsetZ	Trimmed to 0LSB	Trimmed to 0LSB
OffsetDriftXL, OffsetDriftXH, OffsetDriftYL, OffsetDriftYH, OffsetDriftZL, OffsetDriftZH	Trimmed to 0LSB/°C	Trimmed to 0LSB/°C
SensXY, SensZ	Trimmed to $400LSB_{16}$/mT	Trimmed to $140LSB_{16}$/mT
WocXYThreshold, WocZThreshold, WocTThreshold, WocVThreshold	0	0

Table 22: Default NVRAM content

[22] *If enabled, the magnetic measurements will be corrupted and current consumption is increased.*

18.4. Measurement Filters

The MLX90395 has several options to filter the measurements. The first type is available for all components: the oversampling rate OSR) of the decimation filter at the ADC. OSR is for magnetic measurements, OSR2 for the temperature measurement and OSR3 for the voltage measurement. The second type is an averaging filter (DigFilt, averaging over $2^{DigFilt}$ measurements) which is only present on the magnetic measurements.

Changing these parameters directly impacts the typical conversion time per measurement. This according the formulas below:

$$T_{mag}[\mu s] = 67 + 32 \cdot 2^{OSR} \cdot \left(2 + 2^{DigFilt}\right)$$

$$T_{temp}[\mu s] = 67 + 96 \cdot 2^{OSR2}$$

$$T_{V}[\mu s] = 67 + 96 \cdot 2^{OSR3}$$

The MLX90395 offers a 2kHz 3-axis (magnetic) measurement or 2kHz 2-axis + temperature if the filter and oversampling rate are set to 0:

$$T_{3-axis} = 3 \cdot [67 + 32 \cdot 2^0 \cdot (2 + 2^0)] + 11 = 500\ \mu s$$

$$T_{2-axis\,+\,temperature} = 67 + 96 \cdot 2^0 + 2 \cdot [67 + 32 \cdot 2^0 \cdot (2 + 2^0)] + 11 = 500\ \mu s$$

Note that with OSR=0, the three LSBits of the 19-bit ADC are 0. This is because they cannot be determined accurately in the short integration time.

18.5. Communication and I²C Filters

The communication mode in which the MLX90395 needs to respond to is selectable by CommMode.

CommMode	Accepted Protocol	MS pin
0b00 or 0b01	I²C and SPI (first come, first serve)	Keep high for I²C Use as Chip Select (CS) for SPI
0b10	SPI only	CS pin for SPI
0b11	I²C only	Keep high for 200 µs after POR, then don't care

Table 23: CommMode

Due to NXP's specification on I²C, where is stated that the delay between SDA and SCL toggling can be 0µs, there is a delay implemented on the SDA line (when data from µController to IC) to ensure that the IC can properly decode the commands. This parameter is called TrimDelSDAIn, and can be programmed as follows:

- 0b00: 70ns
- 0b01: 110ns (recommended)
- 0b10: 140ns
- 0b11: 160ns

TrimDelSDAOut controls the delay (when data from IC to µController) between SCL switching from high to low and SDA toggling to the new data bit value. This is indicated on the below picture. The delay is also present on the acknowledge of the IC.

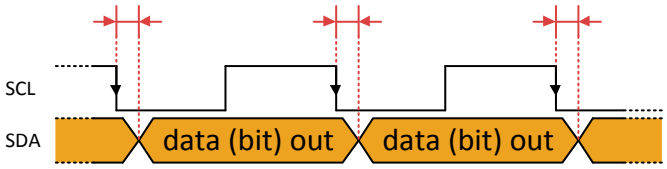


Figure 24: TrimDelSDAOut Definition

The delay is programmed follows:

- 0b00: 80ns (recommended)
- 0b01: 110ns
- 0b10: 130ns
- 0b11: 150ns

Note: These delays are only active after a reset, so a memory store command is needed.

18.6. Sensitivity

The sensitivity in LSB_{16} out vs. magnetic field applied can be adjusted in the MLX90395 with several parameters. GainSel changes the gain stages before the input of the ADC. Table 24 provides the relative gain/attenuation for these 2 stages.

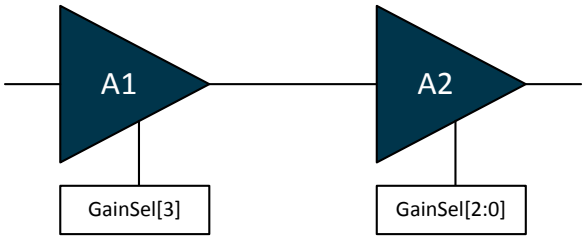


Figure 25: Gain Stages

GainSel[3]	GainSel[2:0]	Gain A1	Gain A2	Total Gain (A1 x A2)
0	0	1	0.2	0.2
0	1	1	0.25	0.25
0	2	1	1/3	1/3
0	3	1	0.4	0.4
0	4	1	0.5	0.5
0	5	1	0.6	0.6
0	6	1	0.75	0.75
0	7	1	1	1
1	0	0.5	0.2	0.1
1	1	0.5	0.25	0.125
1	2	0.5	1/3	1/6
1	3	0.5	0.4	0.2
1	4	0.5	0.5	0.25
1	5	0.5	0.6	0.3
1	6	0.5	0.75	0.375
1	7	0.5	1	0.5

Table 24: Relative Gain Table

SensXY and SensZ adjust the sensitivity after the ADC, so fully digital. SensXY and SensZ are always positive.

With ResX, ResY, and ResZ, 16 bits of the 19-bit ADC value can be selected. An increase of this parameter leads to a change in sensitivity by factor 2. Note that for resolution 2 and 3, the saturation of the analog chain becomes visible. The used span is 17.2 bits, of the 19 available bits.

For small adjustments, it is recommended to use SensXY, SensZ and the ResX, ResY, ReZ parameters. It is recommended to keep GainSel constant as an optimization is done to be at the optimal range at the input of the ADC. The default for resolution is 1, and for GainSel it is 9 for the medium field version and 8 for the high field version.

The relation on the measurements for SensXY and SensZ is given by the formula below:

$$MAG = MAG \times \left[1 + \frac{SensXY\ or\ SensZ}{2^9}\right]$$

For ResX, ResY, and ResZ, the below figure shows the implementation:

19-bit output (after corrections are applied)																		
18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			Selected bits for resolution 0															
		Selected bits for resolution 1																
	Selected bits for resolution 2																	
Selected bits for resolution 3																		

18.7. Offset

The offset on the magnetic output of the MLX90395 can be adjusted. This is done by parameters OffsetX, OffsetY, and OffsetZ. Important to note is that the parameter is implemented as unsigned 16-bit code. This means that 0x8000 (default value) corresponds to no offset adjustment. Also important is that the offset is adjusted right on the 19-bit ADC value, so before the sensitivity adjustments, thermal compensations and resolution selection.

$$MAG = MAG - 4 \cdot OFFSET_{X/Y/Z}$$

18.8. Burst and WOC Parameters

In burst mode and in WOC mode, the rate of measurements can be selected, as well as the components to be measured. The rate is adjusted by BurstDataRate, in steps of 20ms (min = 0ms, max is 1260ms). This time is measured between the finish of the previous set of measurements and the start of the next set of measurements.

BurstSel selects the components to be measured if this is not given by the command initially. The bit order is Z (MSbit), Y, X, T (LSbit).

Selection between differential and absolute WOC mode is done with WOCDiff. Set to 1 for differential mode.

Finally, the thresholds for each of the components (X and Y, Z, T, and V) can be set by WocXYThreshold, WocZThreshold, WocTThreshold, and WocVThreshold.

WOCStart can be set to force the IC in WOC mode after power-on. **Note that this mode, if WOCStart is set, can never be ended.** No commands will be accepted, except for the RM command. But note that the data itself is not synchronized (same for CRC). This mode is intended for use only with the INT pin, not for communication.

18.9. Thermal Drift

The user can choose to enable the temperature compensation. This is done with the TCmpEn parameter. Set it to enable the on-chip thermal offset drift and thermal sensitivity drift compensation.

Thermal sensitivity drift and thermal offset drift are trimmed by Melexis in order to minimize the error. In case the user wishes to change the parameters, this is possible but not recommended. For information, the formulas below show the usage of the parameters SensTCH, SensTCL (both always positive) and OffsetDrift* (2's complement format).

Parameters denoted with L are for used for low temperatures, below TRef, parameters with H are for high temperatures, above TRef. Tref can only be set positive, and TRef[9:0] maps to T[13:4] of the output

temperature value. With a slope of 50LSB/°C, this corresponds to a resolution of 0.32°C (=0.02<<4). All calculations are done on the 19-bit data.

First offset corrections: $MAG = MAG - 4 \cdot Offset - \frac{\left[OffsetDrift \times \left(\frac{T_{OUT}}{2^4} - TRef\right)\right]}{2^6}$

Then sensitivity corrections: $MAG = MAG \times \left[1 + \frac{Sens}{2^9}\right] \times \left[1 + \frac{\left[\left(\frac{SensTC}{2^4}\right) \times \left(\frac{T_{OUT}}{2^4} - TRef\right)\right]}{2^{12}}\right]$

In case temperature compensation is disabled, the red terms are not executed.

18.10. External Trigger

The MLX90395 provides an option to trigger single measurements by means of the TRG pin. To enable this pin, it needs to be configured accordingly.

TrigIntSel is used to change the function of the INT/TRG pin. In case it is set, the pin is an output and used as INT pin. In case it is 0, the pin becomes an input and can see the rising edge event.

ExtTrig is set to enable the single measurement by rising edge. Note that this is only active after an SM command has been executed, or a HS followed by reset.

18.11. NVRAM Lock (SPI mode) - Not available in BAA version

The NVRAM can be locked to avoid accidental rewriting of the settings in the application. It is basically disabling the writing commands. Two bits are available:

- Lock_HS: blocks the SPI memory store command (HS).
- Lock_WR: blocks the SPI write register command (WR).

As it applies to SPI mode, it is also recommended to set CommMode to “SPI only”.

This option is **not available in the BAA** version. For detailed information, please contact Melexis.

18.11.1. Temporary NVRAM Lock

The sequence below has to be executed to initialise the IC to be used with the temporary NVRAM lock feature:

1. Write Lock_HS to ‘1’ and keep Lock_WR to ‘0’.
2. Execute a memory store command (HS).
3. Power cycle. [23]

In application, the sequence below has to be executed in order to configure and protect the volatile memory of the IC:

1. Write configuration needed.
2. Write Lock_WR to ‘1’ (Lock_HS kept to ‘1’).
3. Start measurement. From this point on, the memory is protected.

In application, the sequence below has to be executed in order to enable reconfiguration of the volatile memory of the IC:

1. Execute a memory recall command (HR).
2. Start measurement. From this point on, the memory is unprotected.

Note: also a power cycle or reset (RT) enables reconfiguration of the volatile memory of the IC, hence reducing the level of protection.

[23] Recommended action is the power cycle, but a reset command (RT), or a memory recall (HR) + start measurement (SM) will also work. Mind to respect the T_{HS_WAIT}.

18.11.2. Permanent NVRAM Lock

Although the temporary NVRAM lock is offering a good protection, it is strongly recommended to use the permanent NVRAM lock, to avoid accidental NVRAM corruption in harsh environments. This is not suitable for applications requiring dynamic reconfiguration of the volatile memory. The sequence is shown below:

1. Write both Lock_HS and Lock_WR to '1'.
2. Execute a memory store command (HS).
3. Power cycle. (23)

18.12. Other Controls

VMeasEN enables a voltage measurement. Here the supply voltage is measured. In case it is set to 0x0, even though the command might ask for a voltage measurement, the result will be 0. Also in burst mode, when the zyxt in the command is empty, this parameter is used to determine doing the voltage measurement or not.

HallConf and ZSeries are not to be touched. It is recommended to keep HallConf to 0x0 and ZSeries to 0x0 for optimal performance. Note that in both cases of ZSeries, the Z-field can be measured.

19. Recommended Application Diagrams

In case of long cable length or wire harness, it is recommended to add a series resistor on the communication lines (including INT and INT/TRIG) close to the IC to reduce coupling. The value has to be evaluated carefully to keep EMC emissions to a minimum.

19.1. Wiring with the MLX90395 in SOIC-8/TSSOP-16 Package

19.1.1. SPI Mode

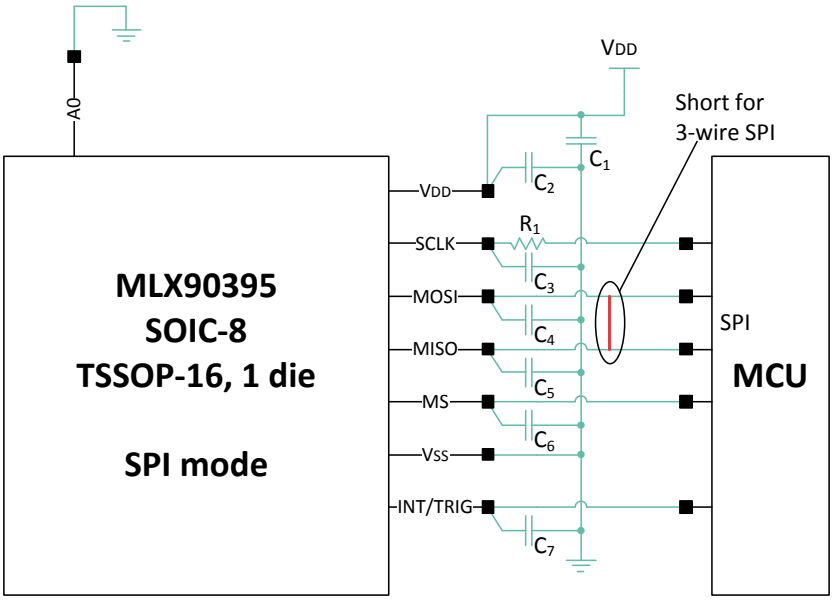


Figure 26: Application diagram SOIC-8 or TSSOP-16 (only one die represented) in SPI mode

Component	Standard routing			EMC robust routing			Remark
	Min.	Typ.	Max.	Min.	Typ.	Max.	
C_1	100nF		1µF	100nF		1µF	
C_2 [24]					100pF		
C_3 [24, 25]			18pF			12pF	f_{SCLK} = 10MHz
C_3 [24, 25]			110pF			82pF	f_{SCLK} = 2MHz
C_3 [24, 25]		47pF	220pF		47pF	160pF	f_{SCLK} = 1MHz
C_4 [24]					47pF		
C_5 [24]					47pF		
C_6 [24]					220pF		> C_3 for improved immunity
C_7 [24]					100pF		
R_1					100Ω		For improved filtering

Table 25: Recommended values for SOIC-8 or TSSOP-16 (one die) in SPI mode, BAA version

Component	Standard routing			EMC robust routing			Remark
	Min.	Typ.	Max.	Min.	Typ.	Max.	
C_1	100nF		1µF	100nF		1µF	
C_2 [24]					100pF		
C_3 [24]		-			-		
C_4 [24]					-		
C_5 [24]					47pF		
C_6 [24]					-		> C_3 for improved immunity
C_7 [24]					100pF		
R_1		-			-		

Table 26: Recommended values for SOIC-8 or TSSOP-16 (one die) in SPI mode, BBA version

[24] *Place at the pin, keep connection below 1mm and use ground via. MCU assumed to have output impedance of 300Ω.*
[25] *Values calculated for rapid flanks, f_{co} = 1/(2πRC), and are strongly dependent on driver strength and cable length.*

19.1.2. I²C Mode

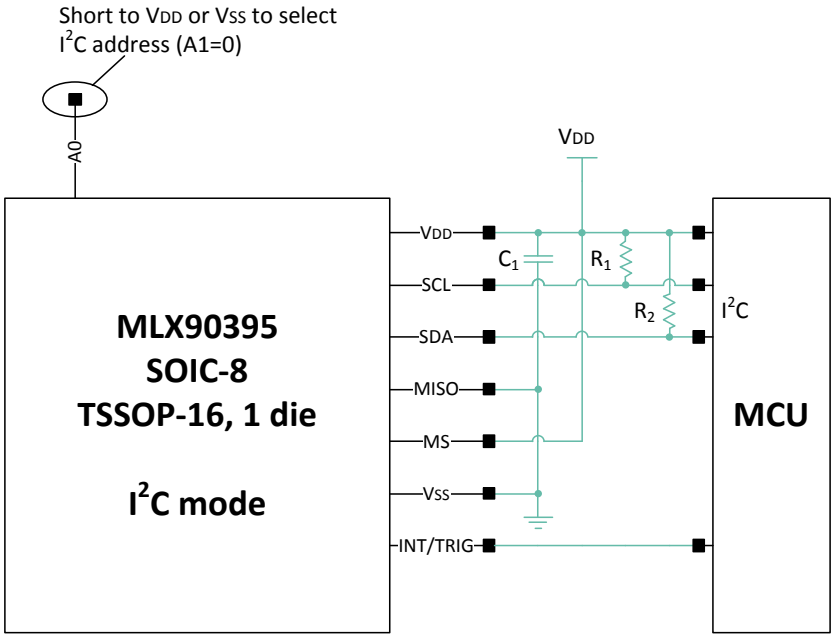


Figure 27: Application diagram SOIC-8 or TSSOP-16 (only one die represented) in I²C mode

Component	Min.	Typ.	Max.	Remark
C_1	100nF		1µF	
R_1		10kΩ		On MCU side, if not internal
R_2		10kΩ		On MCU side, if not internal

Table 27: Recommended values for SOIC-8 or TSSOP-16 (one die) in I²C mode

19.2. Wiring with the MLX90395 in QFN-16 Package

The bottom pad of the QFN package is not connected internally. Grounding is advised to increase robustness against mechanical shocks and improve EMC performance.

19.2.1. SPI Mode

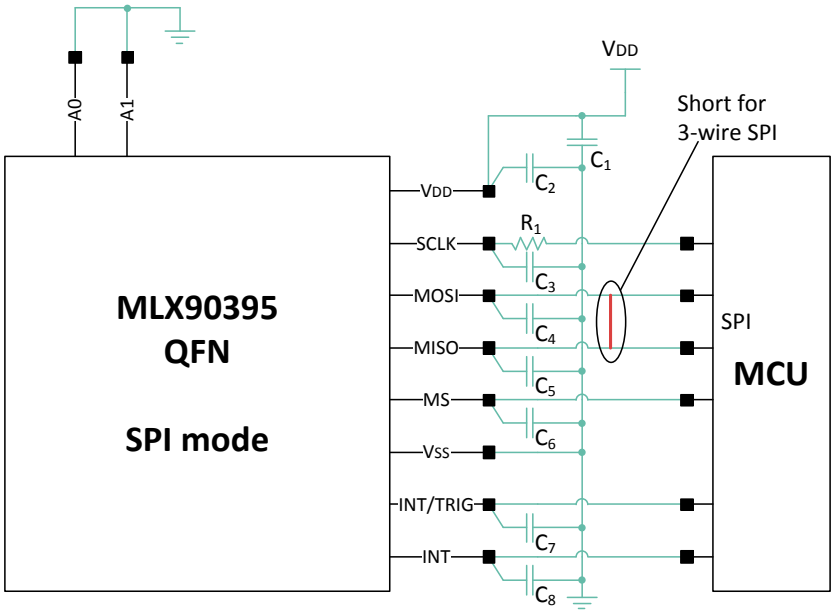


Figure 28: Application diagram QFN-16 in SPI mode

Component	Standard routing			EMC robust routing			Remark
	Min.	Typ.	Max.	Min.	Typ.	Max.	
C_1	100nF		1µF	100nF		1µF	
C_2 [26]					100pF		
C_3 [26, 27]			18pF			12pF	f_{SCLK} = 10MHz
C_3 [26, 27]			110pF			82pF	f_{SCLK} = 2MHz
C_3 [26, 27]		47pF	220pF		47pF	160pF	f_{SCLK} = 1MHz
C_4 [26]					47pF		
C_5 [26]					47pF		
C_6 [26]					220pF		> C_3 for improved immunity
C_7 [26]					100pF		
C_8 [26]					100pF		
R_1					100Ω		For improved filtering

Table 28: Recommended values for QFN-16 in SPI mode, BAA version

Component	Standard routing			EMC robust routing			Remark
	Min.	Typ.	Max.	Min.	Typ.	Max.	
C_1	100nF		1µF	100nF		1µF	
C_2 [26]					100pF		
C_3 [26]		-			-		
C_4 [26]					-		
C_5 [26]					47pF		
C_6 [26]					-		> C_3 for improved immunity
C_7 [26]					100pF		
C_8 [26]					100pF		
R_1		-			-		

Table 29: Recommended values for QFN-16 in SPI mode, BBA version

[26] *Place at the pin, keep connection below 1mm and use ground via. MCU assumed to have output impedance of 300Ω.*
[27] *Values calculated for rapid flanks, f_{co} = 1/(2πRC), and are strongly dependent on driver strength and cable length.*

19.2.2. I²C Mode

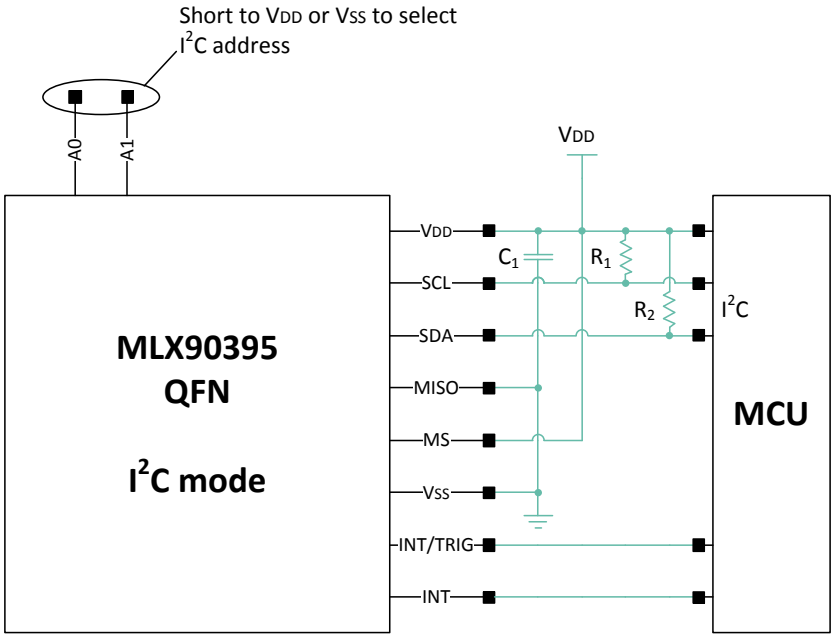


Figure 29: Application diagram QFN-16 in I²C mode

Component	Min.	Typ.	Max.	Remark
C_1	100nF		1µF	
R_1		10kΩ		On MCU side, if not internal
R_2		10kΩ		On MCU side, if not internal

Table 30: Recommended values for QFN-16 in I²C mode

20. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/en/quality-environment/soldering)

For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc.), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends consulting the dedicated trim&form recommendation application note: lead trimming and forming recommendations (http://www.melexis.com/en/documents/documentation/application-notes/lead-trimming-and-forming-recommendations).

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment.

21. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

22. Package Information

22.1. SOIC-8 Package

22.1.1. SOIC-8 - Package Dimensions

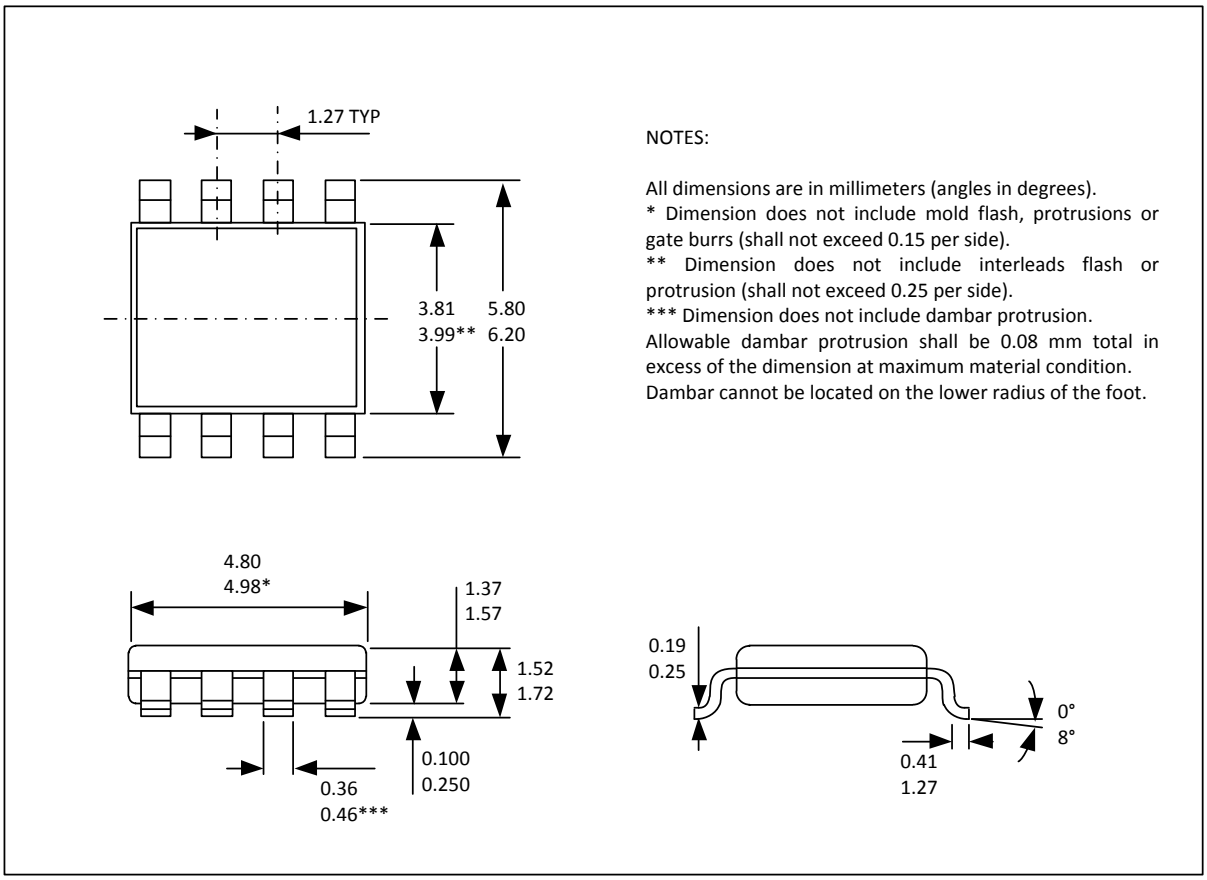


Figure 30: SOIC-8 Package Dimensions

22.1.2. SOIC-8 - Pinout and Marking

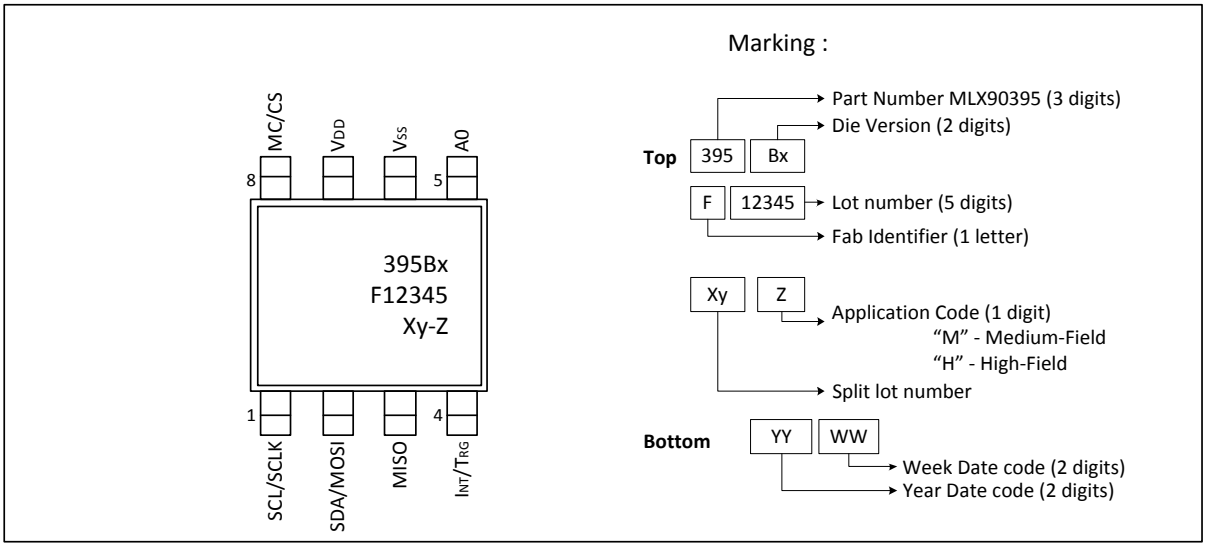


Figure 31: SOIC-8 Pinout and Marking

22.1.3. SOIC-8 - Sensitive Spot Location

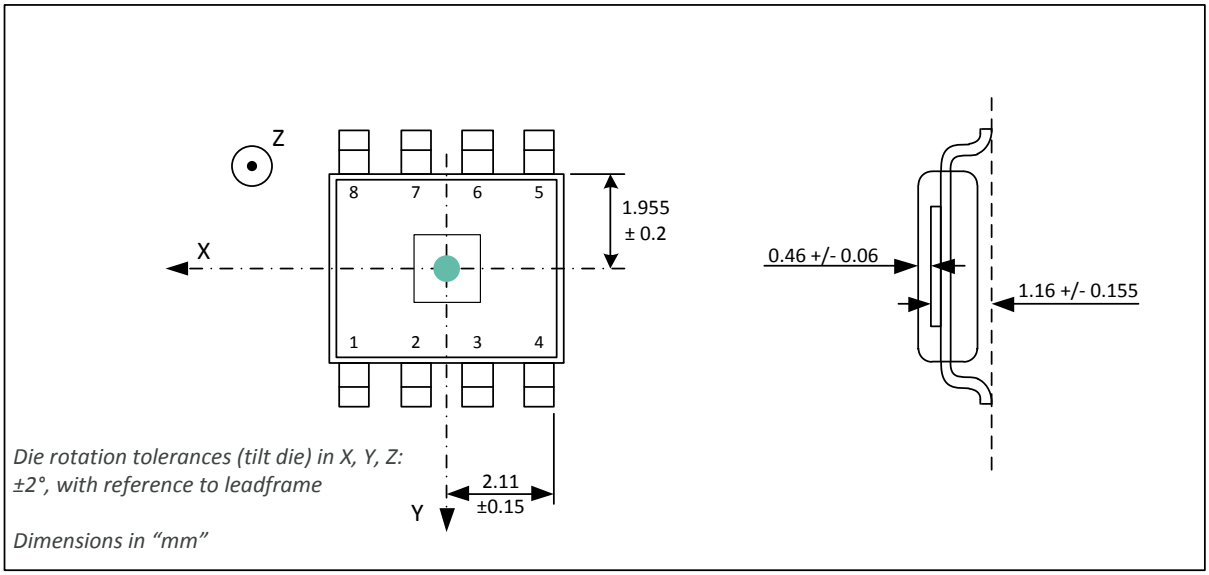
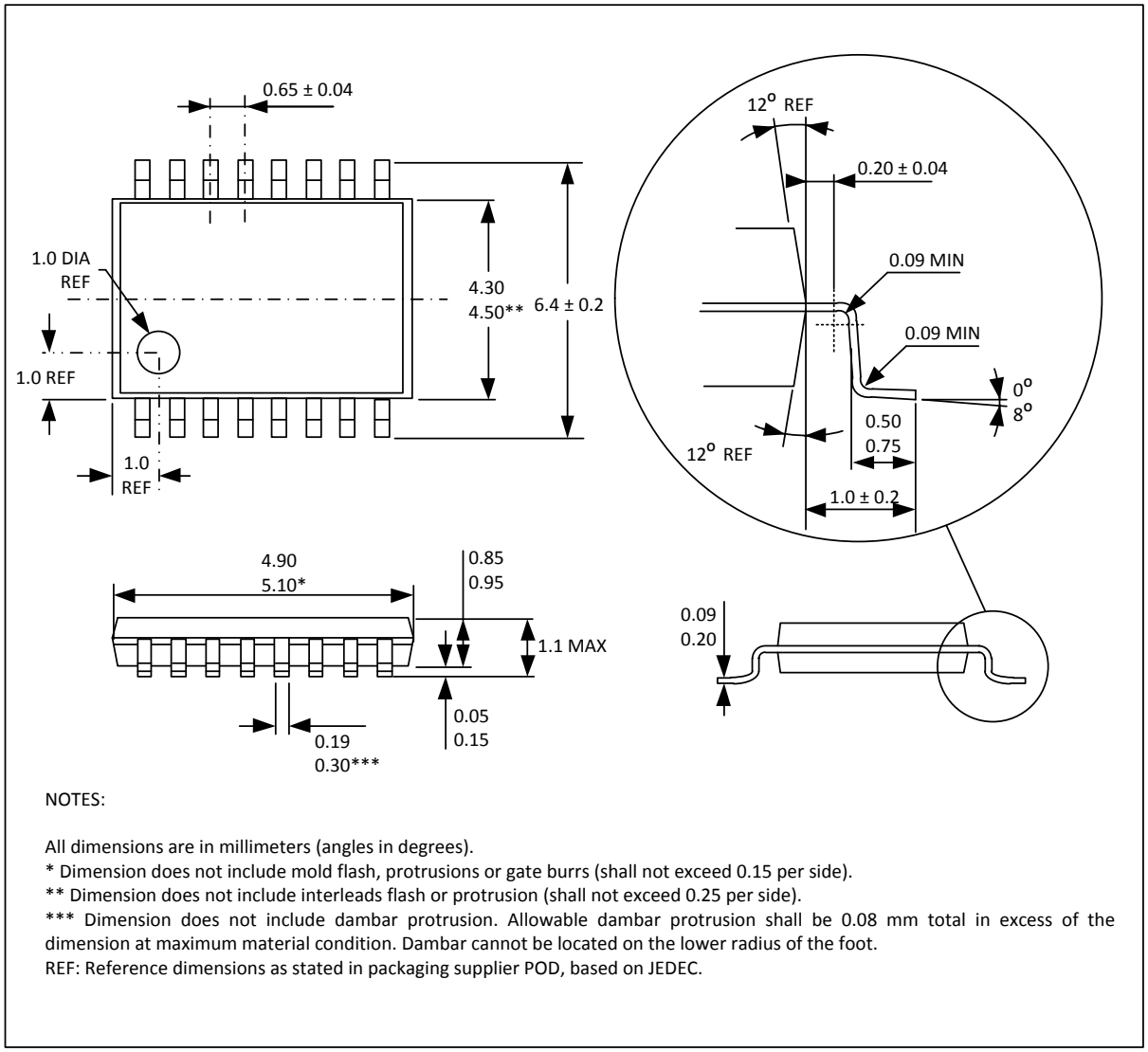


Figure 32: SOIC-8 Sensitive Spot Location

22.2. TSSOP-16 Package

22.2.1. TSSOP-16 - Package Dimensions



NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
REF: Reference dimensions as stated in packaging supplier POD, based on JEDEC.

Figure 33: TSSOP-16 Package Dimensions

22.2.2. TSSOP-16 - Pinout and Marking

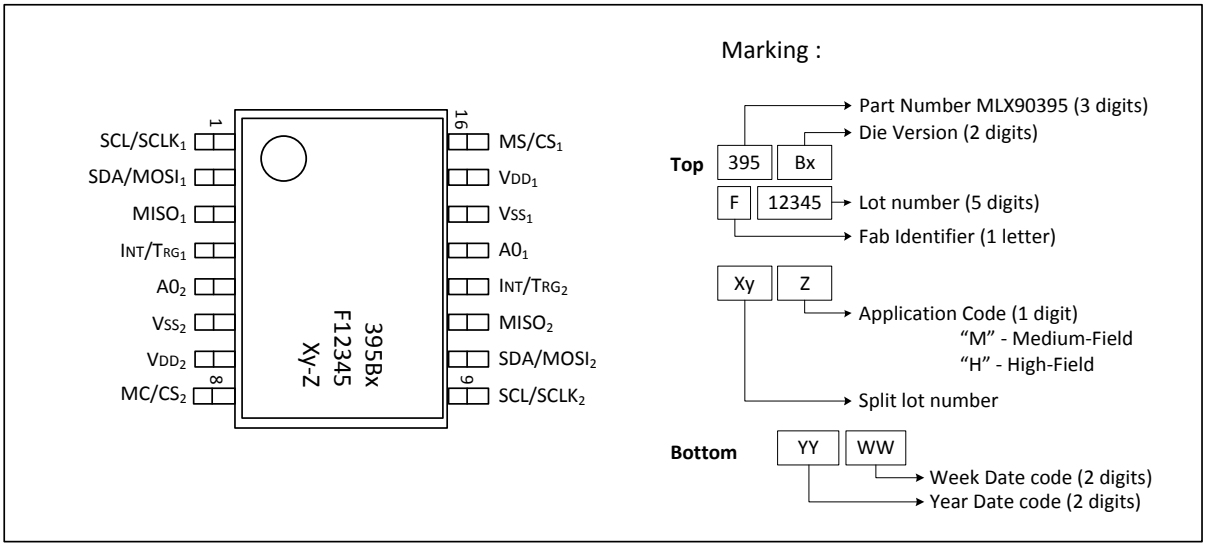


Figure 34: TSSOP-16 Pinout and Marking

22.2.3. TSSOP-16 - Sensitive Spot Location

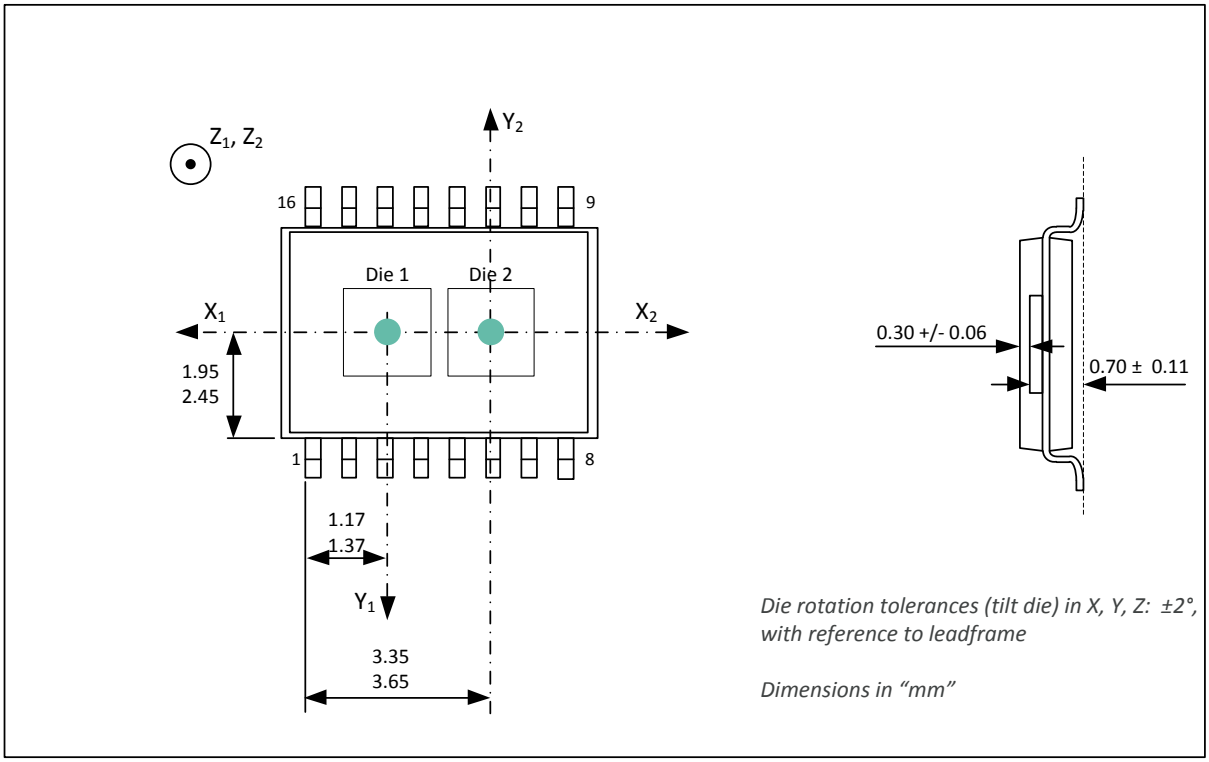


Figure 35: TSSOP-16 Sensitive Spot Location

22.3. QFN-16 Package

22.3.1. QFN-16 - Package Dimensions and Sensitive Spot Location

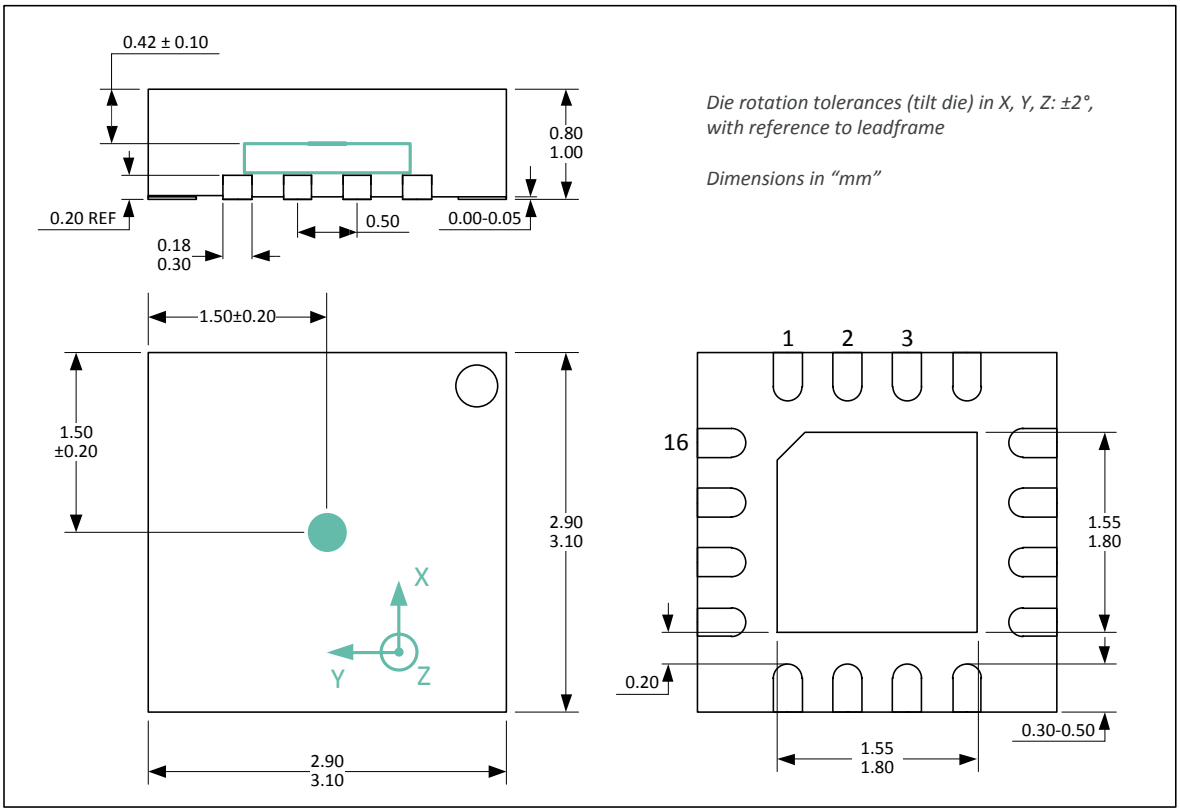


Figure 36: QFN-16 Package Dimensions and Sensitive Spot Location

22.3.2. QFN-16 - Pinout and Marking (BAA version)

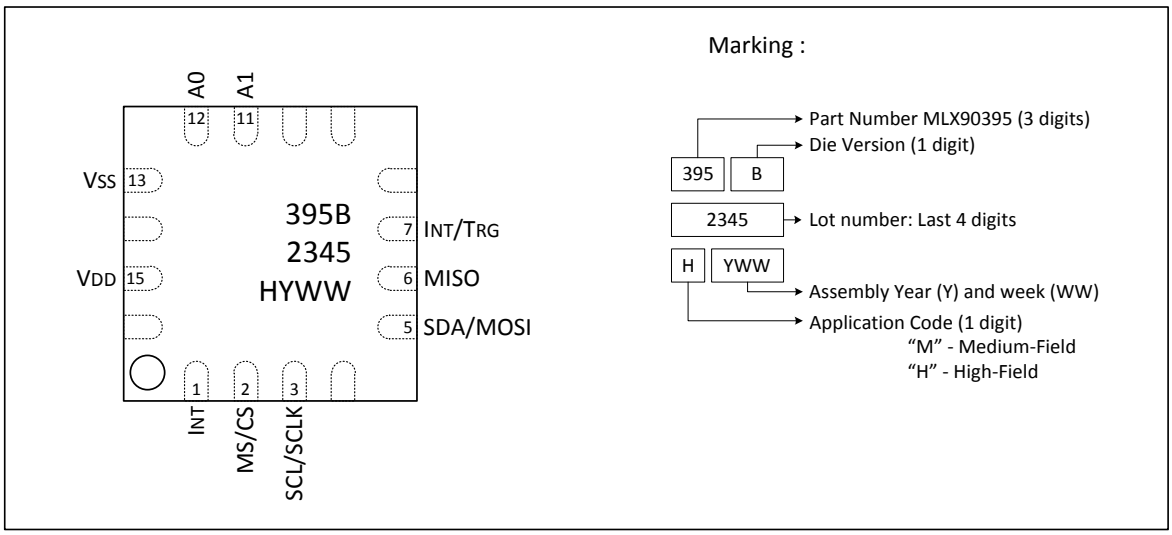


Figure 37: QFN-16 Pinout and Marking (BAA version)

22.3.3. QFN-16 - Pinout and Marking (BBA version)

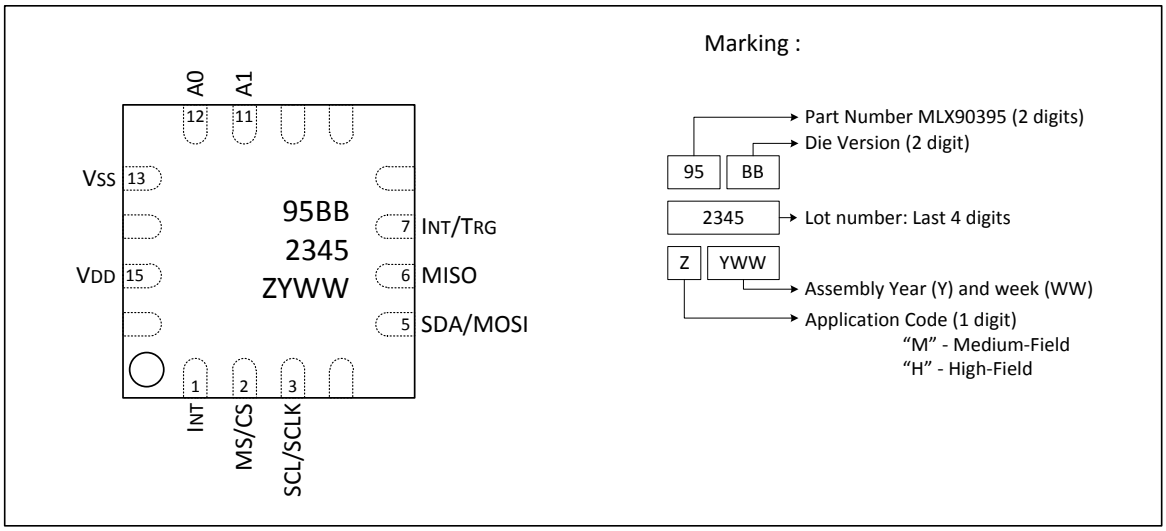


Figure 38: QFN-16 Pinout and Marking (BBA version)

22.4. Package Thermal Performances

The table below describes the thermal behaviour of available packages following JEDEC EIA/JESD 51.X standard.

Package	Junction to Case - θjc	Junction to Ambient - θja (JEDEC 1s2p board)	Junction to Ambient - θja (JEDEC 1s0p board)
SOIC-8	38.8 K/W	112 K/W	153 K/W
TSSOP-16	27.6 K/W	99.1 K/W	137 K/W
QFN-16	21 K/W	185 K/W	213 K/W

Table 31: Package Thermal Performance

23. Contact

For the latest version of this document, go to our website at http://www.melexis.com.

For additional information, please contact our Direct Sales team and get help for your specific needs:

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	Email: sales_europe@melexis.com
Americas	Telephone: +1 603 223 2362
	Email: sales_usa@melexis.com
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