ML6428

S-Video Filter and 75Ω Line Drivers with Summed Composite Output

Features

- 6.7MHz Y and C filters, with CV out for NTSC or PAL
- 75Ω cable line driver for Y, C, CV, and TV modulator
- 43dB stopband attenuation at 27MHz
- 1dB flatness up to 4.8MHz
- No external frequency select components or clocks
- 12ns group delay flatness up to 10MHz
- 5% overshoot on any input edge
- AC coupled input and output (ML6428CS-1)
- AC coupled input and DC coupled output (ML6428CS-2)
- 0.4% differential gain on all channels, 0.4º differential phase on all channels
- 0.7% total harmonic distortion on all channels
- 5V ±10% operation
- DC restore with low tilt

General Description

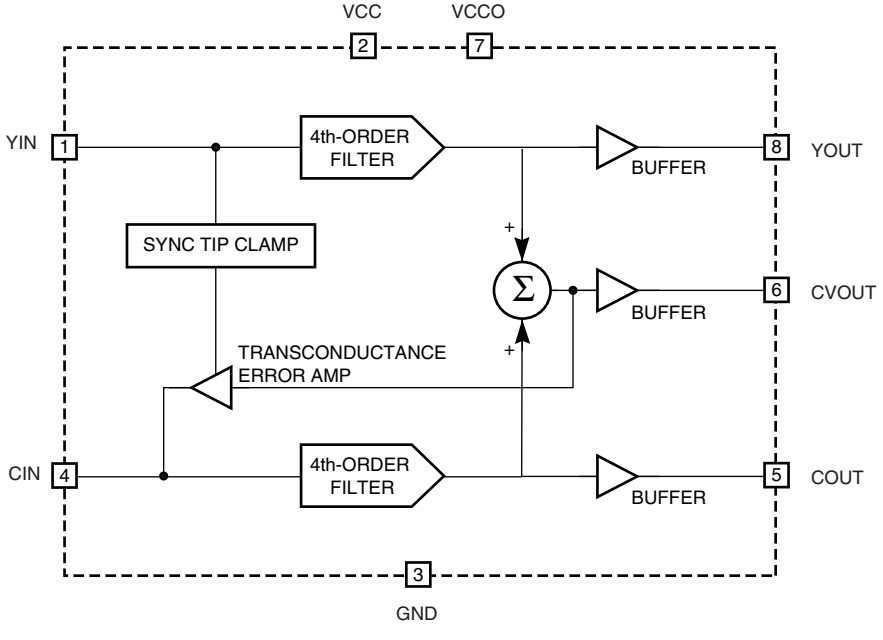
The ML6428 is a dual Y/C 4th-order Butterworth lowpass video filter optimized for minimum overshoot and flat group delay. The device also contains a summing circuit to generate filtered composite video.

The Y and C input signals from DACs are AC coupled into the ML6428. Both channels have DC restore circuitry to clamp the DC input levels during video sync. The Y channel uses a sync tip clamp. The CV and the C channels share a feedback clamp.

All outputs must be AC coupled into their loads for the -1 version. The -2 version must be DC coupled. All inputs (-1 and -2 versions) are AC coupled. The Y or C outputs can drive 2VP-P into a 150Ω load, while the CV output can drive 2VP-P into 75Ω. Thus the CV output is capable of driving two independent 150Ω loads to 2VP-P.

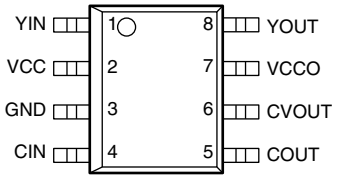
On the CV output, one of the 75Ω loads can be shorted to ground with no loss of drive to the remaining load. The Y, C and CV channels have a gain of 2 (6dB) with 1VP-P input levels.

Block Diagram



Pin Configuration

ML6428
8-Pin SOIC (S08)



TOP VIEW

Pin Description

Pin	Name	Function
1	YIN	Luminance input
2	VCC	5V supply for filters and references
3	GND	Ground
4	CIN	Chrominance input
5	COUT	Chrominance output
6	CVOUT	Composite video output
7	VCCO	5V supply for output stages
8	YOUT	Luminance output

Electrical Characteristics

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Units
DC Supply Voltage	-0.3	7	V
Analog & Digital I/O	GND – 0.3	V_{CC} + 0.3	V
Output Current (Continuous) CV Channel C and Y Channels Junction Temperature		 60 30 150	 mA mA °C
Storage Temperature Range	–65	150	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Thermal Resistance (θ_{JA})		67	°C/W

Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range	0	70	°C
VCC Range	4.5	5.5	V

Electrical Table Unless otherwise specified, V_{CC} = 5V ±10%, All inputs AC coupled with 100nF, ML6428-1 outputs must be AC coupled, ML6428-2 outputs must be DC coupled. T_A = Operating Temperature Range[1]

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
ICC	Supply Current		No Load (VCC = 5.0V)		52	80	mA
AV	Low Frequency Gain (All Channels)		VIN = 100mVP-P at 300KHz	5.34	6.0	6.65	dB
	C DC Output Level (During Sync)		Sync Present on Y	1.7	1.9	2.3	V
	Y Sync Output Level	ML6428-1	Sync Present on Y	0.7	0.9	1.3	V
		ML6428-2	Sync Present on Y	0.35	0.54	0.95	V
	Y+C Sync Output Level	ML6428-1	Sync Present on Y	0.7	0.92	1.3	V
		ML6428-2	Sync Present on Y	0.35	0.48	0.95	V
tCLAMP	Clamp Response Time (Y Channel)		Settled to Within 10mV		2		ms
f1dB	-1dB Bandwidth (Flatness) (All Channels)			4.0	4.8		MHz
fC	-3dB Bandwidth (Flatness) (All Channels)				6.7		MHz
0.8fC	0.8 x fC Attenuation (Y, C)				1.5		dB
fSB	Stopband Rejection (All Channels)		fIN = 27MHz to 100MHz worst case		–42	–38	dB
Vi	Input Signal Dynamic Range		AC Coupled ML6428-1, -2	1.0	1.4		VP-P
NOISE	Output Noise (All Channels)		25Hz to 50MHz		2.3		mVRMS
OS	Peak Overshoot (All Channels)		2VP-P Output Pulse (loaded)		4.3		%
ISC	Output Short Circuit Current (All Channels)		VOUT C, Y, or CV (Note 2)		100		mA
CL	Output Shunt Capacitance (All Channels)		All Outputs			35	pF
dG	Differential Gain (All Channels)		All Outputs		0.4		%
dΦ	Differential Phase (All Channels)		All Outputs		0.4		°
THD	Output Distortion (All Channels)		VOUT = 1.8VP-P, Y/C Out at 3.58MHz/4.43MHz		0.7		%
XTALK	Crosstalk		From C Input of 0.5VP-P at 3.58MHz/4.43MHz, to Y Output		–55		dB
			From Y Input of 0.4VP-P at 3.58MHz, to C Output		–58		dB
PSRR	PSRR (All Channels)		0.5VP-P (100kHz) at VCC		–49		dB
tpd	Group Delay (All Channels)		100kHz		60		ns
Δtpd	Group Delay Deviation from Flatness (All Channels)		to 3.58MHz (NTSC)		4		ns
			to 4.43MHz (PAL) without peaking (see Figures 7 to 11)		7		ns
			to 10MHz		12		ns
tSKEW	Skew Between Y & C Outputs					1	ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.
2: Sustained short circuit protection limited to 10 seconds.

Functional Description

The ML6428 is a dual monolithic continuous time video filter designed for reconstructing the luminance and chrominance signals from an S-Video D/A source. Composite video output is generated by summing the Y and C outputs. The ML6428CS-1 is intended for use in AC coupled input and output applications. The ML6428CS-2 is intended for AC coupled input and DC coupled output applications (see Figures 5 and 6).

The filters have a 4th-order Butterworth characteristic with an optimization toward low overshoot and flat group delay. All outputs are capable of driving 2VP-P into 150Ω video loads, with up to 35pF of load capacitance at the output pin. ML6428CS-1 outputs are AC coupled, ML6428CS-2 outputs are DC coupled. The CV output can drive two video loads plus a high-impedance modulator. Thus the CV output is intended to simultaneously drive a VCR, a TV, and a high-impedance modulator. Y and C are capable of driving a 75Ω load at 1VP-P. The ML6428 is capable of driving two composite loads and a TV modulator simultaneously.

All channels are clamped during sync to establish the appropriate output voltage swing range. Thus the input coupling capacitors do not behave according to the conventional RC time constant. Clamping for all channels settles within 2ms of a change in video input sources.

In most applications, the ML6428's input coupling capacitors are 0.1µF. The Y input sinks 1.6µA during active video, which nominally tilts a horizontal line by 2mV (max) at the Y output (Figure 4). During sync, the clamp typically sources 20µA to restore the DC level. The net result is that the average input current is zero.

Any change in the input coupling capacitor's value will inversely alter the amount of tilt per line. Such a change will also linearly affect the clamp response times.

The C channel has no pulldown current sources and is essentially tilt-free. Its input is clamped by a feedback amp which responds to the CV output. Since CV = Y+C, the CV output will droop by the same amount as Y during active video, and will rise by the same amount as Y during sync.

The ML6428 is robust and stable under all stated load and input conditions. Capacitavely bypassing both VCC pins directly to ground ensures this performance. (See Figures 5 and 6)

Luminance (Y) I/O

The luma input is driven by either a low impedance source of 1VP-P or the output of a 75Ω terminated line. The input is required to be AC coupled via a 0.1uF coupling capacitor which allows for a nominal settling time of 2ms. The luma output is capable of driving a 150Ω load at 2VP-P or 1VP-P into a 75Ω load. ML6428CS-1 outputs are AC coupled, ML6428CS-2 outputs are DC coupled.Up to 35pF of load capacitance (at the output pin) can be driven without stability or slew issues. A 220µF AC coupling capacitor is recommended at the output (ML6428-1 only).

Chrominance (C) I/O

The chroma input is driven by a low impedance source of 0.7VP-P or the output of a 75Ω terminated line. The input is required to be AC coupled via a 0.1uF coupling capacitor which allows for a nominal clamping time of 1ms. The chroma output is capable of driving a 150Ω load at 2VP-P or 1VP-P into a 75Ω load. ML6428CS-1 outputs are AC coupled, ML6428CS-2 outputs are DC coupled. Up to 35pF of load capacitance can be driven without stability or slew issues. A 220µF AC coupling capacitor is recommended at the output (ML6428-1 only).

Composite video (CV) output

The composite video output is capable of driving 2 CV loads to 2VP-P and a high input impedance CV modulator. ML6428CS-1 outputs are AC coupled, ML6428CS-2 outputs are DC coupled. It is intended to drive three devices: TV, VCR, and a modulator. The TV or VCR input can be shorted to ground and the other outputs will still meet specifications. Up to 35pF of load capacitance (at the output pin) can be driven without stability or slew issues.

Using the ML6428 for PAL Applications

The ML6428 can be optimized for PAL video by adding frequency peaking to the composite and S-video outputs. Figures 7 and 8 illustrate the use of a additional external capacitor, 330pF, added in parallel to the output source termination resistor. This raises the frequency response from 1.6 dB down at 4.8Mhz to 0.35dB down at 4.8MHz allowing for accurate reproduction of the upper sideband of the PAL subcarrier. Figure 9 shows the frequency response of PAL video with various values of peaking capacitors (0pF, 220pF, 270pF, 330pF) between 0 and 10MHz.

For NTSC applications without the peaking capacitor the rejection at 27MHz is 42dB (typical) while for PAL applications with the peaking capacitor the rejection at 27MHz is 38dB (typical). This is shown in Figure 10. The differential group delay is shown in Figure 11 with and without a peaking capacitor (0pF, 220pF, 270pF, and 330pF) varies slightly with capacitance, going from 8ns to 13ns.

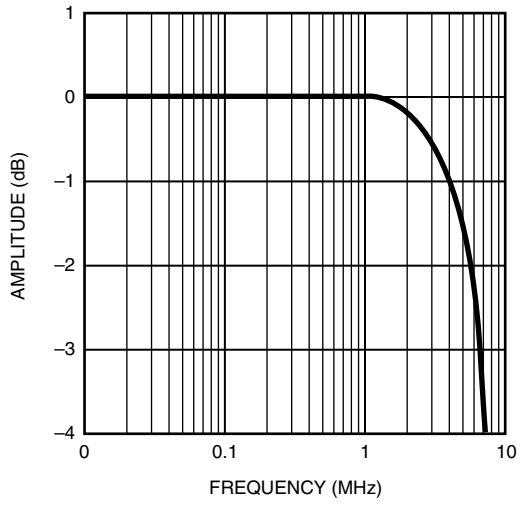


Figure 1. Passband Flatness
All outputs. (Normalized) Passband is ripple-free.

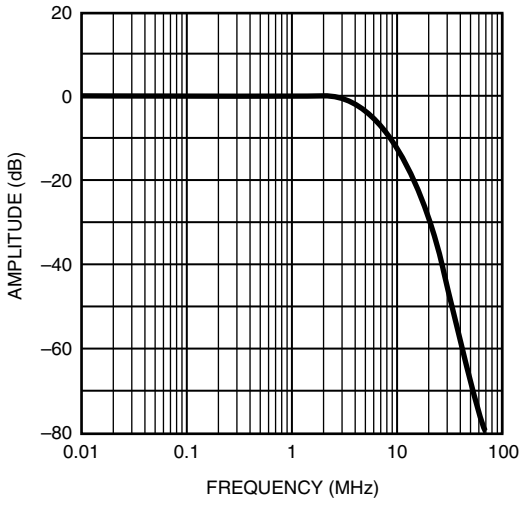


Figure 2. Passband/Stopband Rejection Ratios
All outputs. (Normalized)

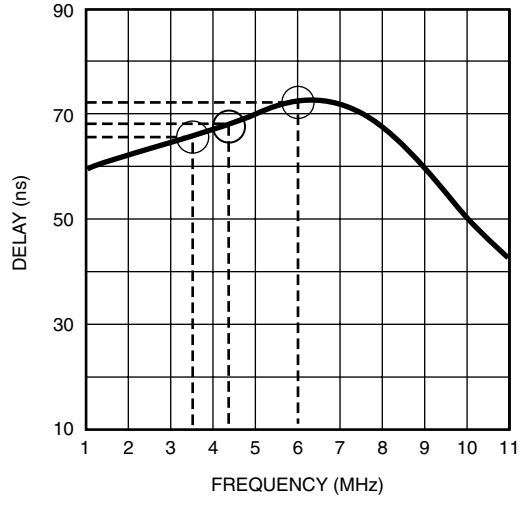


Figure 3. Group Delay, all Outputs
Low frequency group delay is 62ns. At 3.58MHz group delay increases by only 4ns. At 4.43MHz group delay increases by only 7ns. The maximum deviation from flat group delay of 12ns occurs at 6MHz.

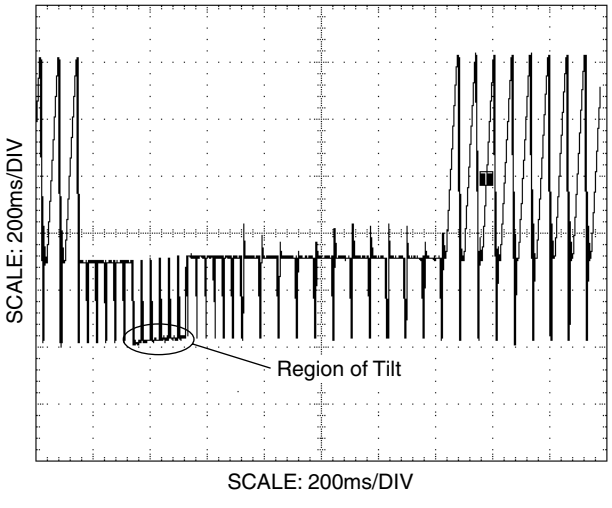


Figure 4. DC Restore Performance of Luma Output
Luma ramp test pattern is shown to have minimal tilt during vertical sync.

In most applications, the ML6428's input coupling capacitors are 0.1µF. The Y input sinks 1.6µA during active video, which tilts a horizontal line by 2mV at the Y output

Typical Applications

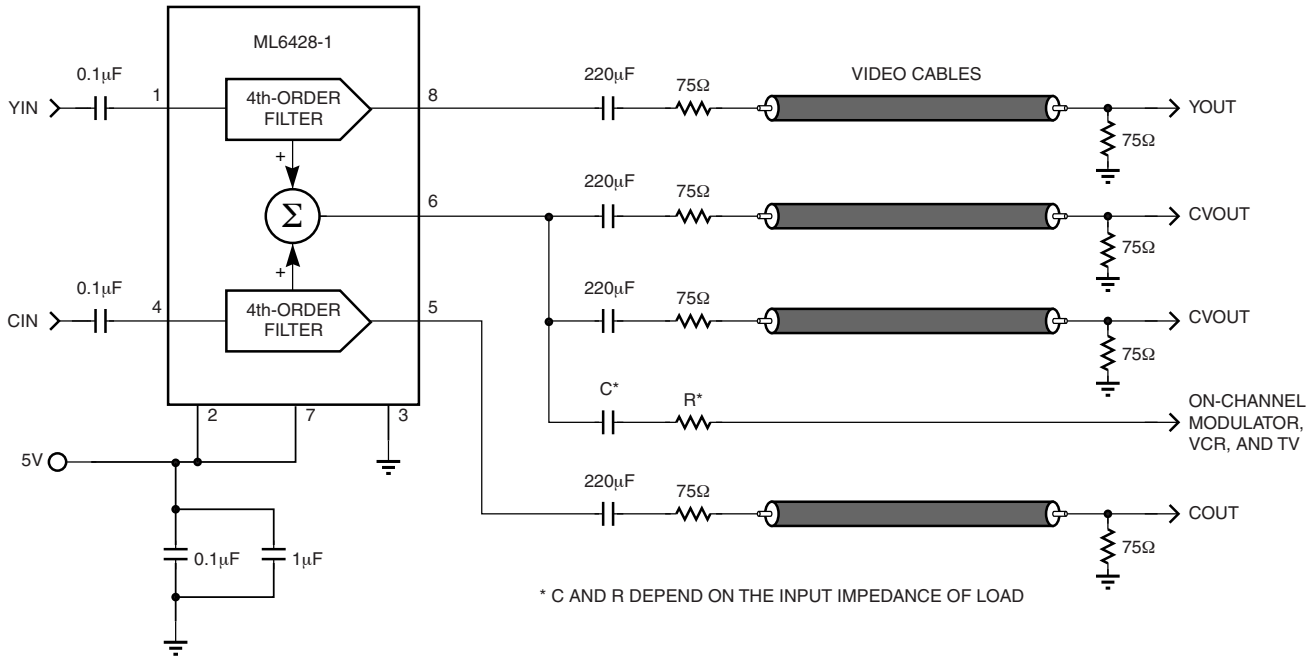


Figure 5. AC Coupled S-Video and Composite Video Line Driver for NTSC (Note: ML6428-1 outputs must be AC coupled)

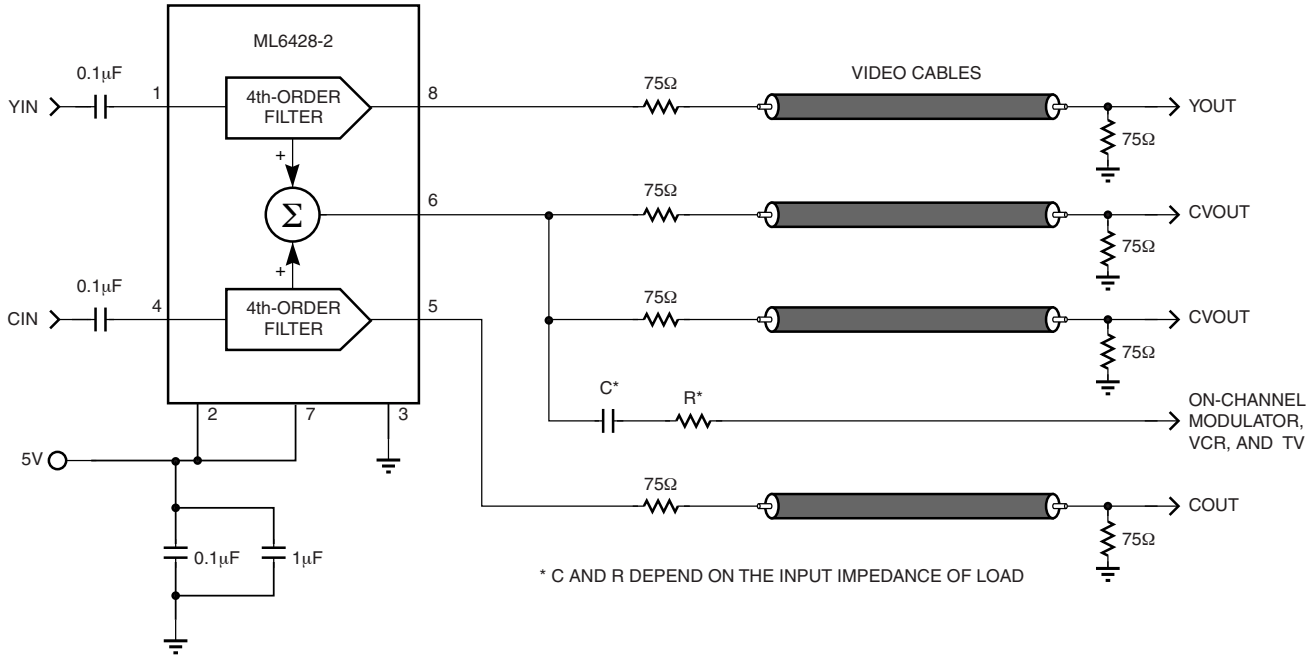


Figure 6. DC Coupled S-Video and Composite Video Line Driver for NTSC (Note: ML6428-2 outputs must be DC coupled)

Typical Applications

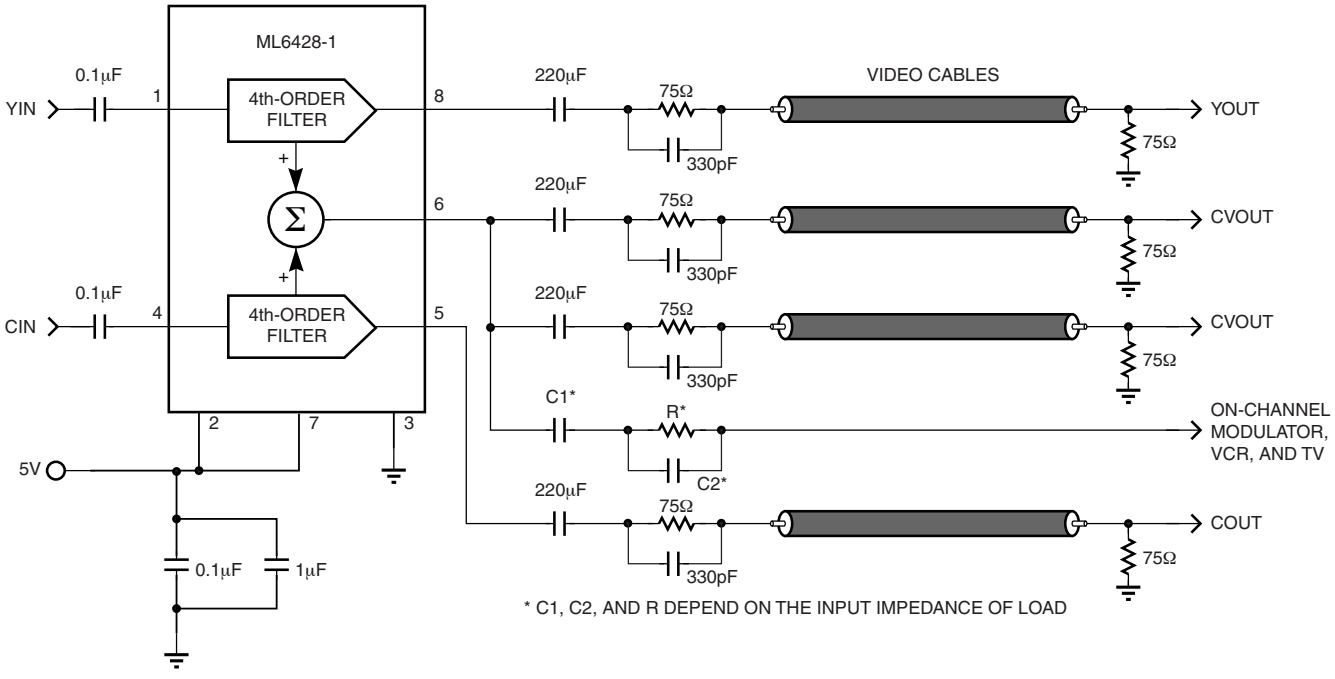


Figure 7. AC Coupled S-Video and Composite Video Line Driver for PAL (Note: ML6428-1 outputs must be AC coupled)

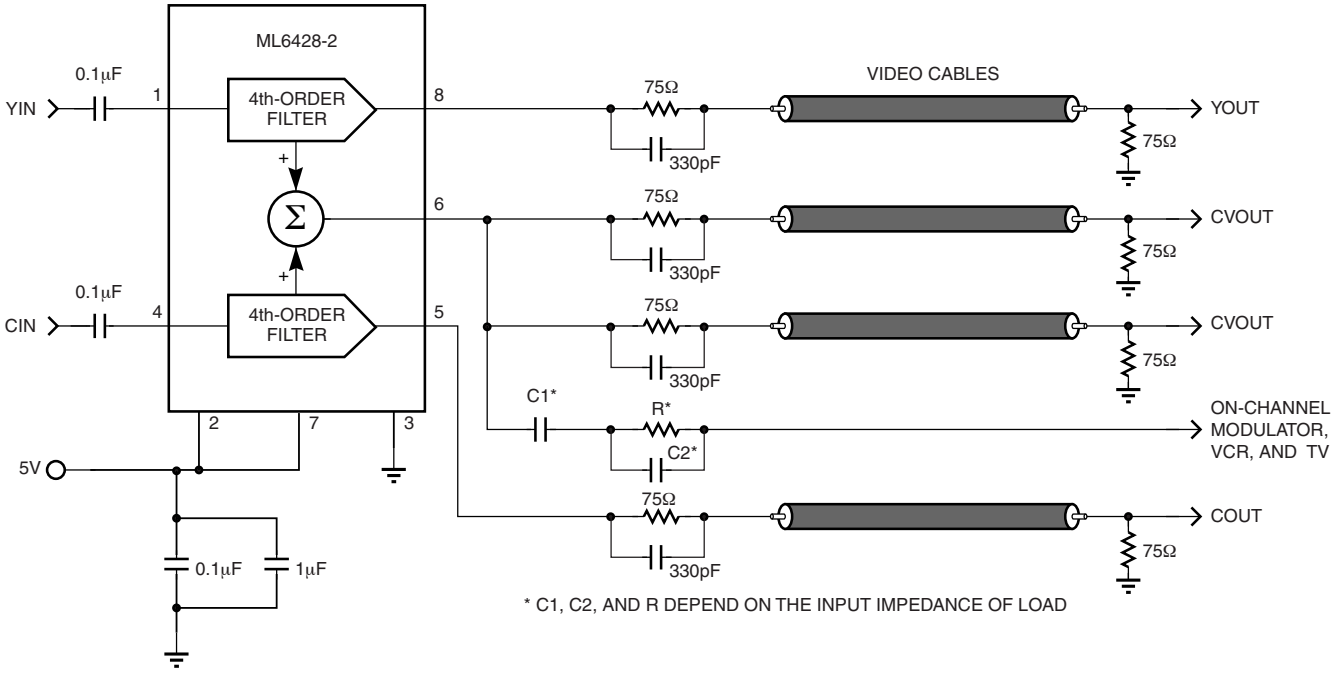


Figure 8. DC Coupled S-Video and Composite Video Line Driver for PAL (Note: ML6428-2 outputs must be DC coupled)

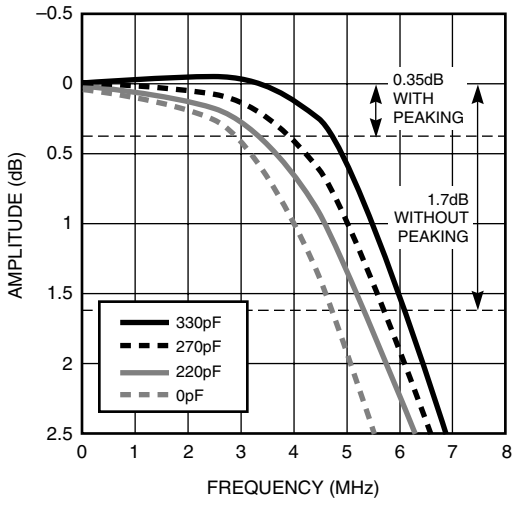


Figure 9. NTSC/PAL Video Frequency Response With and Without Peaking Capacitor

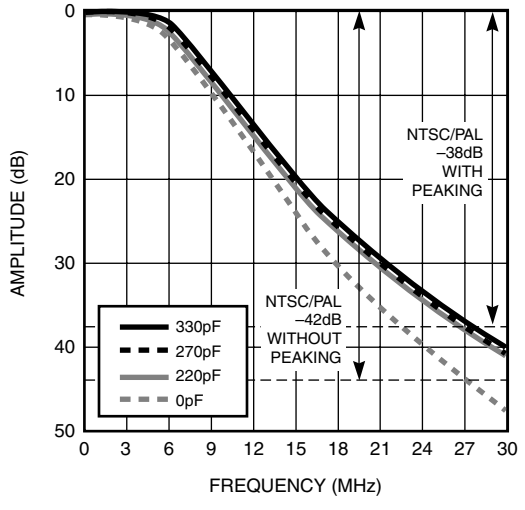


Figure 10. Stopband Rejection at 27MHz With and Without Peaking Capacitor

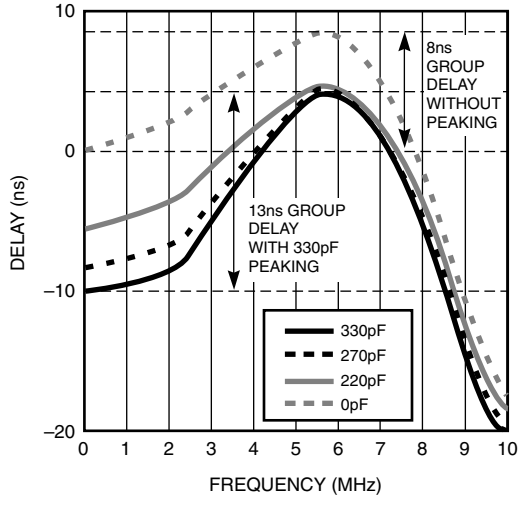
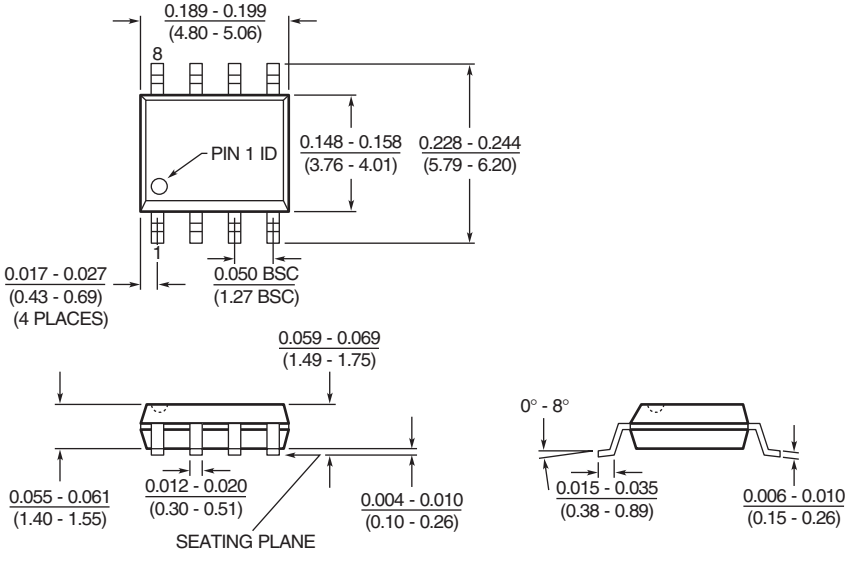


Figure 11. Group Delay at 5.5MHz (PAL) With and Without Peaking Capacitor

Mechanical Dimensions inches (millimeters)

Package: S08
8-Pin SOIC



Ordering Information

Part Number	Temperature Range	Package
ML6428CS-1	0°C to 70°C	8 Pin SOIC (S08)
ML6428CS-2	0°C to 70°C	8 Pin SOIC (S08)

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

© 2003 Fairchild Semiconductor Corporation