

Mask Set Errata for Mask 1N86P

This report applies to mask 1N86P for these products:

- MKV58F1M0VMD24
- MKV58F1M0VLL24
- MKV58F1M0VLQ24
- MKV56F1M0VMD24
- MKV56F1M0VLL24
- MKV56F1M0VLQ24
- MKV58F512VMD24
- MKV58F512VLL24
- MKV58F512VLQ24
- MKV56F512VMD24
- MKV56F512VLL24
- MKV56F512VLQ24

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR004647	UART: Flow control timing issue can result in loss of characters if FIFO is not enabled
ERR007735	MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock
ERR008341	FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating.
ERR009265	FTM: Incorrect match may be generated if intermediate load feature is used in toggle mode
ERR009586	Core: Lock Status Indication incorrectly reads as one for debugger reads
ERR009587	Core: TPIU cannot be flushed in Debug state if Cortex-M7 TPIU is used
ERR009588	Core: Incorrect behavior of profiling counters
ERR010083	eFlexPWM: Half cycle automatic fault clearing does not work for PWM submodule 0 under certain conditions
ERR010420	Flashloader: Returns incorrect value to the host for property ID FlashBlockCount.
ERR010487	eFlexPWM: Possible missed output edges when using dithering under certain conditions
ERR011392	System: GPIO pins drive low during power-up and power-down



Table 2. Revision History

Revision	Changes
16 OCT 2019	The following erratum was added. • ERR011392
5 AUG 2016	The following erratum was added. • ERR010487
14 JUN 2016	The following erratum was added. • ERR010420
8 FEB 2016	Initial revision

ERR004647: UART: Flow control timing issue can result in loss of characters if FIFO is not enabled

Description: On UARTx modules with FIFO depths greater than 1, when the /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: Always enable the RxFIFO if you are using flow control for UARTx modules with FIFO depths greater than 1. The receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

Note that only UARTx modules with FIFO depths greater than 1 are affected. The UARTs that do not have the RxFIFO feature are not affected. Check the Reference Manual for your device to determine the FIFO depths that are implemented on the UARTx modules for your device.

ERR007735: MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock

Description: When transitioning from MCG clock modes FBE or FEE to either FBI or FEI, the MCG_S[IREFST] bit will set to 1 before the IREFS clock multiplexor has actually selected the slow IRC as the reference clock. The delay before the multiplexor actually switches is:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

In the majority of cases this has no effect on the operation of the device.

Workaround: In the majority of applications no workaround is required. If there is a requirement to know when the IREFS clock multiplexor has actually switched, and OSCERCLK is no longer being used by the FLL, then wait the equivalent time of:

2 cycles of the slow IRC + 2 cycles of OSCERCLK
after MCG_S[IREFST] has been set to 1.

ERR008341: FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating.

Description: In the Flexible Controller Area Network (FlexCAN) module, if the Freeze Enable bit (FRZ) in the Module Configuration Register (MCR) is asserted and the Freeze Mode is requested by asserting the Halt bit (HALT) in MCR, in some cases, the Freeze Mode Acknowledge bit (FRZACK) in the MCR may never be asserted.

In addition, the Low-Power Mode Acknowledge bit (LPMACK) in the MCR may never be asserted in some cases when the Low-Power Mode is requested.

Under the two scenarios described above, the loss of ACK assertion (FRZACK, LPMACK) causes a lock condition. A soft reset action is required in order to remove the lock condition.

The change from Normal Mode to Low-Power Mode cannot be done directly. Instead, first change mode from Normal to Freeze Mode, and then from Freeze to Low-Power Mode.

Workaround: To avoid the lock condition, the following procedures must be used:

A) Procedure to enter in Freeze Mode:

1. Set both the Freeze Enable bit (FRZ) and the Halt bit (HALT) in the Module Control Register (MCR).
2. Check if the Module Disable bit (MDIS) in MCR register is set. If yes, clear the MDIS bit.
3. Poll the MCR register until the Freeze Mode Acknowledge bit (FRZACK) in MCR is set or the timeout is reached (see NOTE below).
4. If the Freeze Mode Acknowledge bit (FRZACK) is set, no further action is required. Skip steps 5 to 8.
5. If the timeout is reached because the Freeze Mode Acknowledge bit (FRZACK) is still cleared, then set the Soft Reset bit (SOFTTRST) in MCR.
6. Poll the MCR register until the Soft Reset bit (SOFTTRST) bit is cleared.
7. Reconfigure the Module Control Register (MCR)
8. Reconfigure all the Interrupt Mask Registers (IMASKn).

After Step 8, the module will be in Freeze Mode.

NOTE: The minimum timeout duration must be equivalent to:

- a) 730 CAN bits if the CAN FD Operation Enable bit (FDEN) in MCR is set (CAN bits calculated at arbitration bit rate),
- b) 180 CAN bits if the FDEN bit is cleared.

B) Procedure to enter in Low-Power Mode:

1. Enter in Freeze Mode (execute the procedure A).
2. Request the Low-Power Mode.
3. Poll the MCR register until the Low-Power Mode Acknowledge (LPMACK) bit in MCR is set.

ERR009265: FTM: Incorrect match may be generated if intermediate load feature is used in toggle mode

Description: When a channel (n) match is used as an intermediate reload, an incorrect second match may occur immediately following the correct match. The issue is problematic only if channel (n) is configured for output compare with the output configured to toggle mode. In this scenario, channel (n) toggles on the correct match and again on the incorrect match. The issue may also occur if a certain channel has a match which is coincident with an intermediate reload point of any other channel.

Workaround: If any channel is configured for output compare mode with the output set for toggle mode, the intermediate reload feature must not be used.

ERR010083: eFlexPWM: Half cycle automatic fault clearing does not work for PWM submodule 0 under certain conditions

Description: When Submodule 0 selects the EXT_SYNC signal to cause initialization (PWMx_SM0_CTRL2[INIT_SEL] = 0b11) and a FAULTx input is associated with submodule 0 outputs using the Submodule 0 Fault Disable Mapping Registers (PWMx_SM0DISMAPn) and

1) the respective bit for that FAULTx is 1 in the FHALF bitfield of the Fault Status Register PWMx_FSTS_n and

2) the respective bit for that FAULTx is 0 in the FFULL bitfield of the Fault Status Register PWMx_FSTS_n and

3) the respective bit for that FAULTx is 1 in the FAUTO bitfield of the Fault Control Register PWM_FCTRL_n,

then the automatic fault clearing will not work in submodule 0 and its outputs will remain disabled.

Workaround: When the EXT_SYNC signal is used to cause initialization in submodule 0 and the submodule 0 PWM outputs are disabled by a specific FAULTx input, use full cycle automatic fault clearing for the specific FAULTx input by setting the corresponding bit of the Fault Status Register PWM_FSTS_n[FFULL].

ERR010420: Flashloader: Returns incorrect value to the host for property ID FlashBlockCount.

Description: The Kinetis Flashloader will return incorrect value to the host for property ID FlashBlockCount. It returns a value of 2 whereas the correct value is 1.

Workaround: None. Software suites utilizing the FlashBlockCount property should either ignore the FlashBlockCount property or hard-code this value to 1.

ERR010487: eFlexPWM: Possible missed output edges when using dithering under certain conditions

Description: In PWM submodules that do not have a fractional delay block and support dithering instead, the PWM will fail to create falling/rising edges on its output under certain special conditions.

- 1) If a submodule does not have a fractional delay block but is instead using dithering mode (FRCTRL[FRAC*_EN]==1) and
- 2) that submodule is using the master sync signal from submod0 as its initialization source (CTRL2[INIT_SEL]==10) and
- 3) in that submodule VAL1==VAL3 or VAL1==VAL5 and
- 4) FRACVAL3 (or FRACVAL5) does not equal 0,

then over the course of the dithering, the submodule's output falling edge will occasionally be scheduled at cycle VAL3+1 in order to create the dithering. Since VAL3+1 is greater than VAL1 (since VAL1==VAL3), the falling edge is scheduled beyond the submodule's "normal" period as defined by INIT and VAL1. Since the submodule is using the master sync signal, the submodule counter will continue past VAL1 but the logic in the submodule will use the VAL1 timing to recalculate the edge placement and the falling edge will be lost.

Workaround: The work around for this issue is to set VAL1 in the submodule to a value greater than VAL3 or VAL5 but less than the period of the master submodule 0.

ERR011392: System: GPIO pins drive low during power-up and power-down

Description: GPIO pins drive low for a brief time during power-up and power-down instead of being in the high impedance state. This condition exists during the interval when VDD is between approximately 0.6V to 1.5V. This affects all GPIO port pins except PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.

The only use cases affected are input pins that are pulled high by the system, output pins that are active low, and unused pins pulled high with a very low resistance. For input pins that are pulled up externally, the system should be evaluated to ensure that a low on that signal will not affect any active devices on that node. For outputs that are active low (these pins are normally pulled high externally to guarantee a safe (off) state), the system should be evaluated to ensure that an active low level will not affect the load during power transitions.

Workaround: The workaround for input pins that are pulled high and active low outputs is to use GPIO pins that do not have this issue.

The recommended workaround for unused pins is to leave unused GPIO pins floating, or tie them to ground through a high value resistor (10k or greater) if that is your company's requirement.

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