MJE200 - NPN, MJE210 - PNP

Preferred Device

Complementary Silicon Power Plastic Transistors

These devices are designed for low voltage, low−power, high−gain audio amplifier applications.

Features

- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain −
  h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current−Gain − Bandwidth Product −
  f_T = 65 MHz (Min) @ I_C
  = 100 mAdc
- Annular Construction for Low Leakage −
  I_{CBO} = 100 nAdc @ Rated V_{CB}
- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CB}	25	Vdc
Emitter−Base Voltage	V_{EB}	8.0	Vdc
Collector Current − Continuous − Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	W mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 0.012	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction−to−Ambient	θ_{JC}	83.4	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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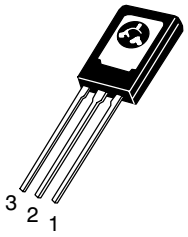
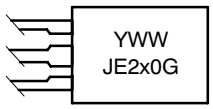
5.0 AMPERES POWER TRANSISTORS COMPLEMENTARY SILICON 25 VOLTS, 15 WATTS



TO−225
CASE 77
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week
JE2x0 = Device Code
x = 0 or 1
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE200	TO−225	500 Units/Box
MJE200G	TO−225 (Pb−Free)	500 Units/Box
MJE210	TO−225	500 Units/Box
MJE210G	TO−225 (Pb−Free)	500 Units/Box
MJE210T	TO−225	50 Units/Rail
MJE210TG	TO−225 (Pb−Free)	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 – –	 100 100	 nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}	 –	 100	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 70 45 10	 – 180 –	–
Collector–Emitter Saturation Voltage (Note 1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	 – – –	 0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (Note 1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base–Emitter On Voltage (Note 1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain – Bandwidth Product (Note 2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200 MJE210	C_{ob}	 – –	 80 120	pF

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

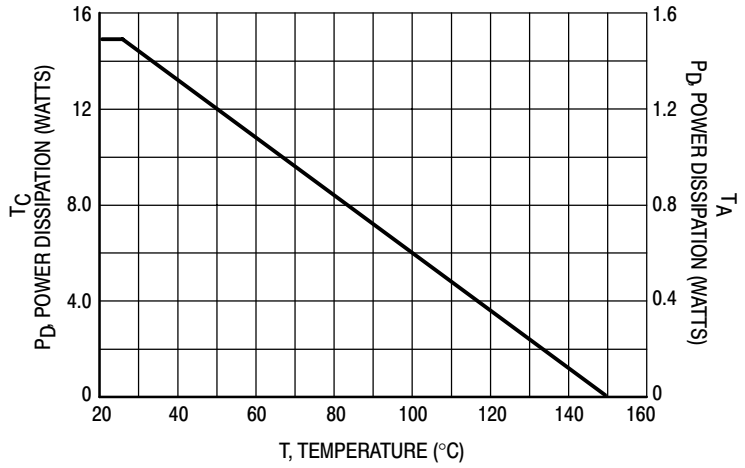


Figure 1. Power Derating

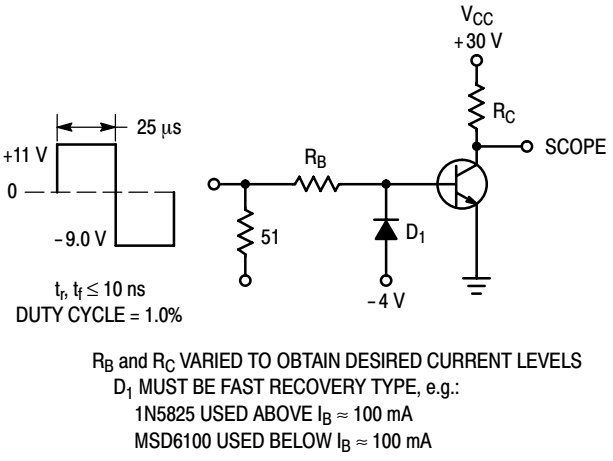


Figure 2. Switching Time Test Circuit

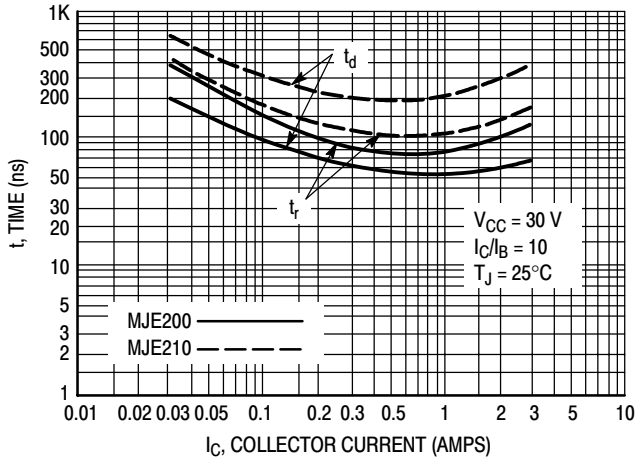


Figure 3. Turn–On Time

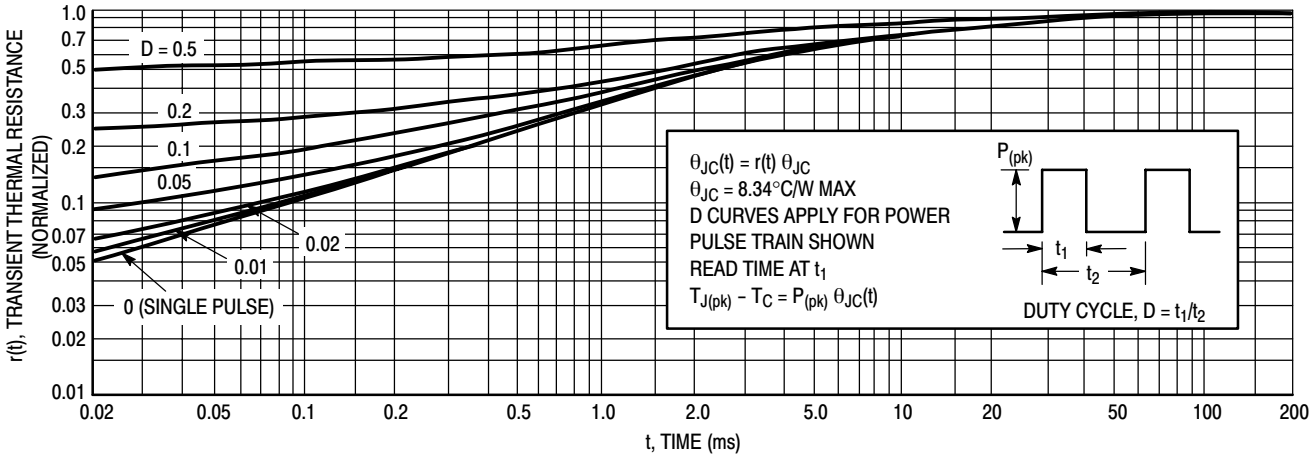


Figure 4. Thermal Response

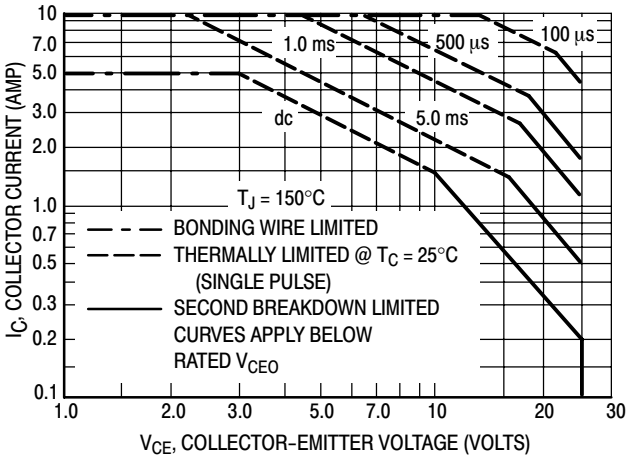


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

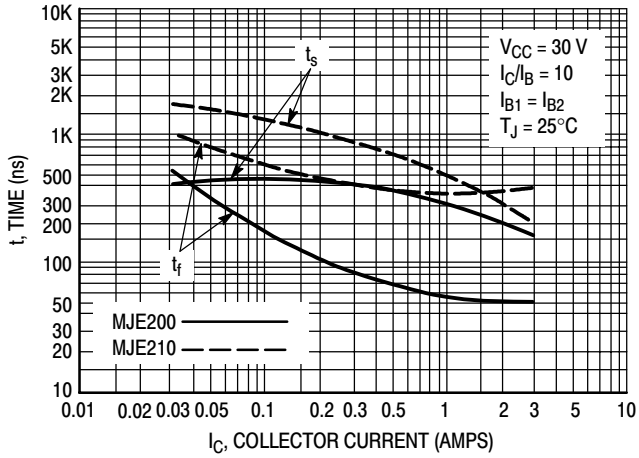


Figure 6. Turn–Off Time

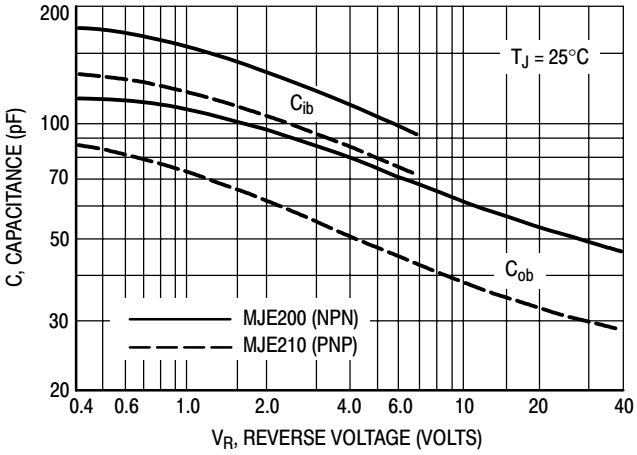
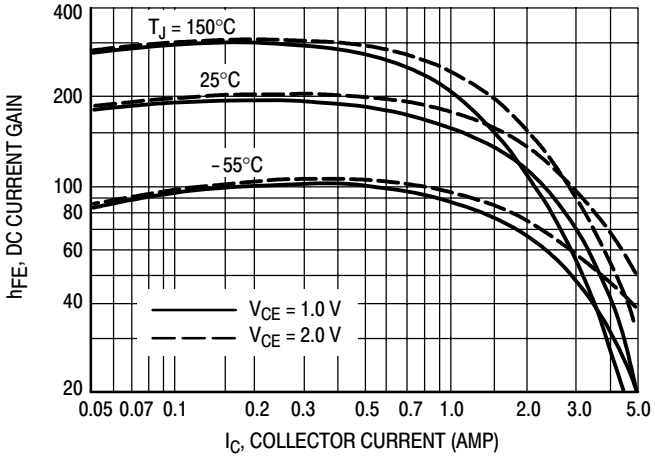


Figure 7. Capacitance

NPN
MJE200



PNP
MJE210

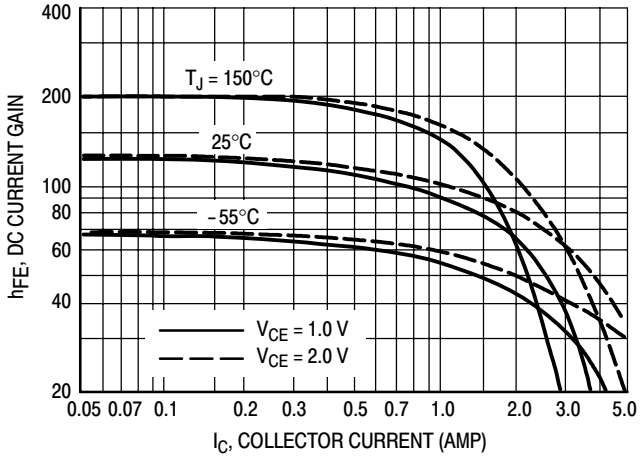
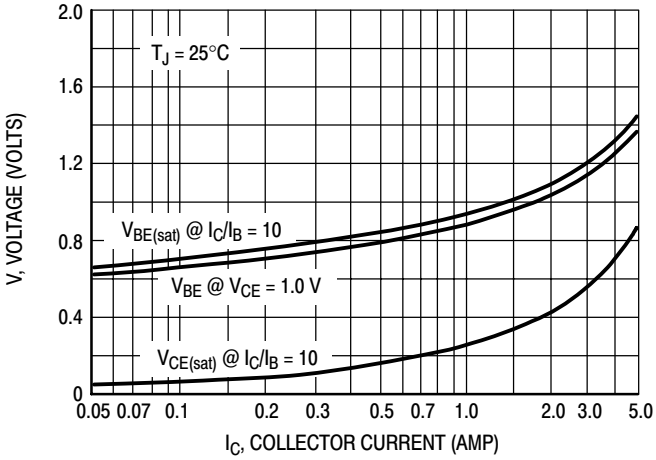


Figure 8. DC Current Gain



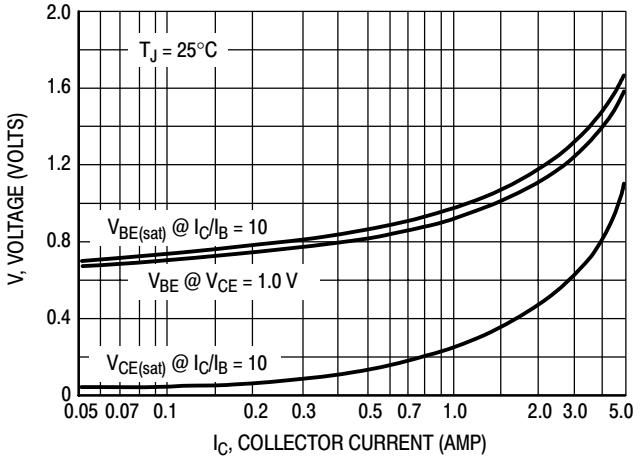
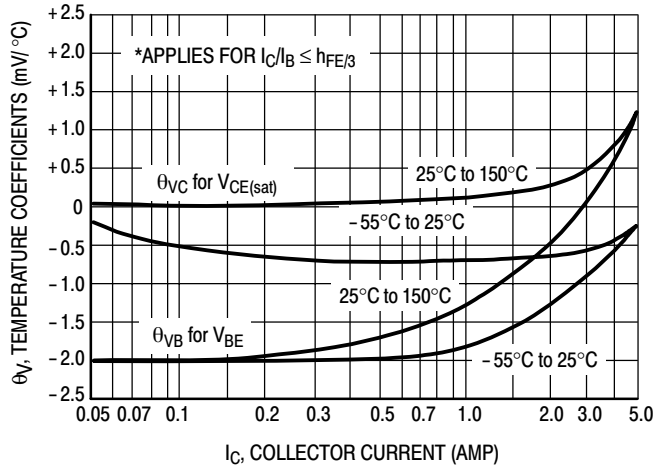


Figure 9. “On” Voltage



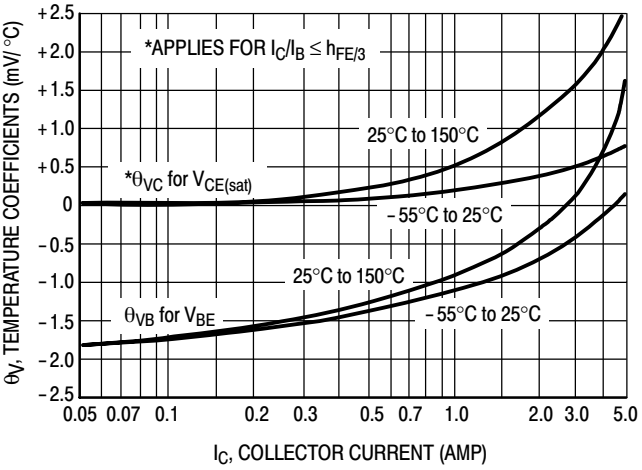
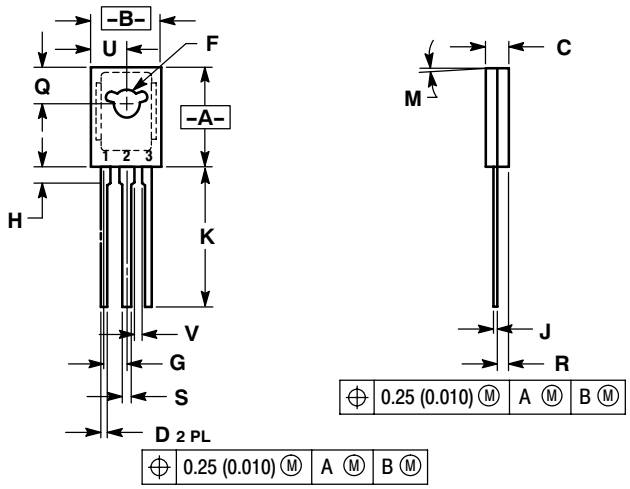


Figure 10. Temperature Coefficients

PACKAGE DIMENSIONS

TO–225
CASE 77–09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077–01 THRU –08 OBSOLETE, NEW STANDARD 077–09.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

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MJE200/D