

**MJE13005-K****NPN SILICON TRANSISTOR****NPN SILICON POWER TRANSISTORS****DESCRIPTION**

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE.

FEATURES

- * $V_{CEQ(SUS)} = 400\text{ V}$
- * Reverse bias SOA with inductive loads @ $T_C = 100^\circ\text{C}$
- * Inductive switching matrix 2 to 4 Amp, 25 and 100°C
 t_c @ 3A, 100°C is 180 ns (Typ)
- * 700V blocking capability
- * SOA and switching applications information

APPLICATIONS

- * Switching regulator's, inverters
- * Motor controls
- * Solenoid/Relay drivers
- * Deflection circuits

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
MJE13005L-K-x-TA3-T	MJE13005G-K-x-TA3-T	TO-220	B	C	E	Tube
MJE13005L-K-x-TF3-T	MJE13005G-K-x-TF3-T	TO-220F	B	C	E	Tube
MJE13005L-K-x-TM3-T	MJE13005G-K-x-TM3-T	TO-251	B	C	E	Tube
MJE13005L-K-x-TMS4-T	MJE13005G-K-x-TMS4-T	TO-251S4	B	C	E	Tube
MJE13005L-K-x-TN3-R	MJE13005G-K-x-TN3-R	TO-252	B	C	E	Tape Reel
MJE13005L-K-x-T60-R	MJE13005G-K-x-T60-K	TO-126	B	C	E	Bulk

Note: Pin Assignment: B: Base C: Collector E: Emitter

MJE13005L-K-x-TA3-T (1) Packing Type (2) Package Type (3) Rank (4) Green Package		(1) T: Tube, R: Tape Reel, K: Bulk (2) TA3: TO-220, TF3: TO-220F, TM3: TO-251, TMS4: TO-251S4, TN3: TO-252, T60: TO-126 (3) x: refer to Classification of h_{FE1} (4) L: Lead Free, G: Halogen Free and Lead Free
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MARKING

TO-220 / TO-220F / TO-251 TO-251S4 / TO-252	TO-126
UTC MJE13005 Lot Code ← Data Code 1 L: Lead Free G: Halogen Free	UTC 13005 Lot Code ← Data Code 1 L: Lead Free G: Halogen Free

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		$V_{CEO(SUS)}$	400	V
Collector-Emitter Voltage ($V_{BE}=0$)		V_{CES}	700	V
Collector-Base Voltage		V_{CBO}	700	V
Emitter Base Voltage		V_{EBO}	9	V
Collector Current	Continuous	I_C	4	A
	Peak (1)	I_{CM}	8	A
Base Current	Continuous	I_B	2	A
	Peak (1)	I_{BM}	4	A
Emitter Current	Continuous	I_E	6	A
	Peak (1)	I_{EM}	12	A
Power Dissipation at $T_C=25^\circ\text{C}$	TO-220	P_D	75	W
	TO-220F		40	
	TO-251/TO-251S4		50	
	TO-252			
	TO-126		20	
Derate above 25°C	TO-220		600	mW/ $^\circ\text{C}$
	TO-220F		320	
	TO-251/TO-251S4		400	
	TO-252			
	TO-126		160	
Operating and Storage Junction Temperature		T_J, T_{STG}	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient Junction to Case	TO-220/TO-220F	θ_{JA}	62.5	$^\circ\text{C/W}$
	TO-251/TO-251S4		80	
	TO-252			
	TO-126		89	
	TO-220	θ_{JC}	1.67	$^\circ\text{C/W}$
	TO-220F		3.125	
	TO-251/TO-251S4		2.5	
	TO-252			
	TO-126		6.25	

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (Note 1)						
Collector-Emitter Sustaining Voltage	V _{CEO(SUS)}	I _C =10mA , I _B =0	400			V
Collector Cutoff Current	I _{CBO}	V _{CBO} =Rated Value, V _{BE(OFF)} =1.5V			1	mA
		V _{CBO} =Rated Value, V _{BE(OFF)} =1.5V, T _C =100°C			5	
Emitter Cutoff Current	I _{EBO}	V _{EB} =9V, I _C =0			1	mA
SECOND BREAKDOWN						
Second Breakdown Collector Current with bass forward biased	I _{S/B}				See Fig. 11	
Clamped Inductive SOA with Base Reverse Biased	RBSOA				See Fig. 12	
ON CHARACTERISTICS (Note 1)						
DC Current Gain	h _{FE1}	I _C =0.5A, V _{CE} =5V	15		50	
	h _{FE2}	I _C =1A, V _{CE} =5V	10		60	
	h _{FE3}	I _C =2A, V _{CE} =5V	8		40	
Collector-Emitter Saturation Voltage	V _{CE(SAT)}	I _C =1A, I _B =0.2A			0.5	V
		I _C =2A, I _B =0.5A			0.6	V
		I _C =4A, I _B =1A			1	V
		I _C =2A, I _B =0.5A, T _a =100°C			1	V
Base-Emitter Saturation Voltage	V _{BE (SAT)}	I _C =1A, I _B =0.2A			1.2	V
		I _C =2A, I _B =0.5A			1.6	V
		I _C =2A, I _B =0.5A, T _C =100°C			1.5	V
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product	f _T	I _C =500mA, V _{CE} =10V, f=1MHz	4			MHz
Output Capacitance	C _{OB}	V _{CB} =10V, I _E =0, f=0.1MHz		65		pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	t _D	V _{CC} =125V, I _C =2A, I _{B1} =I _{B2} =0.4A, t _p =25μs, Duty Cycle≤1%		0.025	0.1	μs
Rise Time	t _R			0.3	0.7	μs
Storage Time	t _S			1.7	4	μs
Fall Time	t _F			0.4	0.9	μs

Note: 1. Pulse Test: Pulse Width=5ms, Duty Cycle≤10%

2. Pulse Test: P_W=300μs, Duty Cycle≤2%

■ CLASSIFICATION OF h_{FE1}

RANK	A	B	C	D	E
RANGE	15 ~ 20	20 ~ 25	25 ~ 30	30 ~ 40	40 ~ 50

■ APPLICATION INFORMATION

Table 1. Test Conditions for Dynamic Performance

Reverse Bias Safe Operating Area and Inductive Switching		Resistive Switching
Test Circuits	DUTY CYCLE $\leq 10\%$ $t_r, t_f \leq 10\text{ns}$ Note: P_w and V_{cc} Adjusted for Desired I_c R_B Adjusted for Desired I_{B1} *SELECTED FOR $\geq 1\text{kV}$	
Circuit Values	Coil Data : $V_{CC}=20\text{V}$ FERROXCUBE core #6656 Full Bobbin (~ 16 Turns) #16 GAP for 200 $\mu\text{H}/20\text{A}$ $L_{COIL}=200\mu\text{H}$ $V_{CLAMP}=300\text{V}$	$V_{CC}=125\text{V}$ $R_C=62\Omega$ $D1=1\text{n}5820$ or Equiv. $R_B=22\Omega$
Test Waveforms	OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_c $t_1 = \frac{L_{COIL}(I_{CPK})}{V_{CC}}$ $t_2 = \frac{L_{COIL}(I_{CPK})}{V_{CLAMP}}$ Test Equipment Scope-Tektronics 475 or Equivalent	$t_R, t_F < 10\text{ns}$ Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

RESISTIVE SWITCHING PERFORMANCE

Fig. 1 Turn-On Time

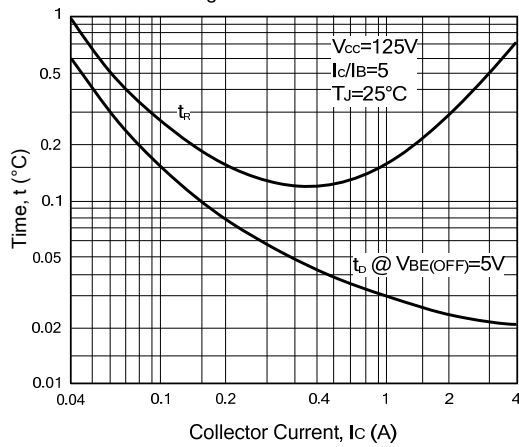


Fig. 2 Turn-Off Time

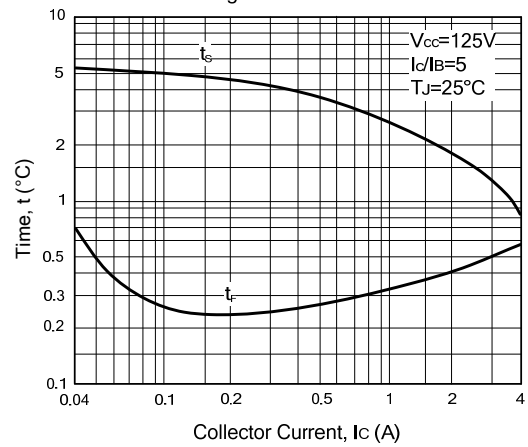


Fig. 3 Typical Thermal Response [$Z_{\theta JC}(t)$]

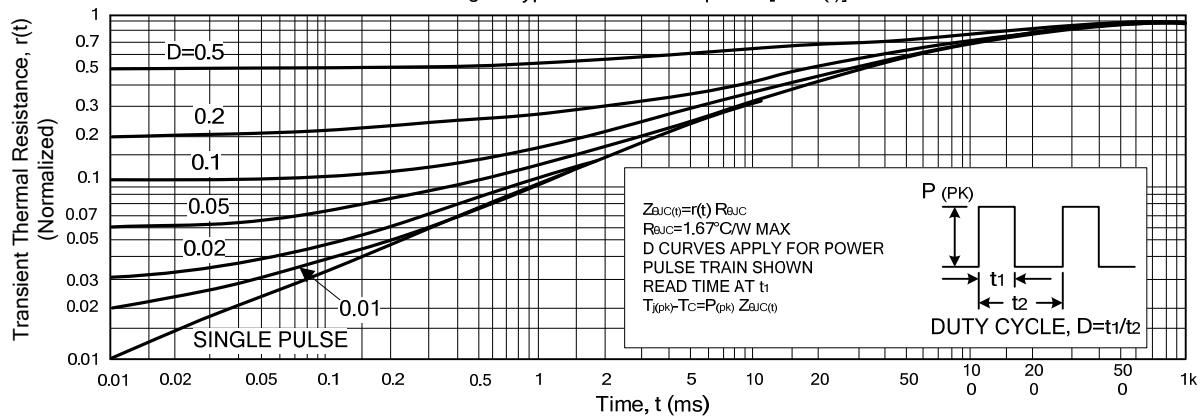


Fig. 4 Forward Bias Safe Operating Area

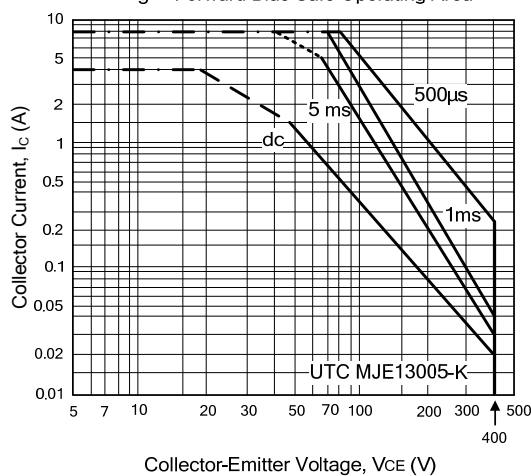
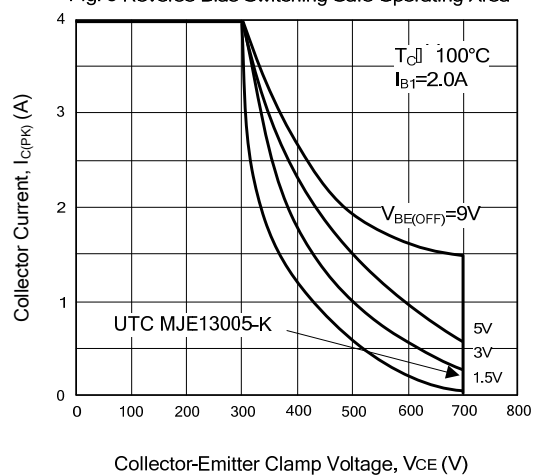
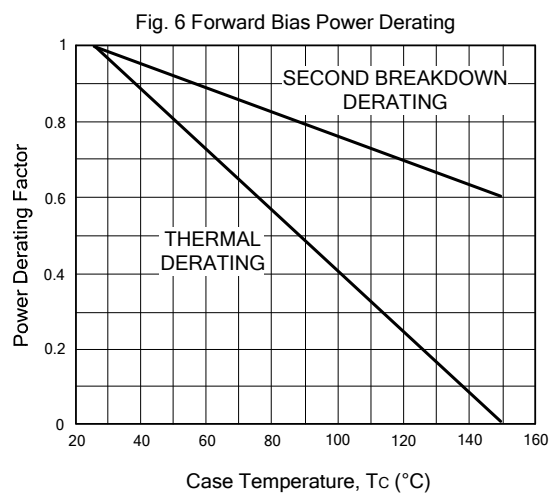


Fig. 5 Reverse Bias Switching Safe Operating Area



■ RESISTIVE SWITCHING PERFORMANCE (Cont.)



■ SAFE OPERATING AREA INFORMATION**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 4 is based on $T_C = 25^\circ\text{C}$; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Fig. 4 may be found at any case temperature by using the appropriate curve on Fig. 6.

$T_{J(PK)}$ may be calculated from the data in Fig. 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives the complete RBSOA characteristics.

TYPICAL CHARACTERISTICS

Figure 7. DC Current Gain

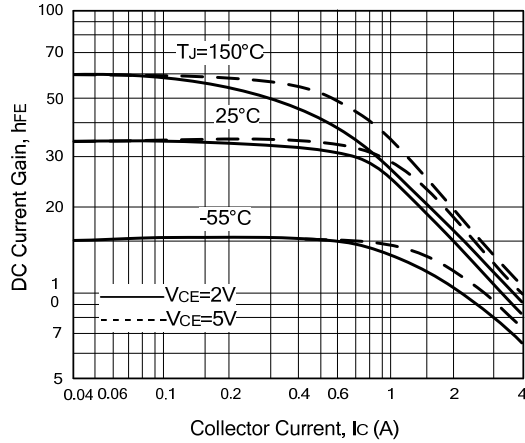


Figure 8. Collector Saturation Region

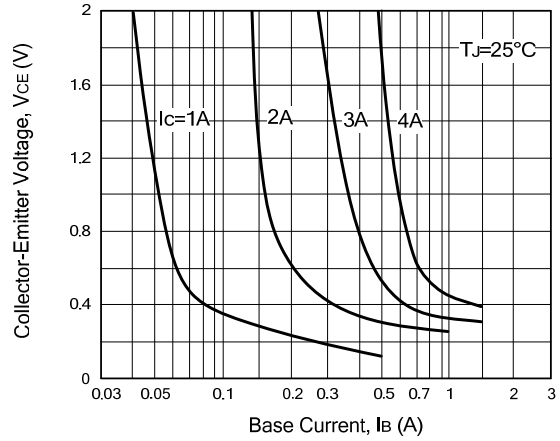


Figure 9. Base-Emitter Voltage

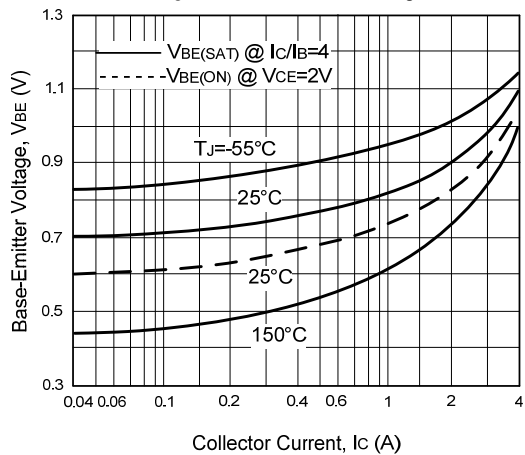


Figure 10. Collector-Emitter Saturation Voltage

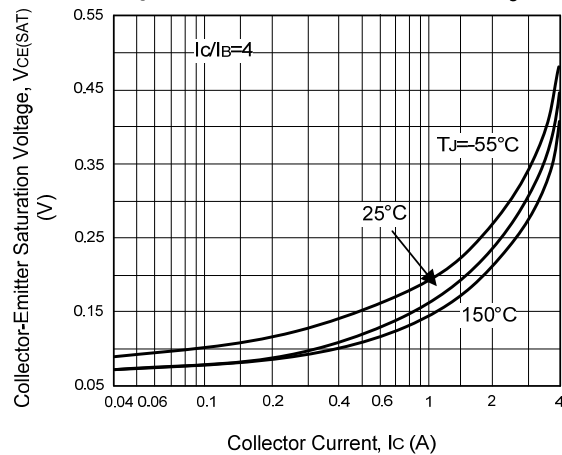


Figure 11. Collector Cutoff Region

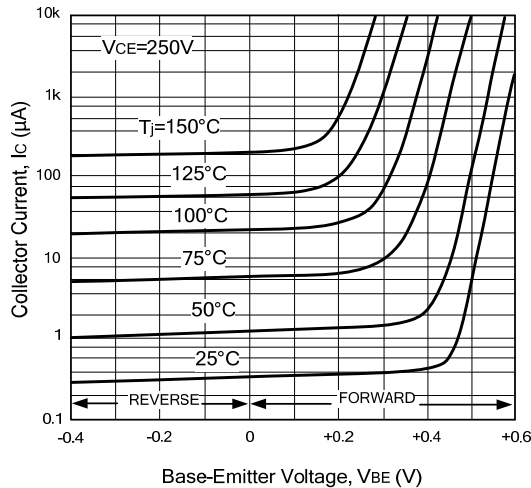
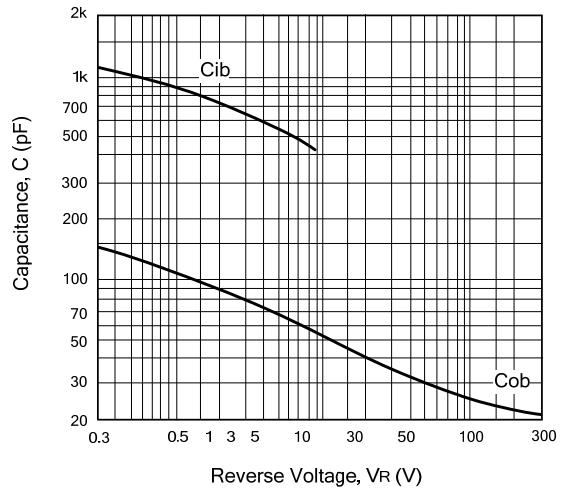


Figure 12. Capacitance



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