

**MJE13003K****NPN SILICON TRANSISTOR****NPN SILICON POWER TRANSISTOR****DESCRIPTION**

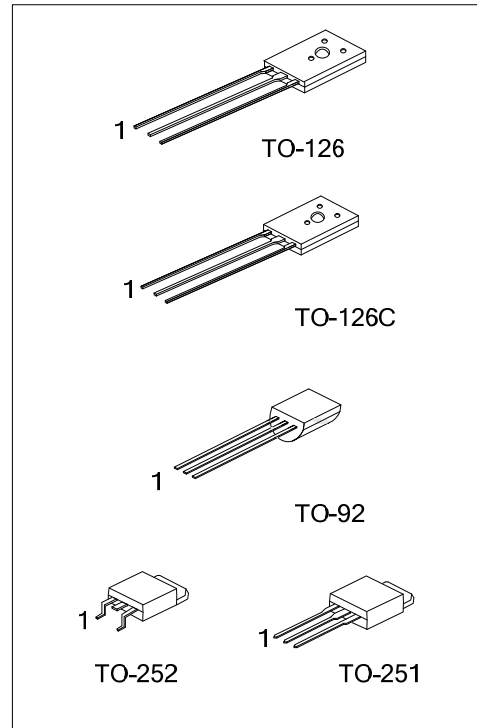
These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220V SWITCHMODE.

FEATURES

- * Reverse biased SOA with inductive load @ $T_c=100^\circ\text{C}$
- * Inductive switching matrix 0.5 ~ 1.5 Amp, 25 and 100°C
Typical $t_c = 290\text{ns}$ @ 1A, 100°C .
- * 700V blocking capability

APPLICATIONS

- * Switching regulator's, inverters
- * Motor controls
- * Solenoid/relay drivers
- * Deflection circuits

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
MJE13003KL-x-x-T60-K	MJE13003KG-x-x-T60-K	TO-126	B	C	E	Bulk
MJE13003KL-x-x-T6C-A-K	MJE13003KG-x-x-T6C-A-K	TO-126C	E	C	B	Bulk
MJE13003KL-x-x-T6C-F-K	MJE13003KG-x-x-T6C-F-K	TO-126C	B	C	E	Bulk
MJE13003KL-x-x-T92-B	MJE13003KG-x-x-T92-B	TO-92	E	C	B	Tape Box
MJE13003KL-x-x-T92-K	MJE13003KG-x-x-T92-K	TO-92	E	C	B	Bulk
MJE13003KL-x-x-T92-R	MJE13003KG-x-x-T92-R	TO-92	E	C	B	Tape Reel
MJE13003KL-x-x-T9L-B	MJE13003KG-x-x-T9L-B	TO-92L	E	C	B	Tape Box
MJE13003KL-x-x-T9L-K	MJE13003KG-x-x-T9L-K	TO-92L	E	C	B	Bulk
MJE13003KL-x-x-T9L-R	MJE13003KG-x-x-T9L-R	TO-92L	E	C	B	Tape Reel
MJE13003KL-x-x-TM3-T	MJE13003KG-x-x-TM3-T	TO-251	B	C	E	Tube
MJE13003KL-x-x-TN3-R	MJE13003KG-x-x-TN3-R	TO-252	B	C	E	Tape Reel
MJE13003KL-x-x-TN3-T	MJE13003KG-x-x-TN3-T	TO-252	B	C	E	Tube

	(1) Packing Type
	(2) Pin Assignment
	(3) Package Type
	(4) Rank
	(5) T_s
	(6) Lead Free

(1) B: Tape Box, K: Bulk, R: Tape Reel, T: Tube
 (2) refer to Pin Assignment (for TO-126C)
 (3) T60: TO-126, T6C: TO-126C, T92: TO-92, T9L: TO-92L, TM3: TO-251, TN3: TO-252
 (4) x: refer to Classification of h_{FE1}
 (5) x: Storage Time of T_s
 (6) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		$V_{CEO(SUS)}$	400	V
Collector-Base Voltage		V_{CBO}	700	V
Emitter Base Voltage		V_{EBO}	9	V
Collector Current	Continuous	I_C	1.5	A
	Peak (1)	I_{CM}	3	
Base Current	Continuous	I_B	0.75	A
	Peak (1)	I_{BM}	1.5	
Emitter Current	Continuous	I_E	2.25	A
	Peak (1)	I_{EM}	4.5	
Total Power Dissipation ($T_a=25^{\circ}\text{C}$)	TO-126/ TO-126C	P_D	1.4	W
	TO-92/ TO-92L		1.1	W
Total Power Dissipation ($T_c=25^{\circ}\text{C}$)	TO-252/ TO-251		25	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (Note)							
Collector-Emitter Sustaining Voltage			I _C =10 mA , I _B =0	400			V
Collector Cutoff Current	T _C =25°C	I _{CEO}	V _{CEO} =Rated Value, V _{BE(OFF)} =1.5 V			1	mA
	T _C =100°C					5	
Emitter Cutoff Current		I _{EBO}	V _{EB} =9 V, I _C =0			1	mA
SECOND BREAKDOWN							
Second Breakdown Collector Current with bass forward biased		I _{S/b}		See Figure 5			
Clamped Inductive SOA with base reverse biased		RB _{SOA}		See Figure 6			
ON CHARACTERISTICS (Note)							
DC Current Gain	h _{FE1}	I _C =0.5A, V _{CE} =5V	8		51		
	h _{FE2}	I _C =1A, V _{CE} =2V	5		30		
Collector-Emitter Saturation Voltage	V _{CE(SAT)}	I _C =0.5A, I _B =0.1A			0.5	V	
		I _C =1A, I _B =0.25A			1		
		I _C =1.5A, I _B =0.5A			3		
		I _C =1A, I _B =0.25A, T _C =100°C			1		
Base-Emitter Saturation Voltage	V _{BE(SAT)}	I _C =0.5A, I _B =0.1A			1	V	
		I _C =1A, I _B =0.25A			1.2		
		I _C =1A, I _B =0.25A, T _C =100°C			1.1		
DYNAMIC CHARACTERISTICS							
Current-Gain-Bandwidth Product		f _T	I _C =100mA, V _{CE} =10V, f=1MHz	4	10		MHz
Output Capacitance		Cob	V _{CB} =10V, I _E =0, f=0.1MHz		21		pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	t _D	V _{CC} =125V, I _C =1A, I _{B1} =I _{B2} =0.2A, t _P =25μs, Duty Cycle≤1%		0.05	0.1	μs	
Rise Time	t _R			0.5	1	μs	
Storage Time	t _S			2	4	μs	
Fall Time	t _F			0.4	0.7	μs	
Inductive Load, Clamped (Table 1)							
Storage Time	t _{STG}	I _C =1A, Vclamp=300V, I _{B1} =0.2A, V _{BE(OFF)} =5Vdc, T _C =100°C		1.7	4	μs	
Crossover Time	t _C			0.29	0.75	μs	
Fall Time	t _F			0.15		μs	

Note: Pulse Test : PW=300μs, Duty Cycle≤2%

■ CLASSIFICATION OF h_{FE1}

RANK	A	B	C	D	E	F	G	H
RANGE	8 ~ 16	15 ~ 21	20 ~ 26	25 ~ 31	30 ~ 36	35 ~ 40	40 ~ 46	45 ~ 51

Table 1. Test Conditions for Dynamic Performance

Reverse Bias Safe Operating Area and Inductive Switching		Resistive Switching
Test Circuits	NOTE Pw and Vcc Adjusted for Desired Ic Rb Adjusted for Desired Ib1	
Circuit Values	Coil Data : VCC=20V Ferroxcube core #6656 Vclamp=300V Full Bobbin (~ 200 Turns) #20 GAP for 30 mH/2 A Lcoil=50mH	VCC=125V RC=125Ω D1=1N5820 or Equiv. RC=47Ω
Test Waveforms	Output Waveforms $t_1 \approx \frac{L_{coil}(I_{c(pk)})}{V_{cc}}$ $t_2 \approx \frac{L_{coil}(I_{c(pk)})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent	tr, tf<10ns Duty Cycle=1.0% Ra and Rc adjusted for desired Ia and Ic

Figure 1. Inductive Switching Measurements

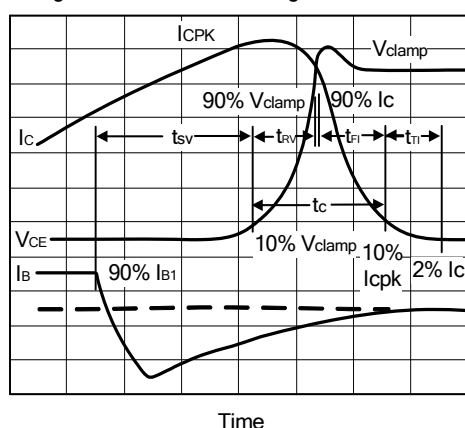


Table 2. Typical Inductive Switching Performance

Ic AMP	Tc °C	tsv μs	trv μs	tFI μs	tFI μs	tc μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads, which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{RV} = Voltage Rise Time, 10 ~ 90% V_{clamp}
- t_{FI} = Current Fall Time, 90 ~ 10% I_C
- t_{TI} = Current Tail, 10 ~ 2% I_C
- t_C = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$PSWT = 1/2 V_{CC} I_C (t_C) f$$

In general, $t_{RV} + t_{FI} \approx t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

Figure 2. Turn-On Time

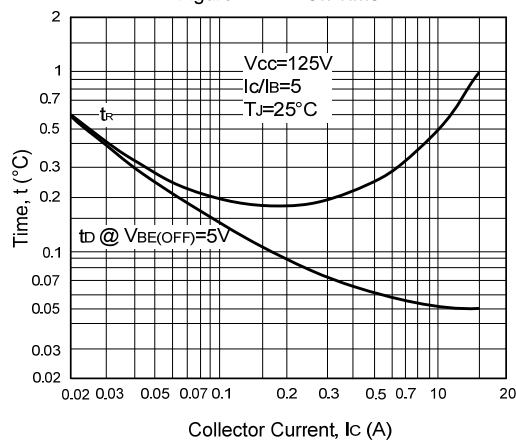


Figure 3. Turn-Off Time

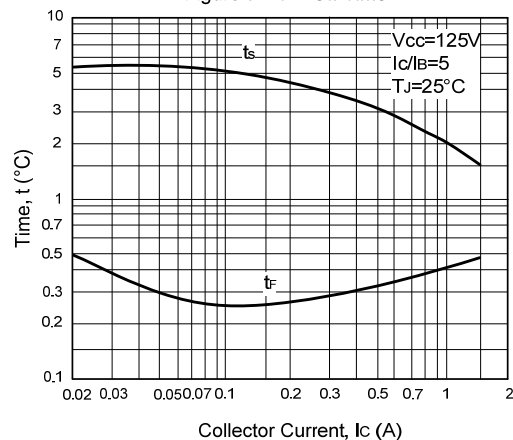
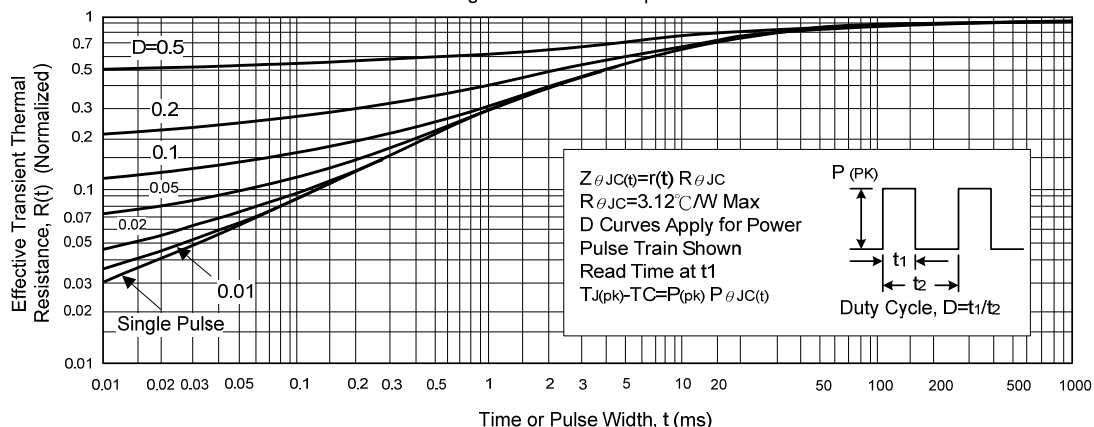


Figure 4. Thermal Response



■ SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

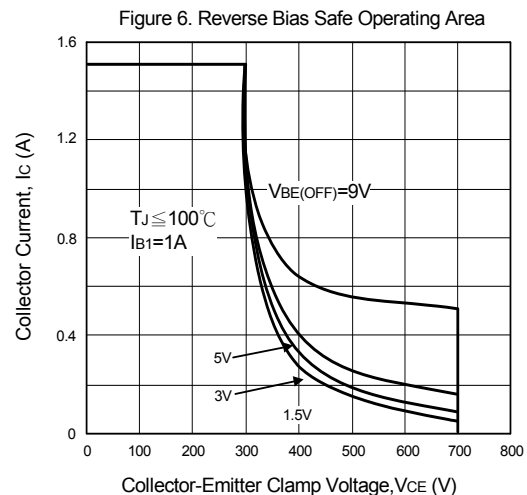
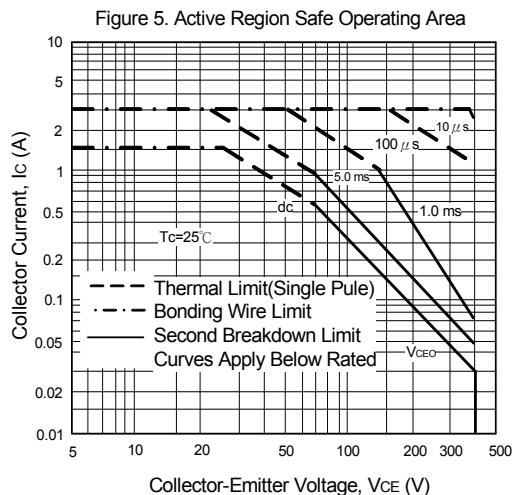
The data of Figure 5 is based on $T_C = 25^\circ\text{C}$; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 5.

$T_{J(PK)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

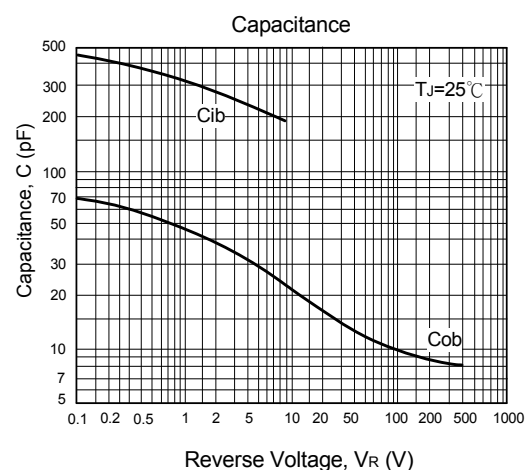
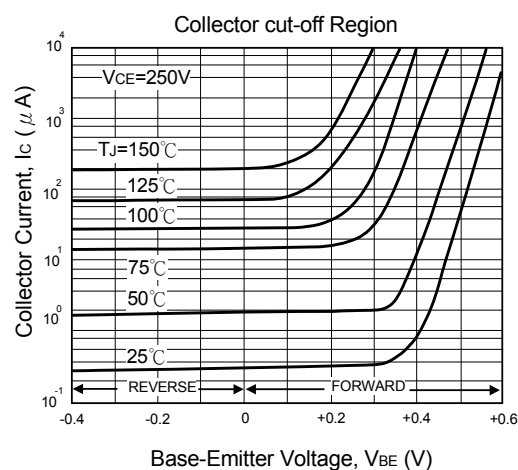
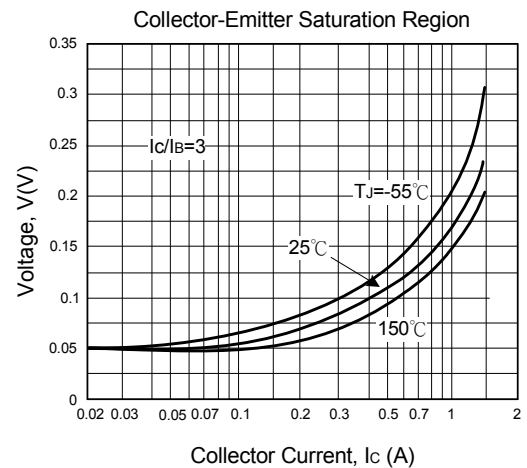
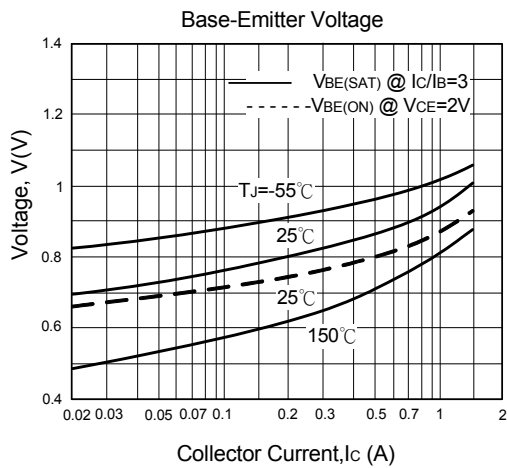
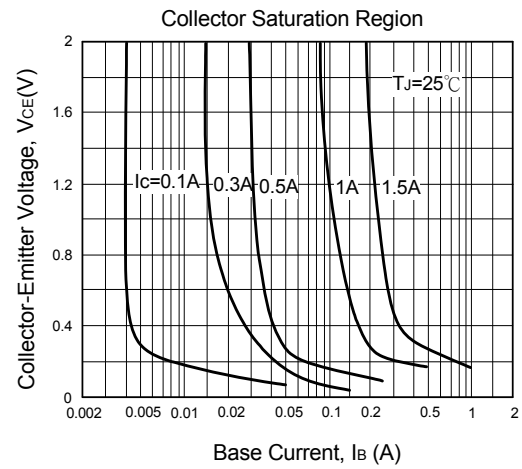
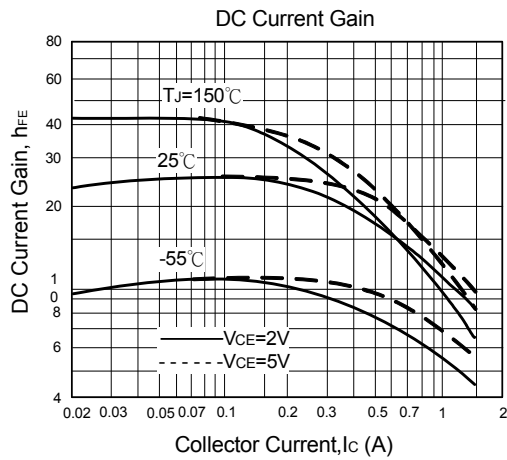
REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 6 gives PBSOA characteristics.

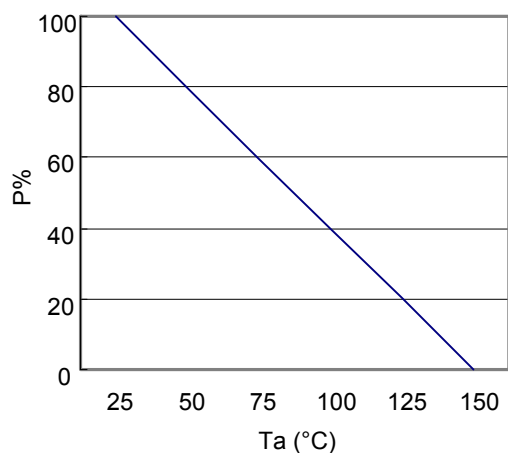
The Safe Operating Area of Figures 5 and 6 are specified ratings (for these devices under the test conditions shown.)



■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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