MICRF010

QwikRadio® Low-Power UHF Receiver

General Description

The MICRF010 is a single chip, ASK/OOK (ON-OFF Keyed) RF receiver IC recommended for new designs replacing the MICRF007. It provides the same function with sensitivity enhancement, typically 6dB better than the MICRF007. Just like all other members of the QwikRadio® family, the MICRF010 achieves low power operation, a very high level of integration, and it is particularly easy to use.

All post-detection data filtering is provided on the MICRF010, so no external baseband filters are required. In fact, the entire receiver circuit is made of very few external components and with the 8-pin SOIC package makes it ideal for small printed circuit board area applications.

The MICRF010 works in fixed-mode (FIX) operation, which functions as a conventional super-heterodyne receiver. Fixed-mode provides better selectivity and sensitivity performance in comparison with sweep mode used in other Micrel receivers intended for lower cost applications.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

QwikRadio™

Features

- High sensitivity (–104dBm)
- 300MHz to 440MHz frequency range
- Data-rate up to 2.0kbps (Manchester encoding)
- Low power consumption
  - 2.9mA fully operational (315MHz)
  - 0.15µA in shutdown
  - 290µA in polled mode (10:1 duty-cycle)
- Shutdown input
- Automatic tuning, no manual adjustment
- Very low RF re-radiation at the antenna
- Highly integrated with extremely low external part count

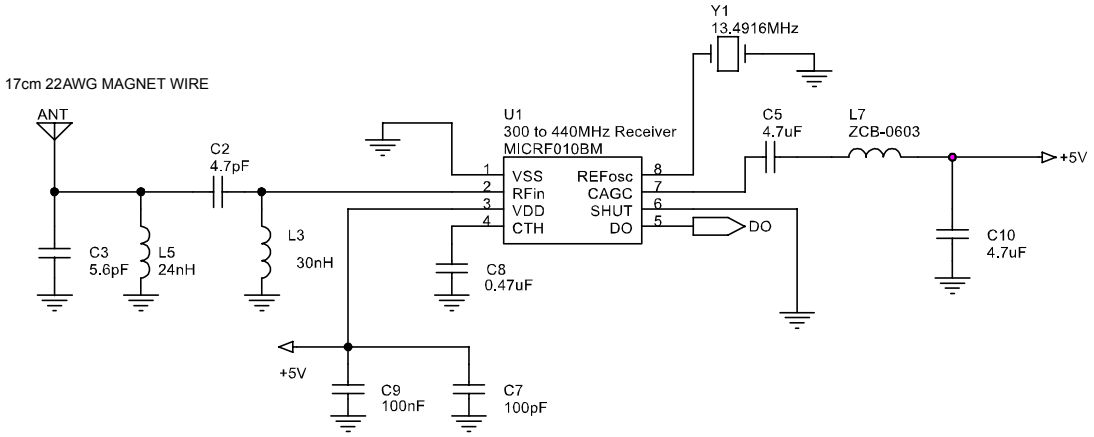
Applications

- Automotive remote keyless entry (RKE)
- Long range RF identification
- Remote fan and light control
- Garage door and gate openers

Ordering Information

Part Number		Operating Mode	Shutdown	Package
Standard	Pb-Free			
MICRF010BM	MICRF010YM	Fixed	Yes	8-pin SOIC

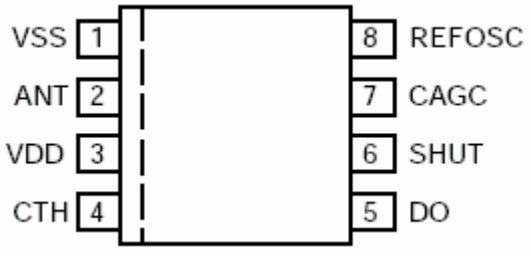
Typical Application



433.92Mhz 1000 bps Manchester Encoded On-Off Keyed Receiver

QwikRadio is a registered trademark of Micrel, Inc. The QwikRadio Ics were developed under a partnership agreement with AIT of Orlando, Florida.

Pin Configuration



Standard 8-Pin SOIC (M)

Pin Description

Pin Number	Pin Name	Pin Function
1	VSS	Ground Return (input): ground return to the power supply. See “Applications Information” for bypass capacitor details.
2	ANT	Antenna (Input): See “Applications Information” for information on input impedance. For optimal performance the antenna impedance should be matched to the antenna pin impedance.
3	VDD	Power Supply (Input): Positive Supply input for the RF IC. Connect a low ESL, low ESR decoupling capacitor from this to VSS, with lead length kept as short as possible.
4	CTH	[Data Slicing] Threshold Capacitor (External Component): Capacitor extracts the DC average value from the demodulated waveform, which becomes the reference for the internal data slicing comparator. See “Applications Information” for selection.
5	DO	Digital Output (Output): CMOS level compatible data output signal.
6	SHUT	Shutdown (Input): Shutdown-mode logic-level control input. Pull low to enable the receiver. This input is pulled-up internally to VDD.
7	CAGC	AGC Capacitor (External Component): Integrating capacitor for on-chip AGC (automatic gain control). See “Applications Information” for capacitor selection.
8	REFOSC	Reference Oscillator (External Component or Input): Timing reference for on-chip tuning and alignment.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DDRF}, V_{DDBB}) ..... +7V
Input/Output Voltage ($V_{I/O}$) ..... V_{SS}–0.3 to V_{DD}+0.3
Max Input Power ..... +20dBm
Junction Temperature (T_J) ..... +150°C
Storage Temperature Range (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +260°C
ESD Rating ..... **Note 3**

Operating Ratings[2]

Supply Voltage (V_{DDRF}, V_{DDBB}) ..... +4.75V to +5.5V
Max Input Power 0dBm
RF Frequency Range ..... 300MHz to 440Hz
Data Duty-Cycle ..... 20% to 80%
Reference Oscillator Input Range ..... $0.2V_{PP}$ to $1.5V_{PP}$
Ambient Temperature (T_A) ..... –40°C to +85°C

Electrical Characteristics[4]

4.75V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V; C_{AGC} = 4.7µF, C_{TH} = 0.022µF; f_{REFOSC} = 9.794MHz (equivalent to f_{RF} = 315MHz); data rate = 600 bps (Manchester encoded). T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; current flow into device pins is positive, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OP}	Operating Current	continuous operation, f_{RF} = 315MHz		2.9	**4.5**	mA
		Polled with 10:1 duty cycle, f_{RF} = 315MHz		290		µA
		Continuous operation, f_{RF} = 433.92MHz		4.7	**7.5**	µA
		Polled with 10:1 duty cycle, f_{RF} = 433.92MHz		470		µA
I_{STBY}	Standby Current	V_{SHUT} = 0.8VDD		0.15	**0.5**	µA
RF Section, IF Section						
	Receiver Sensitivity(4)	f_{RF} = 315MHz Note 4		–105		dBm
		f_{RF} = 433.92MHz Note 4		–103		
f_{IF}	IF Center Frequency	Note 5		0.86		MHz
f_{BW}	IF 3dB Bandwidth	Note 5		0.6		MHz
	Spurious Reverse Isolation	ANT pin, R_{SC} = 50Ω[6]		30		µVrms
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$		0.1		
	AGC Leakage Current	T_A = +85°		±100		nA
Reference Oscillator						
Z_{REFOSC}	Reference Oscillator Input Impedance	Note 7		290		kΩ
	Reference Oscillator Source	Note 8		5.0		µA
Demodulator						
Z_{CTH}	CTH Source Impedance	Note 9		150		kΩ
$I_{ZCTH(leak)}$	CTH Leakage Current	T_A = +85°C		±100		nA
	Demodulator Filter Bandwidth	Note 5		2000		Hz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital/Control Section						
V_{IH}	Input High Voltage	SHUT	**0.8**			V_{DD}
V_{IL}	Input Low Voltage	SHUT			**0.2**	V_{DD}
I_{OUT}	Output Current	DO pin, push-pull		45		µA
V_{OH}	Output High Voltage	DO pin, I_{OUT} = –30µA	**0.9**			V_{DD}
V_{OL}	Output Low Voltage	DO pin, I_{OUT} = +30µA			**0.1**	V_{DD}
t_R, t_F	Output Rise and Fall Time	DO pin, C_{LOAD} = 15pF		4		µs

Notes:

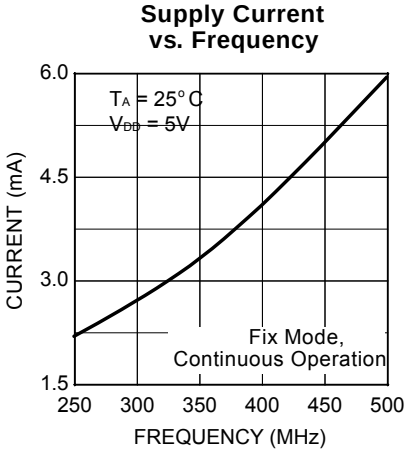
1. Exceeding absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive, use appropriate ESD precautions. The device meets Class 1 ESD test requirements, (human body model HBM), in accordance with MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.
4. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10^{-2} BER (bit error rate). The RF input is assumed to be matched to 50Ω.
5. Parameter scales linearly with reference oscillator frequency f_T. For any reference oscillator frequency other than 9.794MHz, compute new parameter value as the ratio:

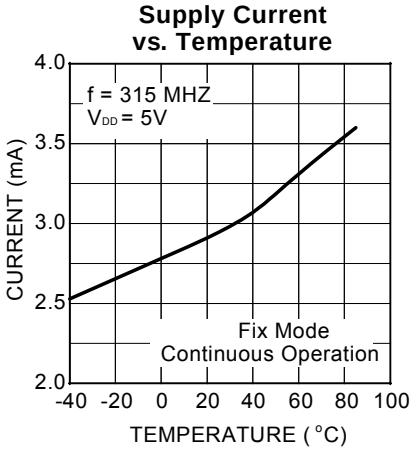
$$\frac{f_{REFOSC}MHZ}{9.794MHz} \times (\text{parameter value at 9.79MHz})$$

6. Spurious reverse isolation represents the spurious components, which appear on the RF input pin (ANT) measured into 50Ω with an input RF matching network.
7. Series resistance of the resonator (ceramic resonator or crystal) should be minimized to the extent possible. In cases where the resonator series resistance is too great, the oscillator may oscillate at a diminished peak-to-peak level, or may fail to oscillate entirely. Micrel recommends that series resistances for ceramic resonators and crystals not exceed 50Ω and 100Ω, respectively.
8. Crystal load capacitor is 10pF. See Figure 5 in “REFOSC” section for reference oscillator operation.
9. Parameter scales inversely with reference oscillator frequency f_T. For any reference oscillator frequency other than 9.794MHz, compute new parameter value as the ratio:

$$\frac{9.794MHz}{f_{REFOSC}MHZ} \times (\text{parameter value at 9.794MHz})$$

Typical Characteristics





Functional Diagram

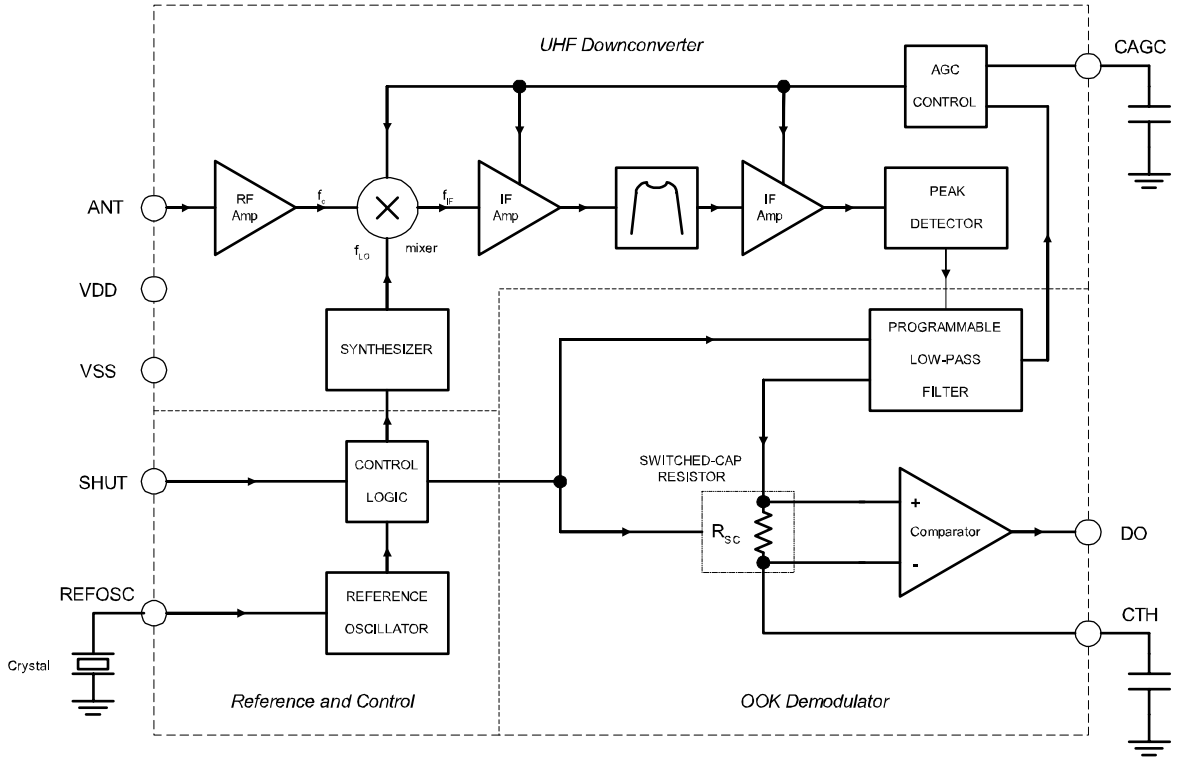


Figure 1. MICRF010 Block Diagram

Application Information and Function Description

"MICRF010 Block Diagram" above shows the IC partitioned into three sections: 1) UHF Downconverter, 2) OOK Demodulator, 3) Reference and Control. Also shown in the figure are two external capacitors (C_{TH}, C_{AGC}) and one timing element, which is usually a crystal. With the exception of a supply decoupling capacitor and antenna impedance matching network, these are the only external components needed by the MICRF010 to assemble a complete UHF receiver.

For optimal performance it is highly recommended that the MICRF010 is impedance-matched to the antenna. The matching network will add an additional two or three components.

The "SHUT" input is the only control input of the IC. It is used in polling operation for decreasing DC current consumption. This input is CMOS compatible and it is internally pulled-up.

The IF Bandpass Filter Roll-off response of the IF Filter is 5th order, and the demodulator data filter has a 2nd order response.

Design Steps:

The following steps are the basic design steps for using the MICRF010 receiver:

1. Select the reference oscillator
2. Select the demodulator filter bandwidth
3. Select the C_{TH} capacitor
4. Select the C_{AGC} capacitor

Step 1: Selecting The Reference Oscillator

All timing and tuning operations on the MICRF010 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of three ways:

1. Connect a crystal.
2. Drive this pin with an external timing signal.

The specific reference frequency required is related to the system transmit frequency.

Crystal Selection

The smaller the crystal, the longer it takes for the oscillator to start from a shutdown operation. If shorter start-up time

is desired, use crystals with lower ESR, which normally are bigger in size, like the HC49 package. “Application Hints 35” provides additional information and recommended sources for crystals. If using an externally applied signal, it should be AC-coupled and limited to the operating range of $0.2V_{PP}$ to $1.5V_{PP}$.

Selecting Reference Oscillator Frequency f_T

As with any super-heterodyne receiver, the difference between the internal LO (local oscillator) frequency f_{LO} and the incoming transmit frequency f_{TX}, should equal the IF center frequency. Equation 1 may be used to compute the appropriate f_{LO} for a given f_{TX}:

$$f_{LO} = f_{TX} \pm \left(0.86 \frac{f_{TX}}{315}\right) \quad (1)$$

Frequencies f_{TX} and f_{LO} are in MHz. Note that two values of f_{LO} exist for any given f_{TX}, distinguished as “high-side mixing” and “low-side mixing.” High-side mixing results in an image frequency above the frequency of interest and low-side mixing results in a frequency below. There is generally no preference of one over the other.

After choosing one of the two acceptable values of f_{LO}, use Equation 2 to compute the reference oscillator frequency f_T:

$$f_T = 2 \times \frac{f_{LO}}{64.5} \quad (2)$$

Frequency f_T is in MHz. Connect a crystal of frequency f_T to REFOSC on the MICRF010. Four-decimal-place accuracy on the frequency is generally adequate. The following table identifies f_T for some common transmit frequencies.

Transmit Frequency (f_{TX})	Reference Oscillator Frequency (f_T)
315.0 MHz	9.7941 MHz
390.0 MHz	12.1260 MHz
418.0 MHz	12.9966 MHz
433.92 MHz	13.4916 MHz

Table 1. Recommended Reference Oscillator Values For Typical Transmit Frequencies (high-side mixing)

Step 2: Selecting C_{TH} Capacitor

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip switched capacitor “resistor” RSC, as shown in the block diagram.

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms. This issue is covered in more detail in “Application Note 22.” Optimization of the value of C_{TH} is required to maximize range.

Selecting Capacitor C_{TH}

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent upon system issues including system decode response time and data code structure (that is, existence of data preamble, etc.) This issue is also covered in more detail in “Application Note 22.”

The effective resistance of R_{SC} is listed in the electrical characteristics table as 150kΩ at 315MHz, this value scales inversely with frequency. R_{SC} value at other frequencies is given by equation (4), where f_T is in MHz:

$$R_{SC} = 150\Omega \frac{9.7941}{f_T} \quad (4)$$

C_{TH} can be calculated using equation (5) with the knowledge of R_{sc} and τ.

$$C_{TH} = \frac{\tau}{R_{SC}} \quad (5)$$

Recommended τ is 5x the bit-rate.

A standard ±20% X7R ceramic capacitor for C_{TH} is generally sufficient. Refer to “Application Hint 42” for C_{TH} and C_{AGC} selection examples.

Step 3: Selecting C_{AGC} Capacitor

The signal path has AGC (automatic gain control) to increase input dynamic range. The attack time constant of the AGC is set externally by the value of the CAGC capacitor connected to the CAGC pin of the device. To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under $10mV_{PP}$ once the control voltage attains its quiescent value. For this reason, capacitor values of at least 0.47µF are recommended.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF010. When the device is placed into shutdown mode (SHUT pin is pulled high), the AGC capacitor floats to retain the voltage. When operation is resumed, only the voltage drop, due to capacitor leakage, must be replenished. A relatively low-leakage capacitor such as a ceramic type is recommended

when the devices are used in duty-cycled operation.

To further enhance duty-cycled operation, the AGC push and pull currents are boosted for approximately 10ms immediately after the device is taken out of shutdown. This compensates for AGC capacitor voltage drop and reduces the time to restore the correct AGC voltage. The current is boosted by a factor of 45.

Selecting CAGC Capacitor in Continuous Mode

A CAGC capacitor in the range of 0.47µF to 4.7µF is typically recommended. Caution! If the capacitor is too large, the AGC may react too slowly to incoming signals. AGC settling time, from a completely discharged (zero-volt) state is given approximately by Equation 6:

$$\Delta t = 1.333 \times C_{AGC} - 0.44 \quad (6)$$

where:

C_{AGC} is in µF, and Δt is in seconds.

Selecting CAGC Capacitor in Duty-Cycle Mode

Voltage droop across the CAGC capacitor during shutdown should be replenished as quickly as possible after the IC is enabled. As mentioned above, the MICRF010 boosts the push-pull current by a factor of 45 immediately after start-up. This fixed time period is based on the reference oscillator frequency f_T. The time is 10.9ms for f_T = 12.00MHz, and varies inversely with f_T. The value of CAGC capacitor and the duration of the shutdown time period should be selected such that the droop can be replenished within this 10ms period.

Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. The worst-case from a recovery standpoint is downward droop, since the AGC pull-up current is 1/10th magnitude of the pull-down current. The downward droop is replenished according to the Equation 7:

$$\frac{I}{C_{AGC}} = \frac{\Delta V}{\Delta t} \quad (7)$$

where:

I = AGC pull-up current for the initial 10ms (67.5µA)

C_{AGC} = AGC capacitor value

Δt = drop recovery time

ΔV = drop voltage

For example, if user desires Δt = 10ms and chooses a 4.7µF CAGC, the allowable droop is about 144mV. Using the same equation with 200nA, the worst-case pin leakage, and assuming 1µA of capacitor leakage in the same direction, the maximum allowable Δt (shutdown time) is about 0.56s for droop recovery in 10ms.

The ratio of decay-to-attack time-constant is fixed at 1:10 (that is, the attack time constant is 10 times of the decay time constant). Generally the design value of 1:10 is adequate for the vast majority of applications. If adjustment is required, adding a resistor in parallel of the C_{AGC} capacitor may vary the ratio. The value of the resistor must be determined on a case-by-case basis.

The Demodulator Filter Bandwidth

There is no external control to set the demodulator bandwidth. The maximum bandwidth is 2000 hertz at 315 MHz. Maximum bandwidth scales linearly with operating frequency. To minimize data pulse stretching, one must calculate the "demodulator BW required" to be certain that it does not exceed demodulator filter bandwidth of MICRF010 at operating frequency. For "demodulator BW required" calculation, one needs to identify the shortest pulse within the data profile and use equation 8 below:

$$\text{Demodulator BW Required} = \frac{0.65}{\text{shortest pulse - width}} \quad (8)$$

Refer to the "Electrical Characteristics" for the exact filter bandwidth at a chosen frequency.

Power Supply Bypass Capacitors

Supply bypass capacitors are strongly recommended. One example is to use 0.1uF ceramic capacitor in parallel with 100pF ceramic capacitor for VDD.

Data Squelching

During quiet periods (no signal), the data output (DO pin) transitions randomly with noise. Most decoders can discriminate between this random noise and actual data. For some systems, random transition due to noise during quiet period is a problem. There are three possible approaches to reduce this output noise:

1. Analog squelch to raise the demodulator threshold.
2. Digital squelch to disable the output when data is not present.
3. Output filter to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is to perform analog squelch by inducing a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal comparator, Usually 20mV to 30mV on CTH pin is sufficient. This may be achieved by connecting a several-meg-ohm resistor from the CTH pin to either VSSBB or VDDBB, depending upon the desired offset polarity. Since MICRF010's receiver AGC noise at the internal comparator input is always the same (set by the AGC), the squelch-offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce sensitivity and range. One should introduce minimal offset to sufficiently quiet the output. Typical squelch resistor values range from 10MΩ to 6.8MΩ for low to high squelch strength.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF010 are diagrammed in Figures 2 through 8. The ESD protection diodes at all input and output pins are not shown.

CTH Pin

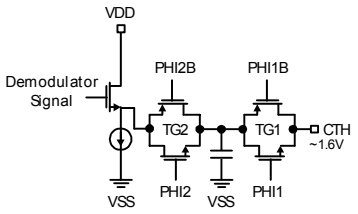


Figure 2. CTH Pin

Figure 2 illustrates the CTH pin interface circuit. The CTH pin is driven from a N-Channel MOSFET source-follower with approximately 10µA of bias. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a "resistance" of approximately 150kΩ. The DC potential at the CTH pin is approximately 1.6V

CAGC Pin

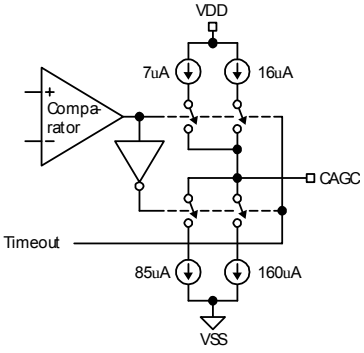


Figure 3. CAGC Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor CAGC. The attack current is nominally 1.5µA, while the decay current is a 10 times scaling of this, approximately 15µA. Signal gain of the RF/IF strip inside the IC diminishes as the voltage on CAGC decreases. By simply adding a capacitor to CAGC pin, the attack/decay time constant ratio is fixed at 10:1. Modification of the attack/decay ratio is possible by adding resistance from the CAGC pin to either VDDBB or VSSBB, as desired.

Both the push and pull current sources are disabled during shutdown, which maintains the voltage across CAGC, and improves recovery time in duty-cycled applications. To further improve duty-cycle recovery, both push and pull currents are increased by 45 times for approximately 10ms after release of the SHUT pin. This allows rapid recovery of any voltage droop on CAGC while in shutdown.

DO Pin

The output stage for the digital output (DO) is shown in Figure 4. The output is a 45µA push and 45µA pull switched-current stage. This output stage is capable of driving CMOS loads. An external buffer-driver is recommended for driving high capacitance loads.

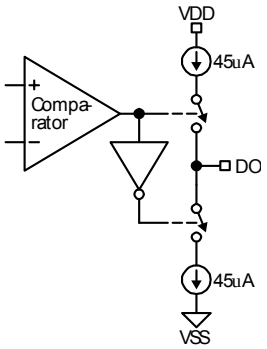


Figure 4. DO Pin

REFOSC Pin

The REFOSC input circuit is shown in Figure 5. Input impedance is quite high (290kΩ). This is a Colpitts oscillator, with internal 10pF capacitors.

Externally applied signals should be AC-coupled, amplitude limited to approximately $0.5V_{PP}$. The nominal DC bias voltage on this pin is 1.4V

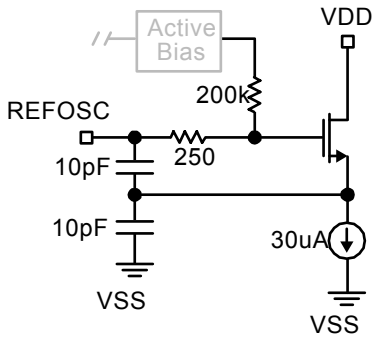


Figure 5. REFOSC Pin

SHUT Pin

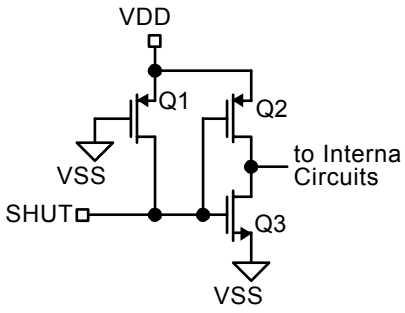


Figure 6. SHUT Pin

Control input circuitry is shown in Figure 6. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-Channel MOSFET Q1 is a large channel length device, which functions essentially as a “weak” pull-up to VDDBB. Typical pull-up current is 5µA, leading to an impedance to the VDD supply of typically 1MΩ.

Additional Applications Information

In addition to the basic operation of the MICRF010, the following enhancements can be made. In particular, it is strongly recommended that the antenna impedance is matched to the input of the IC.

Antenna Impedance Matching

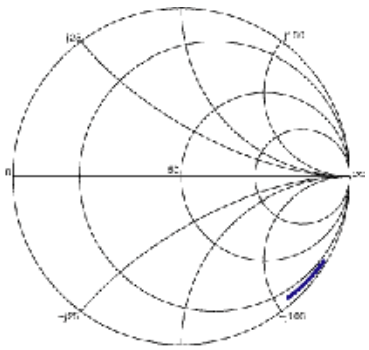


Figure 7. Antenna Pin Input Impedance

Figure 7 and Table 2 presents the antenna pin input impedance. The Antenna pin can be matched to 50Ω with a high pass circuit as shown in Figure 8. That is, a shunt inductor from the ANT Pin to ground and a series capacitor from ANT Pin to the antenna.

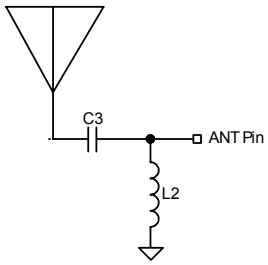


Figure 8. Antenna with Matching Network to ANT Pin

Inductor values may be different from Table 2, depending on PCB material, PCB thickness, ground configuration, and how long the traces are in the layout. Values shown were characterized for a 0.031 inch thickness, FR4 board, solid ground plane on bottom layer, and very short traces. MuRata and Coilcraft wire-wound 0603 or 0805 surface mount inductors were tested, however, any wire-wound inductor with high SRF (self-resonance frequency) should do the job.

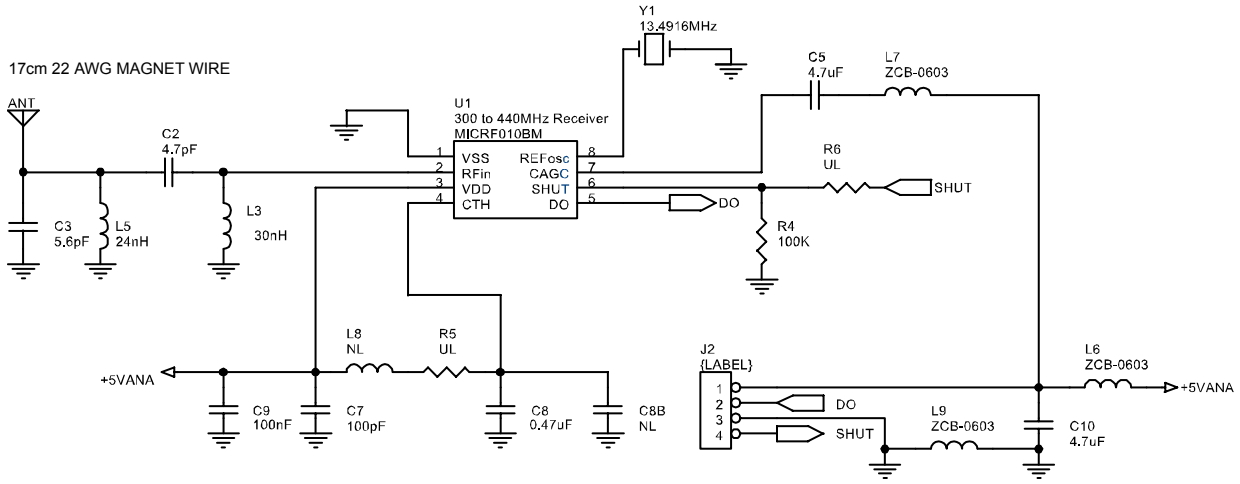
Frequency (Mhz)	S11 Mag, angle	Z11, ohms	C3, pF	L2, nH
300	0.944,-36.65	14.45-j150	2.2	47
305	0.940,-37.499	14.84-j145	2.2	47
310	0.942,-37.579	14.28-j145	2.2	47
315	0.945, -37.66	13.48-j145	2.2	47
320	0.943,-38.237	13.58-j143	2	47
325	0.942, -38.814	13.43-j140	1.8	47
330	0.94, -39.39	13.5-j138	1.8	47
335	0.938, -39.967	13.59-j136	1.8	43
340	0.937, -40.544	13.44-j134	1.8	43
345	0.935, -41.12	13.51-j132	1.8	43
350	0.933, -41.697	13.57-j130	2	39
355	0.931, -42.274	13.62-j123	2.2	36
360	0.93, 42.85	13.48-j126	2.2	36
365	0.928, -43.427	13.52-j124	2	36
370	0.926, -44.004	13.57-j122	1.8	36
375	0.925, -44.581	13.42-j120	2.2	33
380	0.923, -45.157	13.46-j118	2	33
385	0.921, -45.734	13.49-j117	1.8	33
390	0.92, -46.311	13.35-j115	1.8	33
395	0.917, -46.729	13.6-j114	1.8	33
400	0.914, -47.148	13.89-j113	2	30
405	0.912, -47.566	14.00-j112	1.8	30
410	0.909, -47.985	14.25-j110	1.8	30
415	0.907, -48.403	14.34-j109	2.2	27
420	0.906, -48.797	14.28-j108	2	27
425	0.909, -49.152	13.63-j107	2	27
430	0.911, -49.507	13.15-j107	1.8	27
435	0.911, -49.925	12.94-j106	1.8	27
440	0.904, -50.571	13.66-j104	1.8	27

Table 2

Shutdown Function

Duty-cycled operation of the MICRF010 (often referred to as polling) is achieved by turning the MICRF010 on and off via the SHUT pin. The shutdown function is controlled by a logic state applied to the SHUT pin. When VSHUT is high, the device goes into low-power standby mode. This pin is pulled high internally, and it must be externally pulled low to enable the receiver.

Application Example: 433.92Mhz, 1000 bps Manchester Encoded On-Off Keyed Receiver

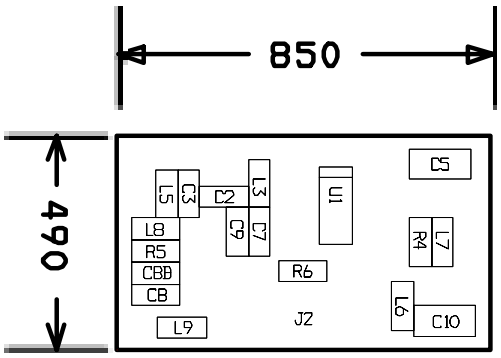


Bill of Materials

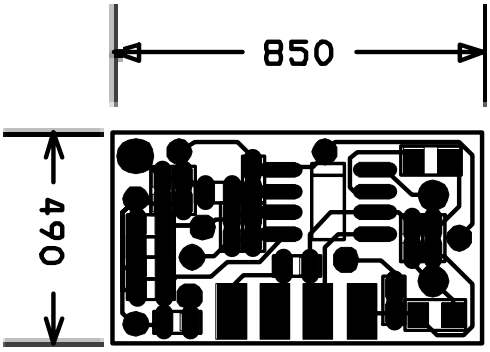
Item	Qty	Reference	Value	Description	Manufacturer	Part#
				CAPACITORS		
2	1	C3	5.6pF	5.6pF Capacitor, 0603, 50VDC, ±5%	MuRata	GRM1885C1H5R6DZ01B
4	1	C7	100pF	100pF Capacitor, 0603, 50VDC, ±5%	MuRata	GRM1885C1H101JA01B
1	1	C2	4.7pF	4.7pF Capacitor, 0603, 50VDC, ±5%	MuRata	GRM1885C1H4R7CZ01B
5	1	C8B	NL			
6	1	C8	0.47uF	0.47uF Capacitor, 0603, 25VDC, ±10%	MuRata	GRM188R61A474KA61B
7	1	C9	100nF	100nF Capacitor, 0603, 25VDC, ±10%	MuRata	GRM188R71E104KA01B
3	2	C5,C10	4.7uF	4.7uF Capacitor, 0805, 10VDC, +80-20%	MuRata	GRM21BF51A475ZA01B
				CONNECTORS		
8	1	J2	4 Pin Header	4 Pin Header	Major League Electronics	TSHS-148-S-06-A-GT
9	1	J1	ANTENNA	17cm 22 AWG magnet wire	Consolidated	
				INDUCTORS		
11	1	L3	30nH	30nH Inductor, 0603, ±5%	Coilcraft	0603CS-30NXJB
12	1	L5	24nH	24nH Inductor, 0603, ±5%	Coilcraft	0603CS-24NXJB
13	3	L6,L7,L9	ZCB-0603	Ferrite bead, >600 Ohm @ 100MHz	ACT	ZCB-0603
14	1	L8	UL	Ferrite bead, >600 Ohm @ 100MHz	ACT	ZCB-0603
				RESISTORS		
15	1	R4	100K		VISHAY	CRCW06031003F
16	2	R5, R6	UL			
				SEMICONDUCTORS		
17	1	U1	MICRF010BM	300-440MHz UHF Receiver	MICREL	MICRF010BM
18	1	Y1	13.4916MHz	10pF, no built-in capacitor	Abracon	ABI-13.4916MHz-10

PCB Layout Information

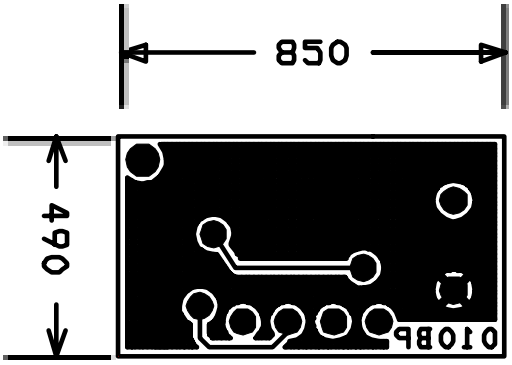
The MICRF010 evaluation board was designed and characterized using two sided 31 mils thick FR4 material with 1 ounce copper clad. If another type of printed circuit board material were to be substituted, impedance matching and characterization data stated in this document may not be valid. The gerber files for this board can be downloaded from the Micrel website at www.micrel.com.
All Units for PCB shown are in mils.



PCB Silk Screen

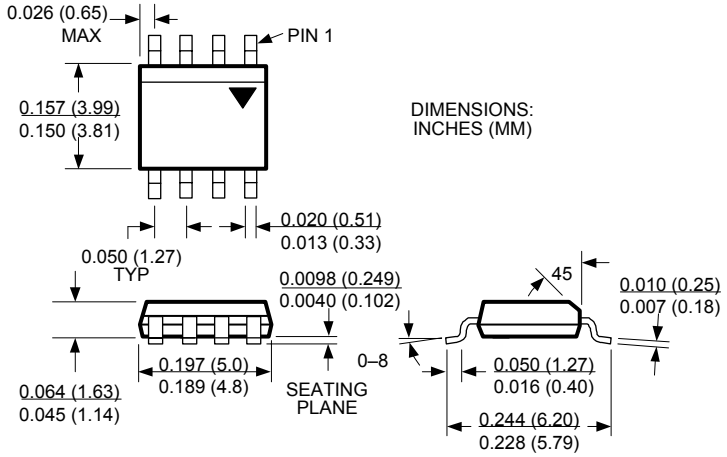


PCB Component Side Layout



PCB Solder Side Layout

Package Information



8-Lead SOIC (M)

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