MIC9130

High-Voltage, High-Speed Telecom DC-to-DC Controller

General Description

The MIC9130 is a current-mode PWM controller that efficiently converts –48V telecom voltages to logic levels. The MIC9130 features a high voltage start-up circuit that allows the device to be connected to input voltages as high as 180V. The high input voltage capability protects the MIC9130 from line transients that are common in telecom systems. The start-up circuitry also saves valuable board space and simplifies designs by integrating several external components.

The MIC9130 is capable of high speed operation. Typically the MIC9130 can control a sub-25ns pulse width on the gate out pin. Its internal oscillator can operate over 2.5MHz, with even higher frequencies available through synchronisation. The high speed operation of the MIC9130 is made safe by the very fast, 34ns response from current sense to output, minimizing power dissipation in a fault condition.

The MIC9130 allows for the designs of high efficiency power supplies. It can achieve efficiencies over 90% at high output currents. Its low 1.3mA quiescent current allows high efficiency even at light loads.

The MIC9130 has a maximum duty cycle of 50%. For designs requiring a high duty cycle, refer to the MIC9131. The MIC9130 is available in a 16-pin SOP and 16-pin QSOP package options. The rated junction temperature range is from –40°C to +125°C.

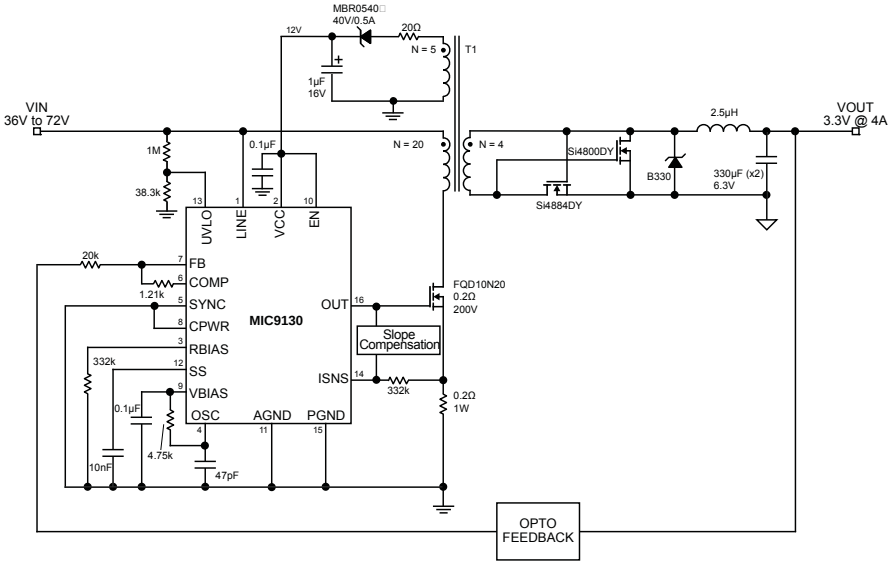
Features

- Input voltages up to 180V
- Internal oscillator capable of >2.5MHz operation
- Synchronisation capability to 4MHz
- Current sense delay of 34ns
- Minimum pulse width <25ns
- 90% efficiency
- 1.3mA quiescent current
- 1µA shutdown current
- Soft-start
- Resistor programmable current sense threshold
- Selectable soft-start retry
- 4Ω sink, 12Ω source output driver
- Programmable under-voltage lockout
- Constant-frequency PWM current-mode control
- 16-pin SOIC and 16-pin QSOP

Applications

- Telecom power supplies
- Line cards
- ISDN network terminators
- Micro- and pico-cell base stations
- Low power (< 30W) dc-dc converters

Typical Application

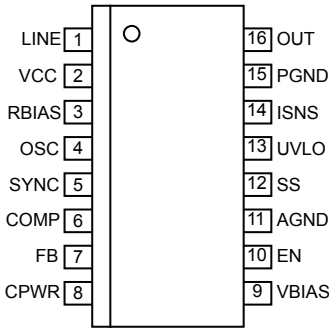


1.5MHz DSL Power Supply

Ordering Information

Part Number		Max. Duty Cycle	Junction Temp. Range	Package
Standard	Pb-Free			
MIC9130BM	MIC9130YM	50%	-40°C to +125°C	16-Pin SOP
MIC9130BQS	MIC9130YQS	50%	-40°C to +125°C	16-Pin QSOP

Pin Configuration



16-Pin SOP (M)

16-Pin QSOP (QS)

Pin Description

Pin Number	Pin Name	Pin Function
1	LINE	Line (Input): 180Vdc maximum supply input. May be floated if unused.
2	VCC	Supply (Input): MIC9130 internal supply input.
3	RBIAS	Bias Resistor (External Component): Connect 562KΩ to ground.
4	OSC	Oscillator RC Network (External Components): Connect external resistor-capacitor network to set oscillator frequency.
5	SYNC	Synchronization (Input): External oscillator input for slave operation of controller. See OSC. Do not float.
6	COMP	Compensation (External Components): Error amplifier output for external compensation network connection.
7	FB	Feedback (Input): Error amplifier inverting input.
8	CPWR	Current Limit Selection (Input): When CPWR is high, an over-current condition at the ISNS input will terminate the gate drive and reset the soft-start latch. If the CPWR pin is low, an over-current condition at the ISNS input will terminate the gate drive signal, but will not cause a reset of the soft-start circuit.
9	VBIAS	Reference (Output): Internal 5V supply. Will source 5mA maximum.
10	EN	Enable (Input): Logic level enable/shutdown input; logic high = enabled (on), logic low = shutdown (off).
11	AGND	Analog Ground (Return)
12	SS	Soft-Start (External Components): Connect external capacitor to slowly ramp up duty cycle during startup and over-current conditions.
13	UVLO	Undervoltage Lockout (External Components): Connect to unbiased resistive divider network to set controller's minimum operating voltage. Connect to VBIAS if not needed.
14	ISNS	Current Sense (Input): Connect between external switching MOSFET source and switch current sense resistor.
15	PGND	Power Ground (Return)
16	OUT	Switch Drive Output (Output): Connect to gate of external switching MOSFET.

Absolute Maximum Ratings (Note 1)

Line Input Voltage (V_{LINE}).....+190V
V_{CC} Input Voltage (V_{CC}).....+19V
Current Sense Input Voltage (V_{ISNS}).....–0.3 to +5.3V
Enable Voltage (V_{EN})..... –0.3 to V_{CC} + 0.3V
Feedback Input Voltage (V_{FB}) .....–0.3 to +5.3V
Sync Input Voltage (V_{SYNC}).....–0.3 to +5.3V
Soft-Start Voltage (V_{SS}).....–0.3 to +5.3V
UVLO Voltage (V_{UVLO}).....–0.3 to +5.3V
Storage Temperature (T_S) ..... –65°C to +150°C
Power Dissipation (P_D)
16-pin SOP .....400mW @ T_A = +85°C
16-pin QSOP .....245mW @ T_A = +85°C
ESD Rating, **Note 3**

Operating Ratings (Note 2)

Line Input Voltage (V_{LINE}).....V_{CC} to +180V, **Note 4**
V_{CC} Input Voltage (V_{CC})..... +9V to +18V
Junction Temperature Range (T_J) ..... –40°C to +125°C
Package Thermal Resistance
16-pin SOP (θ_{JA}) .....100°C/W
16-pin QSOP (θ_{JA}) .....163°C/W

Electrical Characteristics

T_A = 25°C, V_{LINE} = 48V, V_{CC} = 10V, R_t = 9.47KΩ, C_t = 470pF, R_{BIAS} = 562kΩ, V_{EN} = 10V, V_{ISNS} = 0V, V_{UVLO} = 2V, V_{SYNC} = 0V, unless otherwise noted. **Bold** values indicate –40 °C ≤T_J ≤ +125°C.

Parameter	Condition	Min	Typ	Max	Units
Bias Regulator					
Output Voltage	I_{VBIAS} = 0mA; V_{OSC} = 0V (Oscillator OFF)	4.7	4.85	5.0	V
		4.6		**5.1**	V
Line Regulation	9V ≤ V_{CC} ≤18V, I_{VBIAS} = 0mA; V_{OSC} = 0V		24	**40**	mV
Load Regulation	0mA ≤ I_{VBIAS} ≤ 5mA; V_{OSC} = 0V		5	**30**	mV
Oscillator Section					
Initial Accuracy (f_{OSC})	R_t = 9.47KΩ, C_t = 470pF	180	200	220	kHz
Oscillator Output Frequency			$f_{OSC/2}$		kHz
Maximum Duty Cycle			50		%
Voltage Stability (Δf/f)	9V ≤ V_{CC} ≤18V		2.5		%
Temperature Stability ppm/°C	–40°C ≤ T_J ≤ 125°C		100		
Maximum Sync Frequency	**Note 5**		4		MHz
Sync Threshold Level			2.5		V
Sync Hysteresis			0.7		V
Sync Minimum Pulse Width			50		ns
Error Amp Section					
FB Voltage	V_{COMP} = V_{FB}	2.475 **2.45**	2.5	2.525 **2.55**	V
Open Loop Voltage Gain, A_{VOL}			90		dB
Unity Gain Bandwidth			4		MHz
PSRR	9V ≤ V_{CC} ≤ 18V		60		dB
COMP Sink Current	V_{FB} = 2.7V; V_{COMP} = 5V	80	100		µA
COMP Source Current	V_{FB} = 2.3V; V_{COMP} = 0V	1	2.5		mA
V_{COMP} Low	V_{FB} = 2.7V; I_{COMP} = –50µA		115	300	mV
V_{COMP} High	V_{FB} = 2.3V; I_{COMP} = +500µA	3.5	4		V
Input Bias Current (I_{FB})	V_{FB} = V_{COMP}		160		nA
Slew Rate	SINK		1.5		V/µs
	SOURCE		1.5		V/µs

Parameter	Condition	Min	Typ	Max	Units
Preregulator					
Input Leakage Current	V_{LINE} = 180V, V_{CC} = 10V		0.1	**10**	µA
V_{CC} Gate Lockout ($V_{GLO(ON)}$)	V_{LINE} = 48V	7.2	7.5		V
V_{CC} Gate Lockout Hysteresis (ΔV_{GLO})	V_{LINE} = 48V	700	800		mV
V_{CC} Pre-Regulator Off ($V_{PR(OFF)}$)	V_{LINE} = 48V	7.7	$V_{GLO(ON)}$ +0.5V		V
V_{CC} Pre-Regulator Hysteresis (ΔV_{PR})	V_{LINE} = 48V	500	700		mV
Start-up Current	V_{LINE} = 48V, V_{CC} = 7.5V, **Note 4**	9	12		mA
Supply					
Supply Current, I_{VCC}	Pin 16 (OUT) = OPEN		1.3	1.5	mA
Enable Input Current	V_{EN} = 0V ,10V; V_{LINE} = 48V	**–10**	0.1	**10**	µA
Shutdown Supply Current	V_{EN} = 0V ; V_{CC} = 18V		0.1	**10**	µA
Protection and Control					
Current Limit Threshold Voltage		**0.772**	0.83	**0.888**	V
Current Limit Delay to Output	V_{ISNS} = 0V to 5V		34		ns
Current Limit Source Current	V_{ISNS} = 0V	30	40	50	µA
Enable Input Threshold (Turn-on)		1	1.6	2.2	V
Enable Input Hysteresis			150		mV
CPWR Input Current	V_{CPWR} = 5V, 0V	–1		+1	µA
CPWR Threshold			1.6		V
Soft-Start Current	V_{SS} = 0V	2.5	4	6	µA
Line UVLO Threshold (Turn-on)		1.16	1.22	1.28	V
Line UVLO Threshold Hysteresis			140		mV
Thermal Shutdown			145		°C
Thermal Shutdown Hysteresis			25		°C
MOSFET Driver					
Output Minimum On-Time	V_{ISNS} = 5V		21		ns
Output Driver Impedance	SOURCE ; I_{SOURCE} = 200mA		8	12	Ω
	SINK ; I_{SINK} = 200mA		4	6	Ω
Rise Time	C_{OUT} = 500pF		12		ns
Fall Time	C_{OUT} = 500pF		8		ns

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

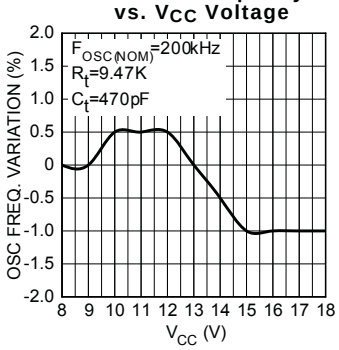
Note 3. Devices are ESD sensitive. Handling precautions recommended.

Note 4. If a substained DC voltage >150V is applied to the LINE pin, a current-limiting 1.8kΩresistor should be used in series with the LINE pin. This condition does not apply for transient conditions over 150V.

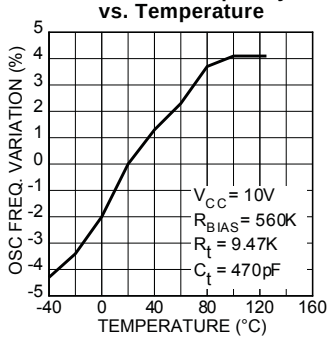
Note 5. For oscillator frequencies above 2.5MHz it may be necessary to power to VBIAS pin from an external power source due to the current limitations of the internal 5V regulator. See *Applications Information* for details

Typical Characteristics

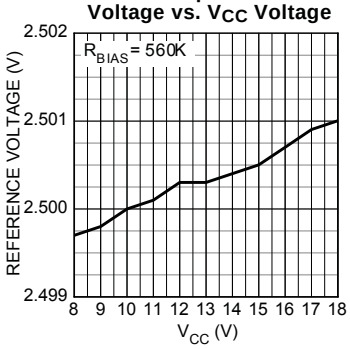
Oscillator Frequency vs. V_{CC} Voltage



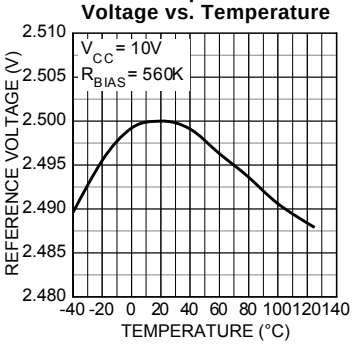
Oscillator Frequency vs. Temperature



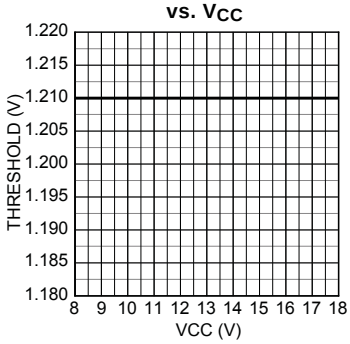
Error Amp Reference Voltage vs. V_{CC} Voltage



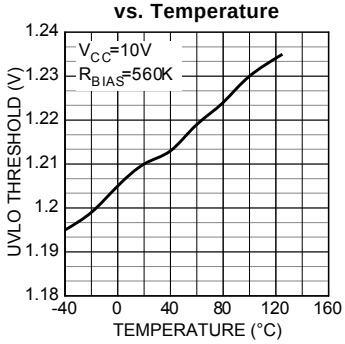
Error Amp Reference Voltage vs. Temperature



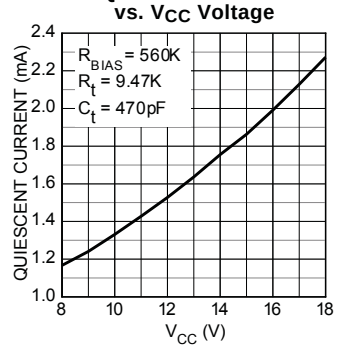
Line UVLO Threshold vs. V_{CC}



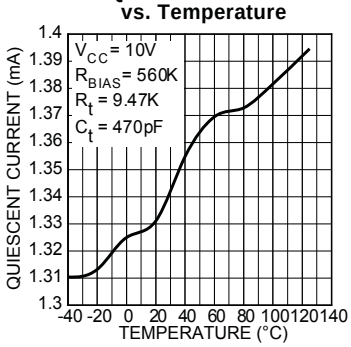
Line UVLO Threshold vs. Temperature



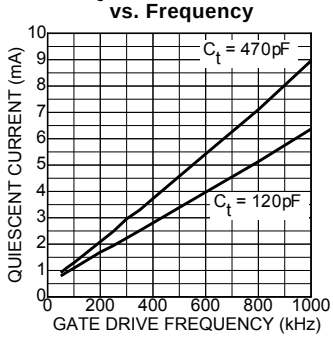
Quiescent Current vs. V_{CC} Voltage



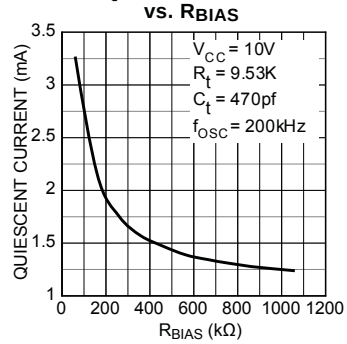
Quiescent Current vs. Temperature



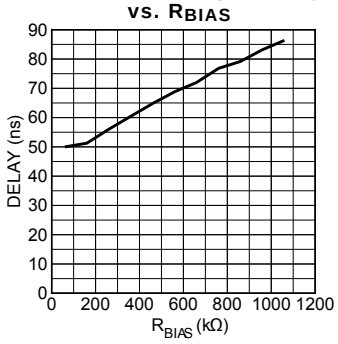
Quiescent Current vs. Frequency



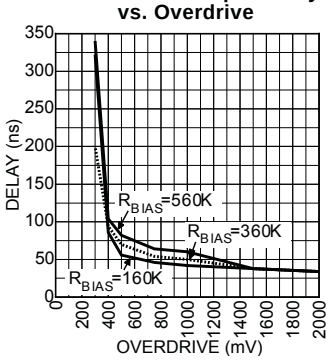
Quiescent Current vs. R_{BIAS}



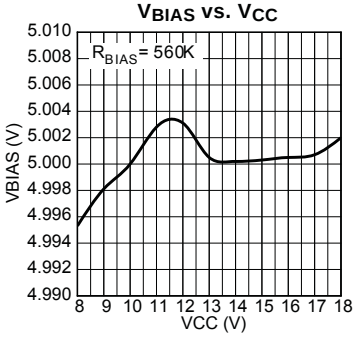
ISNS to Gate Output Delay vs. R_{BIAS}



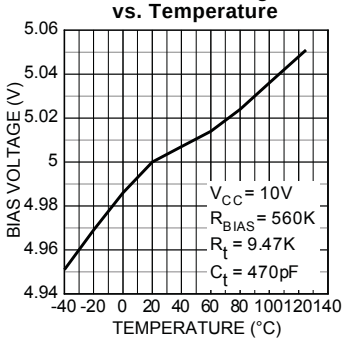
ISNS to Gate Output Delay vs. Overdrive



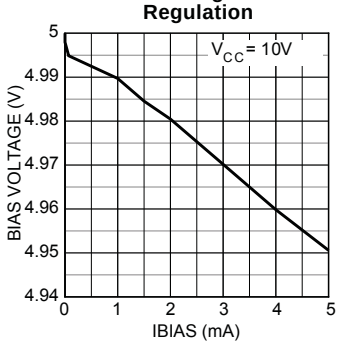
V_{BIAS} vs. V_{CC}



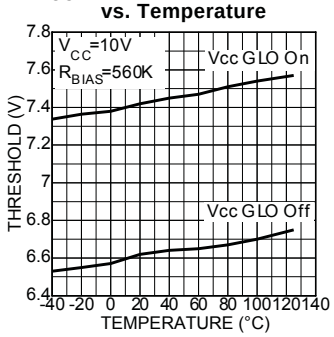
5V V_{BIAS} Voltage vs. Temperature



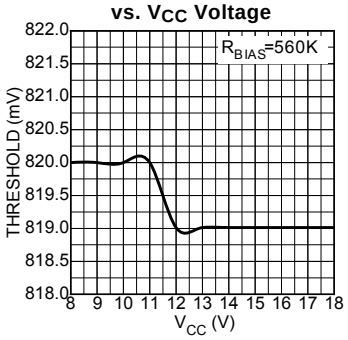
Bias Voltage Load Regulation



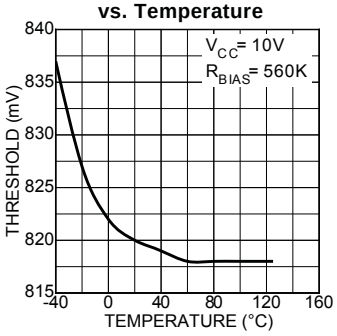
V_{CC} Turn On/Off Thresholds vs. Temperature



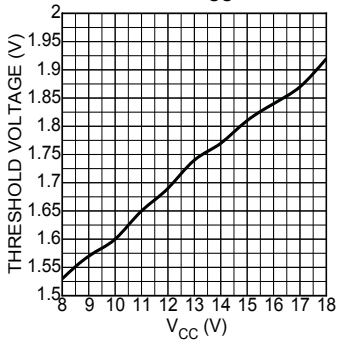
ISNS Current Limit Threshold vs. V_{CC} Voltage



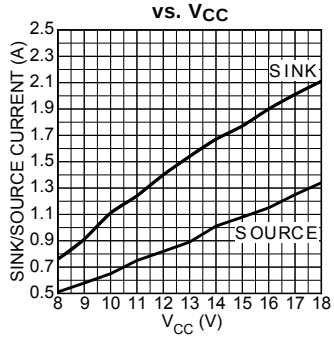
ISNS Current Limit Threshold vs. Temperature



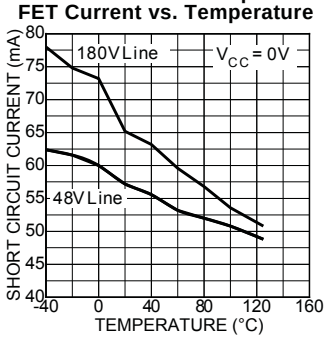
Enable Threshold vs. V_{CC}



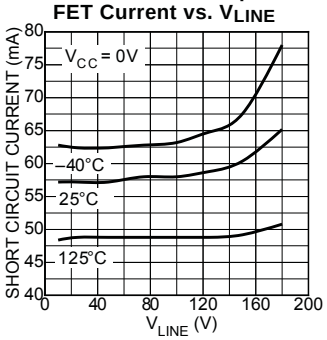
Gate Drive Current vs. V_{CC}



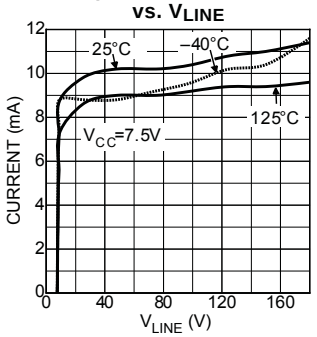
Peak Short Circuit Depletion FET Current vs. Temperature



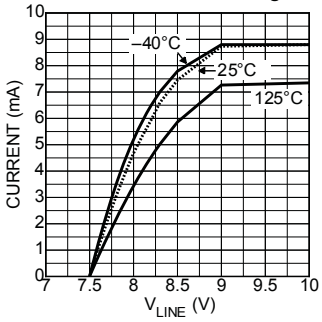
Peak Short Circuit Depletion FET Current vs. V_{LINE}



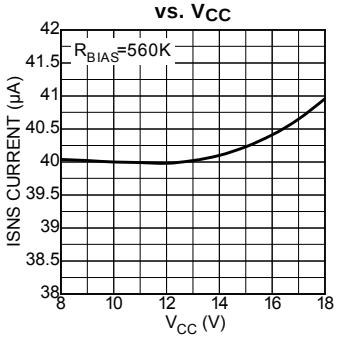
Depletion FET Current vs. V_{LINE}



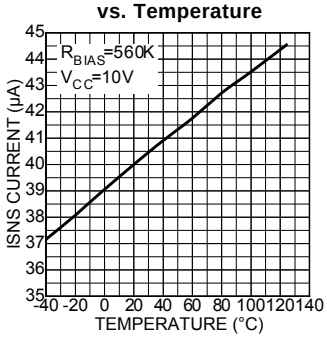
Depletion FET Current vs. Low V_{LINE} Voltage

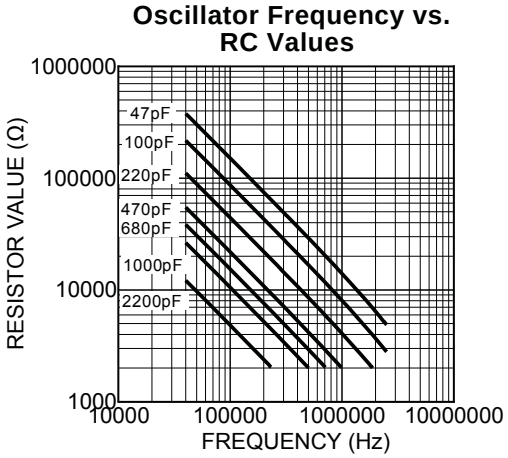


ISNS Pin Source Current vs. V_{CC}



ISNS Pin Source Current vs. Temperature





*See applications section for higher switching frequencies

Functional Block Diagram

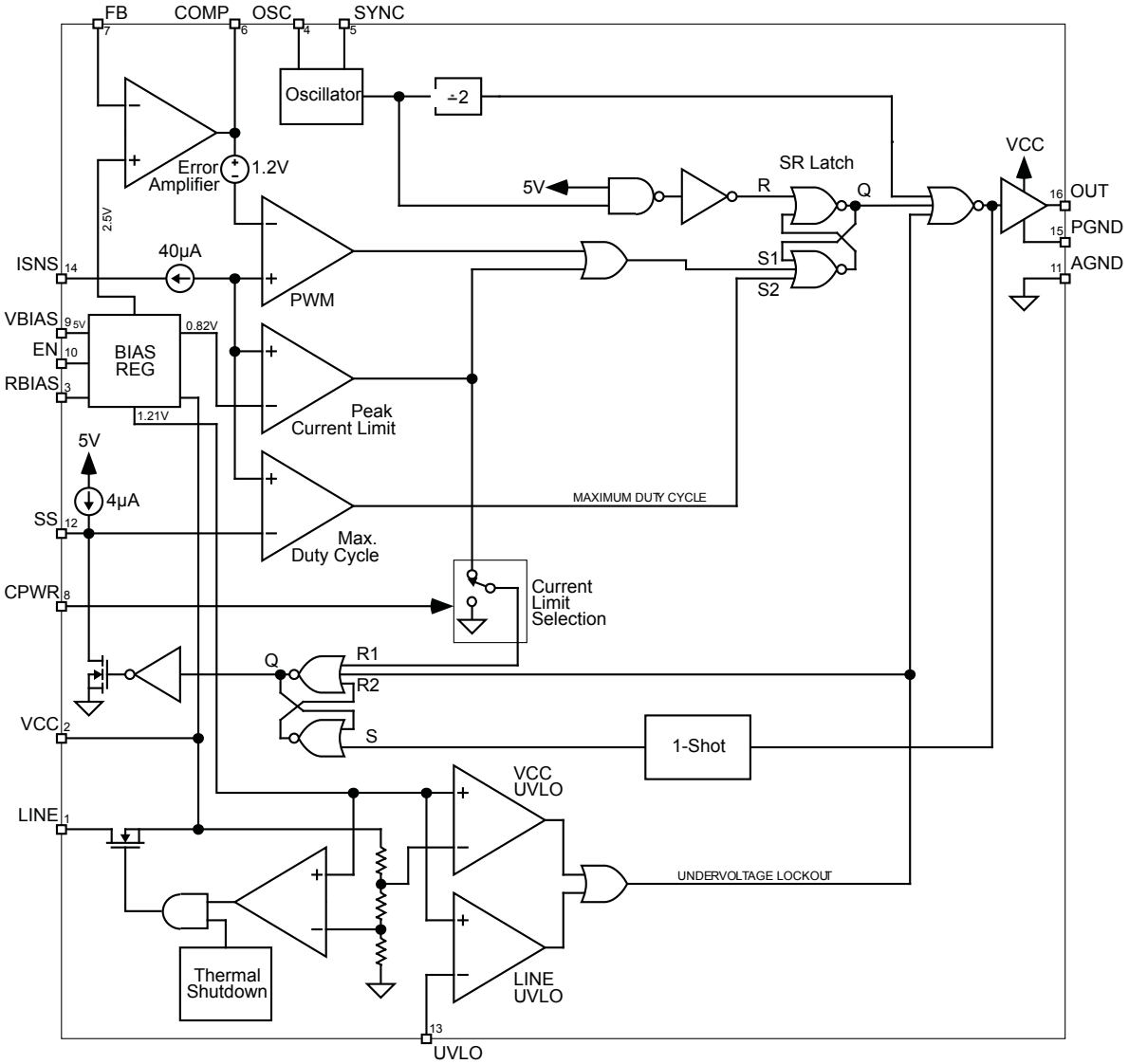


Figure 1

Functional Description

Micrel's MIC9130 is a high voltage, high speed current mode switching power supply controller. It uses a BiC/DMOS process to achieve a high voltage input, low quiescent current and very fast internal delay times. The MIC9130 is designed to drive an external low side N-channel MOSFET, which makes it suitable for controlling Boost, Flyback and Forward converter topologies. The high voltage startup pin eliminates the requirement for an external start up circuit. This makes it ideal for use with Telecom converters.

A block diagram of the MIC9130 is shown in Figure 1. The description of the controller is divided into 6 basic functions:

- Power and bias circuitry
  - High voltage start-up circuit
  - V_{CC} and bias supplies
- Enable and undervoltage monitoring circuits
  - V_{CC} and V_{IN} UVLO
  - Enable
- Oscillator and sync circuitry
- Soft-start and soft-start reset circuits
- MOSFET gate drive circuits
- Control loop operation
  - Current sensing & overcurrent protection
  - Slope compensation
  - Error amplifier

High Voltage Start Up Circuit

Many conventional Off-Line and Telecom power supplies use an external bias resistor and zener diode to supply the initial start-up voltage for the control IC. The control IC gets its supply voltage from a bias winding once the power supply is running. This method has the disadvantages of extra components (diode and power resistor), continuous power dissipation in the resistor and a large bias capacitor, used to supply the IC until the bias winding takes over.

The MIC9130 eliminates these problems by using an internal depletion mode MOSFET as a pre-regulator to provide the start-up bias voltage from the high voltage input of the power supply. This approach eliminates the need for external start up components and reduces the size of the controller's bias supply capacitor. The MOSFET is turned off once the external bias winding takes over, which eliminates power dissipation in the start-up circuit. In some cases, the MIC9130 may be run directly from the input voltage rail, eliminating the need for an external bias winding.

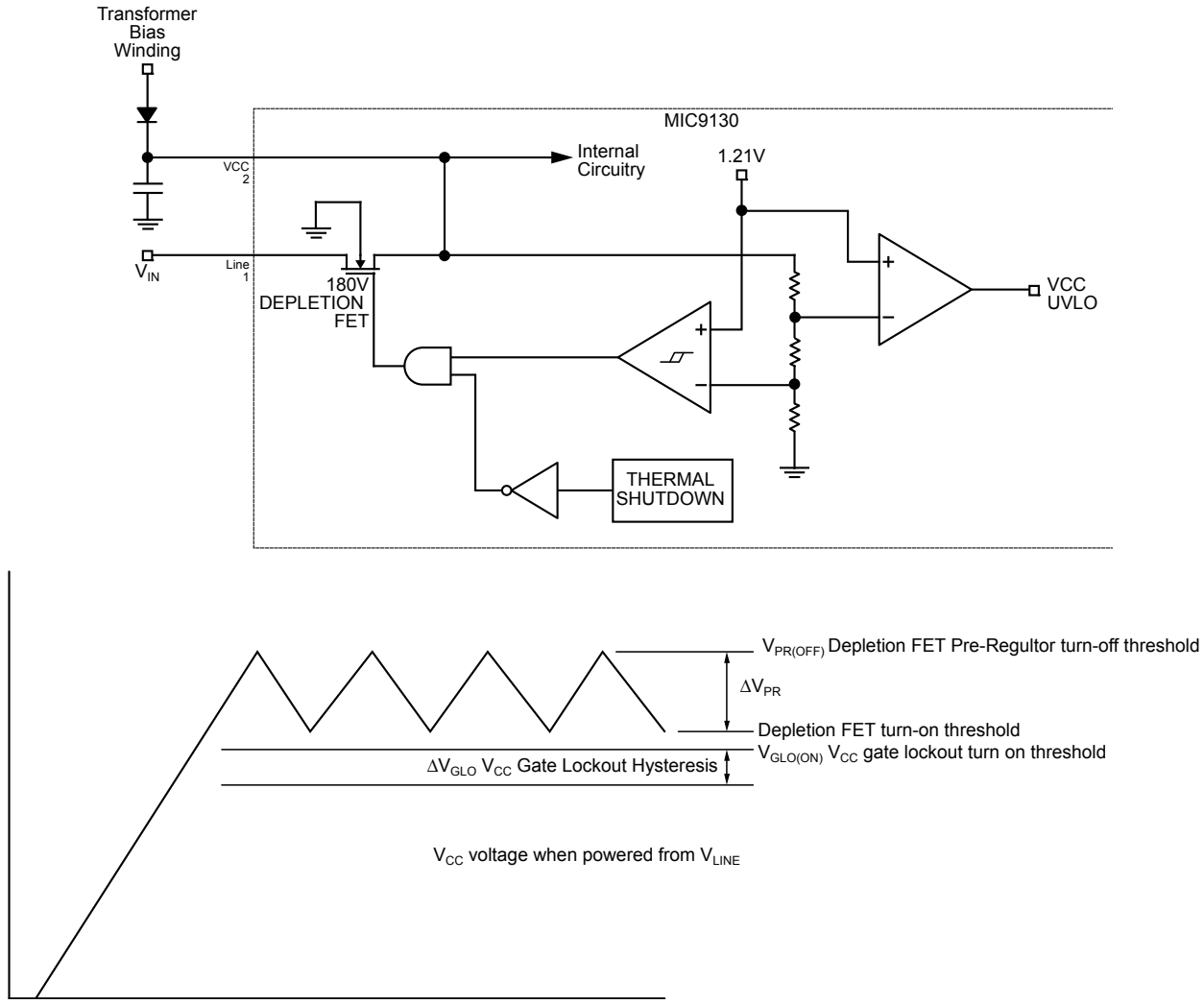


Figure 2

Start-up circuit operation is illustrated in Figure 2. V_{IN} is applied and the depletion FET, which is normally enabled allows current from V_{IN} to charge the V_{CC} bias capacitor. Once the V_{CC} voltage reaches the V_{CC} enable threshold, $V_{GLO}(ON)$, the gate drive is enabled and the MIC9130 starts switching. V_{CC} continues to increase until the Pre-Regulator turn-off threshold, ($V_{PR}(OFF)$), is reached and the depletion FET is turned off. The V_{CC} voltage decreases as energy from the bias capacitor is used to supply the controller. The depletion FET is turned back on when the pre-regulator turn-on threshold is reached. A bias winding derived supply voltage, set higher than the FET turn-off threshold, $V_{PR}(OFF)$, raises the V_{CC} voltage over the threshold and prevents the FET from turning on.

In certain designs the MIC9130 may be powered directly from the Line voltage, eliminating the need for an extra transformer bias winding. When operating in this fashion the designer must insure the power dissipation in the IC does not cause the die temperature to exceed the 125°C maximum. Power dissipation is calculated by:

$$P_{DISS} = (V_{IN} - V_{CC}) \times I_{VCC}$$

Where :

V_{IN} is the line input voltage

V_{CC} is the average V_{CC} voltage (typically 8.5V)

I_{VCC} is the total current drawn by the IC

I_{VCC} is the sum of the operating current of the MIC9130 at a given frequency and the average current required to drive the external switching MOSFET. A plot of typical operating current vs. frequency is given in Figure 3. The average MOSFET gate drive current is calculated in the “MOSFET GATE DRIVE” section of this specification.

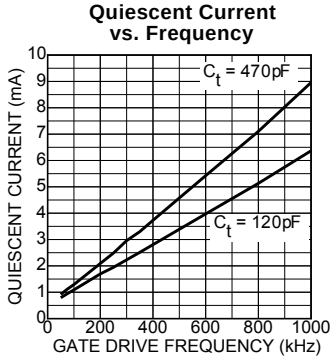


Figure 3

The die junction temperature is calculated by

$$T_J = T_A + P_{DISS} \times \theta_{JA}$$

Where: T_J is the die junction temperature

T_A is the ambient temperature of the circuit

θ_{JA} is the junction to ambient thermal resistance of the MIC9130 (listed in the operating ratings section of the specification.

When powered directly from the Line voltage, the V_{CC} voltage will vary between the upper and lower pre-regulator thresholds. The amplitude of the output gate drive voltage will vary with the V_{CC} voltage. This should not be a problem for most topologies since the variation is small (equal to the ΔV_{PR} hysteresis). The bias regulator in the MIC9130 buffers the internal circuits from V_{CC} variations.

The pre-regulator FET is protected by a thermal shutdown circuit, which turns the MOSFET off if its temperature exceeds approximately 150 degrees C.

When operating at input voltages greater than 150V, a fast input voltage risetime during turn-on (which may occur during a hot plug operation) may cause a high peak current to flow through the depletion FET, damaging the MIC9130. A 1.8kΩ resistor in series between the input voltage and the line pin (pin 1) is recommended when operating at input voltages greater than 150V. This resistor limits the maximum peak current to 100mA (at 180V_{IN}) and protects the part.

The depletion mode MOSFET contains an internal parasitic diode. The V_{IN} pin voltage must be greater than the V_{CC} voltage or the V_{CC} voltage will be clamped to a diode drop greater than the V_{IN} voltage. Excessive power dissipation in the parasitic diode will destroy the IC.

V_{CC} and Bias Supplies

The power for the controller and gate drive circuitry is supplied through the V_{CC} pin. The gate drive current is returned to ground through the power ground pin (PGND). The rest of the supply current is returned to ground through the analog ground pin (AGND). The two ground pins must be connected together through the PCB ground plane.

High frequency decoupling is provided at the V_{CC} pin to supply the gate drive’s peak current requirements. Turn-on of the external MOSFET causes a voltage glitch on the V_{CC} pin. If the glitch is excessive, this disruption can appear as noise or jitter in the oscillator circuit or the gate drive waveform. The decoupling capacitor must be able to supply the MOSFET gate with the charge required to turn it on. A 0.1µF ceramic capacitor is usually sufficient for most MOSFETs. Larger FETs, with a higher gate charge requirement may require a 0.22µF ceramic capacitor or a ceramic capacitor paralleled with a 2.2µF tantalum or 4.7uF aluminum electrolytic. It is recommend that if V_{LINE} is greater than 150V DC than the maximum capacitor recommended on V_{CC} is 2.2µF.The capacitor must be located next to the V_{CC} pin of the MIC9130. The ground end of the capacitor should be connected to the ground plane, making a low impedance connection to the power ground pin (pin 15).

The internal bias regulator block provides several internal and external bias voltages. Referring to Figure 1, a 2.5V reference is used for the internal error amplifier, a 0.82V bias is used by the current limit comparator and a 1.21V reference is used by the Line UVLO circuit. An external 5V bias voltage (V_{BIAS}) powers the oscillator circuit and may be used as a reference voltage for other external components. The V_{BIAS} pin requires a minimum 0.1µf capacitor to ground for decoupling.

Enable and Undervoltage Monitoring circuits

The two undervoltage lockout circuits in the MIC9130 are shown in Figure 4. One monitors the V_{CC} voltage and the other monitors the input line voltage. These signals are OR’d together and either one can disable the gate drive pin and discharge the voltage on the soft start capacitor.

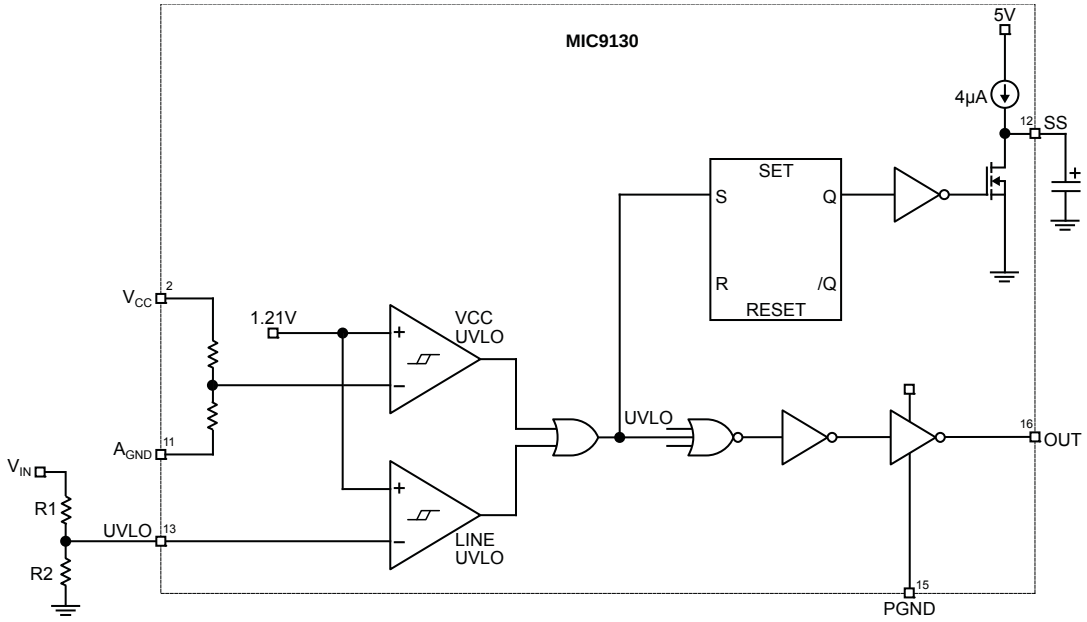


Figure 4: UVLO and Soft Start Circuits

V_{CC} Undervoltage Lockout

The V_{CC} voltage is internally divided down and compared to a 1.21V internal bandgap reference. As V_{CC} rises above the turn-on threshold, it disables the Vcc undervoltage lockout circuit. Once above the turn-on threshold, hysteresis prevents the lockout circuit from disabling the IC until the V_{CC} voltage falls below the lower threshold.

Line Undervoltage Circuit (UVLO)

The line voltage is monitored by an external resistor divider and fed into the negative input of the line UVLO comparator. As the comparator trip point is exceeded, the line UVLO circuit is disabled. Hysteresis built into the comparator prevents the circuit from toggling on an off in the presence of noise or a high input line impedance.

The line voltage turn-on trip point is:

$$V_{LINE_ON} = V_{THRESHOLD} \times \frac{R1+R2}{R2}$$

where: $V_{THRESHOLD}$ is the voltage level of the internal comparator reference, typically 1.21V.

The line hysteresis is equal to:

$$V_{HYSTERESIS} = V_{HYST} \times \frac{R1+R2}{R2}$$

where: V_{HYST} is the internal hysteresis level, typically 75mV.

$V_{HYSTERESIS}$ is the hysteresis of the line input voltage

The MIC9130 will be disabled when the line voltage drops back down to:

$$V_{LINE_OFF} = V_{LINE_ON} - V_{HYTERESIS} =$$

$$\left(V_{THRESHOLD} - V_{HYST}\right) \times \frac{R1+R2}{R2}$$

Enable

A low level on the enable pin turns off all the functions of the MIC9130 and places it in a low quiescent current state. The output driver is in a low state. When the enable pin is pulled high, the MIC9130 goes through its normal start up sequence including undervoltage lock out and soft start. When not used, the pin should be connected to V_{CC}.

Oscillator Block

An external resistor and capacitor set the oscillator frequency. The MIC9130 contains an internal divide-by-two circuit that limits the maximum duty cycle at the gate drive to 50%. The oscillator frequency for the MIC9130 is twice the output switching frequency.

Oscillator Pin

The operation of the oscillator is shown in Figure 5. The voltage waveform at the OSC pin is a sawtooth whose amplitude increases as capacitor Cosc is charged up through R_{OSC} from the 5V bias. When the OSC pin voltage reaches the internal comparator upper threshold, C_{OSC} is quickly discharged to zero volts by an internal MOSFET. After a brief delay, typically 75ns, the internal MOSFET is turned off and the C_{OSC} charges, repeating the cycle. Figure 5 show the relationship between the oscillator and gate drive waveforms. The delays in the IC force the duty cycle of the gate drive signal to be slightly less than 50% duty cycle (typically 48%).

For V_{BIAS} = 5V and a peak oscillator waveform voltage of 3V, the design equations simplify to:

Charging

$$t_{CHARGE} = 0.92 \times R_t \times C_t$$

Discharging

$$t_{DISCHARGE} \approx 40 \times C_t$$

$$T_{P_OSCILLATOR} = t_{CHARGE} + t_{DISCHARGE} + t_{DELAY}$$

Where $t_{DELAY} = 75ns$

$$f_{S_OSCILLATOR} = \frac{1}{T_{P_OSCILLATOR}}$$

$$f_{S_OUTPU} = \frac{1}{4} \times f_{S_OSCILLATOR}$$

The timing capacitor, C_{OSC}, should be an NPO ceramic or a temperature stable film capacitor. Care must be taken when using capacitor values less than 47pF. The high impedance of a small value capacitor makes the OSC pin more susceptible to switching noise. Also, the input capacitance of the OSC pin and the stray capacitance of the board will have a noticeable effect on the oscillator frequency.

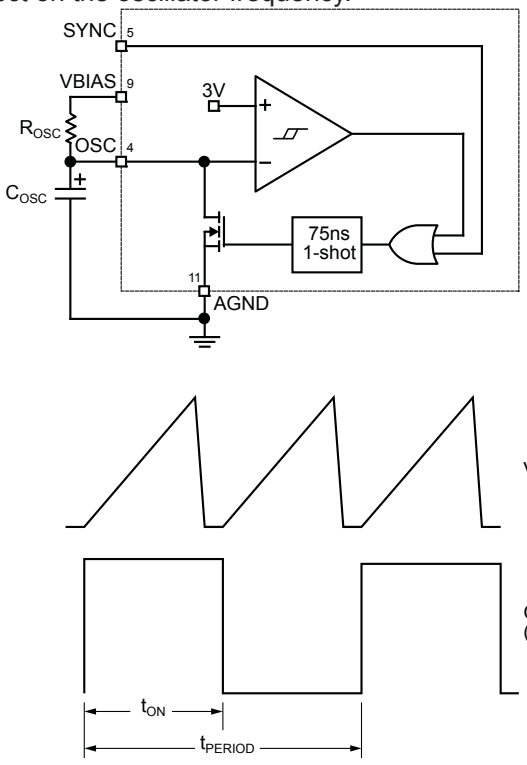


Figure 5a

Higher Switching Frequencies

The MIC9130 is capable of very high switching frequencies. One of the limitations on the maximum frequency is the current capability of the 5V regulator supplying the oscillator and V_{BIAS}. By powering V_{BIAS} with an external source, e.g. linear regulator much higher switching frequencies can be achieved. A simple way of using an external current source is to set an NPN as an emitter follower. Figure 5b shows the MIC9130 oscillator frequency set to 4MHz using an external NPN. The emitter followerj circuit allows the current to be supplied by V_{CC} while the voltage is regulated to a diode drop below V_{BIAS}. This configuration is quite stable over temperature and voltage variations.

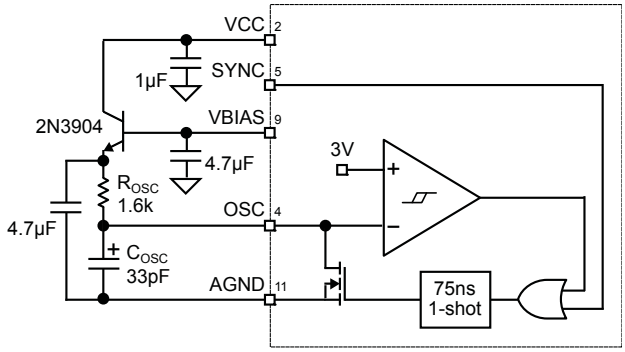


Figure 5b

Oscillator Synchronization

The switching frequency of the MIC9130 can be synchronized to an external oscillator or frequency source. Figure 6 shows the relationship between the sync input, oscillator waveform and gate drive output. The external frequency should be set at least 15% greater than the free running oscillator frequency to account for tolerances in the oscillator circuit and external components. The positive edge of the sync signal resets the oscillator. The sync pulse frequency, like the oscillator, is twice the gate drive frequency. When an external sync signal is applied, the peak amplitude of the oscillator signal (pin 4) is less than when it is free running because the oscillator signal is terminated before it reaches its 3V (typical) amplitude. When not used, the sync pin should be connected to ground to prevent noise from erroneously resetting the oscillator.

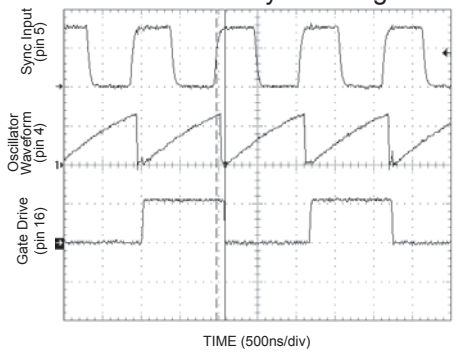


Figure 6. Sync Waveform

Soft Start Circuit

The soft start is programmed by a capacitor on the soft start pin. A 4µA current source charges up the capacitor. At power up, the SS pin is discharged. Once the UVLO and enable functions release the soft start circuit, the voltage of the capacitor increases. The active voltage range of the soft start pin is from typically from 0.9V to 1.7V. The internal current source increases the voltage on the soft start capacitor to approximately 4V. The soft start pin and the current sense voltage are connected to a comparator in tç

PMIC9130. The voltage from the soft start pin effectively limits the peak current through the current sense resistor by prematurely terminating the on-time of the gate drive output. Referring to Figure 1, with the soft start voltage low, the duty cycle of the output is at a minimum. As the soft start voltage increases, the duty cycle of the gate drive output increases

until the error amplifier takes control of the duty cycle. The soft start capacitor is discharged by an internal MOSFET in the MIC9130.

The soft start circuit is activated by the following events:

1. Line undervoltage pin less than the 1.21V threshold
2. V_{CC} becomes less than the pre-regulator voltage turn .....off threshold.
3. The current limit comparator threshold is exceeded. This can be disabled with a low level on the CPWR pin.
4. A low level on the enable pin.

Calculating the soft capacitor depends on many parameters such as the current limit of the circuit input voltage, output power and output loading. A starting value of capacitor should be chosen and the value can be adjusted later in the design. Recommended starting values of soft start capacitance is typically 10nF to 100nF. Values below 1nF may be ineffective in slowing the output voltage turn on time.

CPWR Current Limit Selection

This pin controls whether the soft start circuit is reset if the voltage on the Isns pin exceeds the overcurrent threshold. When the CPWR pin is high, an overcurrent condition at the ISNS pin will terminate the on-time of the gate drive pulse and discharge the soft start capacitor to zero volts. This delay in start up contributes to a reduction in the average output current during an overcurrent or short circuit condition. A smaller MOSFET may be used since the power dissipation in the MOSFET is minimized under short circuit or overcurrent conditions.

If the CPWR pin is low an overcurrent or short circuit conditions will not trip the soft start circuit. The pulse-by-pulse current limit, inherent in current mode control, provides a “brick wall” or constant current limit. With the power supply operating in this mode, a smaller soft start capacitor can be used to increase the turn on speed of the supply.

If the CPWR in is held low during the initial turn on at power up and then raised high, the power supply can maximize the turn-on time at start up and still provide a high level of overcurrent and short circuit protection. The circuit shown in Figure 7 performs this function.

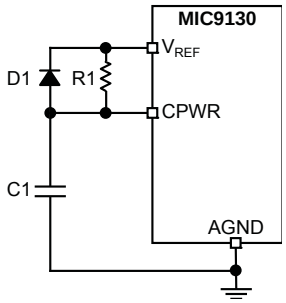


Figure 7

MOSFET Gate Drive Output

The MIC9130 has the capability to directly drive the gate of a MOSFET. The output driver consists of a complimentary P-channel and N-channel pair. The typical switching time of the output is dependent on the IC supply voltage and the gate charge required to turn the MOSFET on and off.

A resistor placed in series with the gate drive output attenuates ringing in the etch connection between the MIC9130 and the MOSFET. Figure 8 shows a single resistor in series between the driver output and the gate of the MOSFET. The zener value should be greater than the gate drive voltage to prevent excessive power dissipation, but less than the maximum gate to source voltage rating.

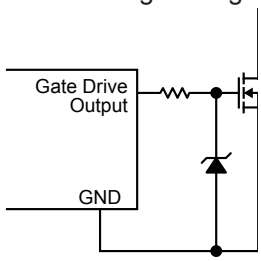


Figure 8

The circuitry shown in figure 9 allow different rise and fall times. R1 and the input capacitance of the MOSFET determine the rise-time of the gate voltage and therefore the turn-on time of the MOSFET. The diode, D1 is reversed biased, which removes R2 from the circuit. At turn-off, D1 is forward biased and the parallel combination of R1 and R2 controls the turn-off time of the MOSFET. The turn on-time is slower, which reduces switching noise and ringing during turn-on. The turn-off time is faster, which minimizes switching losses during turn-off and improves efficiency. If the turn-on time is to be faster than the turn-off time, the diode should be reversed.

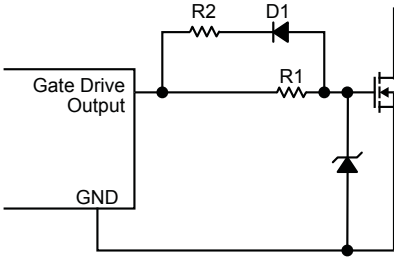


Figure 9

A gate drive transformer is used where an increase in drive voltage, isolation and/or voltage level shifting are required. Gate drive transformers can have multiple windings and drive multiple MOSFETs, including MOSFETs that require a drive signal 180 degrees out of phase with the ICs drive signal.

Figure 10 shows a gate drive transformer circuit. The capacitor, C1 removes DC from the drive circuit and prevents transformer saturation. R1 provides damping to eliminate ringing in the circuit. R1 is usually in the 5 to 20Ω range, depending on the amount of damping necessary. D1 and D2 form a clamp circuit, which prevents the voltage from exceeding the V_{GMAX} level. If the gate drive is well damped, the diodes may be removed R2 is used to allow the transformer to reset properly.

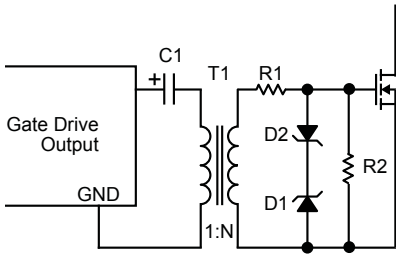


Figure 10

The gate impedance of a MOSFET is capacitive and the power required to drive the gate is proportional to the charge required to turn on the MOSFET, the peak gate voltage and the switching frequency. Assuming the total gate charge for turn on and turn off is equal, the power used to switch the MOSFET on and off is:

$$P_{DRIVE} = Q_G \times V_{GS} \times f_S$$

where: Q_G is the total gate charge at V_{GS}

V_{GS} is the gate to source voltage of the MOSFET usually equal to V_{CC}

f_S is the output switching frequency

The power required to drive the MOSFET is dissipated in the drive circuitry of the MIC9130. This power must not cause the die temperature to exceed the maximum rated junction temperature of 125 degrees C.

MOSFET Driver IC's are used when the drive requirement for the MOSFETs is greater than the capability of the MIC9130 gate drive output. While the peak current of the MIC9130 gate drive is typically 1.2A at V_{IN} =12V, a gate driver ICs will sink or source between 1.2A and 12A of peak current. The higher peak current allows faster rise and fall times for larger MOSFETs.

The drive requirements for selecting a MOSFET driver are determined using the following equation:

$$I_{PK} = 2 \times \frac{Q_G}{t}$$

where: Q_G is the total gate charge required to turn on the MOSFET at a specified I_D, V_G and V_{DS}. This information is usually given in the MOSFET specification sheet.

t is the gate voltage transition time (risetime or fall time)

I_{PK} is the peak current requirement of the MOSFET driver IC.

For example, if a MOSFET is chosen with a Q_G of 60nC and it is desired to have a 50nS gate to source risetime/falltime, the peak current requirement of the MOSFET driver is:

$$I_{PK} = \frac{2 \times 60nC}{50ns} = 2.4A$$

A driver such as the MIC4424 will meet this requirement. For more information on choosing a MOSFET driver, see the Micrel application note AN-24, "*Designing with Low Side MOSFET Drivers*."

Current Sense Circuit

The current sense input of the MIC9130 has three unique features, which are advantageous in a high speed, high efficiency power supply.

1. The overcurrent threshold is nominally 0.82V instead of the typical 1.0V found in most switching control ICs.
2. The current sense pin sources a nominal 40µA of current out of the pin. This is used to raise the current limit threshold of the pin, which allows a smaller current sense resistor to be used. This improves the efficiency of the power supply, especially in lower current applications.
3. The delay from the current sense input to the output is typically 50ns.

The current limit threshold of the ISNS pin was set at 0.82V, allowing the use of a smaller current sense resistor. A stable, bandgap derived 40µA current is sourced from the ISNS pin. A voltage drop across a series resistor placed between the pin and the current sense resistor level increases the current sense signal at the ISNS pin. This allows the use of a smaller current sense resistor if the full 0.82V peak to peak current signal is not required. Decreasing the value of the current sense resistor decreases the power dissipation in the resistor, which improves the efficiency of the power supply.

The delay between the input of the overcurrent comparator and the output gate drive is nominally 50ns. This very fast response time allows the MIC9130 to operate at higher frequencies and still have adequate overcurrent protection.

The operation of the current sense input is as follows. The sensed current in the power supply is converted to a voltage by a resistor or current sense transformer. Referring to Figure 1, this voltage is compared to the output of the error amplifier, which sets the duty cycle of the gate drive output. The current signal is also connected to an Imax comparator. Comparing the current sense signal to the reference voltage sets a maximum current limit. If the maximum amplitude of the current sense signal exceeds the reference, the comparator terminates the gate drive output pulse. It aslo discharges the soft start capacitor when the CPWR pin is high.

Leading Edge Current Spike

The current signal in a power circuit will often have a leading edge spike caused by leakage inductance, parasitic inductance and capacitance, diode reverse recovery effects and snubbers. These spikes can cause premature termination of the switching cycle if they are not eliminated.

A resistor may be added in series between the current sense resistor and the Isns input. The input and board trace capacitance of the ISNS pin (pin 14) is approximately 25pF. A 1k resistor is a good choice, since it attenuates most of the ripple without distorting the current sense waveform. It has a minimal effect on level, offsetting the current sense signal by only 40mV.

A typical rule of thumb is the bandwidth of the RC filter should be at least 6 times the switching frequency. This avoids distorting the current sense waveform and adding excessive delays in the current loop that will interfering with overcurrent protection. For a 100kHz switcher, the maximum

series resistance is 10K, for a 500kHz switcher, the maximum series resistance is 2K.

Sensing Current with a Resistor

The fast transition times of the current signal prohibit the use of inductive resistors. Standard wire wound power resistors will not work. Carbon composition or metal film resistors or low inductance power resistors may be used. The overcurrent range of the power supply and component tolerances must be considered when selecting the current sense resistor value. The power supply specification may call for an overcurrent limit, which must be accounted for when selecting the current sense resistor value. The relationship between the peak primary current and the current sense resistor is:

$$V_{ISNS} = I_P \times R_{ISENSE} + I_{ISNS} \times R_f$$

where: Ip is the current in the sense resistor

R_{ISENSE} is the current sense resistance

I_{ISNS} is the current sourced from the ISNS pin (40µA)

R_f is the series resistor between the ISNS pin and the current sense resistor.

The current sense resistor must not be too small or the current sense signal will be susceptible to noise. If noise is a problem, the current signal level should be increased.

An example is illustrated below.

The maximum peak current, I_{PMAX}= 1A at 120% overcurrent and minimum input voltage

The maximum rms current, I_{RMS}=0.65A

The desired current sense signal amplitude is 500mV at 1A output current.

The current sense resistor value and power dissipation is:

$$R_{SENSE} = \frac{V_{SENSE}}{I_{SENSE}} = \frac{0.5}{1} = 0.5\,\Omega$$

$$P_{DISS} = I_{RMS}^2 \times R_{SENSE} = 0.65^2 \times 0.5 = 0.21W$$

A 0.5Ω, non inductive resistor with at least a 1/2W rating should be selected.

The series resistor is calculated to allow the 500mV-peak signal to reach 0.82V.

$$R_f \frac{V_{ISNS} - \left(I_P \times R_{ISENSE}\right)}{I_{ISNS}} = \frac{0.82 - \left(1 \times 0.5\right)}{40\mu A} = 10.25k\Omega$$

The next lower value of 10kΩ is selected.

The bandwidth of the 10K resistor and the 25pF input capacitance is calculated. The resistor value must be lowered if the bandwidth is too low for the switching frequency.

$$BW = \frac{1}{2 \times \pi \times 10k \times 25pF} = 630kHz$$

The maximum switching frequency of this power supply should be approximately six times less than the BW to prevent current waveform distortion and excessive delays in the current loop. This limits the switching frequency to the range of 100kHz.

Sensing Current with a Current Sense Transformer

At higher power levels, the power dissipation in a current sense resistor is excessive. A current sense transformer can be used to sense the current while minimizing power dissipation. See Figure 11. The schematic shows the circuitry necessary when using a current sense transformer. The resistor, R1, provides a path to reset the current sense transformer. The resistor, R2, converts the scaled down current to a voltage, which is sent to the ISNS pin.

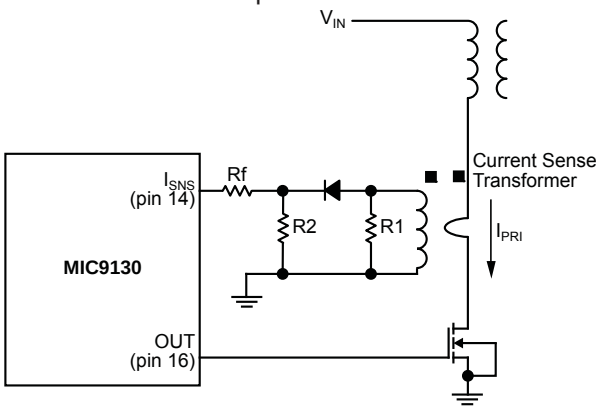


Figure 11

The voltage at the ISNS pin is calculated by:

$$V_{ISNS} = \frac{I_P}{N} \times R2 + I_{ISNS} \times R_f$$

where: I_P is the current in the primary of the current sense transformer

R2 is the current sense resistance at the secondary of the current sense transformer

N is the turns ratio of the current sense transformer (N=Nsec/Npri)

I_{ISNS} is the current sourced from the ISNS pin (40µA)

R_f is the series resistor between the ISNS pin and the current sense resistor.

Current Transformer example:

The maximum peak current, I_{PMAX} = 5A at 120% overcurrent and minimum input voltage

The maximum rms current, I_{RMS} = 3.25A

The full 0.82V peak signal a the ISNS input can be used since very little power is dissipation in the secondary side sense resistor. The maximum peak to peak voltage at the sense pin (pin 14) is 0.82V at the 5A maximum output current.

The current sense resistor value and power dissipation is:

$$R2 = \frac{V_{SENSE} \times N}{I_P} = \frac{0.82 \times 100}{5} = 16.4\,\Omega$$

$$P_{DISS} = \left(\frac{I_{PRMS}}{N}\right)^2 \times R2 = \left(\frac{3.25}{100}\right)^2 \times 16.4 = 17.4\,mW$$

A 16.2 ohm, 1%, non inductive resistor with at least a 50mW rating should be selected. A good choice would be an 0805 size metal film or a 1/8 watt leaded metal film resistor. A series resistor between the current sense transformer and the Isns input is not necessary unless it is used for low pass filtering.

If the current sense transformer were not used, the sense resistor would dissipate 1.7 watts.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{SENSE}} = \frac{0.82}{5} = 0.164\Omega$$

$$P_{DISS} = I_{RMS}^2 \times R_{SENSE} = 3.25^2 \times 0.164 = 1.7\,W$$

Slope Compensation

Power supplies using peak current mode control techniques require slope compensation when they are operating in continuous mode and have a duty cycle greater than 50%. Without slope compensation, the duty cycle of the power supply will alternate wide and narrow pulses commonly referred to as subharmonic oscillations. Even though the MIC9130 operates below a 50% duty cycle, slope compensation adds the benefits of improved transient response and greater noise immunity in the current sense loop (especially when the current ramp is shallow). Slope compensation can be implemented by adding an optimum 1/2 of the inductor current downslope, reflected back to the current sense input. In real world applications, 2/3 of the inductor current downslope is used to allow for component tolerances.

Slope compensation at the ISNS input may be implemented by using a resistor and capacitor as shown in Figure 12. The rectangular waveshape of the gate drive output is integrated by the resistor/capacitor filter, which results in a ramp used for the slope compensation signal. When the gate drive and the current signal at the sense resistor goes low, the capacitor is discharged to 0V.

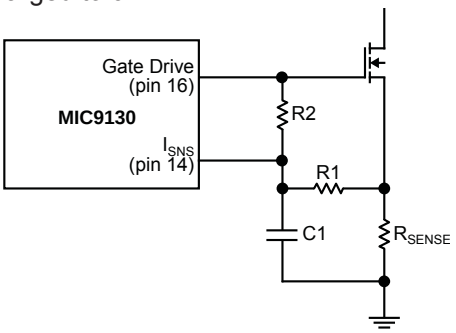


Figure 12

The procedure outlined below demonstrates how to calculate the component values.

Compute the inductor current downslope as seen at the current sense input.

For a flyback, buck or forward mode topology the inductor downslope is equal to:

$$M2 = \frac{di}{dt} = \frac{V_O + V_D}{L}$$

where :

V_O is the output voltage

V_D is the forward voltage drop of the rectifier diode

L is the inductance of the output inductor (or the secondary winding inductance for the flyback topology)

M2 is the inductor current downslope

For a boost topology, the inductor downslope is:

$$M2 = \frac{di}{dt} = \frac{V_{OUT} - V_{IN} + V_D}{L}$$

In a transformer isolated topology, the downslope must be reflected back to the primary by the turns ratio of the transformer. The reflected downslope is:

$$M2_{REFLECTED} = M2 \times \frac{Ns}{Np}$$

where : Ns/Np is the turns ratio of the secondary winding to the primary winding.

$M2_{REFLECTED}$ is the inductor curent downslope reflected to the secondary side of the current sense transformer.

The reflected downslope is multiplied by the current sense resistor to obtain the downslope at the current sense input pin (ISNS).

$$I_{SNS_SLOPE} = M2_{REFLECTED} \times R_S$$

where Rs is the value of the current sense resistor.

The required downslope of the compensation ramp at the ISNS input is:

$$M3 = I_{SNS_SLOPE} \times 0.67$$

R1 is know if a value for the resistor between the current sense resistor and the Isns pin, has already been selected. If not chose a value of 1k, which will minimize any offset and signal degradation at the ISNS pin. Select a value of C1 to minimize signal degradation from the cutoff frequency of R1/C1. The bandwidth should be at least six times the switching frequency.

$$C1 = \frac{1}{2 \times \pi \times f_S \times R1}$$

where: f_S is the switching frequency of the power supply (not the oscillator frequency)

The slope of the generated compensation ramp is:

$$M3 = V_{GATE_DRIVE} \times \frac{R1}{R2 + R1} \times \frac{1}{R2 \times C1}$$

Solving for R2 and assuming R2 is much greater than R1.

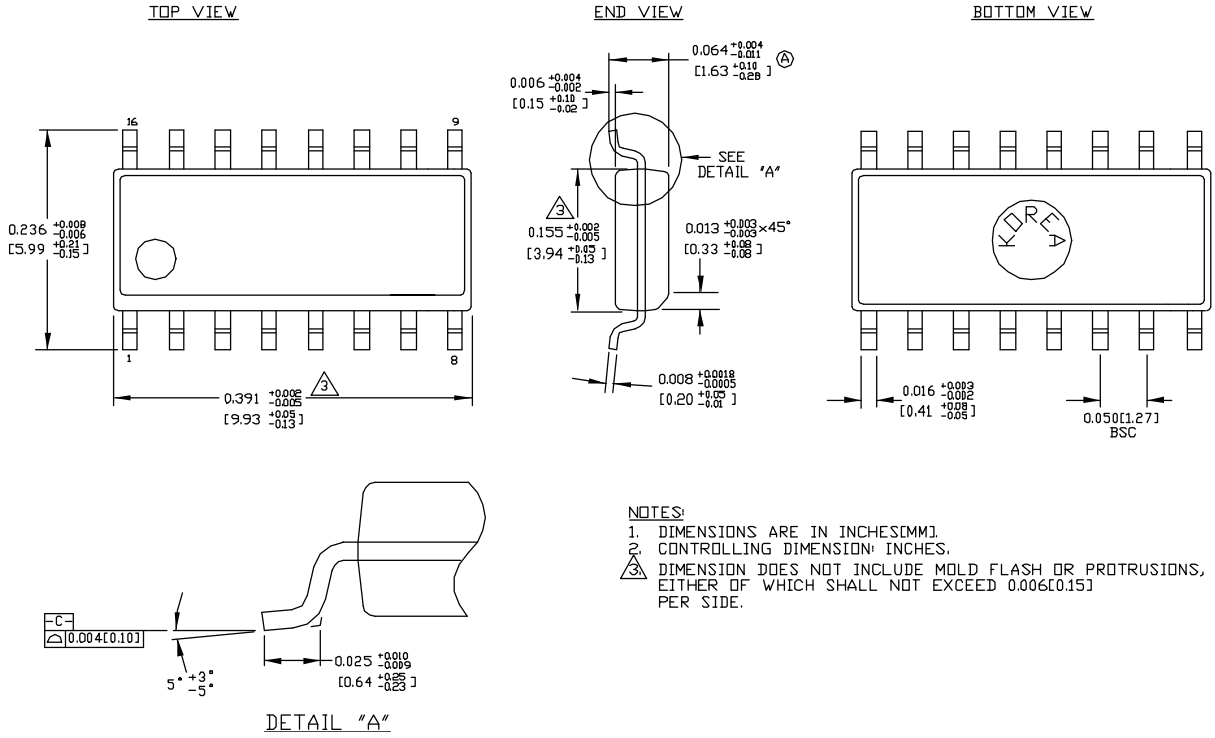
$$R2 = \sqrt{\frac{V_{GATE_DRIVE} \times R1}{M3 \times C1}}$$

where: V_{GATE_DRIVE} is the amplitude of the gate drive waveform

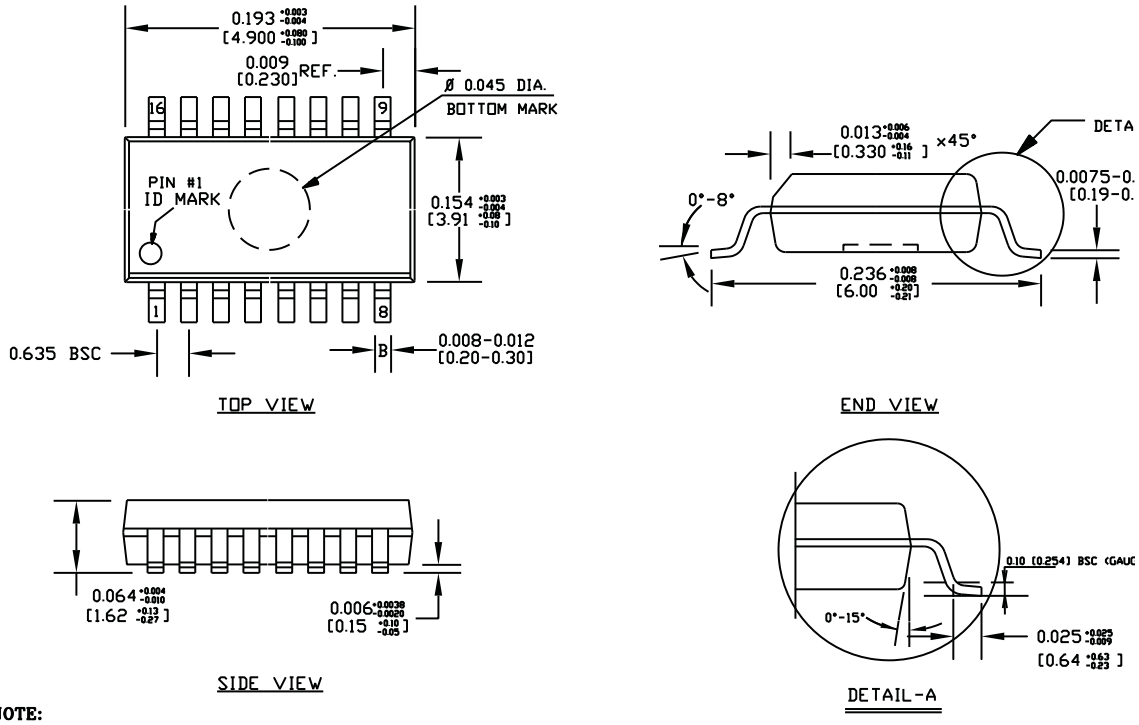
Error Amplifier

The error amplifier is part of the voltage control loop of the power supply. The FB pin is the inverting input to the error amplifier. The non-inverting input is internally connected to a 2.5V reference. The output of the error amplifier, COMP, is connected to the PWM comparator. The error amplifier provides the reference to limit and control the peak current of the power supply. There is a 1.2V level shift between the output of the error amplifier and the PWM comparator. This allows the output of the error amplifier to operate in a linear region and prevents loading on the COMP pin from interfering with proper control of the current signal.

Package Information



16-Lead SOIC (M)



NOTE:

1. **ALL DIMENSIONS ARE IN INCHES [MM].**
2. **LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.**
3. **MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].**
4. **THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.**
5. **BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.**

16-Lead QSOP (QS)

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