MIC4807

80V 8-Channel Addressable Low-Side Driver

General Description

The MIC4807 is an 80V, 8-channel, addressable low side driver with latches and TTL/CMOS compatible logic inputs. Each logic input is composed of a comparator with a 1.4V bandgap-derived reference serving as the trip point. The addresses (A_{IN}, B_{IN}, and C_{IN}) and Data-in logic inputs have an internal 50µA pull-up current source, while the Output Enable (OE), Chip Select ($\overline{CS}$), and $\overline{Clear}$ logic inputs have an internal 75µA pull-down sink. If the logic lines to the MIC4807 are severed, these currents guarantee that the outputs will turn OFF.

Individual latches in the MIC4807 are selected by a binary address presented at inputs A_{IN}, B_{IN}, and C_{IN}. Data-in is directed to the addressed latch while $\overline{CS}$ is held low, allowing an individual output to be pulse-width modulated. When $\overline{CS}$ is set high again, the last Data-in is stored in the latch. If Data-in = "1", the addressed output is turned on, and if Data-in = "0", the addressed output is turned off.

Information presented to Data-in and the address inputs is transferred to the latches while $\overline{CS}$ is pulled low. For application, where several outputs must be (Continued)

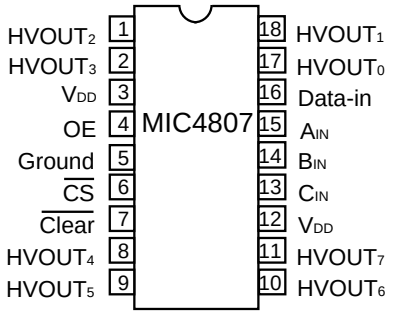
Features

- 4.5V to 16V Operation
- Eight 80V 100mA Outputs
- Off-state Leakage less than 10µA at 25°C
- Short-Circuit Proof
- Thermal Shutdown with Hysteresis
- DMOS Output Devices ($R_{ON} \leq 7\Omega$ at 25°C)

Applications

- Lamp Drivers
- Solenoid Drivers
- Display Drivers
  - -Electroluminescent
  - -Vacuum Fluorescent
  - -Plasma
- Relay Drivers
- Print Head Drivers
- Heater Drivers
- Power Semiconductor Drivers
- Security Systems
- Environmental Controls
- Process Controllers

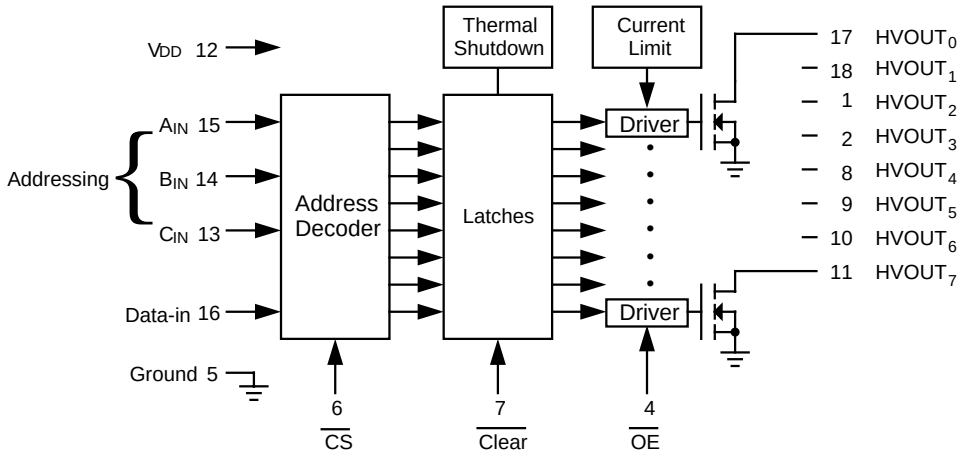
Pin Diagram



Ordering Information

Part Number	Operating Temperature-Range	Package
MIC4807BN	-40°C to 85°C	18-Pin Plastic DIP

Block Diagram



General Description (Continued)

turned on simultaneously, Gray Code address sequencing can be applied to Ain, Bin, Cin, while Data-in is held high and $\overline{CS}$ is held low. Data-in will be transferred to each address in turn, without the need to toggle $\overline{CS}$. Similarly, a set of outputs could be simultaneously turned off by setting Data-in low. Gray Code ensures that no intermediate addresses are inadvertently accessed. A typical Gray Code is 0, 1, 3, 2, 6, 7, 5, 4.

Each output drive circuit has a high-voltage, power DMOS device configured as a transconductance loop. This loop limits the output current to typically 200mA. While current limiting keeps the output device within its allowable safe-operating area (SOA), the power dissipation may be excessive. Long-term survival is guaranteed by thermal shutdown.

When operated below current limit, the outputs appear as small-valued resistors (typically 5.1Ω at 25°C) connected to ground. The "ON" resistance (R_{ON}) has a strong, positive temperature coefficient (approximately 7500 ppm/°C) which promotes current sharing if two or more outputs are paralleled.

Absolute Maximum Ratings (Notes 1, 2 and 3)

Output Voltage (V_{OUT}, OFF)	100V
Supply Voltage (V_{DD})	16.5V
Logic Input Voltage (V_{IN})	–0.3V TO V_{DD} + 0.3
Continuous Output Current (I_{OUT})	Internally Limited
Power Dissipation (P_D, Note 2)	Internally Limited
Ambient Temperature (T_A):	–40°C to +85°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
θ_{JA} - Plastic DIP	130°C/W

Electrical Characteristics: (Note 6) MIC4807BN, T_A = 25°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5		16	V
I_{DD}	Supply Current	OE = L (Note 3) OE = H (Note 4)		5.5 1.5	10 3	mA mA
V_{IN} (0)	Logic Input Voltage	4.5V ≤ V_{DD} ≤ 16V			0.8	V
V_{IN} (1)			2.0			V
I_{IN} (0)	Logic Input Current for A_{IN}, B_{IN}, C_{IN}, and Data-in	V_{IN} = 0V	–150	–70	–25	µA
I_{IN} (1)	Logic Input Current for $\overline{CS}$, OE, and $\overline{Clear}$	V_{IN} = V_{DD}	25	130	250	µA
I_{OUT}	Output Leakage Current	OE = 0V, V_{OUT} = 80V		1	10	µA
R_{ON}	Output "ON" Resistance	Output is ON, V_{OUT} = 0.7V,V_{DD} = 10V		5.1	7	Ω
I_{SC}	Short Circuit Current	Output is ON< V_{OUT} = 50V 10V ≤ V_{DD} ≤ 15V (Note 5)	140	190	250	mA
V_{OUT}	Output Voltage (OFF)				80	V
V_{OUT}	Output Voltage (ON)	I_{OUT} = 50mA,V_{DD} = 10V I_{OUT} = 100mA, V_{DD} = 10V		0.26 0.51	0.35 0.7	V V
	Data and Address Set-up Time	V_{DD} = 10V for all timing tests (A, see **Timing Diagram**)	400			ns
	Data and Address Hold Time	(B)	50			ns
	$\overline{CS}$ Pulse Width	(C)	500			ns
	Turn-on Delay	(D)			2.5	ns

Electrical Characteristics: (Note 6) T_A = 25°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Turn-Off Delay	(E)			2.5	µs
	Output Disable Response Time	(F)			2	µs
	Output Enable Response Time	(G)			2	µs
	$\overline{\text{Clear}}$ Response Time	(H)			2.5	µs
	$\overline{\text{Clear}}$ Pulse Width	(I)	500			ns

Electrical Characteristics: (Note 6) T_A = –55°C to +125°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

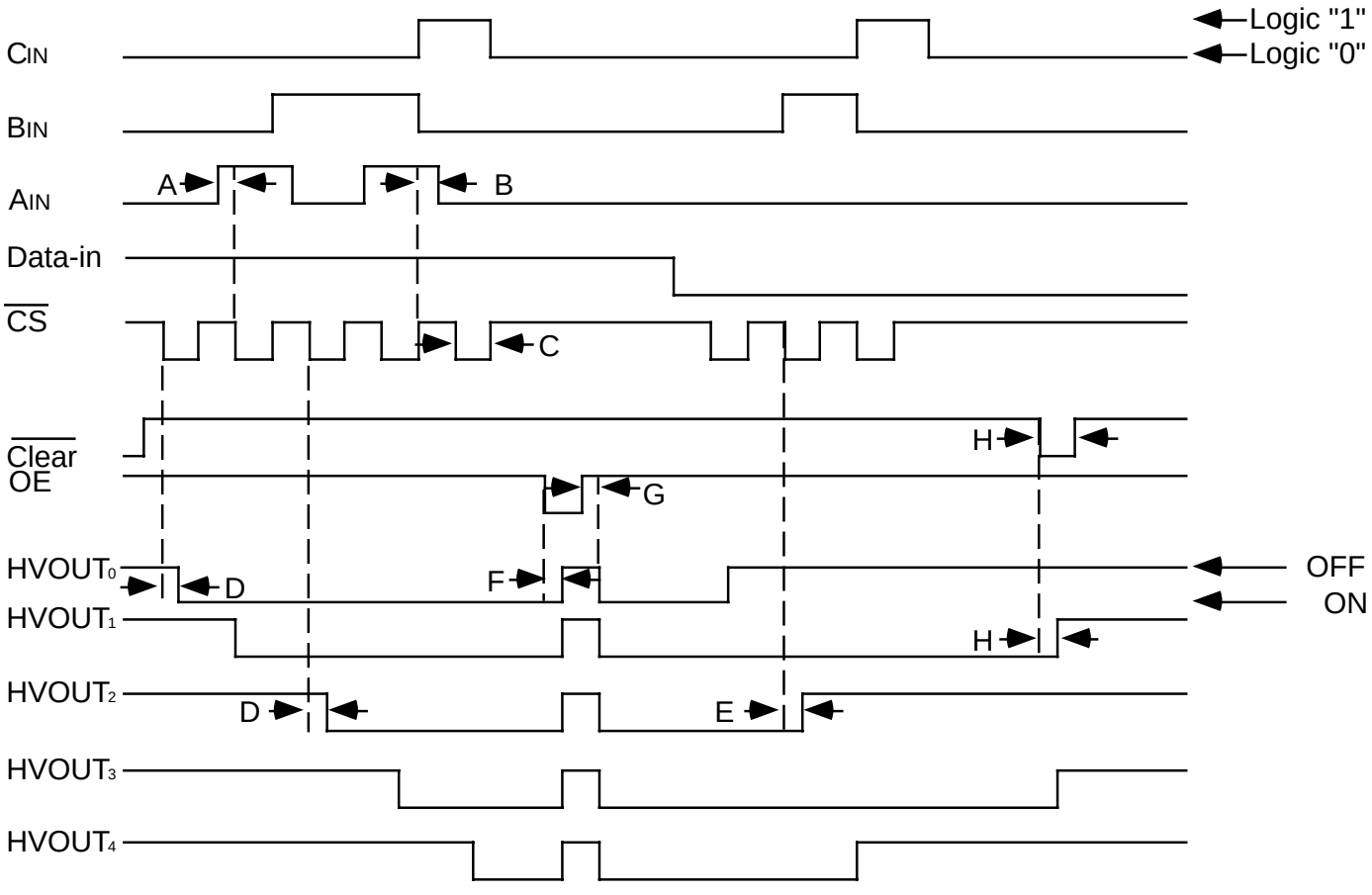
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5		16	V
I_{DD}	Supply Current	OE = L (Note 3) OE = H (Note 4)			15 4	mA mA
V_{IN} (0)	Logic Input Voltage	4.5V ≤ V_{DD} ≤ 16V			0.8	V
V_{IN} (1)			2.0			V
I_{IN} (0)	Logic Input Current for A_{IN}, B_{IN}, C_{IN}, and Data-in	V_{IN} = 0V	–250		–10	µA
I_{IN} (1)	Logic Input Current for $\overline{\text{CS}}$, OE, and $\overline{\text{Clear}}$	V_{IN} = V_{DD}	25		400	µA
I_{OUT}	Output Leakage Current	OE = 0V, V_{OUT} = 80V		5.1	7	µA
R_{ON}	Output "ON" Resistance	Output is ON, V_{OUT} =0.7V,V_{DD}=10V			12	Ω
I_{SC}	Short Circuit Current	Output is ON< V_{OUT} = 50V 10V ≤ V_{DD} ≤ 15V (Note 5)	100		300	mA
V_{OUT}	Output Voltage (OFF)				80	V
V_{OUT}	Output Voltage (ON)	I_{OUT} = 50mA,V_{DD} = 10V I_{OUT} = 100mA, V_{DD} = 10V			0.6 1.2	V V
	Data and Address Set-up Time	V_{DD} = 10V for all timing tests (A, see **Timing Diagram**)	700			ns
	Data and Address Hold Time	(B)	50			ns
	$\overline{\text{CS}}$ Pulse Width	(C)	1000			ns
	Turn-on Delay	(D)			5	µs

Electrical Characteristics: (Note 6) T_A = 25°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

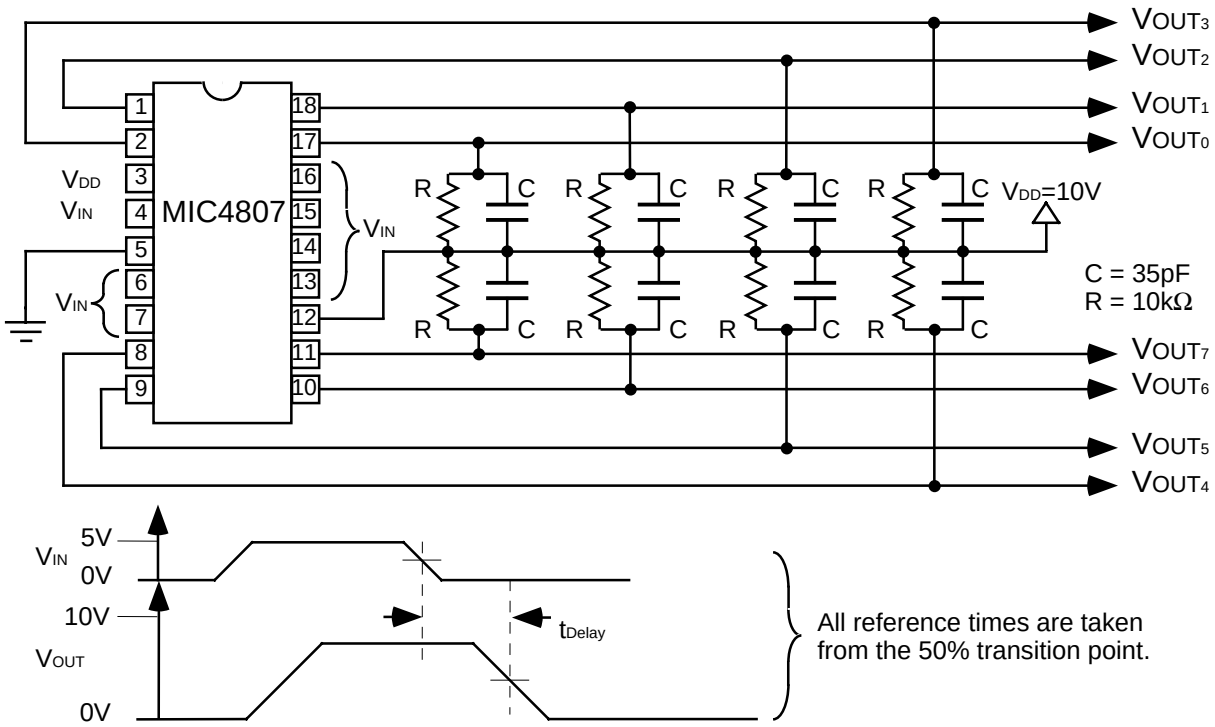
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Turn-Off Delay	(E)			5	µs
	Output Disable Response Time	(F)			4	µs
	Output Enable Response Time	(G)			4	µs
	$\overline{\text{Clear}}$ Response Time	(H)			5	µs
	$\overline{\text{Clear}}$ Pulse Width	(I)	1000			ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating ratings.
Note 2: The junction temperature is internally limited by a thermal shutdown circuit. The maximum power dissipation is a function of T_{JMAX}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C, and the MIC4807 will go into thermal shutdown.
Note 3: All outputs are off when **OUTPUT ENABLE** is pulled low.
Note 4: All outputs are turned on during this test.
Note 5: Pulse testing is used to avoid thermal shutown.
Note 6: Minimum and Maximum limits are tested and 100% guaranteed over the temperature range specified. Typicals are measured at 25°C and represent the most likely parametric norm.

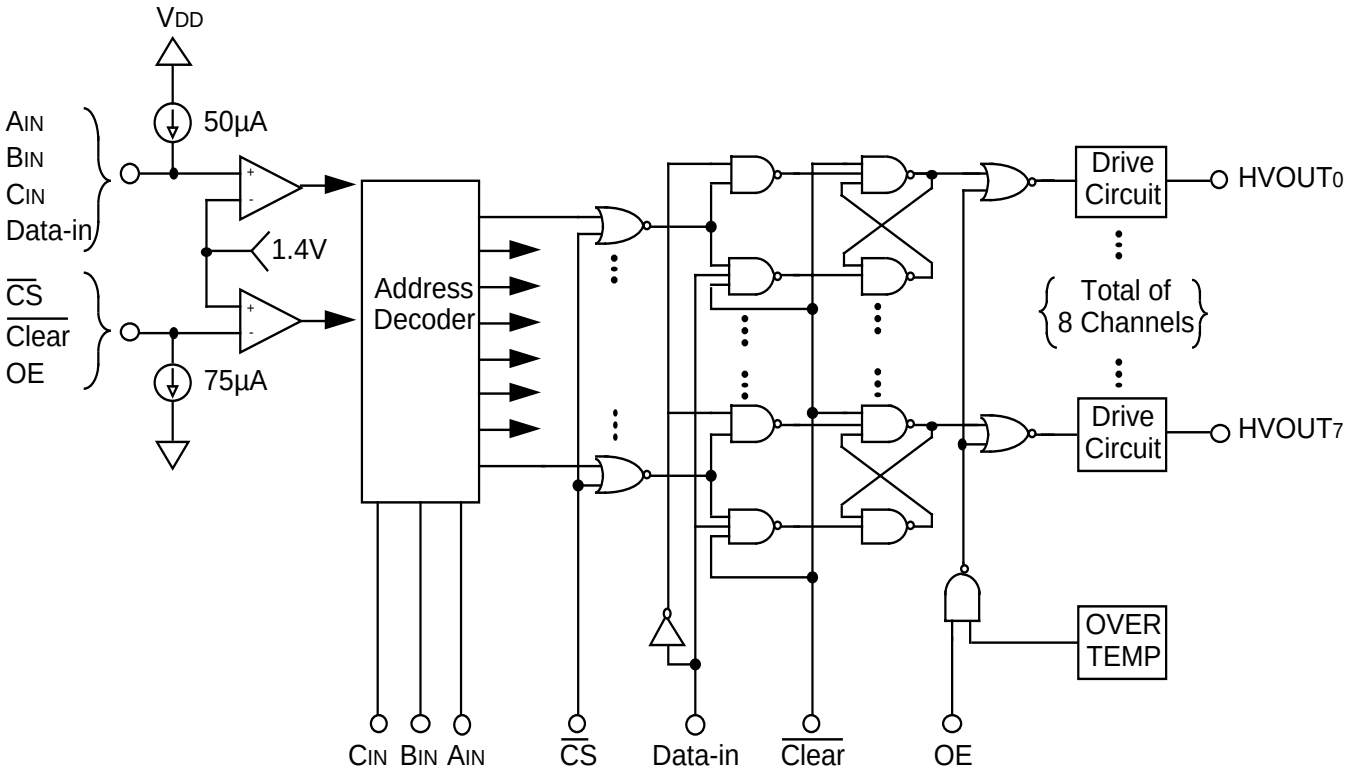
Timing Diagram



Test Circuit and AC Waveform Measurement Standards



Equivalent Logic Diagram



Truth Table

$\overline{CS}$	$\overline{Clear}$	Data-In	C_{IN}	B_{IN}	A_{IN}	OE	$HVOUT_0$	$HVOUT_1$	$HVOUT_2$	$HVOUT_3$	$HVOUT_4$	$HVOUT_5$	$HVOUT_6$	$HVOUT_7$	Functional Mode
X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	Clear
H	H	X	X	X	X	H	P	P	P	P	P	P	P	P	Memory
L	H	D	L	L	L	H	$\overline{D}$	P	P	P	P	P	P	P	Address $HVOUT_0$
L	H	D	L	L	H	H	P	$\overline{D}$	P	P	P	P	P	P	Address $HVOUT_1$
L	H	D	L	H	L	H	P	P	$\overline{D}$	P	P	P	P	P	Address $HVOUT_2$
L	H	D	L	H	H	H	P	P	P	$\overline{D}$	P	P	P	P	Address $HVOUT_3$
L	H	D	H	L	L	H	P	P	P	P	$\overline{D}$	P	P	P	Address $HVOUT_4$
L	H	D	H	L	H	H	P	P	P	P	P	$\overline{D}$	P	P	Address $HVOUT_5$
L	H	D	H	H	L	H	P	P	P	P	P	P	$\overline{D}$	P	Address $HVOUT_6$
L	H	D	H	H	H	H	P	P	P	P	P	P	P	$\overline{D}$	Address $HVOUT_7$
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	Blanking

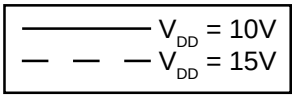
L = Low Logic Level **X = Don't Care**

H = High Logic Level **P = Previous State**

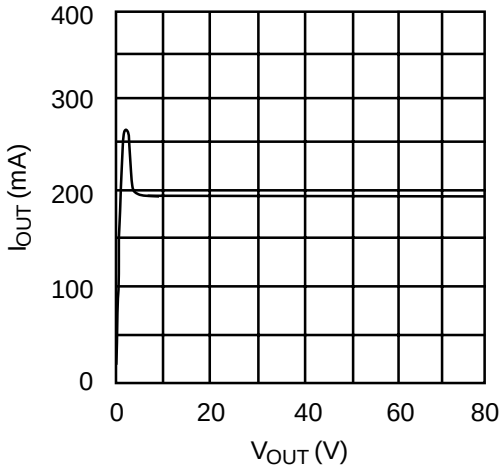
D = Data (High or Low)

Typical DC Output Characteristics for the "On" State:

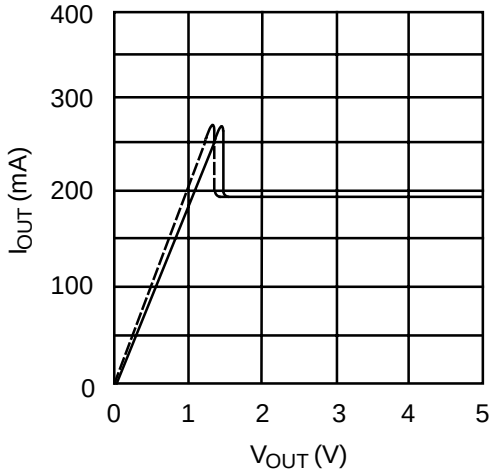
(V_{DD} = 10V and T_A = 25°C unless other wise specified)



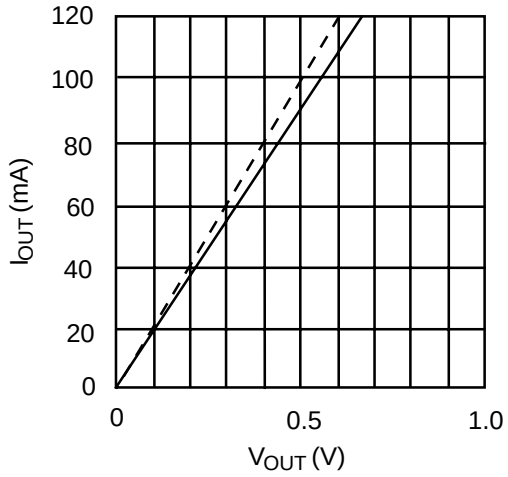
SHORT CIRCUIT CURRENT



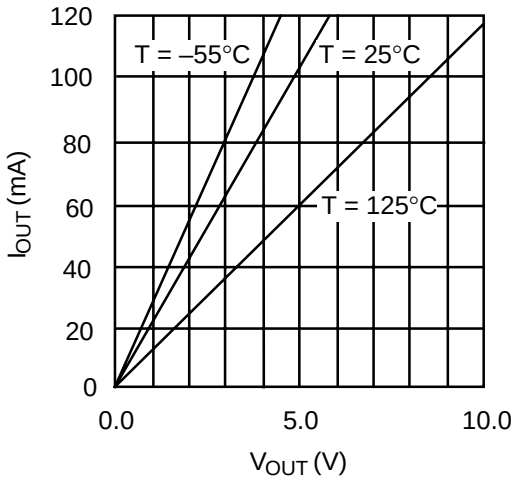
EXPANDED VERSION OF SHORT CIRCUIT CURRENT FOR LOW OUTPUT VOLTAGE (V_{OUT})



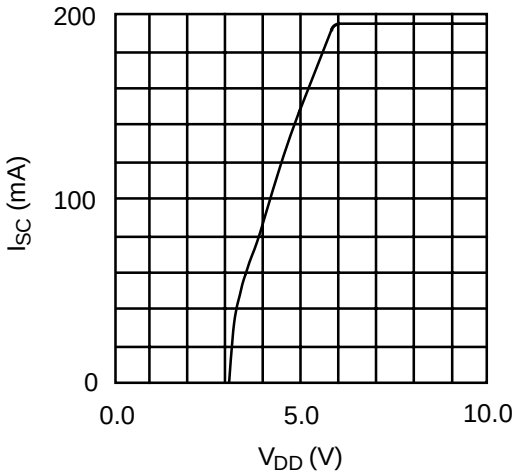
I_{OUT} FOR SEPARATE V_{DD}



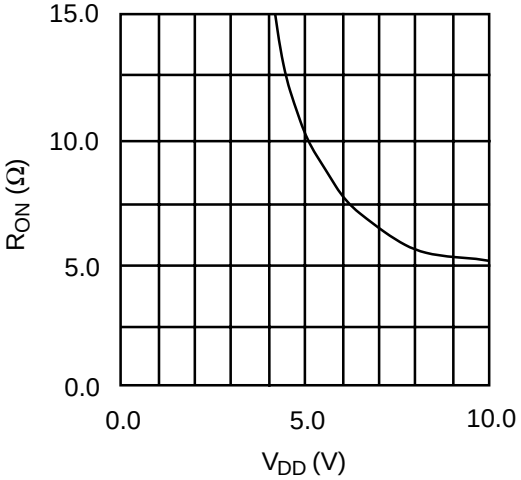
I_{OUT} AT 3 TEMPERATURES



SHORT CIRCUIT CURRENT LIMIT (I_{SC})



ON RESISTANCE (R_{ON})



Pin Description

Pin No.	Pin Name	Functional Description
5	Ground	Electrical ground to chip substrate.
12	V_{DD}	Positive logic supply voltage (10V-15V).
1, 2, 8, 9,10, 11, 17,18	$HVOUT_0$ through $HVOUT_7$	These are the high voltage (HV) open outputs, each of which is capable of sinking 100mA when switched on, and standing off 80V when switched off. In addition, each output channel is equipped with an analog current limiter to protect it from shorts to the positive high voltage supply. When an output is shorted (up to 80V), a maximum of 225mA (200mA nominal) will flow through it to ground.
13, 14, 15	C_{IN}, B_{IN}, $\&A_{IN}$	When these inputs are combined together they form the BCD address used to select the desired output. Each input is TTL compatible with an internal pull-up current source of 50mA.
6	CS	When $\overline{CS}$ is at logic "0" the device is actively addressed, and when $\overline{CS}$ is at logic "1" the decoded address and input Data are inhibited, making the part unaddressable. $\overline{CS}$ is TTL compatible with an internal pull-down current sink of 75µA.
7	$\overline{Clear}$	$\overline{Clear}$ resets all the outputs to the off state when pulled to logic "0", and is TTL compatible with an internal pull-down current sink of 75µA.
16	Data-in	Data-in determines the state of the output being addressed. When Data-in is at logic "0" the addressed output is turned off, and when Data-in is at logic "1" the addressed output is turned on. Data-in is TTL compatible with an internal pull-up current source of 50µA.
4	OE	OE allows the bank of eight outputs to be duty cycled together. When OE is at logic "1" the outputs are enabled to follow their respective latches, and when OE is at logic "0" all the outputs are turned off. OE is TTL Compatible with a pull-down current sink of 75µA.