MIC45116

20V/6A DC/DC Power Module

Features

- Up to 6A Output Current
- >93% Peak Efficiency
- Output Voltage of 0.8V to 85% of Input with ±1% Accuracy
- Fixed 600 kHz Switching Frequency
- Enable Input and Open-Drain Power Good Output
- HyperLight Load® (MIC45116-1) Improves Light Load Efficiency
- Hyper Speed Control® (MIC45116-2) Architecture Enables Fast Transient Response
- Supports Safe Start-Up into Pre-Biased Output
- –40°C to +125°C Junction Temperature Range
- Thermal Shutdown Protection
- Short-Circuit Protection with Hiccup Mode
- Adjustable Current Limit
- Available in 52-Pin 8 mm x 8 mm x 3 mm QFN Package

Applications

- High Power Density Point-of-Load Conversion
- Servers, Routers, Networking, and Base Stations
- FPGAs, DSP, and Low-Voltage ASIC Power Supplies
- Industrial and Medical Equipment

General Description

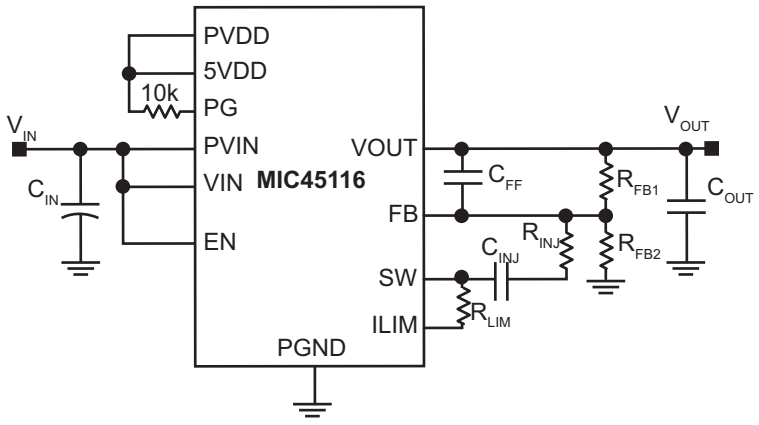
The MIC45116 is a synchronous step-down regulator module, featuring a unique adaptive ON-time control architecture. The module incorporates a DC/DC controller, power MOSFETs, bootstrap diode, bootstrap capacitor, and an inductor in a single package; simplifying the design and layout process for the end user.

This highly integrated solution expedites system design and improves product time-to-market. The internal MOSFETs and inductor are optimized to achieve high efficiency at a low output voltage. The fully optimized design can deliver up to 6A current under a wide input voltage range of 4.75V to 20V without requiring additional cooling.

The MIC45116-1 uses HyperLight Load® (HLL) which maintains high efficiency under light load conditions by transitioning to variable frequency, discontinuous-mode operation. The MIC45116-2 uses Hyper Speed Control® architecture which enables ultra-fast load transient response, allowing for a reduction of output capacitance. The MIC45116 offers 1% output accuracy that can be adjusted from 0.8V to 85% of the input (PV_{IN}) with two external resistors. Additional features include thermal-shutdown protection, adjustable current limit, and short-circuit protection. The MIC45116 allows for safe start-up into a pre-biased output.

Typical Application Circuit

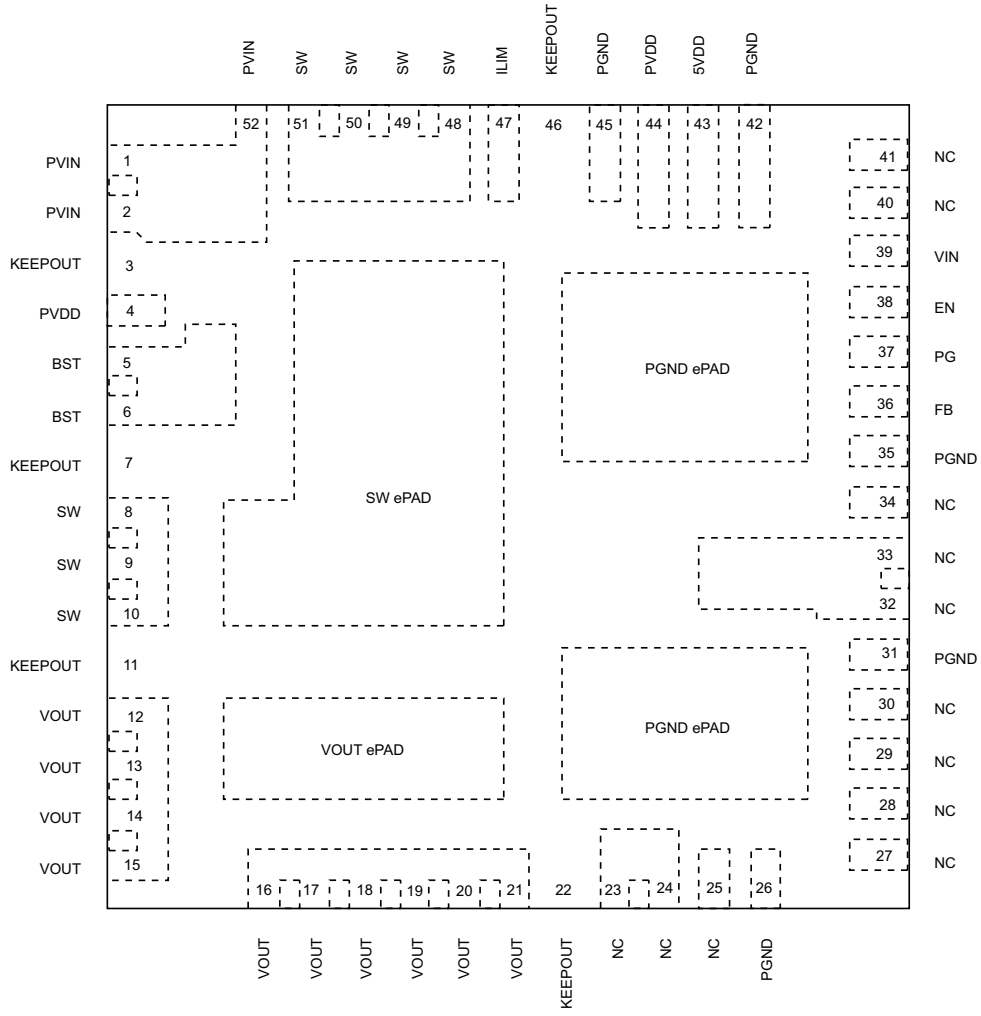
MIC45116
8x8x3 QFN



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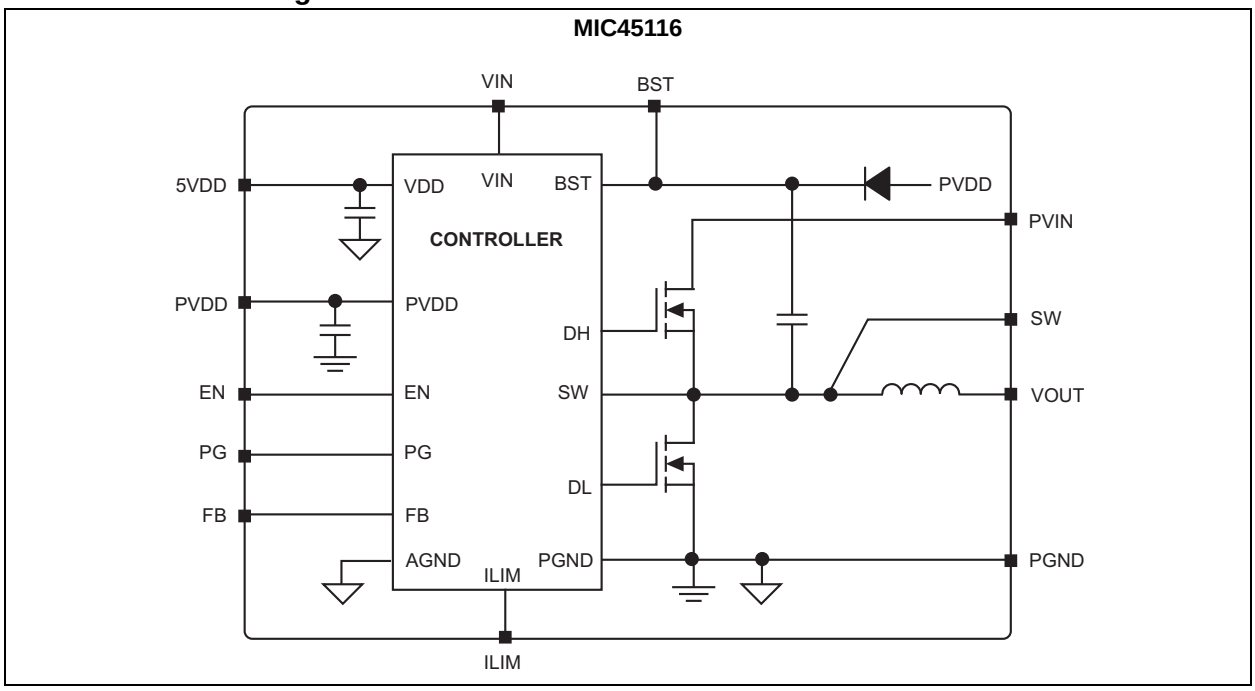
Package Type

MIC45116
8x8x3 QFN (MP)



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Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PV_{IN} – V_{IN} to P_{GND} ..... –0.3V to +30V
PV_{DD} – $5V_{DD}$ to P_{GND} ..... –0.3V to +6V
V_{SW}, V_{ILIM}, V_{EN} to P_{GND} ..... –0.3V to (V_{IN} + 0.3V)
V_{BST} to V_{SW} ..... –0.3V to +6V
V_{BST} to P_{GND} ..... –0.3V to +36V
V_{PG} to P_{GND} ..... –0.3V to ($5V_{DD}$ + 0.3V)
V_{FB} to P_{GND} ..... –0.3V to ($5V_{DD}$ + 0.3V)
ESD Rating(Note 1) ..... ESD Sensitive

Operating Ratings ‡

Supply Voltage (PV_{IN} – V_{IN}) ..... +4.75V to +20V
Output Current 6A
Enable Input (V_{EN}) ..... 0V to V_{IN}
Power Good (V_{PG}) ..... 0V to $5V_{DD}$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{EN} = 12V$, $V_{OUT} = 3.3V$, $V_{BST} – V_{SW} = 5V$, $T_J = +25°C$. **Bold** values indicate $–40°C \le T_J \le +125°C$, unless otherwise noted. **(Note 1)**.						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Input						
V_{IN}, PV_{IN}	Input Voltage Range	**4.75**	—	**20**	V	—
I_Q	Quiescent Supply Current (MIC45116-1)	—	0.35	**0.75**	mA	$V_{FB} = 1.5V$
I_Q	Quiescent Supply Current (MIC45116-2)	—	1.03	—	mA	$V_{FB} = 1.5V$
I_{IN}	Operating Current	—	29.4	—	mA	$PV_{IN} = V_{IN} = 12V$, $V_{OUT} = 1.8V$, $I_{OUT} = 0A$ (MIC45116-2)
I_{SHDN}	Shutdown Supply Current	—	5.3	**10**	µA	$V_{EN} = 0V$
$5V_{DD}$ Output						
V_{DD}	$5V_{DD}$ Output Voltage	**4.8**	5.2	**5.4**	V	$V_{IN} = 7V$ to $20V$, $I_{5VDD} = 10$ mA
UVLO	$5V_{DD}$ UVLO Threshold	**3.8**	4.2	**4.6**	V	V_{5VDD} Rising
UVLO_HYS	$5V_{DD}$ UVLO Hysteresis	—	400	—	mV	V_{5VDD} Falling
—	$5V_{DD}$ Load Regulation	0.6	2	3.6	%	$I_{5VDD} = 0$ mA to 40 mA
Reference						
V_{FB}	Feedback Reference Voltage	0.792	0.8	0.808	V	$T_J = 25°C$
		0.784	0.8	**0.816**		$–40°C \le T_J \le +125°C$
I_{FB_BIAS}	FB Bias Current	—	5	**500**	nA	$V_{FB} = 0.8V$
Enable Control						
EN_{HIGH}	EN Logic Level High	**1.8**	—	—	V	—
EN_{LOW}	EN Logic Level Low	—	—	**0.6**	V	—
EN_{HYS}	EN Hysteresis	—	200	—	mV	—
I_{ENBIAS}	EN Bias Current	—	5	**10**	µA	$V_{EN} = 12V$
Oscillator						
f_{SW}	Switching Frequency	**400**	600	**750**	kHz	$I_{OUT} = 2A$
D_{MAX}	Maximum Duty Cycle	—	85	—	%	—
D_{MIN}	Minimum Duty Cycle	—	0	—	%	$V_{FB} = 1V$
$t_{OFF(MIN)}$	Minimum Off-Time	140	250	350	ns	—
Soft-Start						
t_{SS}	Soft-Start Time	—	3.3	—	ms	FB from 0V to 0.8V
Short-Circuit Protection						
V_{CL}	Current-Limit Threshold	–30	–14	0	mV	$V_{FB} = 0.79V$
V_{SC}	Short-Circuit Threshold	–23	–7	9	mV	$V_{FB} = 0V$
I_{CL}	Current-Limit Source Current	60	80	100	µA	$V_{FB} = 0.79V$
I_{SC}	Short-Circuit Source Current	25	35	45	µA	$V_{FB} = 0V$

Note 1: Specification for packaged product only.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V, V_{BST} – V_{SW} = 5V, T_J = +25ºC. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless otherwise noted. **(Note 1)**.						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Good (PG)						
V_{PG_TH}	PG Threshold Voltage	**85**	88	**95**	% V_{FB}	Sweep V_{FB} from low-to-high
V_{PG_HYS}	PG Hysteresis	—	6	—	% V_{FB}	Sweep V_{FB} from high-to-low
t_{PG_DLY}	PG Delay Time	—	80	—	µs	Sweep V_{FB} from low-to-high
V_{PG_LOW}	PG Low Voltage	—	60	**200**	mV	V_{FB} < 90% x V_{NOM}, I_{PG} = 1 mA
Thermal Protection						
T_{SHD}	Overtemperature Shutdown	—	160	—	°C	T_J rising
T_{SHD_HYS}	Overtemperature Shutdown Hysteresis	—	15	—	°C	—

Note 1: Specification for packaged product only.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	Note 1
Maximum Junction Temperature	—	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistances						
52-pin 8 mm x 8 mm x 3 mm QFN	θ_{JA}	—	22	—	°C/W	Note 2
52-pin 8 mm x 8 mm x 3 mm QFN	θ_{JC}	—	5	—	°C/W	Note 2

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: θ_{JA} and θ_{JC} were measured using the MIC45116 evaluation board.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

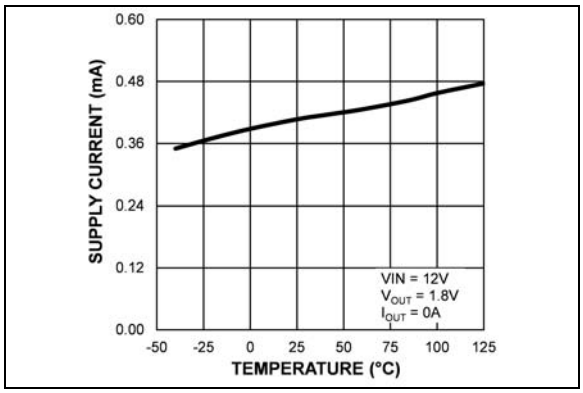


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Temperature (MIC45116-1).*

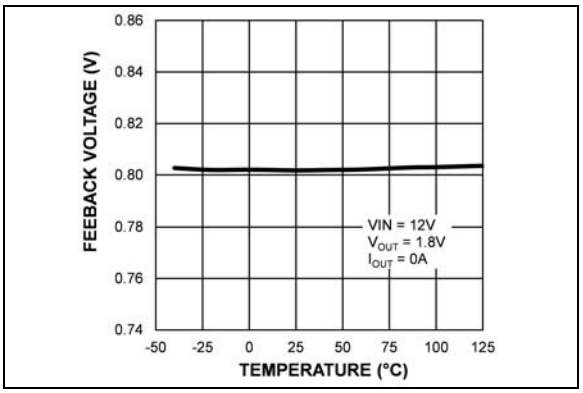


FIGURE 2-4: *Feedback Voltage vs. Temperature.*

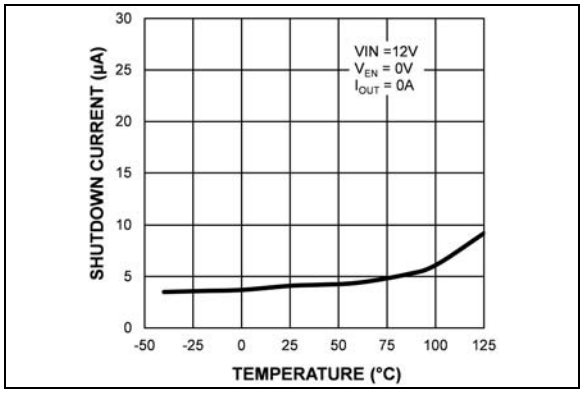


FIGURE 2-2: *V_{IN} Shutdown Current vs. Temperature.*

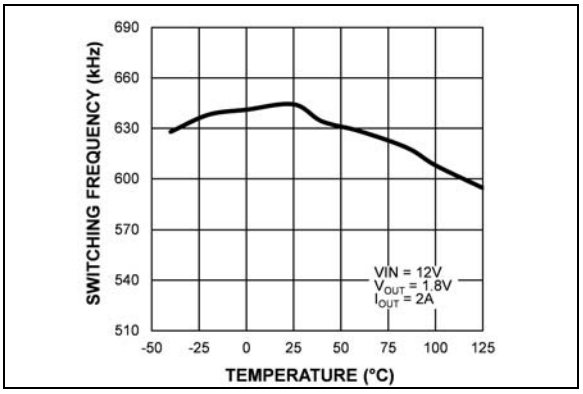


FIGURE 2-5: *Switching Frequency vs. Temperature.*

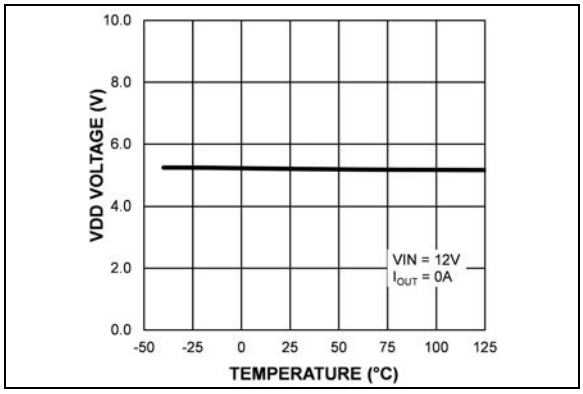


FIGURE 2-3: *V_{DD} Voltage vs. Temperature.*

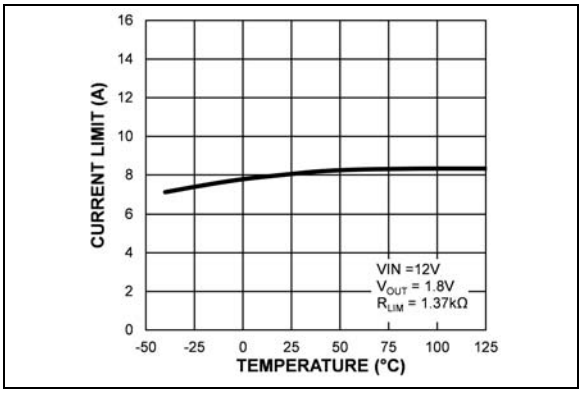


FIGURE 2-6: *Output Current Limit vs. Temperature.*

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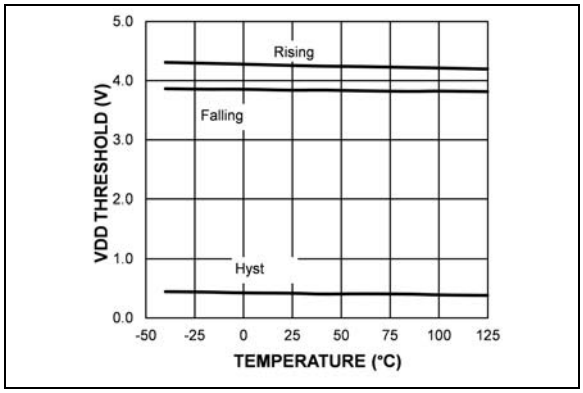


FIGURE 2-7: *V_{DD} UVLO Threshold vs. Temperature.*

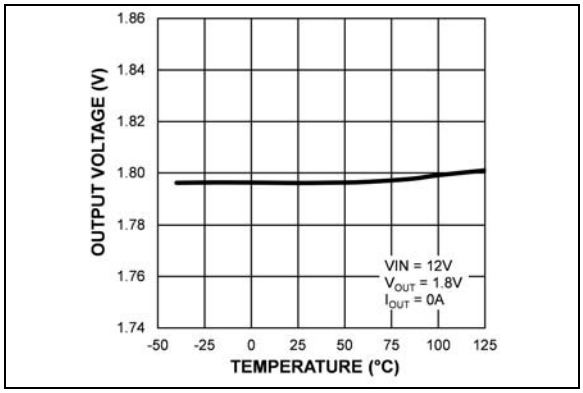


FIGURE 2-10: *Output Voltage vs. Temperature (MIC45116-1).*

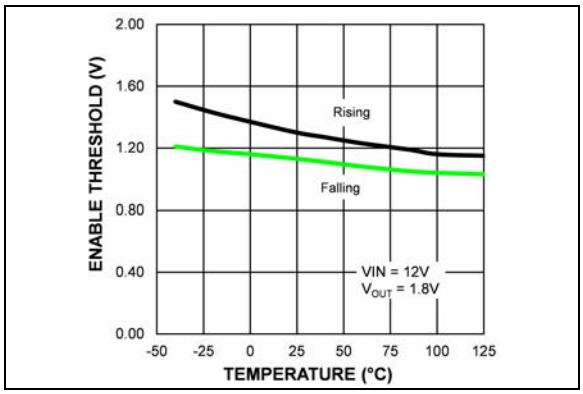


FIGURE 2-8: *Enable Threshold vs. Temperature.*

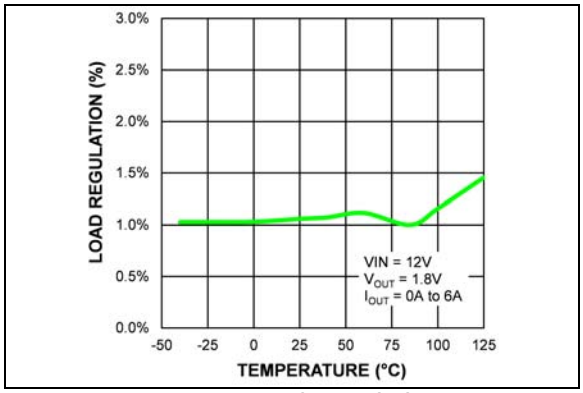


FIGURE 2-11: *Load Regulation vs. Temperature (MIC45116-1).*

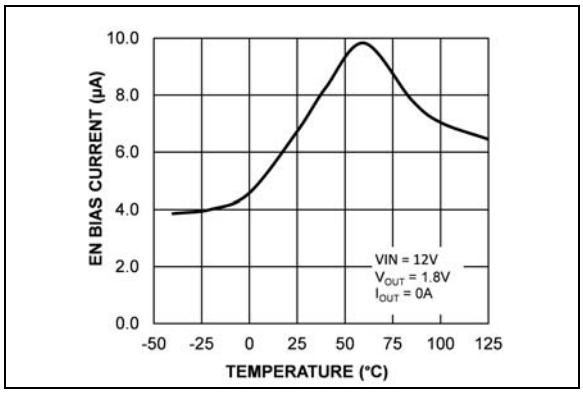


FIGURE 2-9: *EN Bias Curent vs. Temperature.*

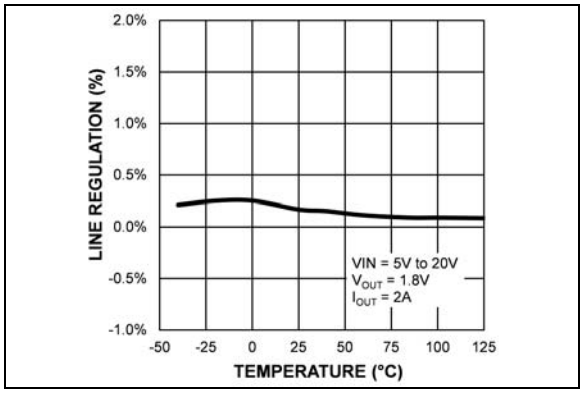


FIGURE 2-12: *Line Regulation vs. Temperature (MIC45116-1).*

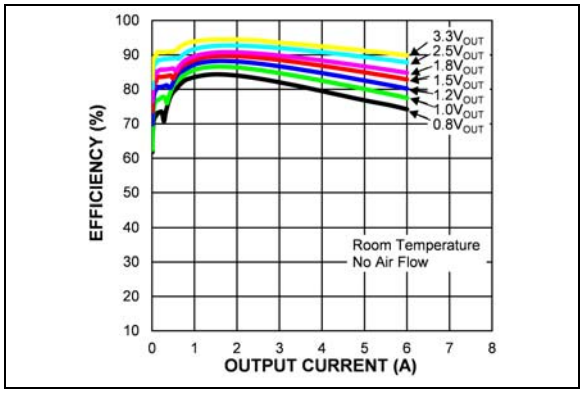


FIGURE 2-13: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC45116-1).*

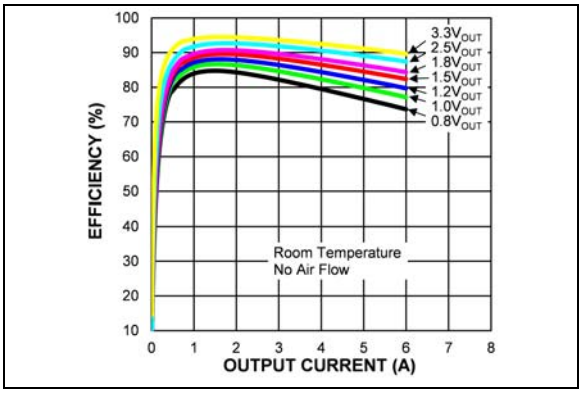


FIGURE 2-16: *Efficiency (V_{IN} = 5V) vs. Output Current (MIC45116-2).*

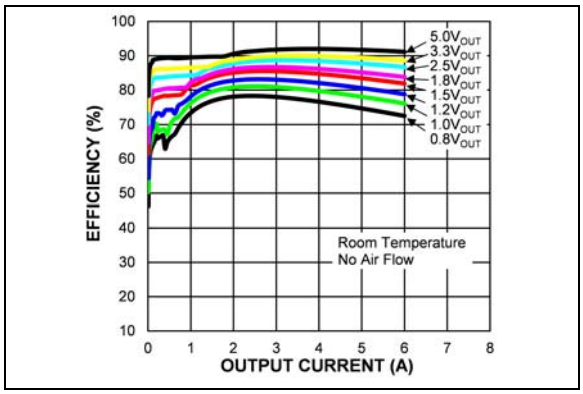


FIGURE 2-14: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC45116-1).*

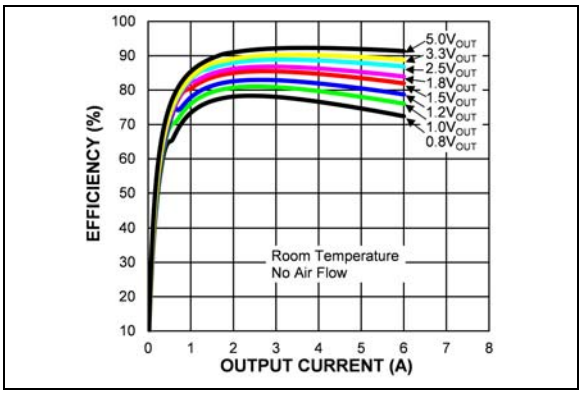


FIGURE 2-17: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC45116-2).*

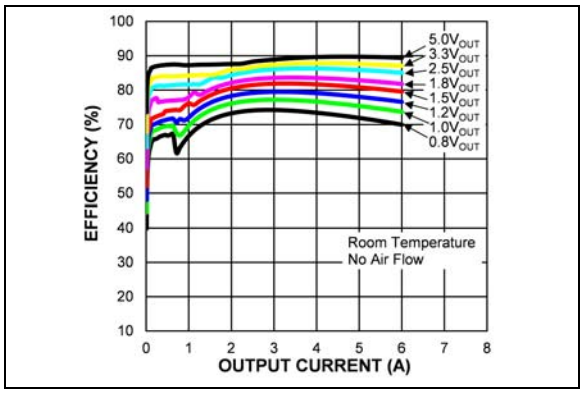


FIGURE 2-15: *Efficiency (V_{IN} = 18V) vs. Output Current (MIC45116-1).*

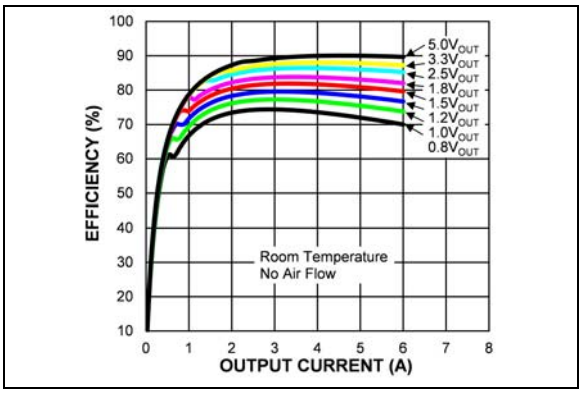


FIGURE 2-18: *Efficiency (V_{IN} = 18V) vs. Output Current (MIC45116-2).*

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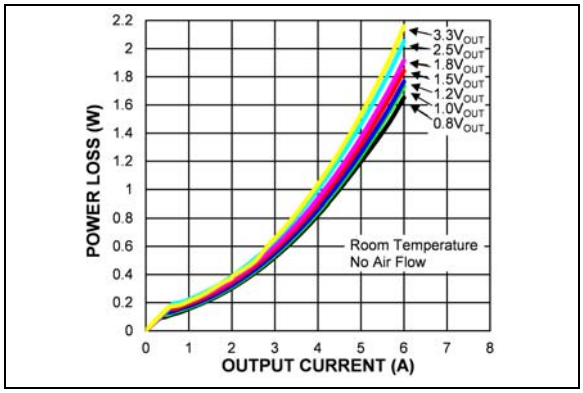


FIGURE 2-19: *Power Dissipation (V_{IN} = 5V) vs. Output Current (MIC45116-1).*

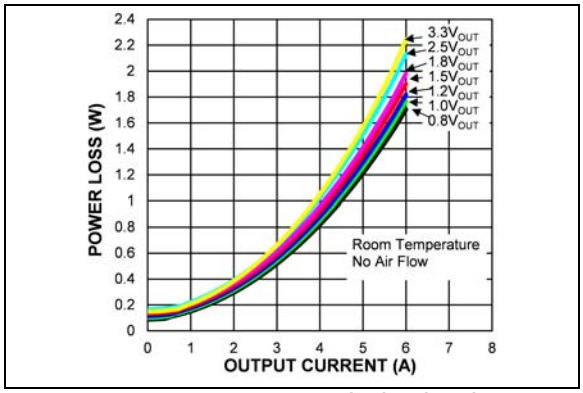


FIGURE 2-22: *Power Dissipation (V_{IN} = 5V) vs. Output Current (MIC45116-2).*

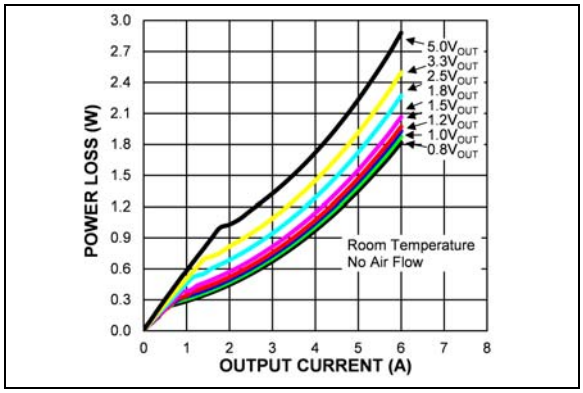


FIGURE 2-20: *Power Dissipation (V_{IN} = 12V) vs. Output Current (MIC45116-1).*

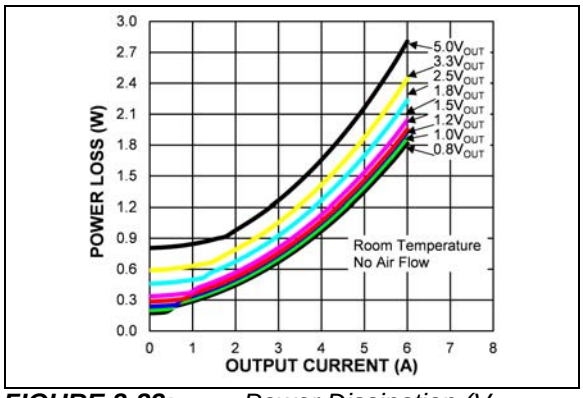


FIGURE 2-23: *Power Dissipation (V_{IN} = 12V) vs. Output Current (MIC45116-2).*

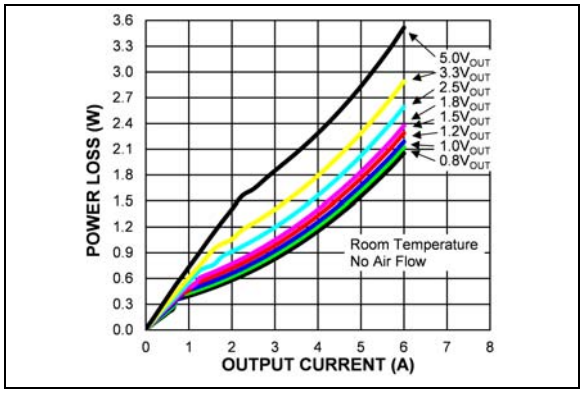


FIGURE 2-21: *Power Dissipation (V_{IN} = 18V) vs. Output Current (MIC45116-1).*

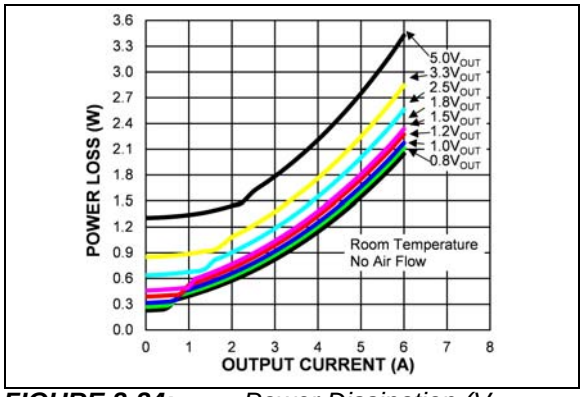


FIGURE 2-24: *Power Dissipation (V_{IN} = 18V) vs. Output Current (MIC45116-2).*

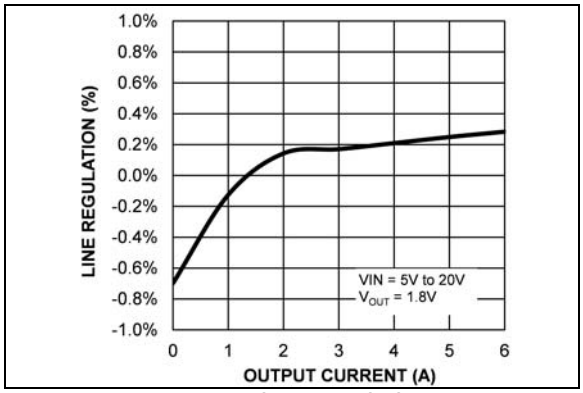


FIGURE 2-25: *Line Regulation vs. Output Current (MIC45116-1).*

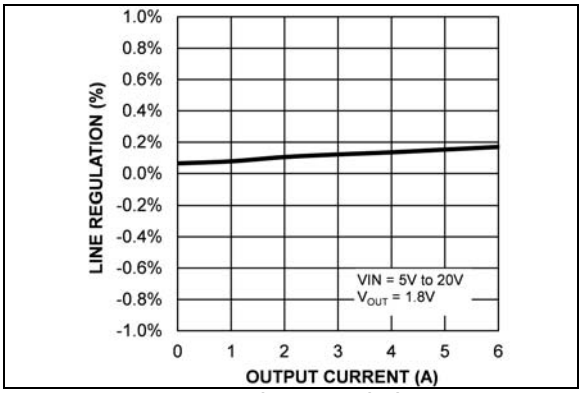


FIGURE 2-28: *Line Regulation vs. Output Current (MIC45116-2).*

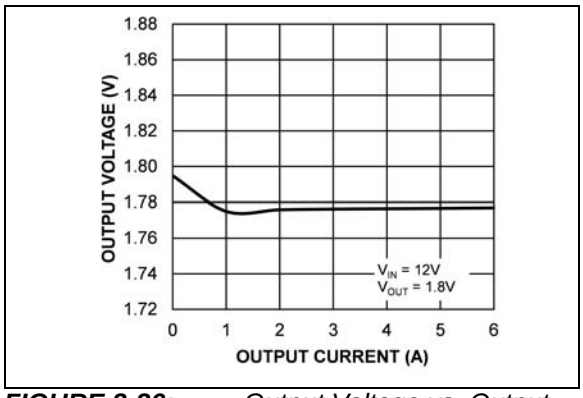


FIGURE 2-26: *Output Voltage vs. Output Current (MIC45116-1).*

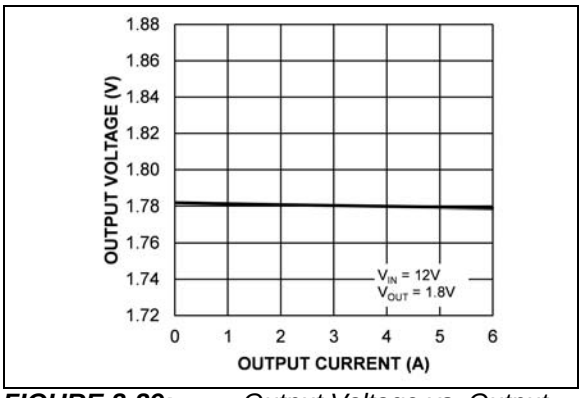


FIGURE 2-29: *Output Voltage vs. Output Current (MIC45116-2).*

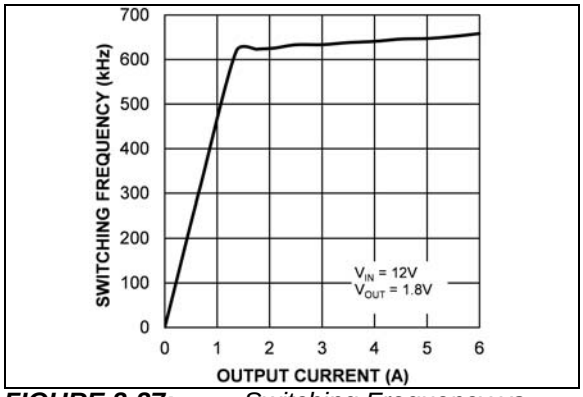


FIGURE 2-27: *Switching Frequency vs. Output Current (MIC45116-1).*

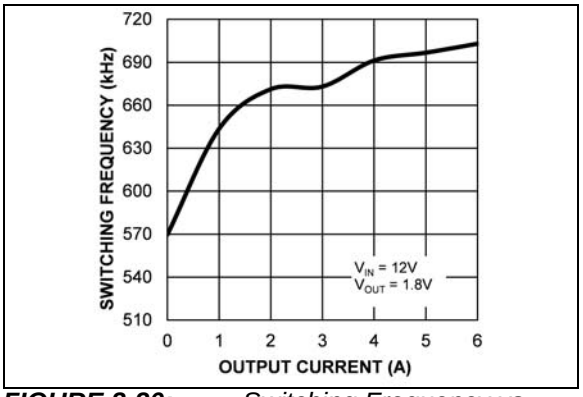


FIGURE 2-30: *Switching Frequency vs. Output Current (MIC45116-2).*

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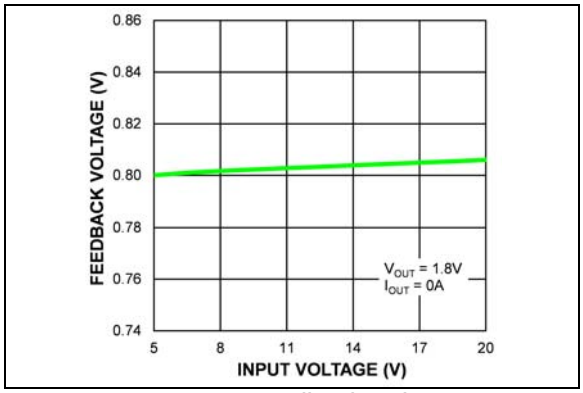


FIGURE 2-31: *Feedback Voltage vs. Input Voltage (MIC45116-1).*

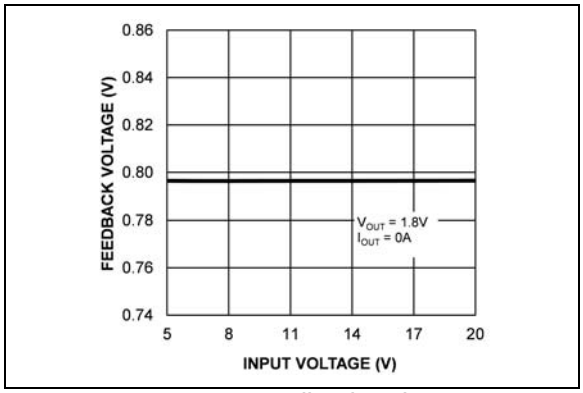


FIGURE 2-34: *Feedback Voltage vs. Input Voltage (MIC45116-2).*

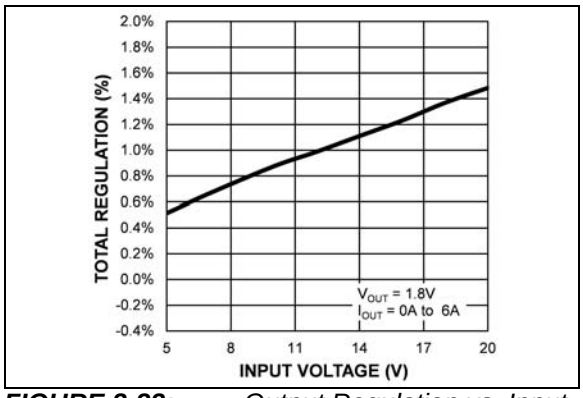


FIGURE 2-32: *Output Regulation vs. Input Voltage (MIC45116-1).*

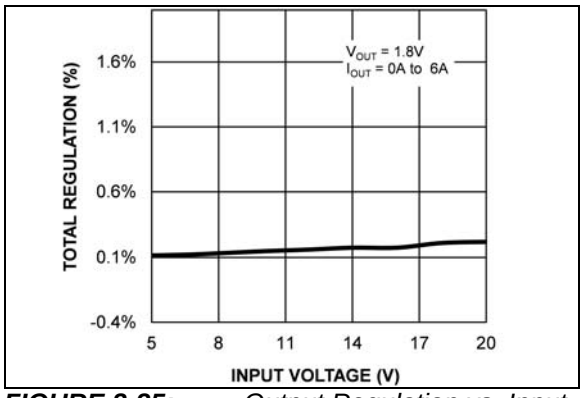


FIGURE 2-35: *Output Regulation vs. Input Voltage (MIC45116-2).*

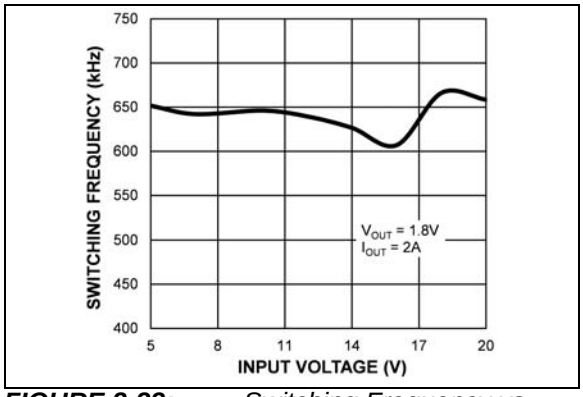


FIGURE 2-33: *Switching Frequency vs. Input Voltage (MIC45116-1).*

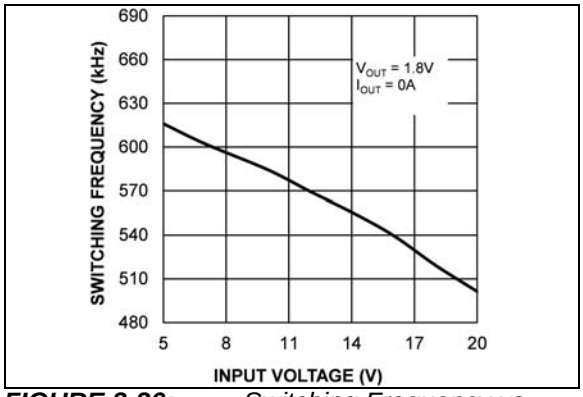


FIGURE 2-36: *Switching Frequency vs. Input Voltage (MIC45116-2).*

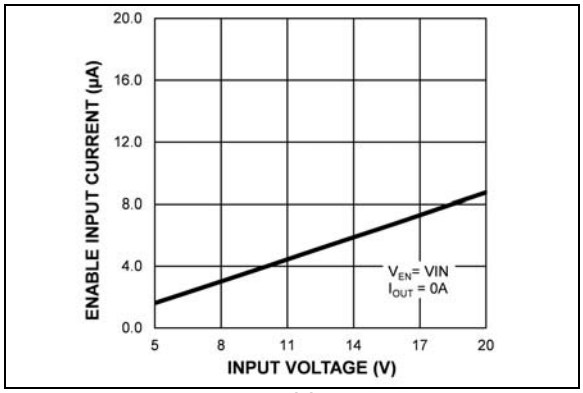


FIGURE 2-37: *Enable Input Current vs. Input Voltage.*

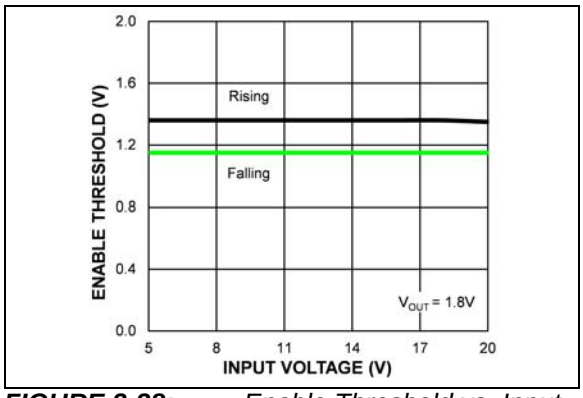


FIGURE 2-38: *Enable Threshold vs. Input Voltage.*

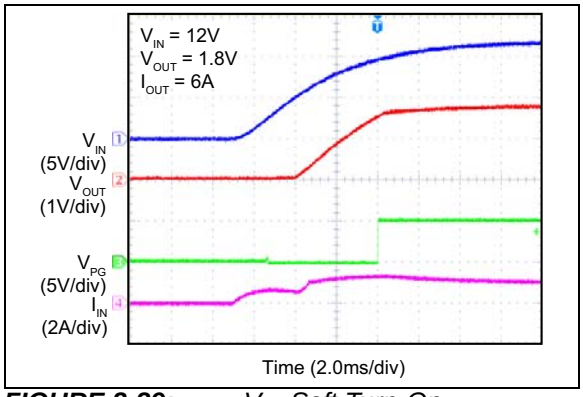


FIGURE 2-39: *V_{IN} Soft Turn-On.*

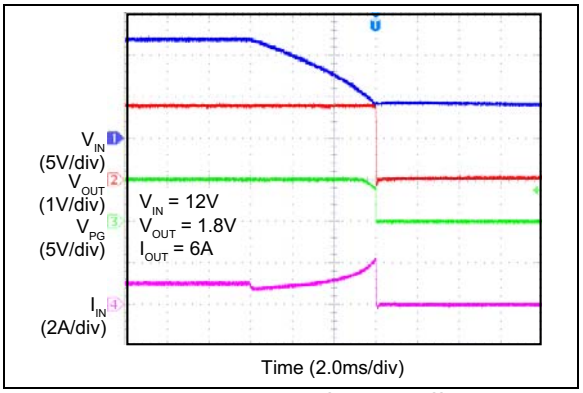


FIGURE 2-40: *V_{IN} Soft Turn-Off.*

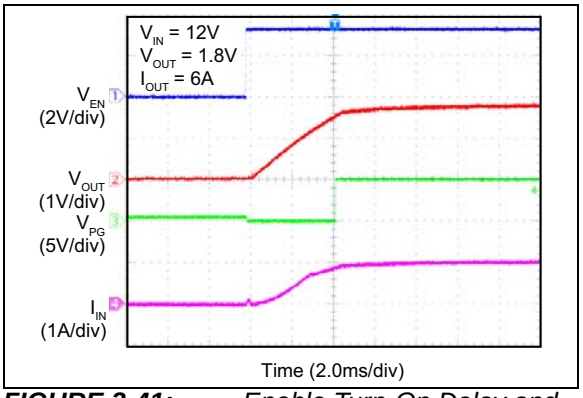


FIGURE 2-41: *Enable Turn-On Delay and Rise Time.*

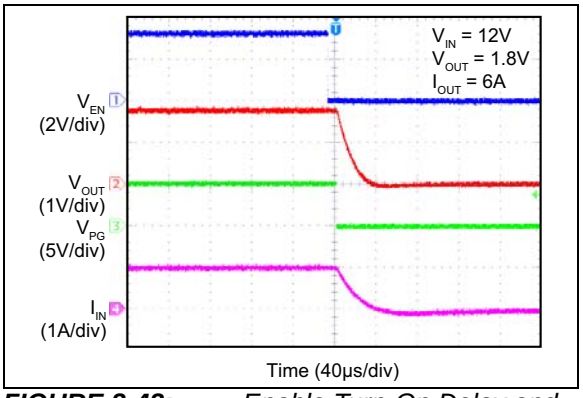


FIGURE 2-42: *Enable Turn-On Delay and Fall Time.*

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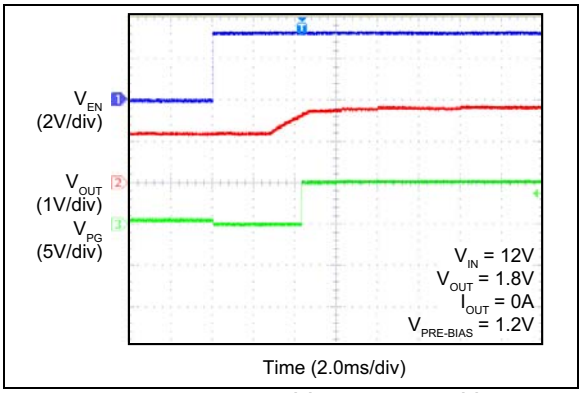


FIGURE 2-43: *Enable Start-Up with Pre-Biased Output.*

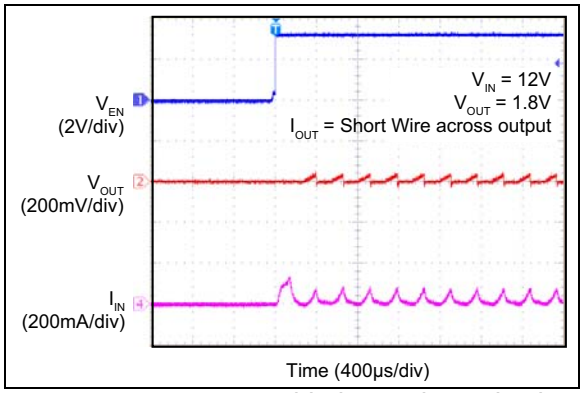


FIGURE 2-46: *Enabled Into Short-Circuit.*

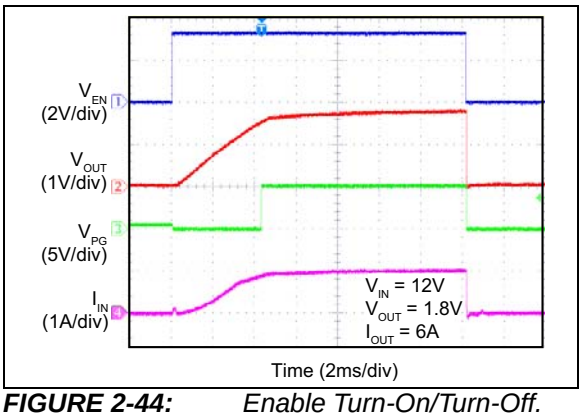


FIGURE 2-44: *Enable Turn-On/Turn-Off.*

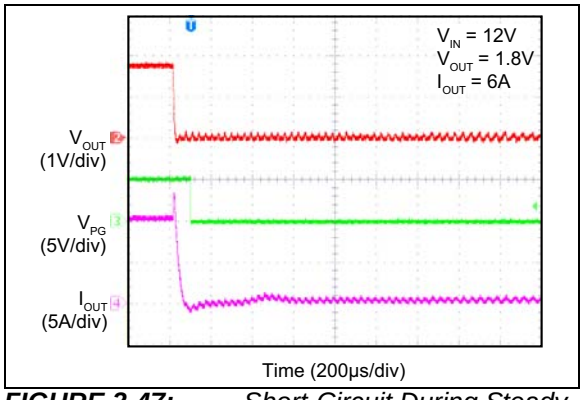


FIGURE 2-47: *Short-Circuit During Steady State.*

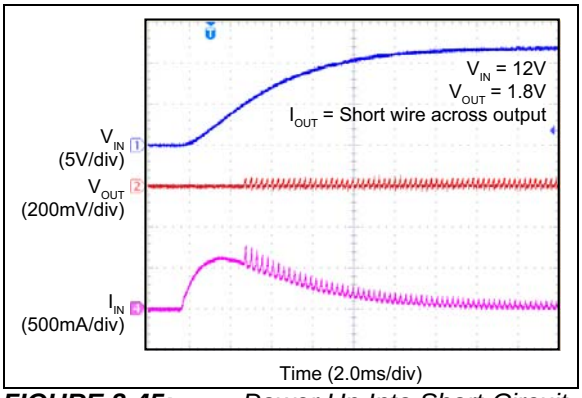


FIGURE 2-45: *Power Up Into Short-Circuit.*

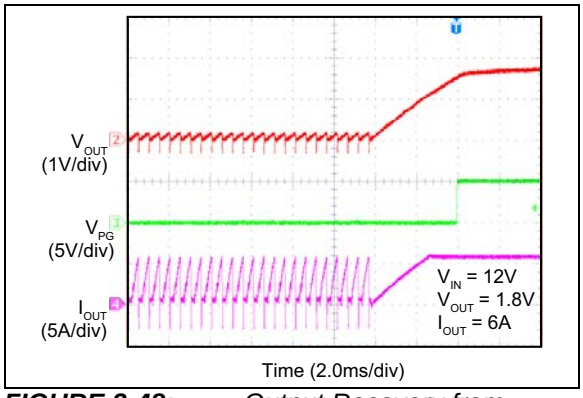


FIGURE 2-48: *Output Recovery from Short-Circuit.*

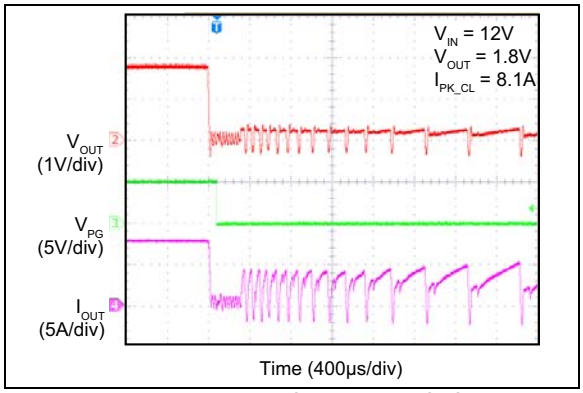


FIGURE 2-49: *Peak Current-Limit Threshold.*

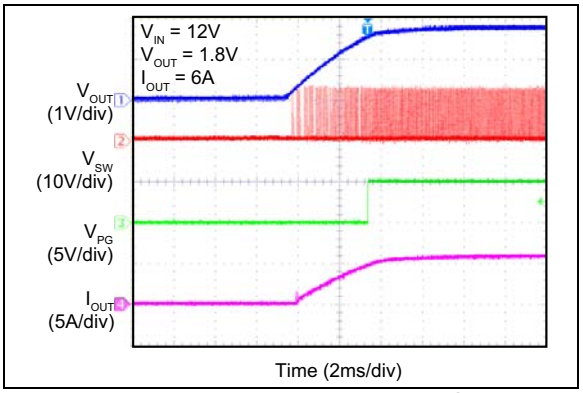


FIGURE 2-52: *Output Recovery from Thermal Shutdown.*

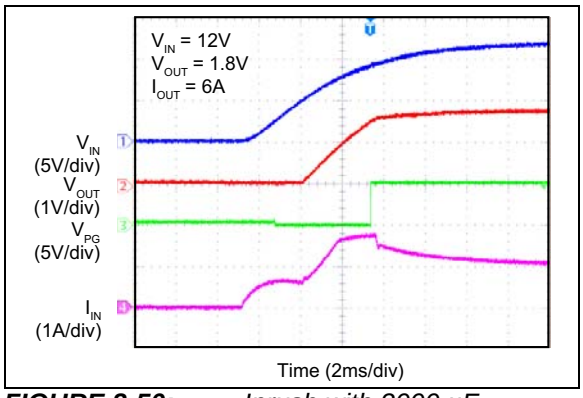


FIGURE 2-50: *Inrush with 3000 µF.*

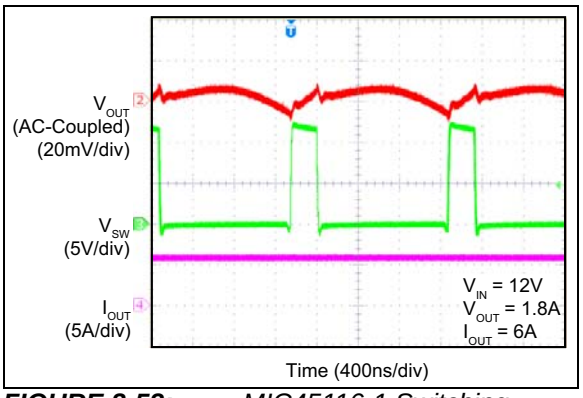


FIGURE 2-53: *MIC45116-1 Switching Waveforms (I_{OUT} = 6A).*

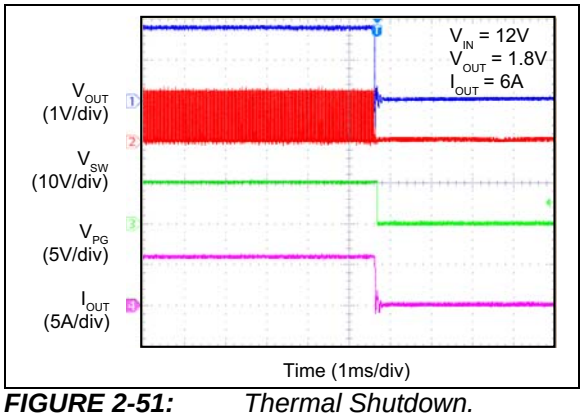


FIGURE 2-51: *Thermal Shutdown.*

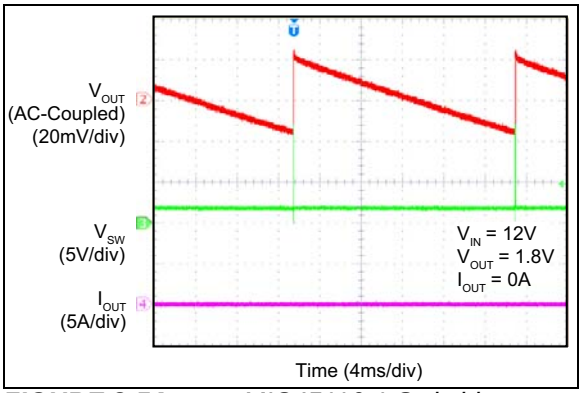


FIGURE 2-54: *MIC45116-1 Switching Waveforms (I_{OUT} = 0A).*

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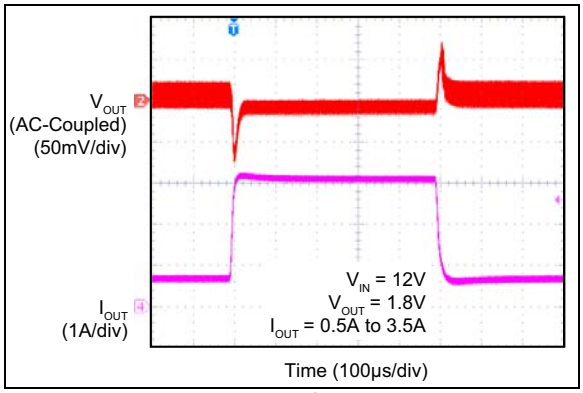


FIGURE 2-55: *Transient Response (MIC45116-1).*

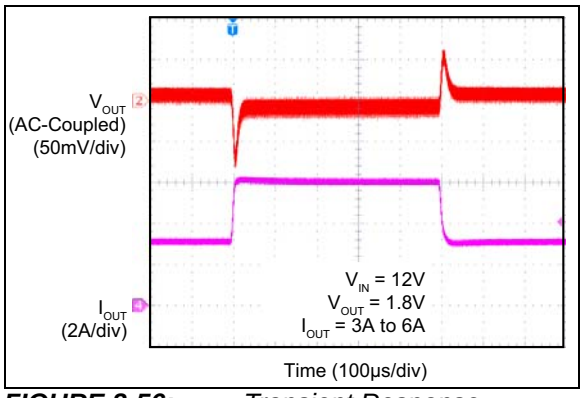


FIGURE 2-56: *Transient Response (MIC45116-2).*

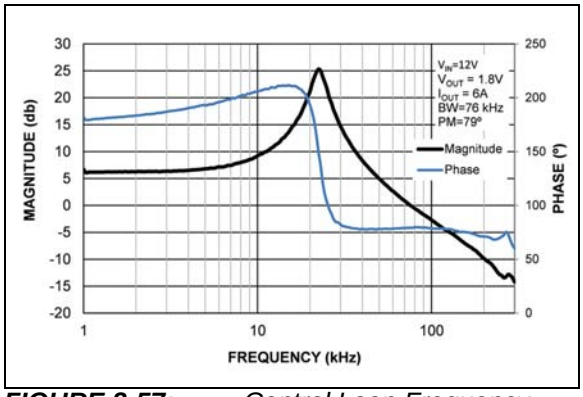


FIGURE 2-57: *Control Loop Frequency Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2, 52	PV_{IN}	Power Input Voltage. Connection to the drain of the internal high-side power MOSFET. Connect an input capacitor from PV_{IN} to P_{GND}.
4, 44	PV_{DD}	Supply input for the internal power MOSFET drivers. Connect PV_{DD} pins together. Do not leave floating.
5, 6	BST	Connection to the internal bootstrap circuitry and high-side power MOSFET drive circuitry. Connect the two BST pins together.
8-10, 48-51	SW	The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time.
12-21	V_{OUT}	Output Voltage. Connected to the internal inductor, the output capacitor should be connected from this pin to P_{GND} as close to the module as possible.
23-25, 27-30, 32-34, 40, 41	NC	Not internally connected.
26, 31, 35, 42, 45	P_{GND}	Power Ground. P_{GND} is the return path for the step-down power module power stage. The P_{GND} pin connects to the source of internal low-side power MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors. Signal Ground and Power Ground of MIC45116 are internally connected.
36	FB	Feedback. Input to the transconductance amplifier of the control loop. The FB pin is referenced to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage. Connect the bottom resistor from FB to system ground. External ripple injection (series R and C) can be connected between FB and SW.
37	PG	Power Good. Open-Drain Output. If used, connect to an external pull-up resistor of at least 10 kΩ between PG and the external bias voltage.
38	EN	Enable. A logic signal to enable or disable the step-down regulator module operation. The EN pin is TTL/CMOS compatible. Logic-high = enable, logic-low = disable or shutdown. EN pin has an internal 1 MΩ (typical) pull-down resistor to GND. Do not leave floating.
39	V_{IN}	Input for the internal linear regulator. Allows for split supplies to be used when there is an external bus voltage available. Connect to PV_{IN} for single supply operation. Bypass with a 0.1 µF capacitor from V_{IN} to P_{GND}.
43	$5V_{DD}$	Internal +5V Linear Regulator Output. Powered by V_{IN}, $5V_{DD}$ is the internal supply bus for the device. In the applications with V_{IN} < +5.5V, $5V_{DD}$ should be tied to V_{IN} to bypass the linear regulator.
47	I_{LIM}	Current Limit. Connect a resistor between I_{LIM} and SW to program the current limit.
3, 7, 11, 22, 46	KEEPOUT	Depopulated pin positions.
—	V_{OUT} ePad	V_{OUT} Exposed Pad. Internally connected to V_{OUT} pins. Please see the PCB Layout Guidelines section.
—	SW ePad	SW Exposed Pad. Internally connected to SW pins. Please see the PCB Layout Guidelines section.
—	P_{GND} ePAD	P_{GND} Exposed Pads. Please see the PCB Layout Guidelines section for the connection to the system Ground.

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4.0 FUNCTIONAL DESCRIPTION

The MIC45116 is an adaptive ON-time synchronous buck regulator module built for high-input voltage to low-output voltage conversion applications. The MIC45116 is designed to operate over a wide input voltage range, from 4.75V to 20V, and the output is adjustable with an external resistor divider. An adaptive ON-time control scheme is employed to obtain a constant switching frequency in steady state and to simplify the control compensation. Hiccup mode over-current protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown. The module has integrated switching FETs, inductor, bootstrap diode, and bypass capacitors.

4.1 Theory of Operation

Figure 4-1, in association with Equation 4-1, shows the output voltage is sensed by the MIC45116 feedback pin (FB) via the voltage divider R_{FB1} and R_{FB2} and compared to a 0.8V reference voltage (V_{REF}) at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases, and the amplifier output falls below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the Fixed t_{ON} Estimator circuitry:

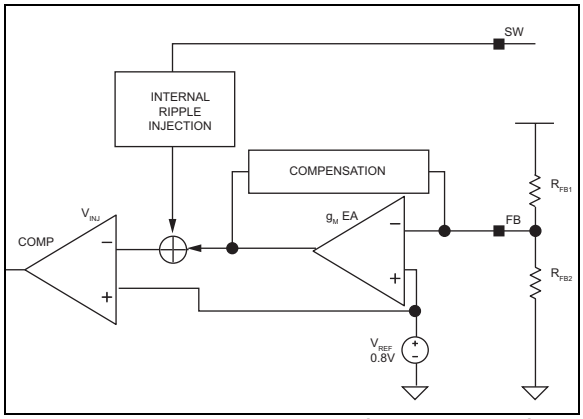


FIGURE 4-1: *Output Voltage Sense via FB Pin.*

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT}	Output Voltage
V_{IN}	Power Stage Input Voltage
f_{SW}	Switching Frequency

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the gm amplifier falls below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 250 ns, the MIC45116 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy in the internal boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 250 ns $t_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{250ns}{t_S}$$

Where:

t_S	$1/f_{SW}$

It is not recommended to use MIC45116 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC45116 during steady state operation. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 4-2 shows the MIC45116 control loop timing during steady-state operation. During steady-state, the gm amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

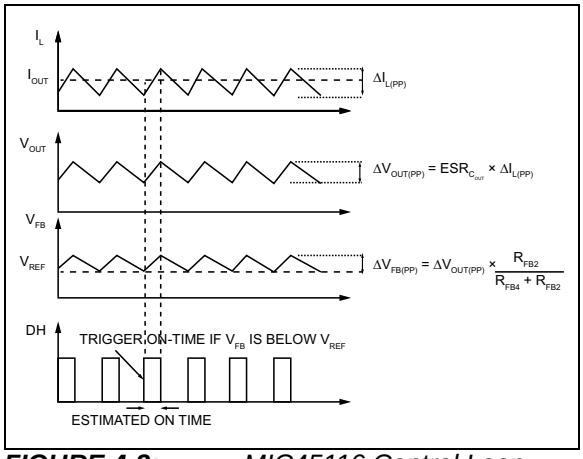


FIGURE 4-2: *MIC45116 Control Loop Timing.*

Figure 4-3 shows the operation of the MIC45116 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(MIN)}$ is generated to charge the bootstrap capacitor (C_{BST}) since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small. Note that the instantaneous switching frequency during load transient remains bounded and cannot increase arbitrarily. The minimum period is limited by t_{ON} + $t_{OFF(MIN)}$. Because the variation in V_{OUT} is relatively limited during load transient, t_{ON} stays virtually close to its steady-state value.

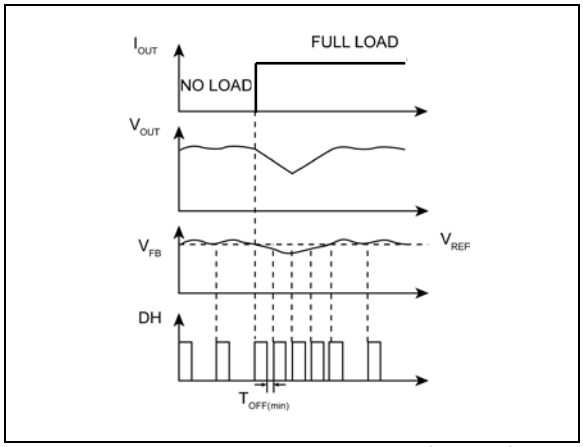


FIGURE 4-3: *MIC45116 Load Transient Response.*

Unlike true current-mode control, the MIC45116 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC45116 feedback voltage ripple should be in phase with the inductor current ripple and is large enough to be sensed by the gm amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV over full input voltage range. If a low ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the gm amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the Ripple Injection subsection in the Application Information section for more details about the ripple injection technique.

4.2 Discontinuous Mode (MIC45116-1 Only)

In continuous mode, the inductor current is always greater than zero; however, at light loads, the MIC45116-1 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4-4. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current as the switching frequency is reduced. The MIC45116-1 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC45116-1 has a zero crossing comparator (Z_C) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC45116-1 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC45116-1 goes into discontinuous mode, both low driver (DL) and high driver (DH) are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4-4 shows the control loop timing in discontinuous mode.

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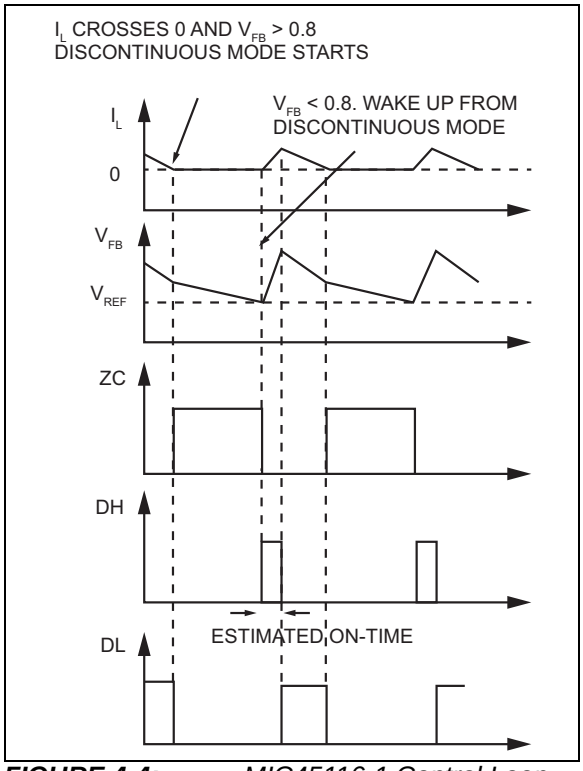


FIGURE 4-4: *MIC45116-1 Control Loop (Discontinuous Mode).*

During discontinuous mode, the bias current of most circuits is substantially reduced. As a result, the total power supply current during discontinuous mode is only about 350 µA, allowing the MIC45116-1 to achieve high efficiency in light load applications.

4.3 Soft-Start

Soft-start reduces the input power supply surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up.

The MIC45116 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 3 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. PV_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

4.4 Current Limit

The MIC45116 uses the $R_{DS(ON)}$ of the low-side MOSFET and external resistor connected from the I_{LIM} pin to SW node to set the current limit.

In each switching cycle of the MIC45116, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage V_{LIM} is compared with the power ground (P_{GND}) after a blanking time of 150 ns. In this way the drop voltage over the resistor R26 (V_{CL}) is compared with the drop over the bottom FET generating the short current limit. The small capacitor (C16) connected from the I_{LIM} pin to P_{GND} filters the switching node ringing during the off-time allowing a better short-limit measurement. The time constant created by R26 and C16 should be much less than the minimum off time.

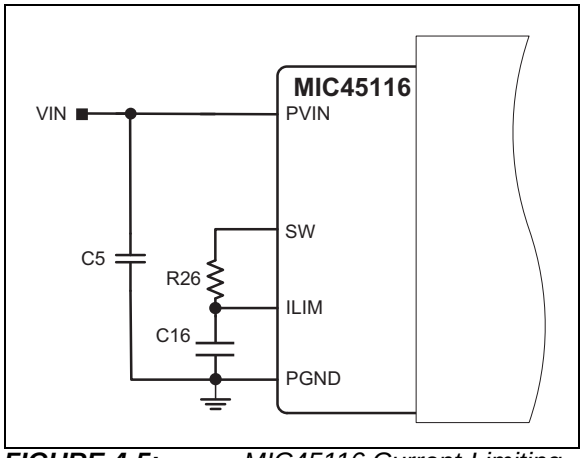


FIGURE 4-5: *MIC45116 Current-Limiting Circuit.*

The V_{CL} drop allows short-limit programming based on the value of the resistor (R26). If the absolute value of the voltage drop on the bottom FET becomes greater than V_{CL}, and the VI_{LIM} falls below P_{GND}, an overcurrent is triggered causing the IC to enter hiccup mode. The hiccup sequence including the soft-start reduces the stress on the switching FETs and protects the load and supply for severe short conditions.

The short-circuit current limit can be programmed by using Equation 4-3.

EQUATION 4-3:

$$R26 = \frac{(I_{CLIM} + \Delta I_{L(PP)} \times 0.5 - 0.1) \times R_{DS(ON)} + V_{CL}}{I_{CL}}$$

Where:

I_{CLIM}	Desired current limit.
$R_{DS(ON)}$	On-resistance of low-side power MOSFET, 16 mΩ typically.
V_{CL}	Current-limit threshold (typical absolute value is 14 mV).
I_{CL}	Current-limit source current (typical value is 80 µA).
$\Delta I_{L(PP)}$	Inductor current peak-to-peak, since the inductor is integrated, use Equation 4-4 to calculate the inductor ripple current.

The peak-to-peak inductor current ripple is:

EQUATION 4-4:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The MIC45116 has a 1.0 µH inductor integrated into the module. In case of a hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft-start is under the folded short limit; otherwise the supply will go in hiccup mode and may not finish the soft-start successfully.

With R26 = 1.62 kΩ and C16 = 15 pF, the typical output current limit is 8A.

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5.0 APPLICATION INFORMATION

5.1 Output Capacitor Selection

The type of the output capacitor is usually determined by the application and its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are MLCC, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The MIC45116 requires ripple injection and the output capacitor ESR affects the control loop from a stability point of view.

Equation 5-1 shows how the maximum value of ESR is calculated.

EQUATION 5-1:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$	Peak-to-peak output voltage ripple
$\Delta I_{L(PP)}$	Peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-2:

EQUATION 5-2:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{COUT}\right)^2}$$

Where:

D	Duty cycle
C_{OUT}	Output capacitance value
f_{SW}	Switching frequency

As described in the Theory of Operation subsection in the Functional Description, the MIC45116 requires at least 20 mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to Ripple Injection subsection for more details.

The output capacitor RMS current is calculated in Equation 5-3:

EQUATION 5-3:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-4:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.2 Input Capacitor Selection

The input capacitor for the power stage input PV_{IN} should be selected for ripple current rating and voltage rating.

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-5:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-6:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

The general rule is to pick the capacitor with a ripple current rating equal to or greater than the calculated worst-case RMS capacitor current.

Equation 5-7 should be used to calculate the input capacitor. Also it is recommended to keep some margin on the calculated value:

EQUATION 5-7:

$$C_{IN} \approx \frac{I_{OUT(MAX)} \times (1 - D)}{f_{SW} \times dV}$$

Where:

dV	Input ripple
f_{SW}	Switching frequency

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5.3 Output Voltage Setting Components

The MIC45116 requires two resistors to set the output voltage as shown in Figure 5-1.

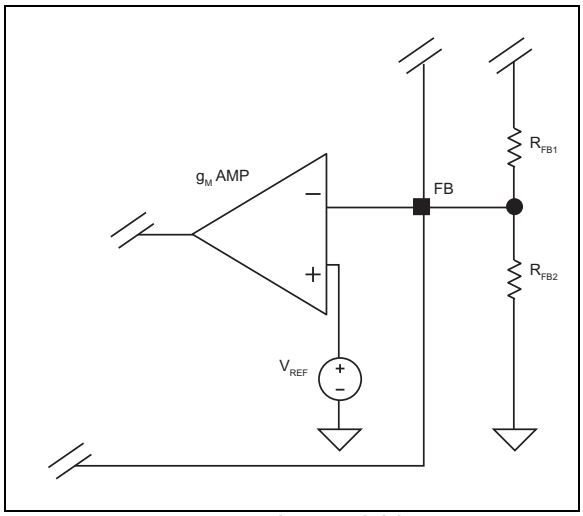


FIGURE 5-1: *Voltage Divider Configuration.*

The output voltage is determined by Equation 5-8:

EQUATION 5-8:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Where:

V_{FB} 0.8V

A typical value of R_{FB1} used on the standard evaluation board is 10 kΩ. If R_{FB1} is too large, it may allow noise to be introduced into the voltage feedback loop. If R_{FB1} is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_{FB1} is selected, R_{FB2} can be calculated using Equation 5-9:

EQUATION 5-9:

$$R_{FB2} = \frac{V_{FB} \times R_{FB1}}{V_{OUT} - V_{FB}}$$

For fixed R_{FB1} = 10 kΩ, output voltage can be selected by R_{FB2}. Table 5-1 provides R_{FB2} values for some common output voltages.

TABLE 5-1: V_{OUT} PROGRAMMING RESISTOR LOOK-UP

R_{FB2}	V_{OUT}
OPEN	0.8V
40.2 kΩ	1.0V
20 kΩ	1.2V
11.5 kΩ	1.5V
8.06 kΩ	1.8V
4.75 kΩ	2.5V
3.24 kΩ	3.3V
1.91 kΩ	5.0V

5.4 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC45116 g_m amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally too small to provide enough ripple amplitude at the FB pin and this issue is more visible in lower output voltage applications. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the MIC45116 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

- Enough ripple at the feedback voltage due to the large ESR of the output capacitors (Figure 5-2). The converter is stable without any ripple injection.

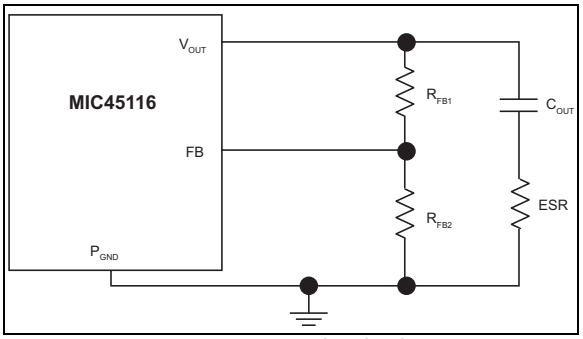


FIGURE 5-2: *Enough Ripple at FB.*

The feedback voltage ripple is:

EQUATION 5-10:

$$\Delta V_{FB(PP)} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$ Peak-to-Peak Value of the Inductor Current Ripple

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- Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

  The output voltage ripple is fed into the FB pin through a feed-forward capacitor, C_{FF} in this situation, as shown in Figure 5-3. The typical C_{FF} value is between 1 nF and 100 nF.

EQUATION 5-11:

$$\Delta V_{FB(PP)} = ESR_{COUT} \times \Delta I_{L(PP)}$$

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple.

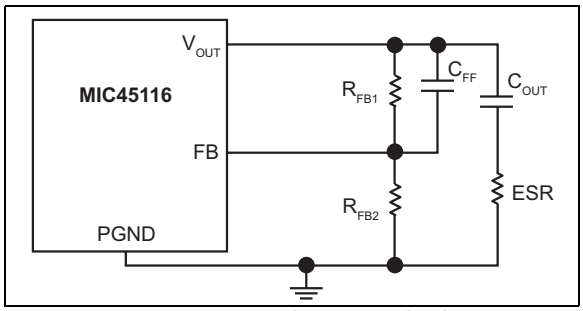


FIGURE 5-3: *Inadequate Ripple at FB.*

- Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors, such is the case with ceramic output capacitors.

  In this situation, the V_{FB} ripple waveform needs to be generated by injecting suitable signal. A series RC network between the SW pin and FB pin, R_{INJ} and C_{INJ} as shown in Figure 5-4 injects a square-wave current waveform into the FB pin, which, by means of integration across the capacitor (C_{FF}), generates an appropriate sawtooth FB ripple waveform.

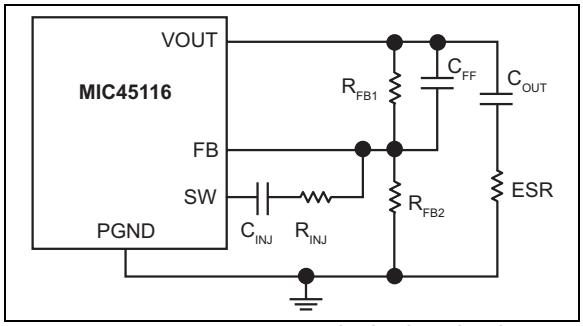


FIGURE 5-4: *External Ripple Injection Circuit at FB.*

The injected ripple is calculated via:

EQUATION 5-12:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:

V_{IN}	Power stage input voltage
D	Duty cycle
f_{SW}	Switching frequency
τ	$(R_{FB1}//R_{FB2}//R_{INJ}) \times C_{FF}$

EQUATION 5-13:

$$K_{div} = \frac{R_{FB1}//R_{FB2}}{R_{INJ} + R_{FB1}//R_{FB2}}$$

Where:

R_{INJ}	20 kΩ

In Equation 5-13 and Equation 5-14, it is assumed that the time constant associated with C_{FF} must be much greater than the switching period:

EQUATION 5-14:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors R_{FB1} and R_{FB2} are in the kΩ range, a C_{FF} of 1 nF to 100 nF can easily satisfy the large time constant requirements.

5.5 Thermal Measurements and Safe Operating Area (SOA)

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36-gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

The safe operating area (SOA) of the MIC45116 is shown in Figure 10 and Figure 11. These thermal measurements were taken on MIC45116 evaluation board with no air flow. Since the MIC45116 is an entire system comprised of switching regulator controller, MOSFETs, and inductor, the part needs to be considered as a system. The SOA curves will give guidance to reasonable use of the MIC45116.

SOA curves should only be used as a point of reference. SOA data was acquired using the MIC45116 evaluation board. Thermal performance depends on the PCB layout, board size, copper thickness, number of thermal vias, and actual airflow.

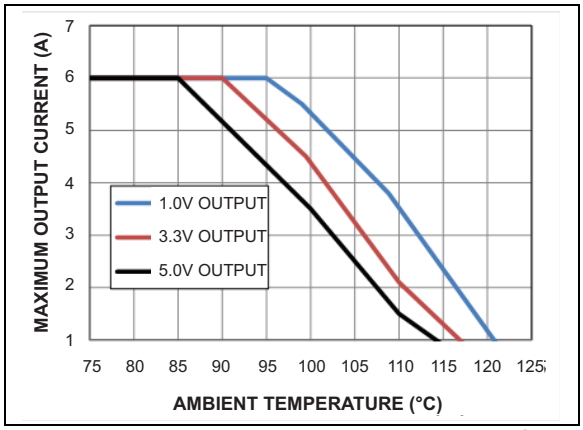


FIGURE 5-5: *MIC45116 Power Derating vs. Output Voltage with 12V Input with No Airflow.*

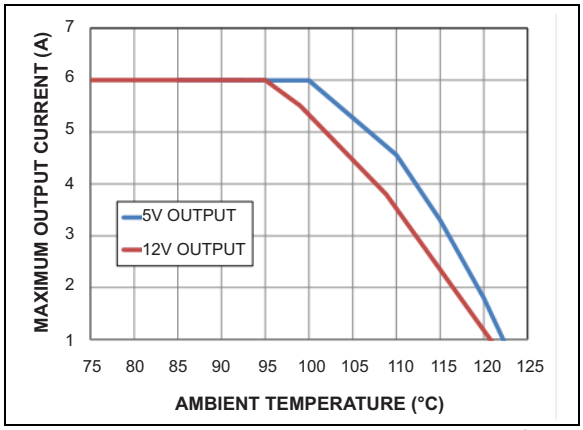


FIGURE 5-6: *MIC45116 Power Derating vs. Input Voltage with 1.0V Output with No Airflow.*

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6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The following guidelines should be followed to ensure proper operation of the MIC45116 module.

6.1 Module

- Place the module close to the point-of-load.
- Use wide polygons to route the input and output power lines.
- Follow the instructions in Package Information and Recommended Landing Pattern to connect the Ground exposed pads to system ground planes.

6.2 Input Capacitor

- Place the input capacitors on the same side of the board and as close to the module as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the ceramic input capacitor.
- If a non-ceramic input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage.
- In “Hot-Plug” applications, an electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied. If hot-plugging is the normal operation of the system, using an appropriate hot-swap IC is recommended.

6.3 RC Snubber (Optional)

- Depending on the operating conditions, a RC snubber can be used. Place the RC and as close to the SW pin as possible if needed. Placement of the snubber on the same side as module is preferred.

6.4 SW Node

- Do not route any digital lines underneath or close to the SW node.
- Keep the switch node (SW) away from the feedback (FB) pin.

6.5 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

Figure 6-1 is optimized from a small form factor point of view shows top and bottom layer of a four layer PCB. It is recommended to use mid layer 1 as a continuous ground plane.

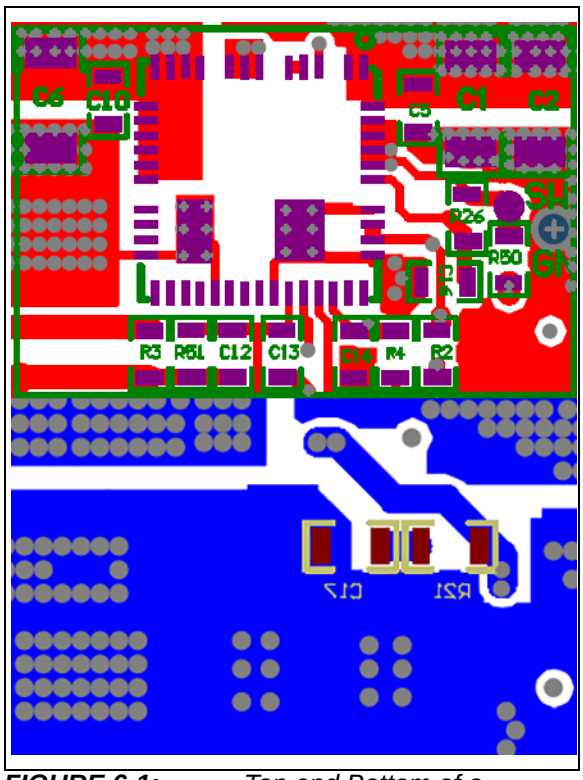


FIGURE 6-1: *Top and Bottom of a Four-Layer Board.*

7.0 SIMPLIFIED PCB DESIGN RECOMMENDATIONS

7.1 Periphery I/O Pad Layout and Large Pad for Exposed Heatsink

The board design should begin with copper/metal pads that sit beneath the periphery leads of a mounted QFN. The board pads should extend outside the QFN package edge a distance of approximately 0.20 mm per side:

EQUATION 7-1:

$$TotalPadLength = 8mm + (0.20mm \times 2sides) = 8.4mm$$

After completion of the periphery pad design, the larger exposed pads will be designed to create the mounting surface of the QFN exposed heatsink. The primary transfer of heat out of the QFN will be directly through the bottom surface of the exposed heatsink. To aid in the transfer of generated heat into the PCB, the use of an array of plated through-hole vias beneath the mounted part is recommended. The typical via hole diameter is 0.30 mm to 0.35 mm, with center-to-center pitch of 0.80 mm to 1.20 mm.

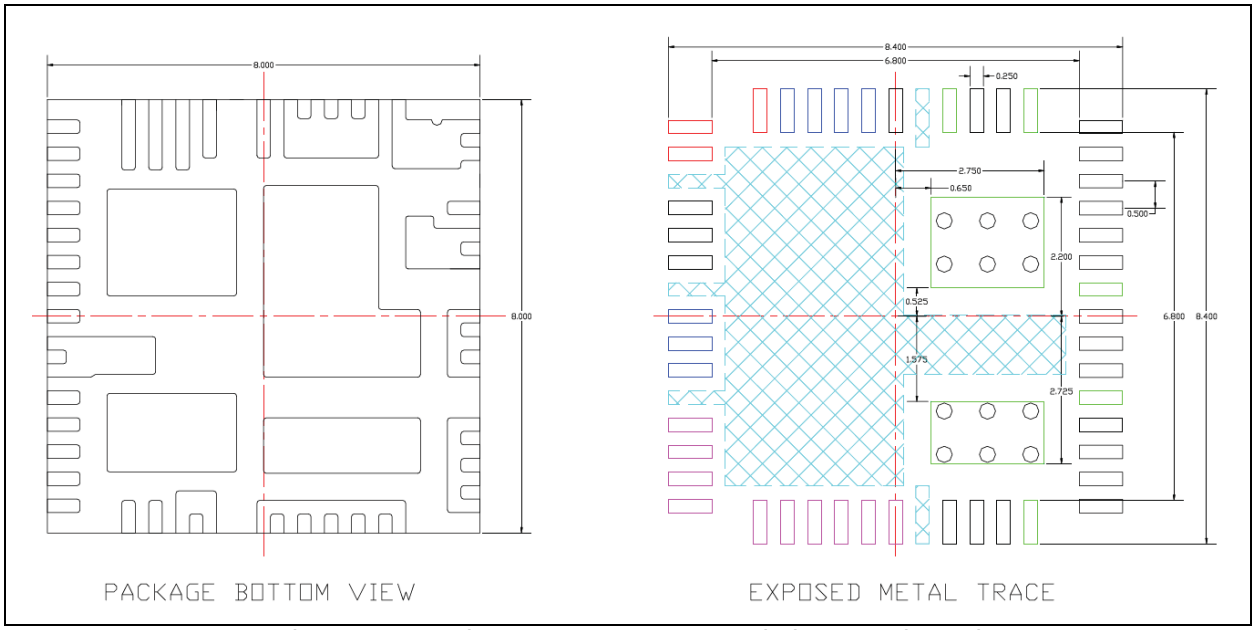


FIGURE 7-1: *Package Bottom View vs. PCB Recommended Exposed Metal Trace.*

Please note the exposed metal trace is a “mirror image” of the package bottom view.

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7.2 Solder Paste Stencil Design (Recommended Stencil Thickness = 112.5 ±12.5 µm)

The solder stencil aperture openings should be smaller than the periphery or large PCB exposed pads to reduce any chance of build-up of excess solder at the large exposed pad area which can result to solder bridging.

The suggested reduction of the stencil aperture opening is typically 0.20 mm smaller than exposed metal trace.

Please note that a critical requirement is to not duplicate land pattern of the exposed metal trace as solder stencil opening because the design and dimension values are different.

Cyan-colored shaded pad areas indicate exposed trace keep-out area in Figure 7-2 and Figure 7-3.

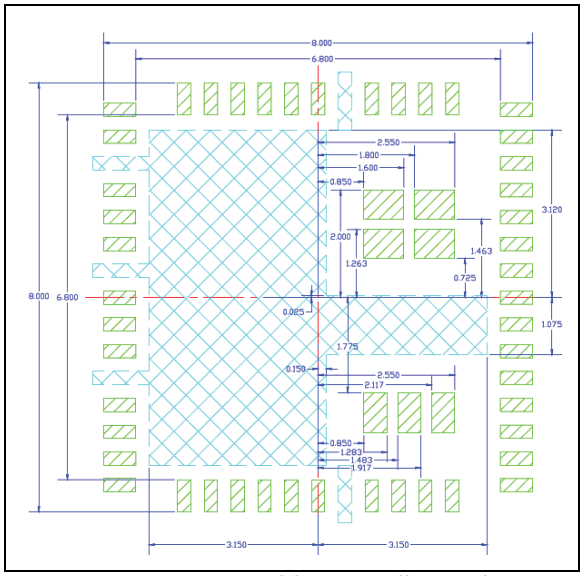


FIGURE 7-2: *Solder Stencil Opening.*

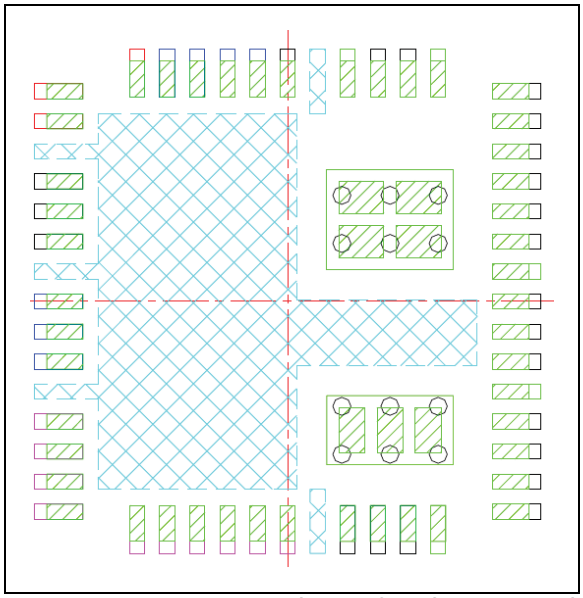
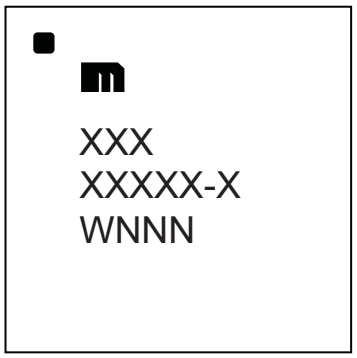


FIGURE 7-3: *Stack-Up of Pad Layout and Solder Paste Stencil.*

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

52-Pin QFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) symbol may not be to scale.	

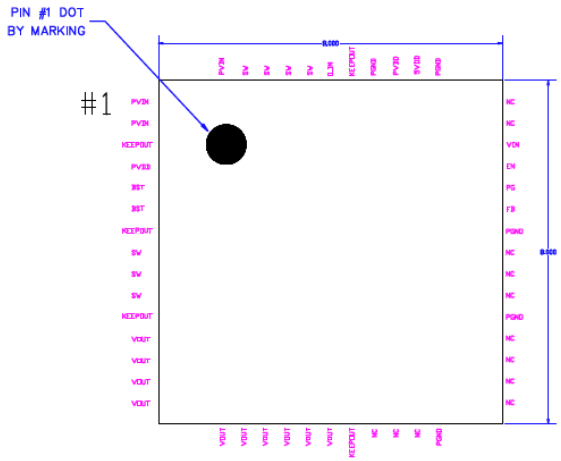
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52-Lead H3QFN 8 mm x 8 mm Package Outline and Recommended Land Pattern

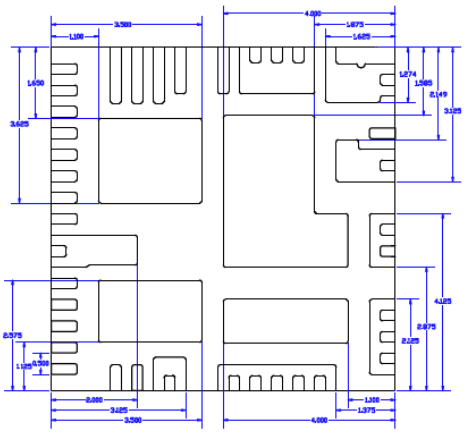
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TITLE
52 LEAD H3QFN 8x8mm PACKAGE (Module) OUTLINE & RECOMMENDED LAND PATTERN

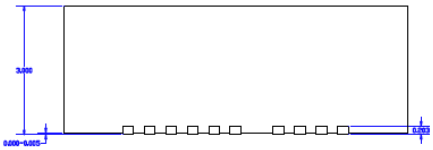
DRAWING #	H3QFN88-52LD-PL-3	**UNIT**	MM
Lead Frame	Copper	**Lead Finish**	Matte Tin



Top View
NOTE: 1, 2, 3



Bottom View
NOTE: 1, 2, 3



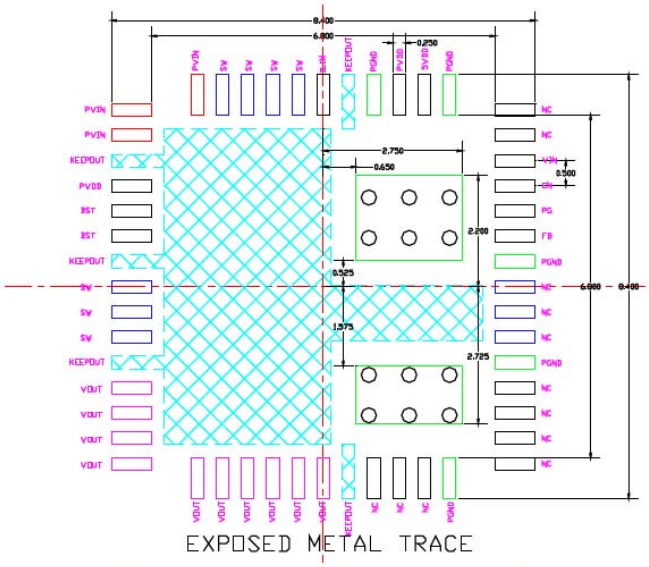
Side View
NOTE: 1, 2, 3

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

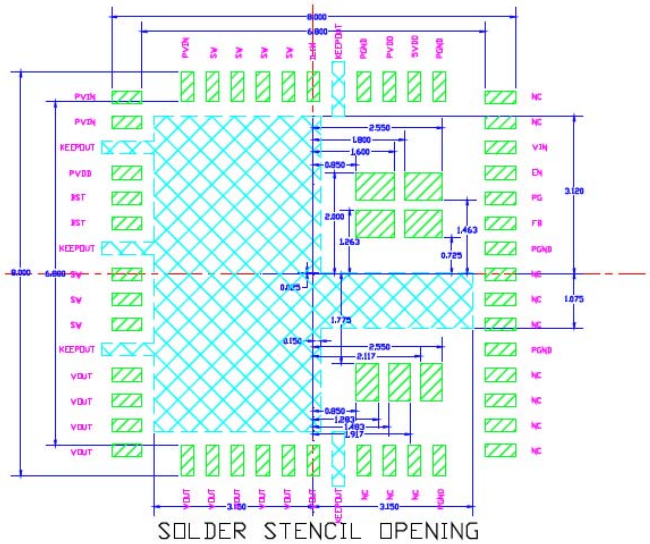
Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP



EXPOSED METAL TRACE



SOLDER STENCIL OPENING

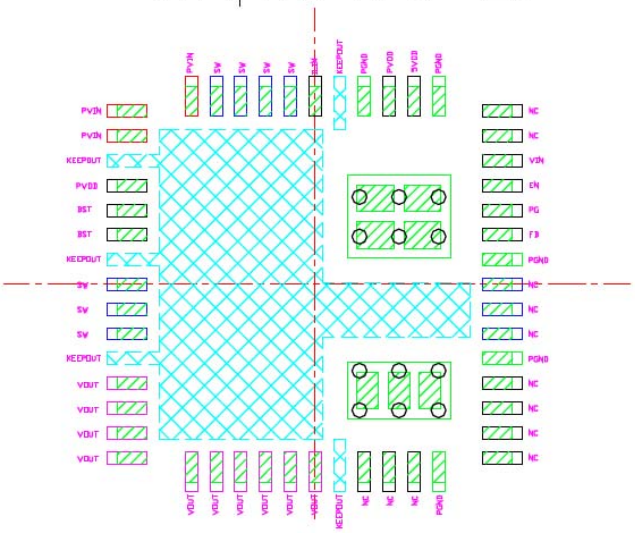
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Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Recommended Land Pattern

NOTE: 4, 5, 6

Simplified LP

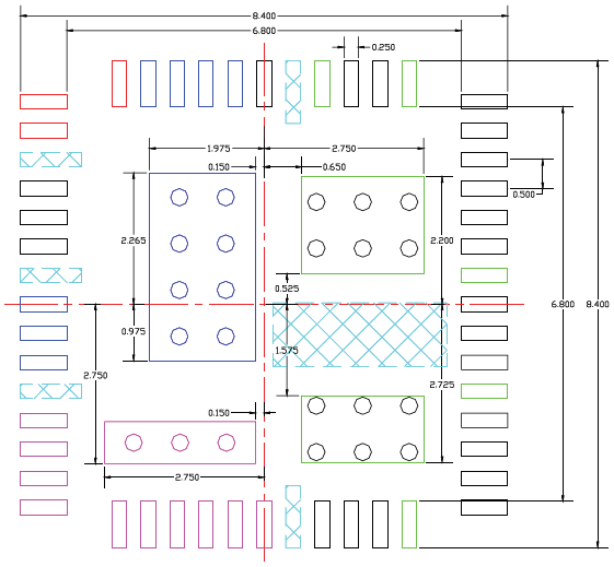


STACKED UP

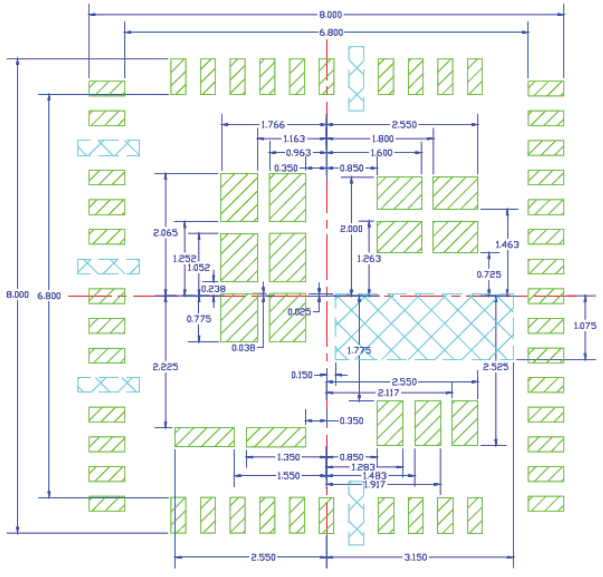
NOTE:

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. BLACK CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED SHADED PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.

Thermally Enhanced Land Pattern

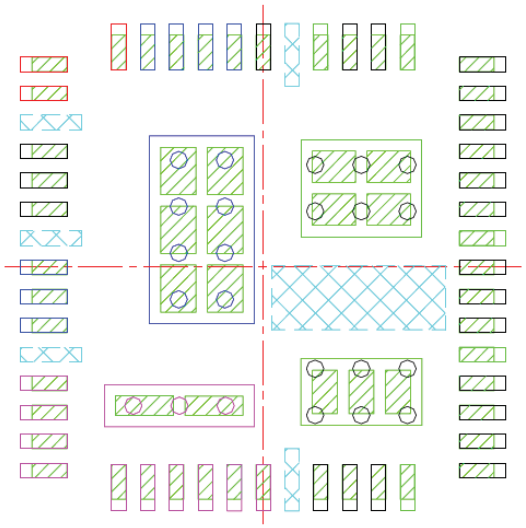


EXPOSED METAL TRACE



SOLDER STENCIL OPENING

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STACKED UP

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. BLACK CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, RECOMMENDED SIZE IS 0.30-0.35mm, AT 0.80mm PITCH & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
6. CYAN COLORED SHADED PAD REPRESENT EXPOSED TRACE KEEP OUT AREA.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (August 2016)

- Converted Micrel document MIC45116 to Microchip data sheet DS20005571A.
- Minor text changes throughout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	X	X	XX	–	XX
Device		Features	Temperature	Package		Media Type

Device:	MIC45116:	20V/6A DC/DC Power Module	
Features:	1	=	HyperLight Load
	2	=	Hyper Speed Control
Temperature:	Y	=	–40°C to +125°C
Package:	MP	=	52-Pin 8 mm x 8 mm x 3 mm QFN
Media Type:	TR	=	1,500/Reel

Examples:

a) MIC45116-1YMP-TR: 20V/6A DC/DC Power Module, HyperLight Load, –40°C to +125°C Temp. Range, 52-Pin QFN, 1,500/Reel

b) MIC45116-2YMP-TR: 20V/6A DC/DC Power Module, Hyper Speed Control, –40°C to +125°C Temp. Range, 52-Pin QFN 1,500/Reel

NOTES:

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