MIC28511

60V_{IN}, 3A Synchronous Buck Regulator

Features

- 4.6V to 60V Operating Input Voltage Supply
- Up to 3A Output Current
- Integrated High-Side and Low-Side N-Channel MOSFETs
- HyperLight Load (MIC28511-1) and Hyper Speed Control (MIC28511-2) Architecture
- Enable Input and Power Good (PGOOD) Output
- Programmable Current-Limit and Foldback "Hiccup" Mode Short-Circuit Protection
- Built-In 5V Regulator for Single-Supply Operation
- Adjustable 200 kHz to 680 kHz Switching Frequency
- Fixed 5 ms Soft-Start
- Internal Compensation and Thermal Shutdown
- Thermally-Enhanced 24-Pin 3 mm x 4 mm FQFN Package
- –40°C to +125°C Junction Temperature Range

Applications

- Industrial Power Supplies
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage Single-Board Systems

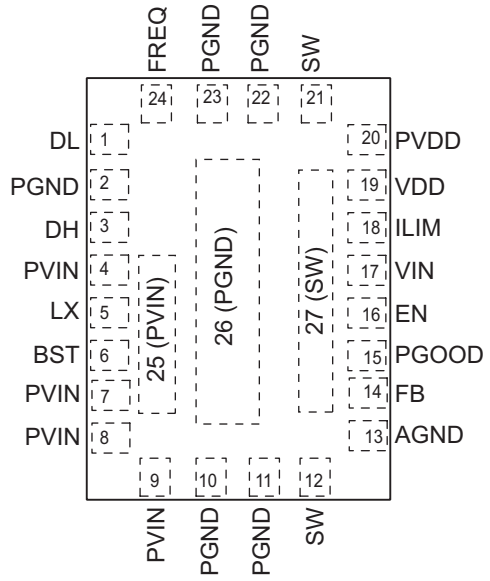
General Description

The MIC28511 is a synchronous step-down switching regulator with internal power switches capable of providing up to 3A output current from a wide input supply range from 4.6V to 60V. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%. A constant switching frequency can be programmed from 200 kHz to 680 kHz. The Hyper Speed Control® and HyperLight Load® architectures of the MIC28511 allow for high V_{IN} (low V_{OUT}) operation and ultra-fast transient response while reducing the required output capacitance and providing very good light-load efficiency.

The MIC28511 offers a full suite of features to ensure protection under fault conditions. These include undervoltage lockout to ensure proper operation under power sag conditions, internal soft-start to reduce inrush current, foldback current-limit, "hiccup" mode short-circuit protection and thermal shutdown.

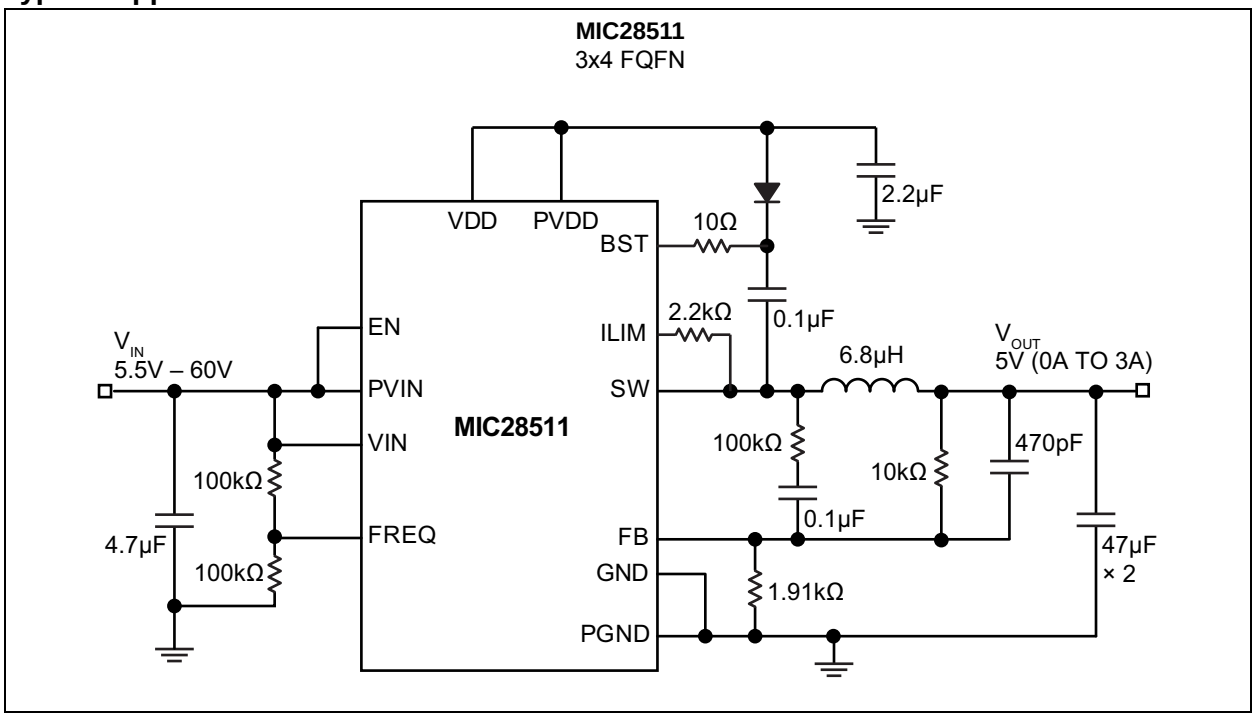
Package Type

MIC28511
24-Pin 3 mm x 4 mm FQFN (FL)

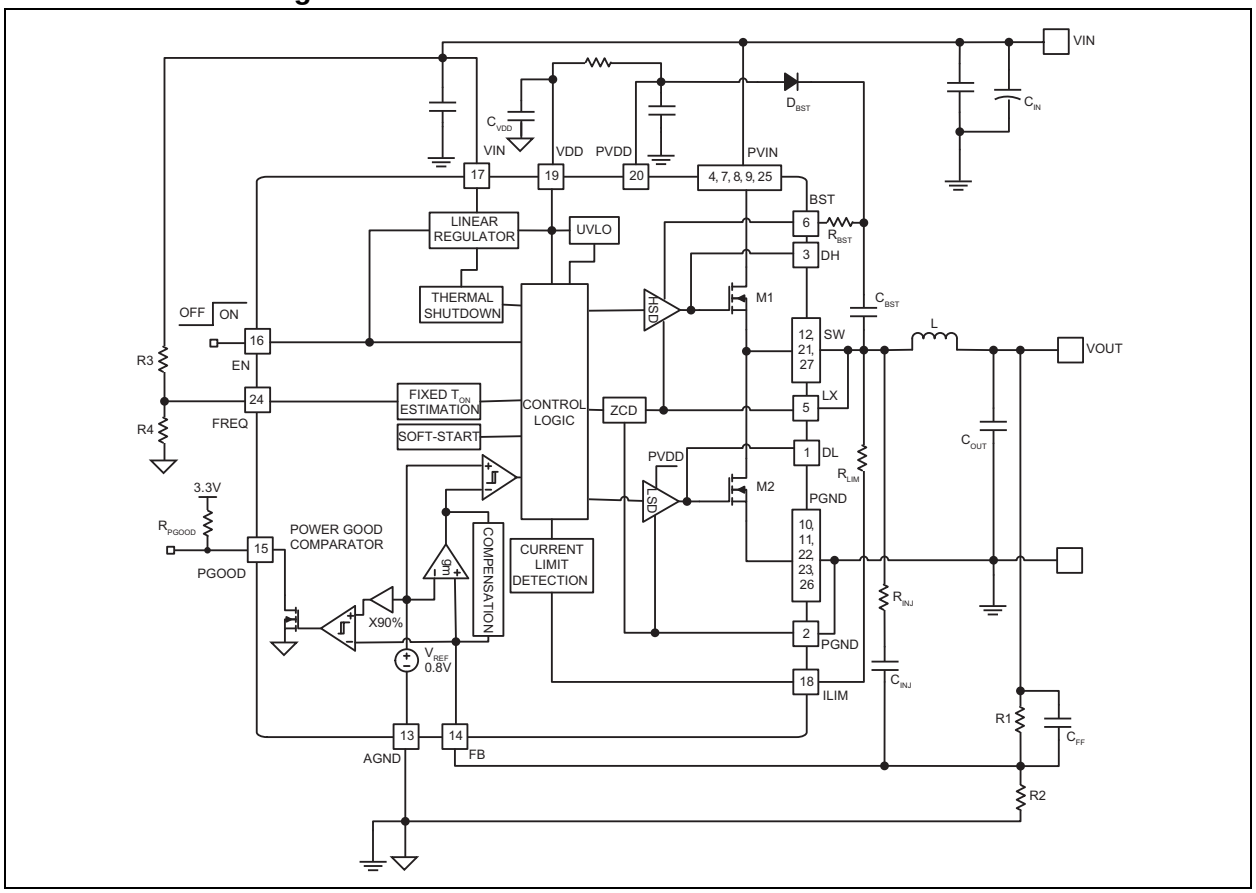


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Typical Application Circuit



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PV_{IN}, V_{IN} to PGND ..... –0.3V to +65V
V_{DD}, P_{VDD} to PGND ..... –0.3V to +6V
V_{BST} to V_{SW}, V_{LX} ..... –0.3V to +6V
V_{BST} to PGND ..... –0.3V to (V_{IN} + 6V
V_{SW} to PGND ..... –0.3V to (V_{IN} + 0.3V)
V_{LX}, V_{FB}, V_{PG}, V_{FREQ}, V_{ILIM}, V_{EN} to AGND ..... –0.3V to (V_{DD} + 0.3V)
PGND to AGND ..... –0.3V to +0.3V
ESD Rating(1) (HBM) ..... 1.5 kV
ESD Rating(1) (MM) 150V

Operating Ratings ‡

Supply Voltage (PV_{IN}, V_{IN}) ..... +4.5V to +60V
Enable Input (V_{EN}) ..... 0V to V_{IN}
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN} ..... 0V to V_{IN}

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 12V, T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. (Note 1).					
Parameters	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Input					
Input Voltage Range (PV_{IN}, V_{IN})	**4.6**	—	**60**	V	—
Quiescent Supply Current	—	0.4	**0.75**	mA	V_{FB} = 1.5V (MIC28511-1)
	—	0.7	**1.5**		V_{FB} = 1.5V (MIC28511-2)
Shutdown Supply Current	—	0.1	**10**	µA	SW unconnected, V_{EN} = 0V
V_{DD} Supply					
V_{DD} Output Voltage	**4.8**	5.2	**5.4**	V	V_{IN} = 7V to 60V, I_{VDD} = 10 mA
V_{DD} UVLO Threshold	**3.8**	4.2	**4.6**	V	V_{DD} rising
V_{DD} UVLO Hysteresis	—	400	—	mV	—
Load Regulation at 40 mA	0.6	2	4.0	%	—
Reference					
Feedback Reference Voltage	**0.792**	0.8	**0.808**	V	0°C ≤ T_J ≤ +85°C (±1.0%)
	0.784	0.8	**0.816**		–40°C ≤ T_J ≤ +125°C (±2%)
FB Bias Current	—	5	**500**	nA	V_{FB} = 0.8V
Enable Control					
EN Logic Level High	**1.8**	—	—	V	—
EN Logic Level Low	—	—	**0.6**		—
EN Hysteresis	—	200	—	mV	—
EN Bias Current	—	5	**40**	µA	V_{EN} = 12V
Oscillator					
Switching Frequency	**450**	680	**800**	kHz	V_{FREQ} = V_{IN}
	—	340	—		V_{FREQ} = 50% x V_{IN}
Maximum Duty Cycle	—	85	—	%	—
Minimum Duty Cycle	—	0	—		V_{FB} > 0.8V
Minimum Off-Time	110	200	270	ns	—
Internal MOSFET					
High-Side NMOS On-Resistance	—	51	—	mΩ	—
Low-Side NMOS On-Resistance	—	28	—		—
Short-Circuit Protection					
Current-Limit Threshold	–30	–14	0	mV	V_{FB} = 0.79V
Short-Circuit Threshold	–27	–7	8		V_{FB} = 0V
Current-Limit Source Current	50	70	90	µA	V_{FB} = 0.79V
Short-Circuit Source Current	25	36	43		V_{FB} = 0V

Note 1: Specification for packaged product only.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 12V, T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. (**Note 1**).					
Parameters	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Leakage					
SW, BST Leakage Current	—	—	50	µA	—
Power Good (PGOOD)					
PGOOD Threshold Voltage	**85**	90	**95**	%V_{OUT}	Sweep V_{FB} from low to high
PGOOD Hysteresis	—	6	—		Sweep V_{FB} from low to high
PGOOD Delay Time	—	100	—	µs	Sweep V_{FB} from low to high
PGOOD Low Voltage	—	70	**200**	mV	V_{FB} < 90% x V_{NOM}, I_{PGOOD} = 1 mA
Thermal Protection					
Overtemperature Shutdown	—	160	—	°C	T_J Rising
Overtemperature Shutdown Hysteresis	—	15	—	°C	—
Soft-Start					
Soft-Start Time	—	**5**	—	ms	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	–40	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Temperature	T_J	—	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance 3 mm x 4 mm FQFN-24LD	θ_{JA}	—	30	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

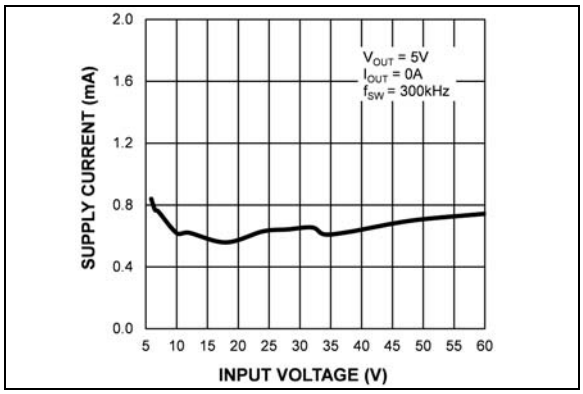


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Input Voltage (MIC28511-1).*

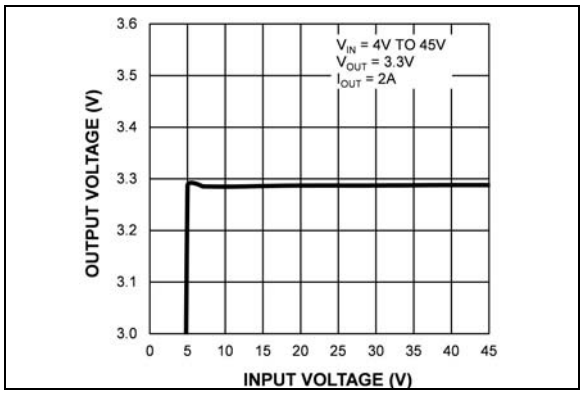


FIGURE 2-4: *Output Voltage vs. Input Voltage (MIC28511-1).*

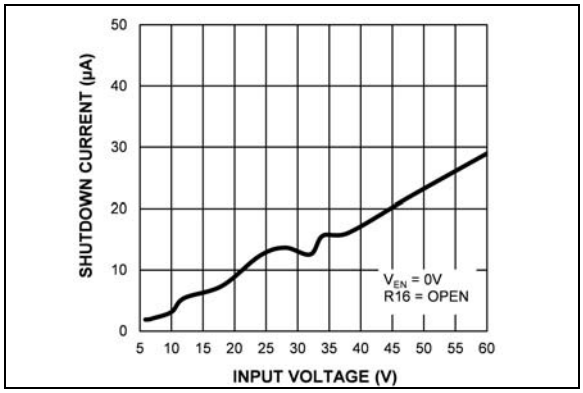


FIGURE 2-2: *V_{IN} Shutdown Current vs. Input Voltage.*

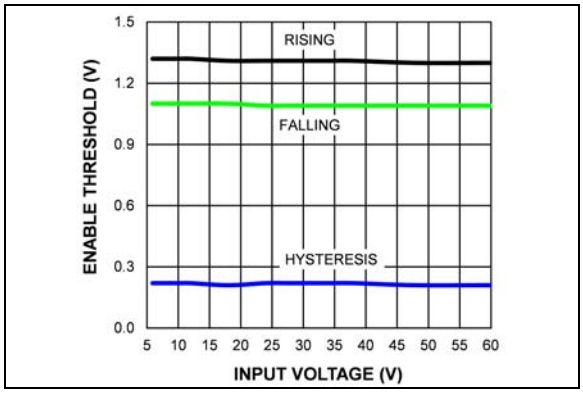


FIGURE 2-5: *Enable Threshold vs. Input Voltage (MIC28511-1).*

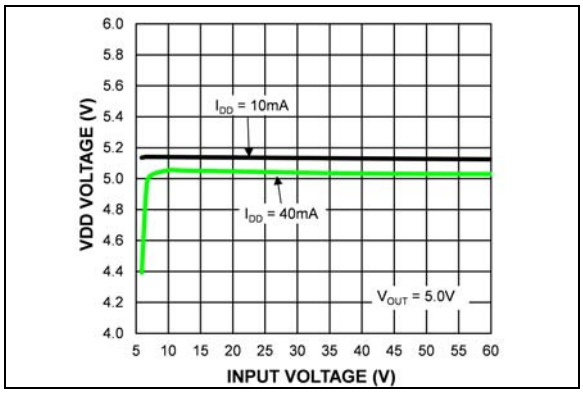


FIGURE 2-3: *V_{DD} Voltage vs. Input Voltage (MIC28511-1).*

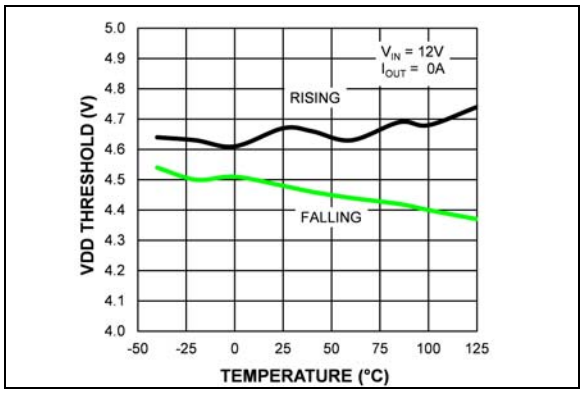


FIGURE 2-6: *V_{DD} UVLO Threshold vs. Temperature (MIC28511-1).*

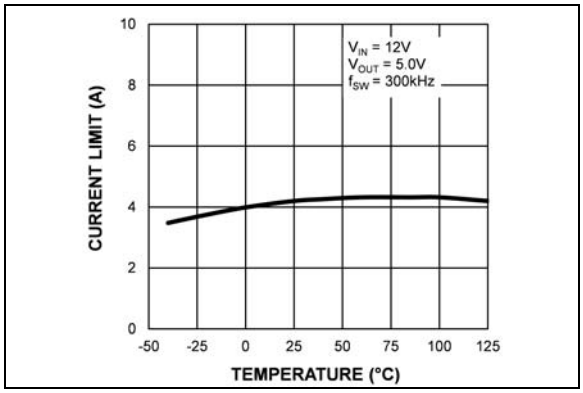


FIGURE 2-7: *Output Peak Current Limit vs. Temperature (MIC28511-1).*

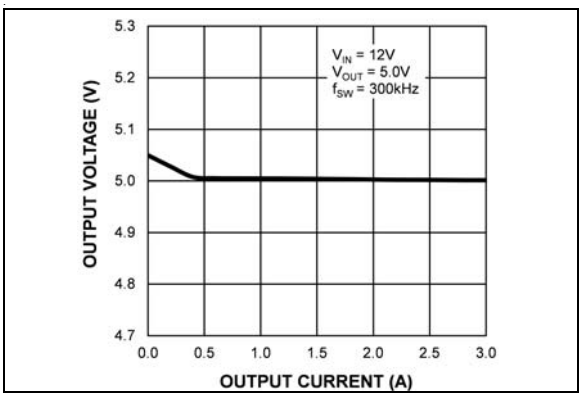


FIGURE 2-10: *Output Voltage vs. Output Current (MIC28511-1).*

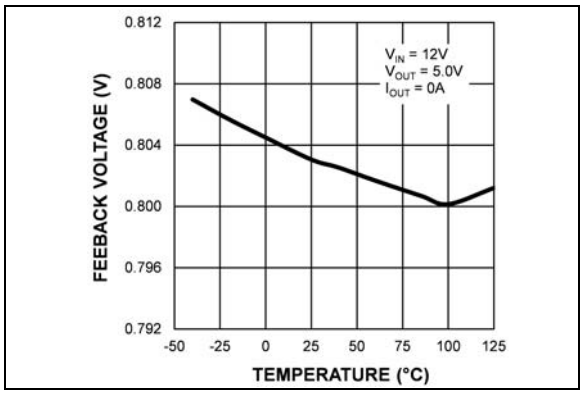


FIGURE 2-8: *Feedback Voltage vs. Temperature (MIC28511-1).*

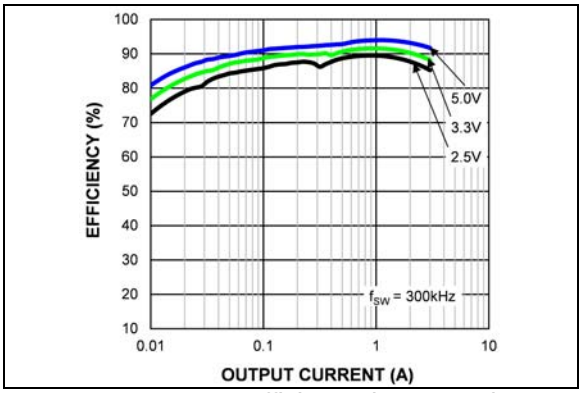


FIGURE 2-11: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC28511-1).*

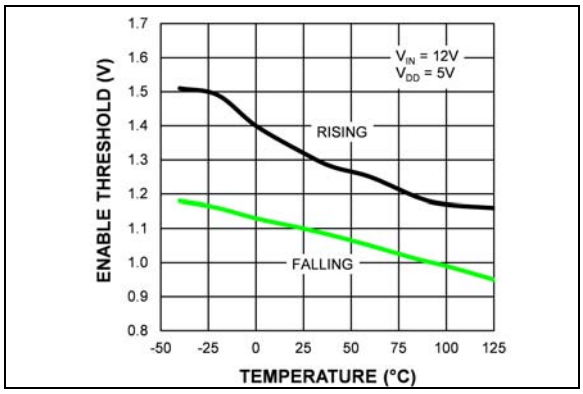


FIGURE 2-9: *Enable Threshold vs. Temperature (MIC28511-1).*

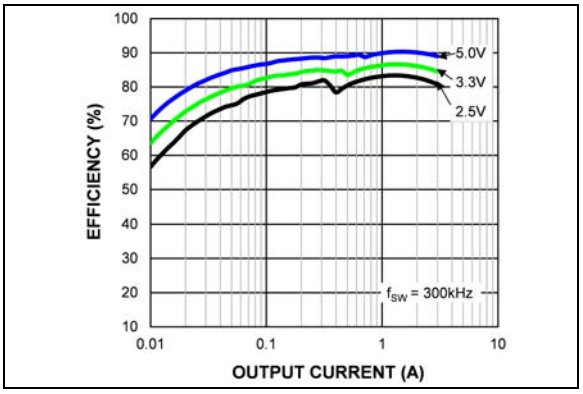


FIGURE 2-12: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC28511-1).*

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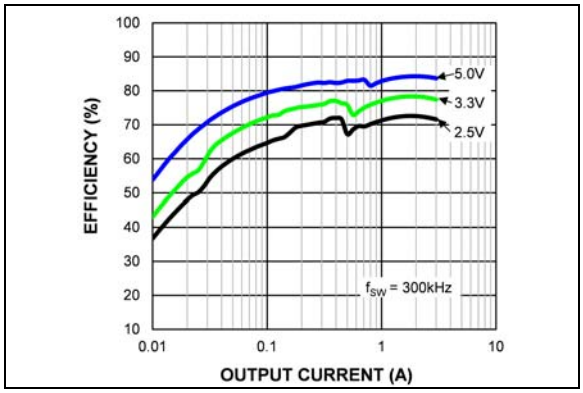


FIGURE 2-13: *Efficiency (V_{IN} = 48V) vs. Output Current (MIC28511-1).*

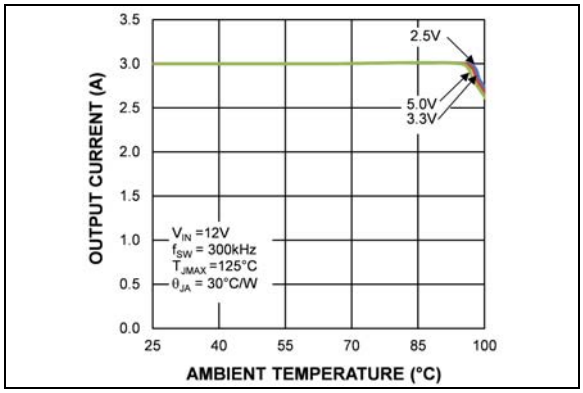


FIGURE 2-16: *12V Input Thermal Derating (MIC28511-1).*

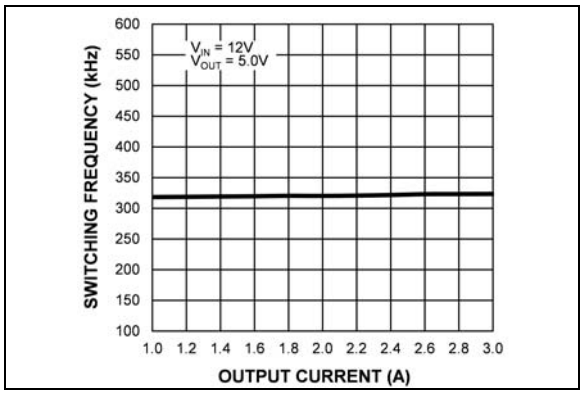


FIGURE 2-14: *Switching Frequency vs. Output Current (MIC28511-1).*

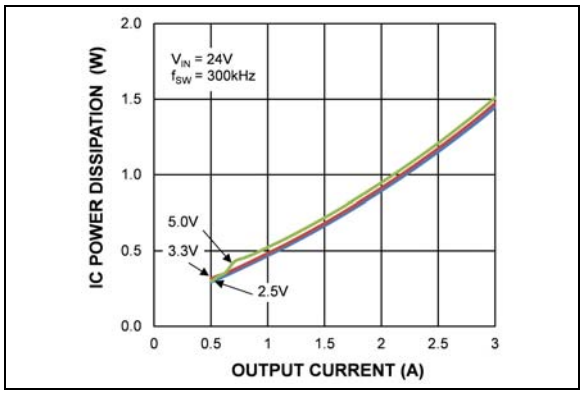


FIGURE 2-17: *IC Power Dissipation vs. Output Current (MIC28511-1).*

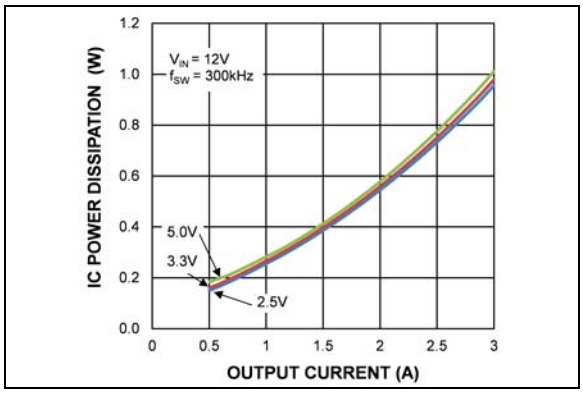


FIGURE 2-15: *IC Power Dissipation vs. Output Current (MIC28511-1).*

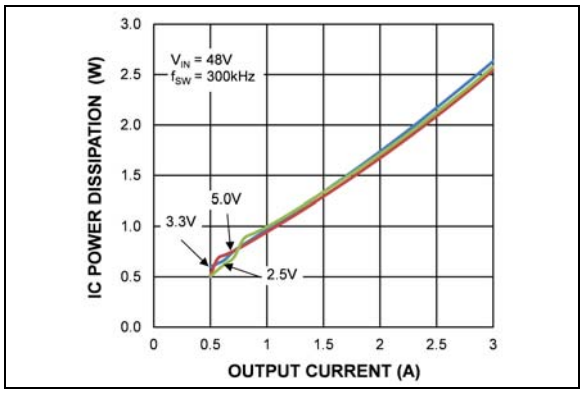


FIGURE 2-18: *IC Power Dissipation vs. Output Current (MIC28511-1).*

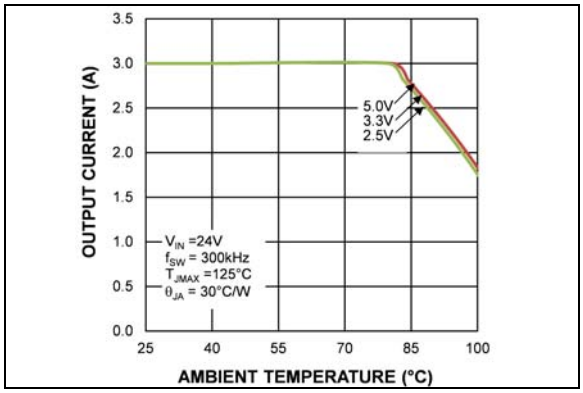


FIGURE 2-19: *24V Input Thermal Derating (MIC28511-1).*

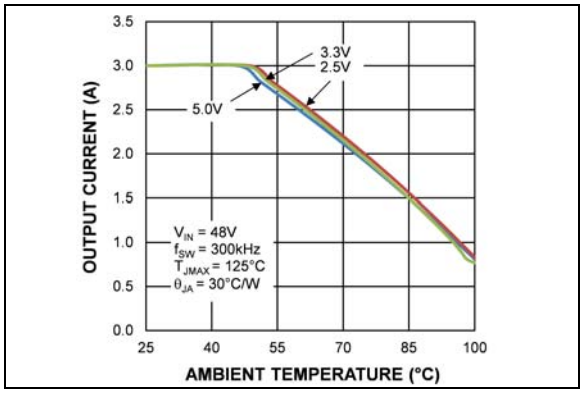


FIGURE 2-20: *48V Input Thermal Derating (MIC28511-1).*

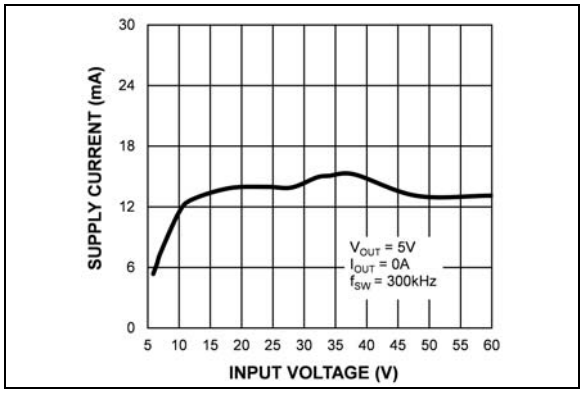


FIGURE 2-21: *V_{IN} Operating Supply Current vs. Input Voltage (MIC28511-2).*

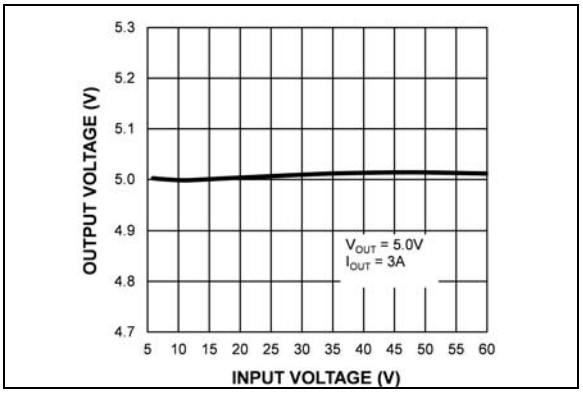


FIGURE 2-22: *Output Voltage vs. Input Voltage.*

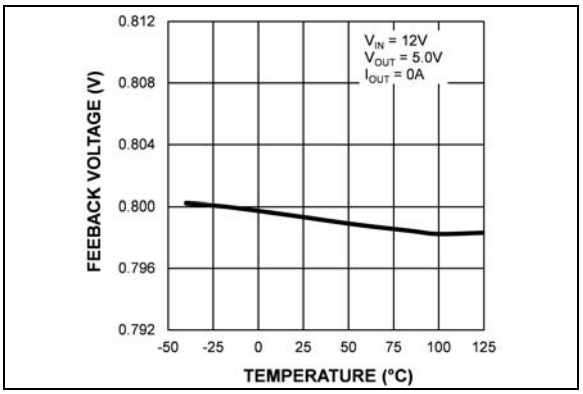


FIGURE 2-23: *Feedback Voltage vs. Temperature (MIC28511-2).*

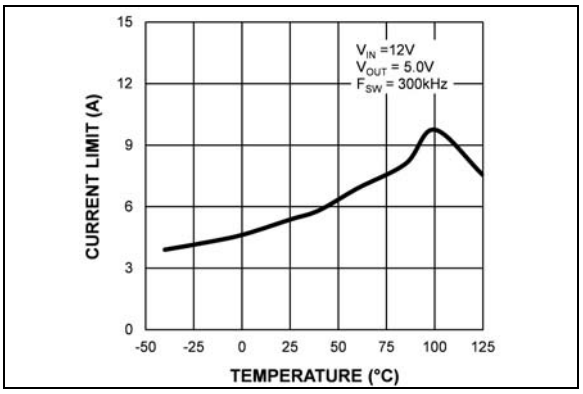


FIGURE 2-24: *Output Peak Current Limit vs. Temperature (MIC28511-2).*

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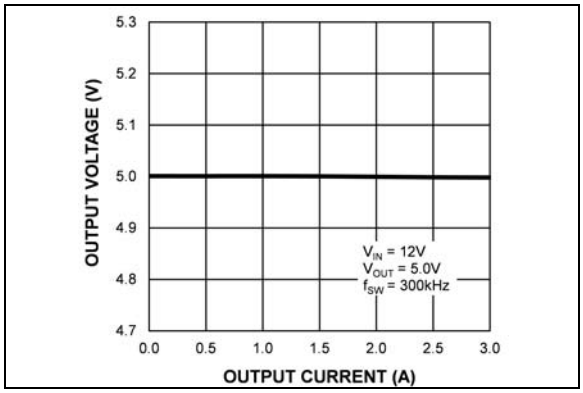


FIGURE 2-25: *Output Voltage vs. Output Current (MIC28511-2).*

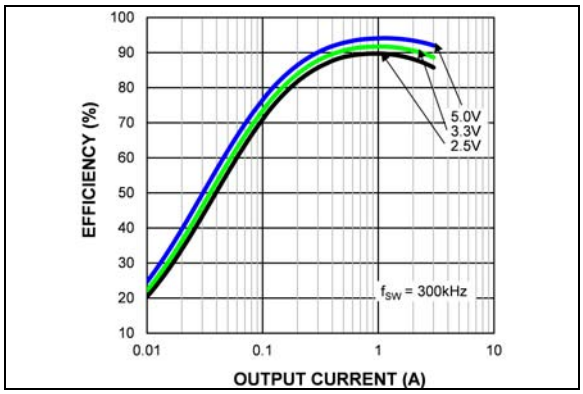


FIGURE 2-26: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC28511-2).*

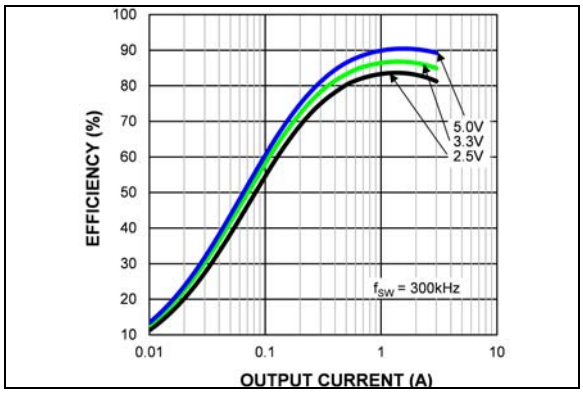


FIGURE 2-27: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC28511-2).*

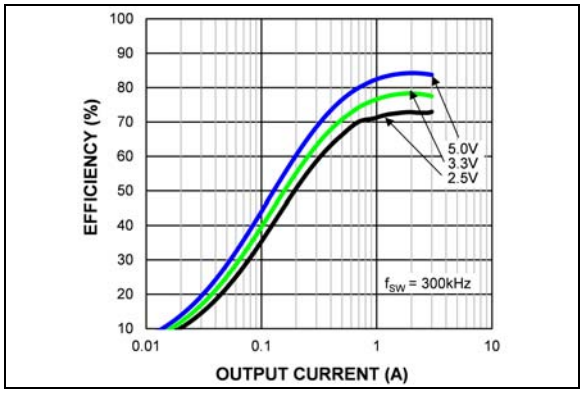


FIGURE 2-28: *Efficiency (V_{IN} = 48V) vs. Output Current (MIC28511-2).*

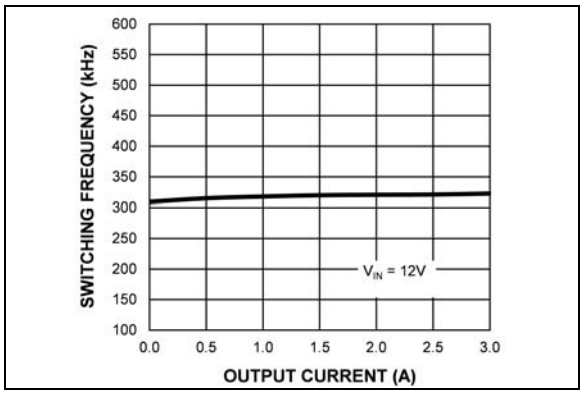


FIGURE 2-29: *Switch Frequency vs. Output Current (MIC28511-2).*

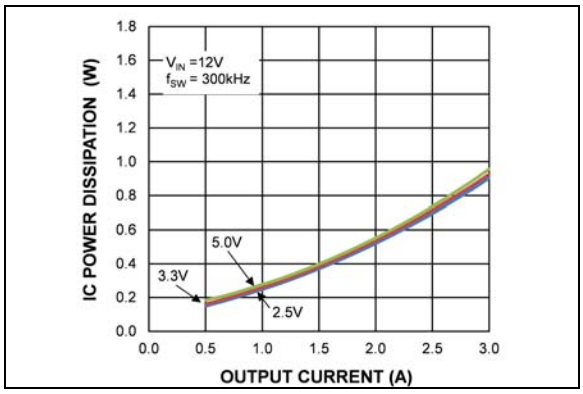


FIGURE 2-30: *IC Power Dissipation vs. Output Current (MIC28511-2).*

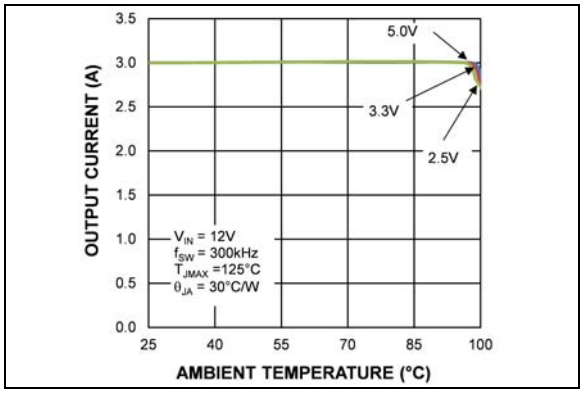


FIGURE 2-31: *12V Input Thermal Derating (MIC28511-2).*

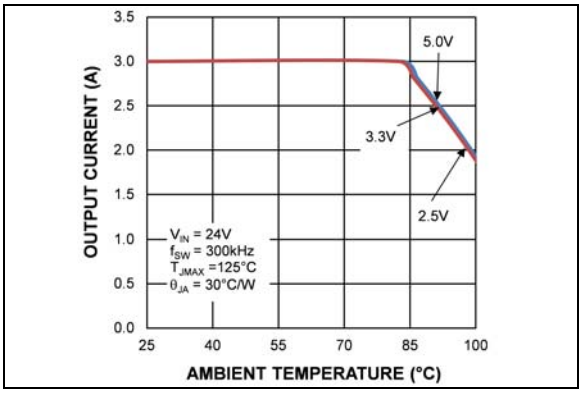


FIGURE 2-34: *24V Input Thermal Derating (MIC28511-2).*

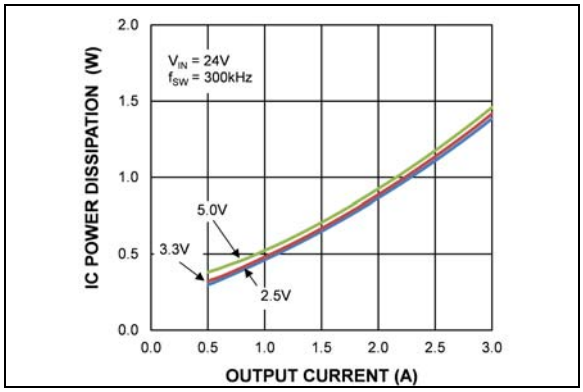


FIGURE 2-32: *IC Power Dissipation vs. Output Current (MIC28511-2).*

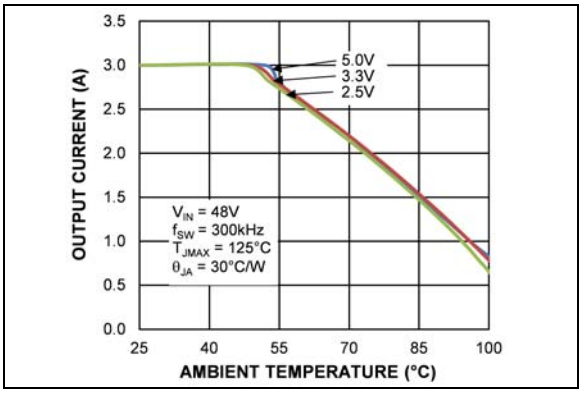


FIGURE 2-35: *48V Input Thermal Derating (MIC28511-2).*

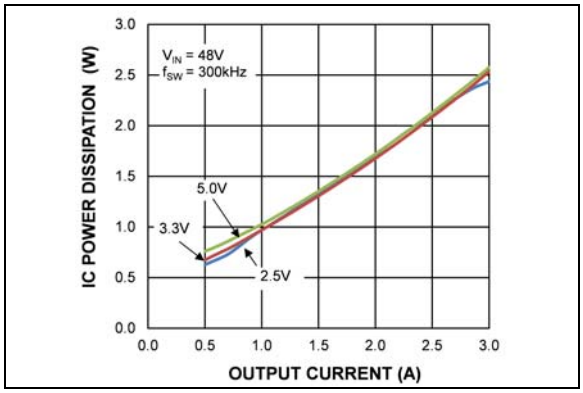


FIGURE 2-33: *IC Power Dissipation vs. Output Current (MIC28511-2).*

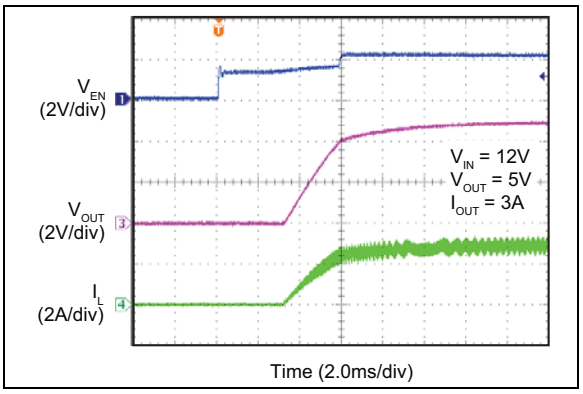


FIGURE 2-36: *Enable Turn-On Delay and Rise Time.*

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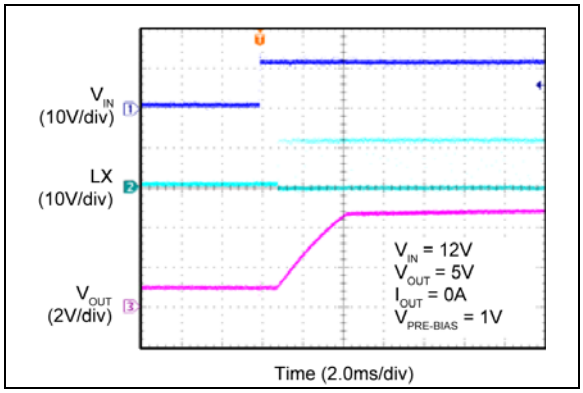


FIGURE 2-37: *Start-Up with Pre-Biased Output at 1V.*

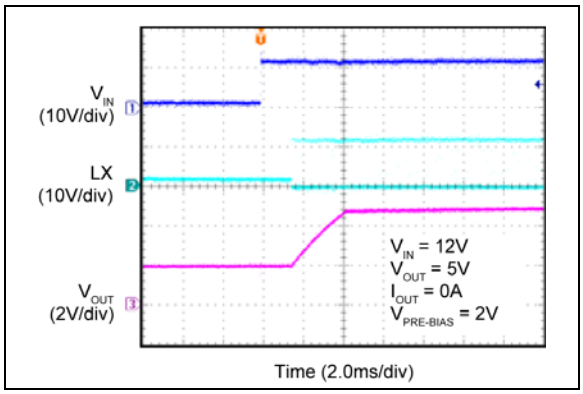


FIGURE 2-38: *Start-Up with Pre-Biased Output at 2V.*

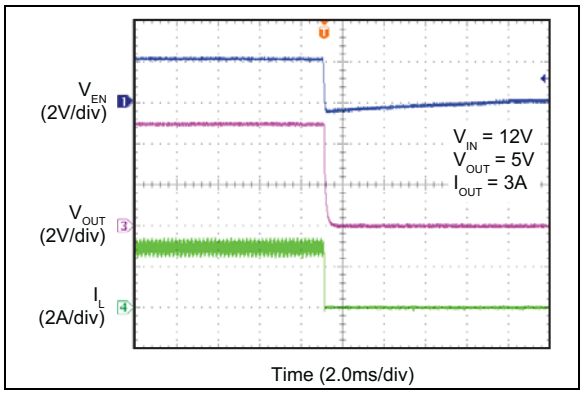


FIGURE 2-39: *Enable Turn-Off Delay and Fall Time.*

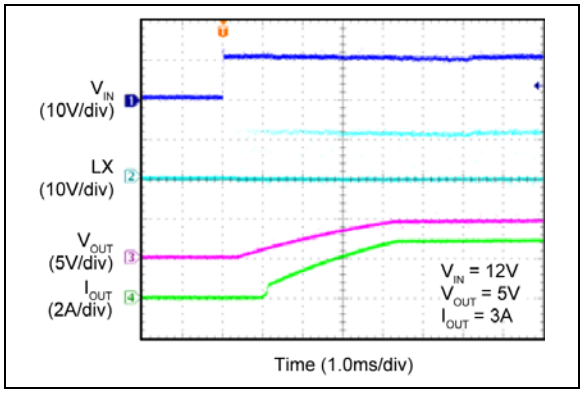


FIGURE 2-40: *V_{IN} Turn-On.*

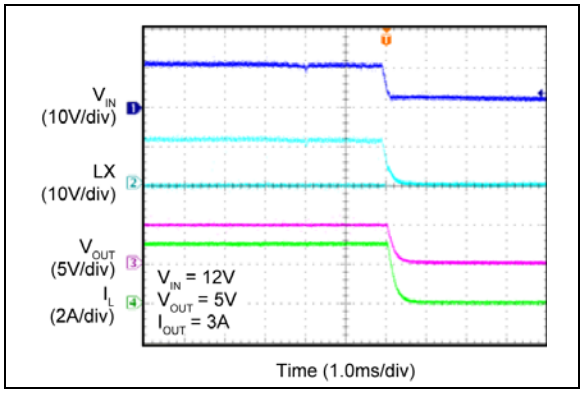


FIGURE 2-41: *V_{IN} Turn-Off.*

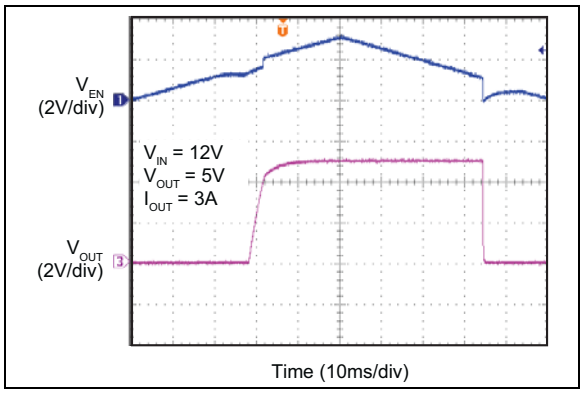


FIGURE 2-42: *Enable Turn-On/Turn-Off.*

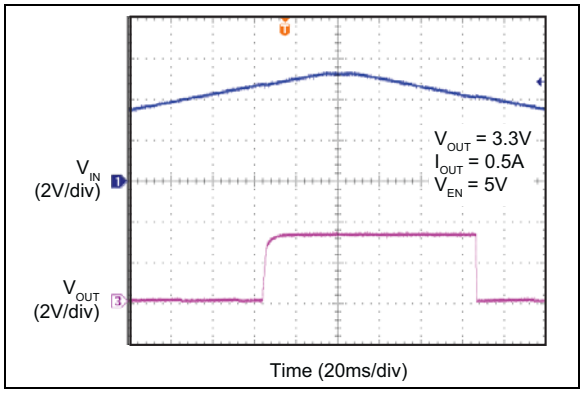


FIGURE 2-43: *V_{IN} UVLO Thresholds.*

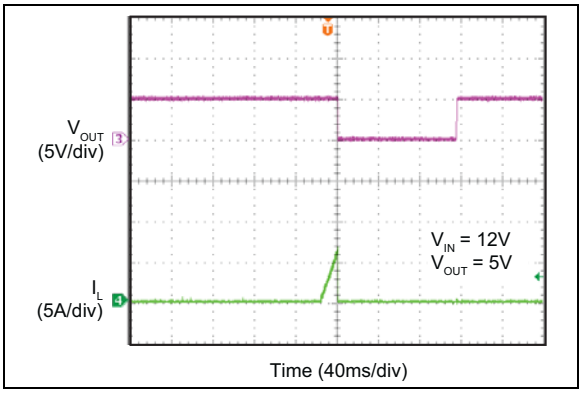


FIGURE 2-46: *Output Peak Current-Limit Threshold.*

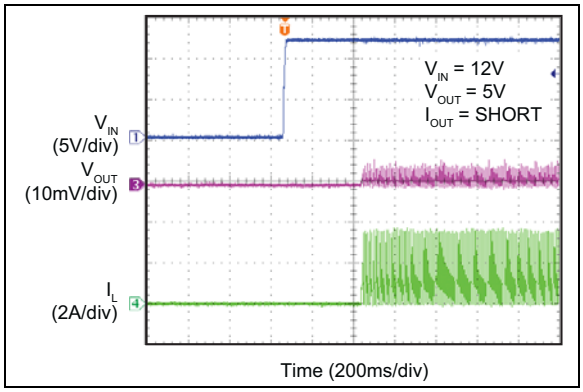


FIGURE 2-44: *Power-Up into Short-Circuit.*

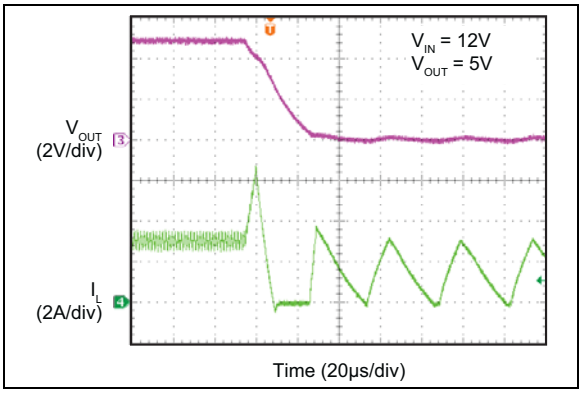


FIGURE 2-47: *Short-Circuit.*

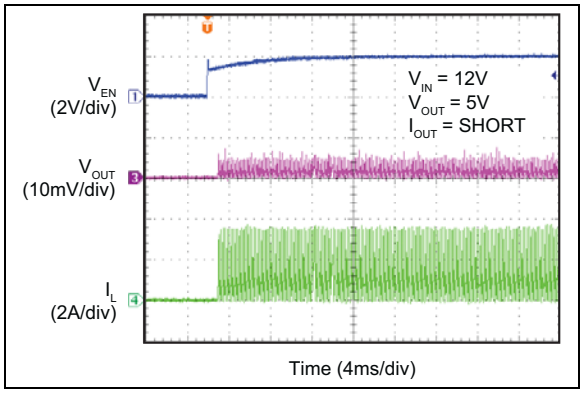


FIGURE 2-45: *Enabled into Short.*

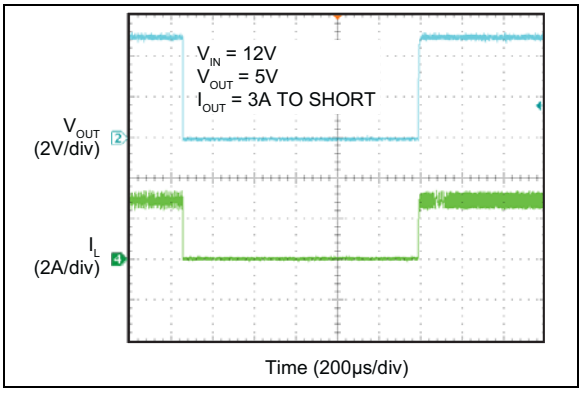


FIGURE 2-48: *Output Recovery from Short-Circuit.*

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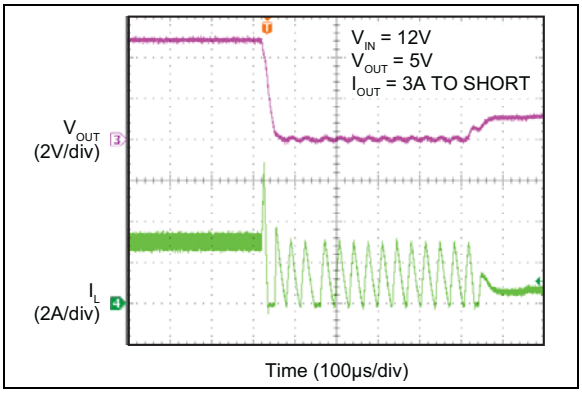


FIGURE 2-49: *Output Recovery from Short-Circuit (Zoomed-In Version).*

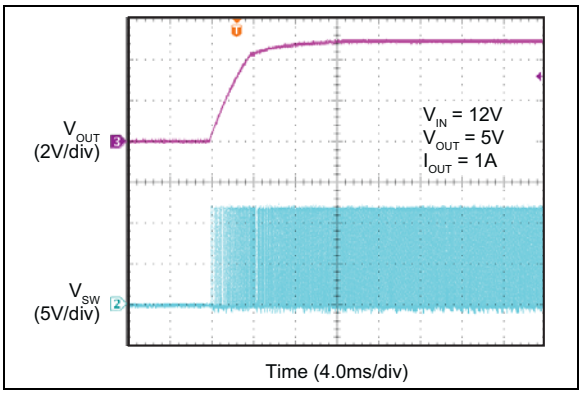


FIGURE 2-50: *Output Recovery from Thermal Shutdown.*

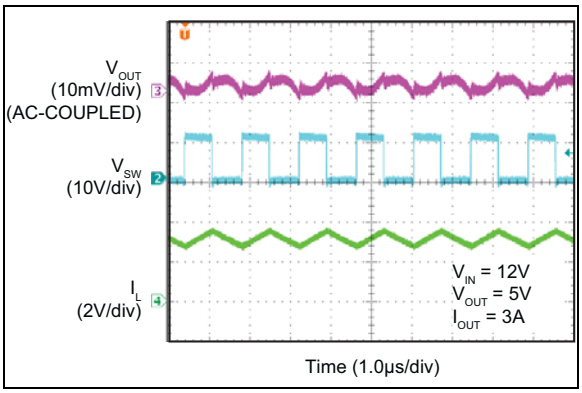


FIGURE 2-51: *MIC28511-2 Switching Waveforms, I_{OUT} = 3A.*

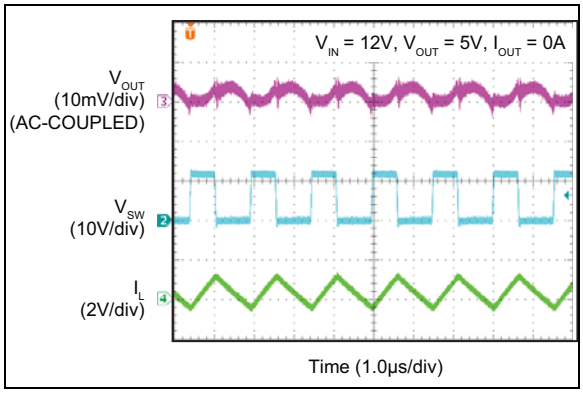


FIGURE 2-52: *MIC28511-2 Switching Waveforms, I_{OUT} = 0A.*

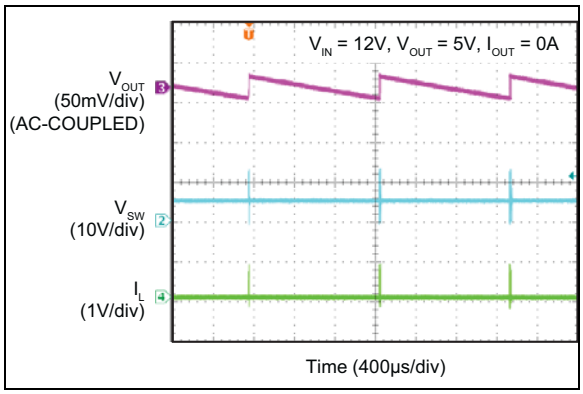


FIGURE 2-53: *MIC28511-1 Switching Waveforms, I_{OUT} = 0A.*

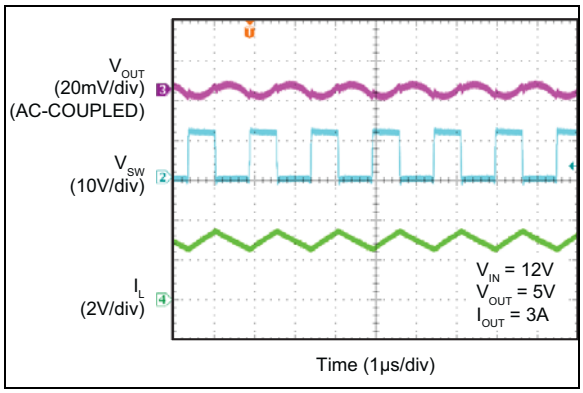


FIGURE 2-54: *MIC28511-1 Switching Waveforms, I_{OUT} = 3A.*

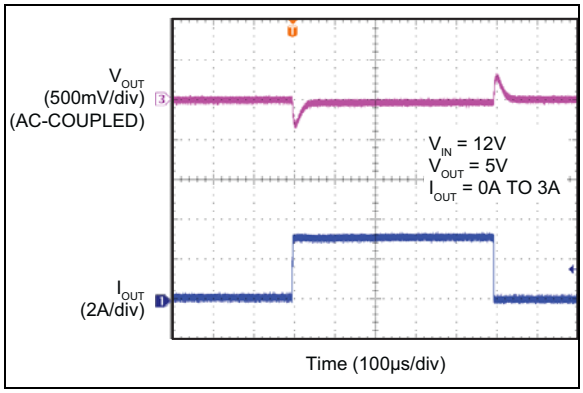


FIGURE 2-55: *MIC28511-2 Transient Response.*

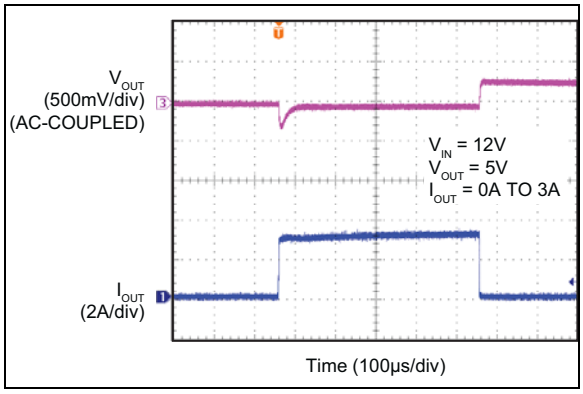


FIGURE 2-56: *MIC28511-1 Transient Response.*

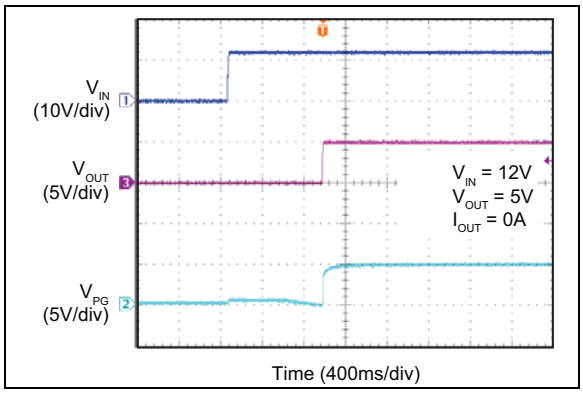


FIGURE 2-57: *Power Good at V_{IN} Soft Turn-On.*

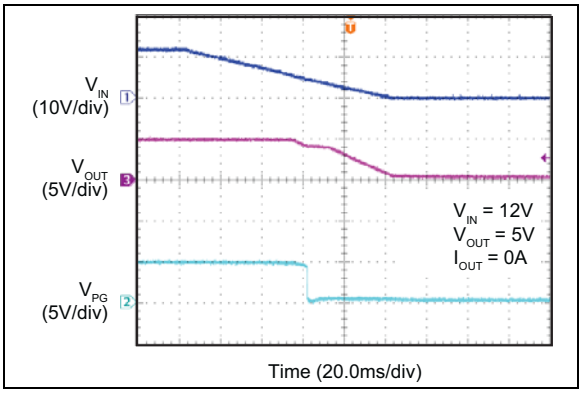


FIGURE 2-58: *Power Good at V_{IN} Soft Turn-Off.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	DL	Low-Side Gate Drive. Internal low-side power MOSFET gate connection. This pin must be left unconnected or floating.
2	PGND	PGND is the return path for the low-side driver circuit. Connect to the source of low-side MOSFET's (PGND, pins 10, 11 22, 23, and 26) through a low-impedance path.
3	DH	High-Side Gate Drive. Internal high-side power MOSFET gate connection. This pin must be left unconnected or floating.
4, 7, 8, 9, 25 (25 is ePad)	PV_{IN}	Power Input Voltage. The PV_{IN} pins supply power to the internal power switch. Connect all PV_{IN} pins together and bypass locally with ceramic capacitors. The positive terminal of the input capacitor should be placed as close as possible to the PV_{IN} pins, the negative terminal of the input capacitor should be placed as close as possible to the PGND pins 10,11, 22, 23, and 26.
5	LX	The LX pin is the return path for the high-side driver circuit. Connect the negative terminal of the bootstrap capacitor directly to this pin. Also connect this pin to the SW pins 12, 21, and 27, with a low-impedance path. The controller monitors voltages on this and PGND for zero current detection.
6	BST	Bootstrap Pin. This pin provides bootstrap supply for the high-side gate driver circuit. Connect a 0.1 µF capacitor and an optional resistor in series from the LX (pin 5) to the BST.
10, 11, 22, 23, 26 (26 is ePad)	PGND	Power Ground. These pins are connected to the source of the low-side MOSFET. They are the return path for the step-down regulator power stage and should be tied together. The negative terminal of the input decoupling capacitor should be placed as close as possible to these pins.
12, 21, 27 (27 is ePad)	SW	Switch Node. The SW pins are the internal power switch outputs. These pins should be tied together and connected to the output inductor.
13	AGND	Analog Ground. The analog ground for V_{DD} and the control circuitry. The analog ground return path should be separate from the power ground (PGND) return path.
14	FB	Feedback Input. The FB pin sets the regulated output voltage relative to the internal reference. This pin is connected to a resistor divider from the regulated output such that the FB pin is at 0.8V when the output is at the desired voltage.
15	PGOOD	The power good output is an open drain output requiring an external pull-up resistor to external bias. This pin is a high impedance open circuit when the voltage at FB pin is higher than 90% of the feedback reference voltage (typically 0.8V).
16	EN	Enable Input. The EN pin enables the regulator. When the pin is pulled below the threshold, the regulator will shut down to an ultra-low current state. A precise threshold voltage allows the pin to operate as an accurate UVLO. Do not tie EN to V_{DD}
17	V_{IN}	Supply voltage for the internal LDO. The VIN operating voltage range is from 4.6V to 60V. A ceramic capacitor from V_{IN} to AGND is required for decoupling. The decoupling capacitor should be placed as close as possible to the supply pin.
18	I_{LIM}	Current Limit Setting. Connect a resistor from this pin to the SW pin node to allow for accurate current limit sensing programming of the internal low-side power MOSFET.
19	V_{DD}	Internal +5V Linear Regulator: V_{DD} is the internal supply bus for the IC. Connect to an external 1 µF bypass capacitor. When V_{IN} is <5.5V, this regulator operates in drop-out mode. Connect V_{DD} to V_{IN}.
20	P_{VDD}	A 5V supply input for the low-side N-channel MOSFET driver circuit, which can be tied to V_{DD} externally. A 1 µF ceramic capacitor from PV_{DD} to PGND is recommended for decoupling.
24	FREQ	Switching Frequency Adjust pin. Connect this pin to V_{IN} to operate at 680 kHz. Place a resistor divider network from V_{IN} to the FREQ pin to program the switching frequency.

4.0 FUNCTIONAL DESCRIPTION

The MIC28511 is an adaptive on-time synchronous buck regulator with integrated high-side and low-side MOSFETs suitable for high-input voltage to low-output voltage conversion applications. It is designed to operate over a wide input voltage range (4.6V to 60V) which is suitable for automotive and industrial applications. The output is adjustable with an external resistive divider. An adaptive on-time control scheme is employed to produce a constant switching frequency in continuous-conduction mode and reduced switching frequency in discontinuous-operation mode, improving light-load efficiency. Overcurrent protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown.

4.1 Theory of Operation

As illustrated in the Functional Block Diagram, the output voltage of the MIC28511 is sensed by the feedback (FB) pin via voltage dividers R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low-gain transconductance (g_M) amplifier. If the feedback voltage decreases and the amplifier output is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the fixed t_{ON} estimator circuitry:

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT}	Output Voltage
V_{IN}	Power Stage Input Voltage
f_{SW}	Switching Frequency

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_M amplifier is below 0.8V, then the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 200 ns (typical), the MIC28511 control logic will apply the $t_{OFF(MIN)}$ instead. The $t_{OFF(MIN)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from Equation 4-2.

EQUATION 4-2:

$$D_{MAX} = 1 - t_{OFF(MIN)} \times f_{SW}$$

It is not recommended to use MIC28511 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC28511. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

Figure 4-1 shows the allowable range of the output voltage versus the input voltage. The minimum output voltage is 0.8V which is limited by the reference voltage. The maximum output voltage is 24V which is limited by the internal circuitry.

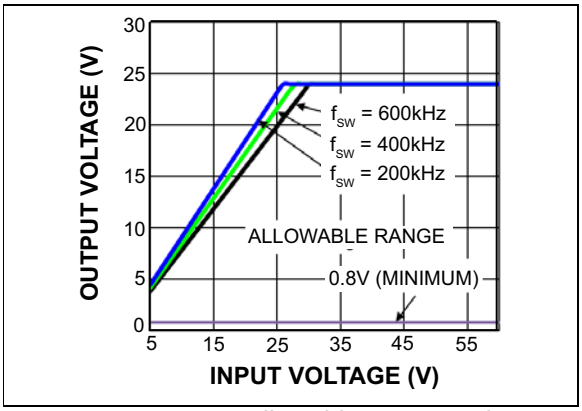


FIGURE 4-1: *Allowable Output Voltage Range vs. Input Voltage.*

To illustrate the control loop operation, both the steady-state and load transient scenarios will be analyzed.

Figure 4-2 shows the MIC28511 control loop timing during steady-state operation. During steady-state, the g_M amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

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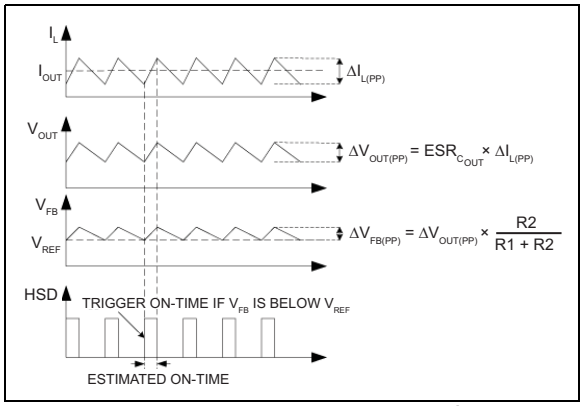


FIGURE 4-2: *MIC28511 Control Loop Timing.*

Figure 4-3 shows the operation of the MIC28511 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(MIN)}$ is generated to charge C_{BST} because the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC28511 converter.

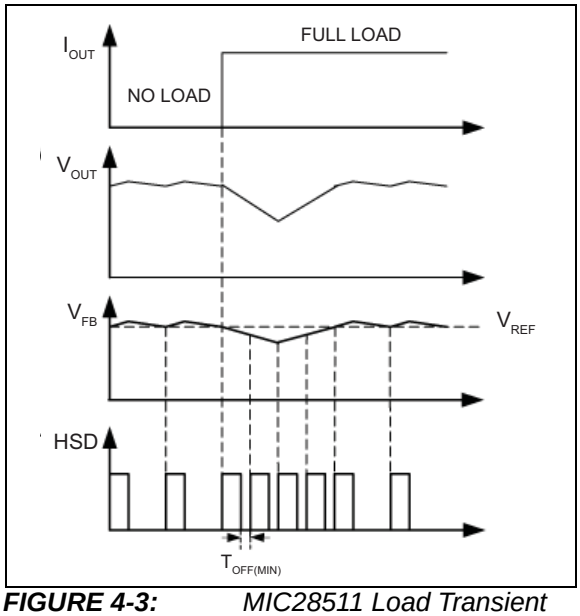


FIGURE 4-3: *MIC28511 Load Transient Response.*

Unlike true current-mode control, the MIC28511 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC28511 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the MIC28511 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_M amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV ~ 100 mV.

If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_M amplifier and the error comparator. Also, if the ESR of the output capacitor is very low, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple. In these cases, ripple injection is required to ensure proper operation. Please refer to the Ripple Injection subsection for more details about the ripple injection technique.

4.2 Discontinuous Mode (MIC28511-1 Only)

In continuous mode, the inductor current is always greater than zero; however, at light loads the MIC28511-1 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode occurs when the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4-4. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC28511-1 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC28511-1 has a zero crossing comparator that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC28511-1 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC28511-1 goes into discontinuous mode, both DH and DL are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, and then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4-4 shows the control loop timing in discontinuous mode.

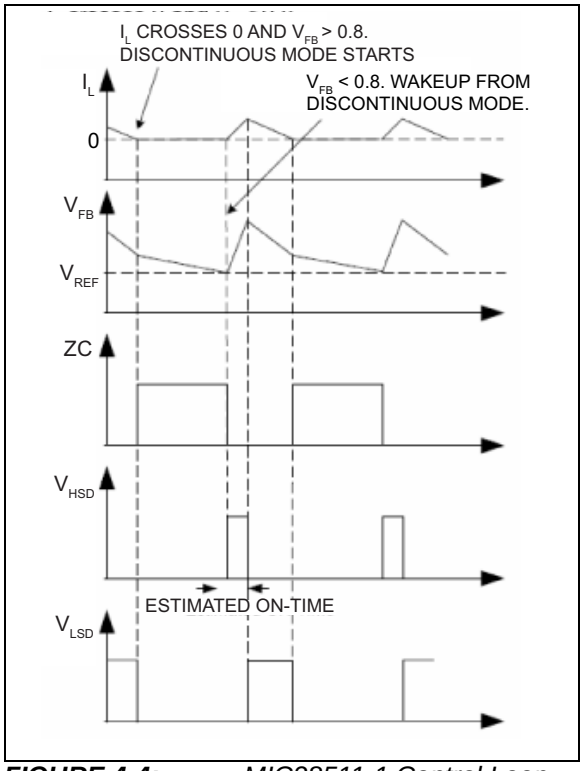


FIGURE 4-4: *MIC28511-1 Control Loop Timing (Discontinuous Mode).*

During discontinuous mode, the bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 450 µA, allowing the MIC28511-1 to achieve high efficiency in light load applications.

4.3 V_{DD} Regulator

The MIC28511 provides a 5V regulated V_{DD} to bias internal circuitry for V_{IN} ranging from 5.5V to 60V. When V_{IN} is less than 5.5V, V_{DD} should be tied to V_{IN} pins to bypass the internal linear regulator.

4.4 Soft-Start

Soft-start reduces the power supply inrush current at startup by controlling the output voltage rise time while the output capacitor charges.

The MIC28511 implements an internal digital soft-start by ramping up the 0.8V reference voltage (V_{REF}) from 0 to 100% in about 5 ms with 9.7 mV steps. This controls the output voltage rate of rise at turn on, minimizing inrush current and eliminating output voltage overshoot. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption.

4.5 Current Limit

The MIC28511 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense overcurrent conditions. In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during its ON period. The sensed voltage, $V_{(ILIM)}$, is compared with the power ground (PGND) after a blanking time of 150 ns.

The voltage drop of the resistor R_{ILIM} is compared with the low-side MOSFET voltage drop to set the overcurrent trip level. The small capacitor connected from the I_{LIM} pin to PGND can be added to filter the switching node ringing, allowing a better short limit measurement. The time constant created by R_{ILIM} and the filter capacitor should be much less than the minimum off time.

The overcurrent limit can be programmed by using Equation 4-3:

EQUATION 4-3:

$$R_{ILIM} = \frac{(I_{CLIM} - 0.5 \times \Delta I_{L(PP)}) \times R_{DS(ON)} + V_{CL}}{I_{CL}}$$

Where:

I_{CLIM}	Desired Current Limit
$\Delta I_{L(PP)}$	Inductor Current Peak-to-Peak Use Equation 4-4 to calculate the inductor ripple current
$R_{DS(ON)}$	On-Resistance of Low-Side Power MOSFET (40 mΩ typical)
V_{CL}	Current-limit threshold. 14 mV (typical absolute value). See the Electrical Characteristics table.
I_{CL}	Current-limit source current. 70 µA (typical). See the Electrical Characteristics table.

The peak-to-peak inductor current ripple is calculated with Equation 4-4.

EQUATION 4-4:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to use the $R_{DS(ON)}$ at maximum junction temperature with a 20% margin to calculate R_{ILIM} in Equation 4-3.

In case of hard short, the current-limit threshold is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitor during soft-start is under the folded

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short limit; otherwise the supply will go into hiccup mode and may not be finishing the soft-start successfully.

4.6 Power Good (PGOOD)

The power good (PGOOD) pin is an open-drain output that indicates logic-high when the output is nominally 90% of its steady state voltage.

4.7 MOSFET Gate Drive

The Functional Block Diagram shows a bootstrap circuit, consisting of D_{BST}, C_{BST}, and R_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D_{BST} is reverse-biased and C_{BST} floats high while continuing to bias the high-side gate driver. The bias current of the high-side driver is less than 10 mA, so a 0.1 µF to 1 µF capacitor is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. ΔBST = 10 mA x 1.25 µs/0.1 µF = 125 mV. When the low-side MOSFET is turned back on, C_{BST} is then recharged through the boost diode. A 30Ω resistor R_{BST}, which is in series with the BST pin, is required to slow down the turn-on time of the high-side N-channel MOSFET.

5.0 APPLICATION INFORMATION

5.1 Output Voltage Setting Components

The MIC28511 requires two resistors to set the output voltage as shown in Figure 5-1.

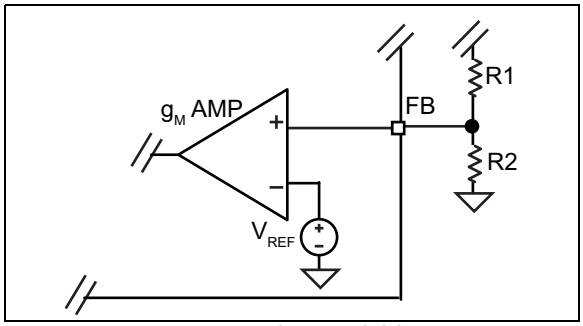


FIGURE 5-1: *Voltage Divider Configuration.*

The output voltage is determined by Equation 5-1.

EQUATION 5-1:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{FB}	0.8V

A typical value of R1 used on the standard evaluation board is 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using Equation 5-2:

EQUATION 5-2:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

5.2 Setting the Switching Frequency

The MIC28511 switching frequency can be adjusted by changing the resistor divider network from V_{IN}.

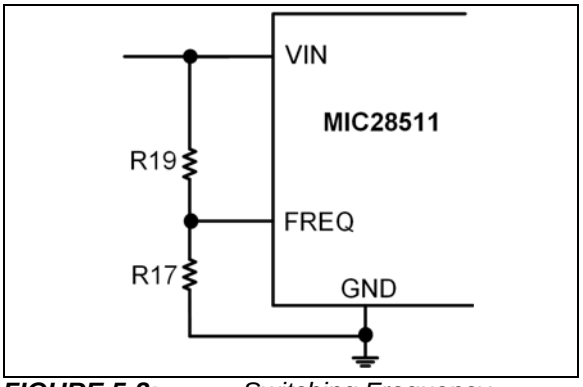


FIGURE 5-2: *Switching Frequency Adjustment.*

Equation 5-3 gives the estimated switching frequency.

EQUATION 5-3:

$$f_{SW} = f_0 \times \left(\frac{R17}{R17 + R19}\right)$$

Where:

f_0	Switching frequency when R17 is open; typically 680 kHz.

Figure 5-3 shows the switching frequency versus the resistor R17 when R19 = 100 kΩ.

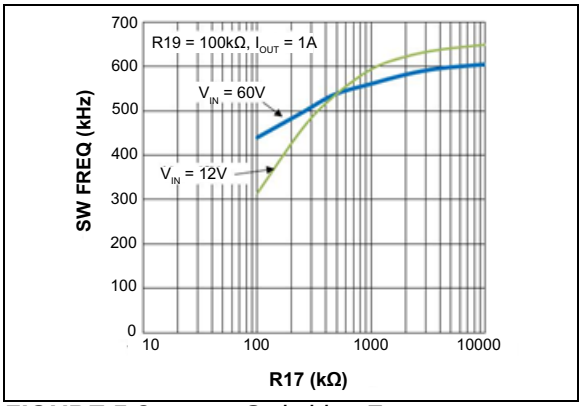


FIGURE 5-3: *Switching Frequency vs. R17.*

5.3 Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and

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MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by:

EQUATION 5-4:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times \Delta I_{L(PP)} \times f_{SW}}$$

Where:

f_{SW}	Switching Frequency
$\Delta I_{L(PP)}$	The peak-to-peak inductor current ripple; typically 20% of the maximum output current

In continuous conduction mode, the peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

EQUATION 5-5:

$$I_{L(PK)} = I_{OUT} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-6:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{I^2}}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC28511 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels.

The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-7:

EQUATION 5-7:

$$P_{L(CU)} = I_{L(RMS)}^2 \times DCR$$

The resistance of the copper wire, DCR, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 5-8:

$$DCR_{(HT)} = DCR_{(20C)} \times (1 + 0.0042 \times [T_H - T_{20C}])$$

Where:

T_H	Temperature of wire under full load
T_{20C}	Ambient temperature
$DCR_{(20C)}$	Room temperature winding resistance (usually specified by the manufacturer)

5.4 Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are also important factors in selecting an output capacitor. Recommended capacitor types are ceramic, tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. For high ESR electrolytic capacitors, ESR is the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. For a low ESR ceramic output capacitor, ripple is dominated by the reactive impedance. The maximum value of ESR is calculated by Equation 5-9.

EQUATION 5-9:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$	Peak-to-Peak Output Voltage Ripple
$\Delta I_{L(PP)}$	Peak-to-Peak Inductor Current Ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated by Equation 5-10.

EQUATION 5-10:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{2 \times \Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right) + (\Delta I_{L(PP)} \times ESR_{COUT})^2}$$

Where:

D	Duty Cycle
C_{OUT}	Output Capacitance Value
f_{SW}	Switching Frequency

As described in the Theory of Operation subsection of the Functional Description, the MIC28511 requires at least 20 mV peak-to-peak ripple at the FB pin for the g_M amplifier and the error comparator to operate properly. Also, the ripple on FB pin should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Refer to the Ripple Injection subsection for details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-11.

EQUATION 5-11:

$$I_{C_{OUT(RMS)}} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-12:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^{2} \times ESR_{COUT}$$

5.5 Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-13:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-14:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-15:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^{2} \times ESR_{CIN}$$

5.6 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC28511's g_M amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. If the feedback voltage ripple is so small that the g_M amplifier and error comparator can't sense it, then the MIC28511 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

- Enough ripple at the feedback voltage due to the large ESR of the output capacitors (Figure 5-4). The converter is stable without any ripple injection.

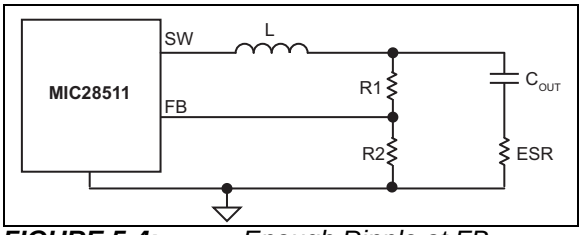


FIGURE 5-4: *Enough Ripple at FB.*

The feedback voltage ripple is:

EQUATION 5-16:

$$\Delta V_{FB(PP)} = \frac{R2}{R1 + R2} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$	Peak-to-Peak Value of the Inductor Current Ripple

- Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

  The output voltage ripple is fed into the FB pin through a feed-forward capacitor, C_{FF} in this situation, as shown in Figure 5-5. The typical C_{FF} value is selected by using Equation 5-17.

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EQUATION 5-17:

$$R1 \times C_{FF} \approx \frac{10}{f_{SW}}$$

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple.

EQUATION 5-18:

$$\Delta V_{FB(PP)} \approx ESR \times \Delta I_{L(PP)}$$

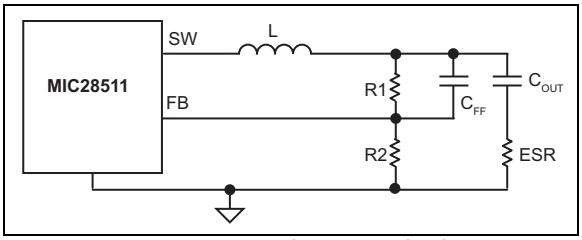


FIGURE 5-5: *Inadequate Ripple at FB.*

- Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors.

  In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{INJ} and a capacitor C_{INJ}, as shown in Figure 5-6.

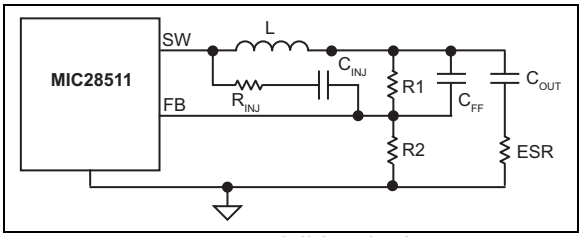


FIGURE 5-6: *Invisible Ripple at FB.*

The injected ripple is calculated via:

EQUATION 5-19:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{div} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:

V_{IN}	Power stage input voltage
D	Duty cycle
f_{SW}	Switching frequency
τ	(R1//R2//R_{INJ}) x C_{FF}

EQUATION 5-20:

$$K_{div} = \frac{R1//R2}{R_{INJ} + R1//R2}$$

In Equation 5-19 and Equation 5-20, it is assumed that the time constant associated with C_{FF} must be much greater than the switching period:

EQUATION 5-21:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{FF} of 1 nF to 100 nF can easily satisfy the large time constant requirements. Also, a 100 nF injection capacitor C_{INJ} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is as follows.

- Select C_{FF} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{FF} is 1 nF to 100 nF if R1 and R2 are in the kΩ range.
- Select R_{INJ} according to the expected feedback voltage ripple using Equation 5-22:

EQUATION 5-22:

$$K_{div} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

The value of R_{INJ} is calculated using Equation 5-23.

EQUATION 5-23:

$$R_{INJ} = (R1//R2) \times \left(\frac{1}{K_{div}} - 1\right)$$

- Select C_{INJ} as 100 nF, which could be considered as short for a wide range of the frequencies.

6.0 PCB LAYOUT GUIDELINES

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

Figure 6-1 is optimized from a small form-factor point of view and shows the top and bottom layers of a four-layer PCB. It is recommended to use Mid-Layer 1 as a continuous ground plane.

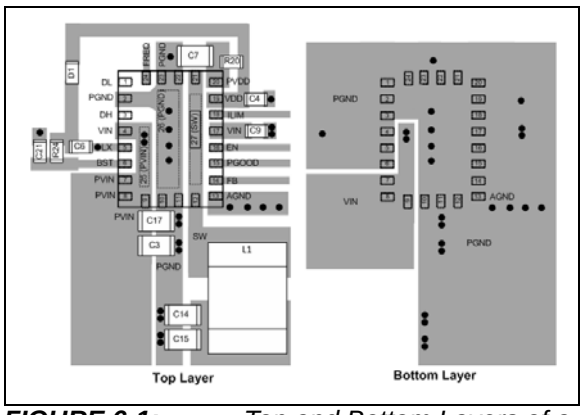


FIGURE 6-1: *Top and Bottom Layers of a Four-Layer Board.*

The following guidelines should be followed to ensure proper operation of the MIC28511 converter.

6.1 IC

- The analog ground pin (AGND) must be connected directly to the ground planes. Do not route the AGND pin to the PGND pin on the top layer.
- Place the IC close to the point-of-load (POL).
- Use copper planes to route the input and output power lines.
- Analog and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- Place the input capacitors on the same side of the board and as close to the PV_{IN} and PGND pins as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply with power is suddenly applied.

6.3 SW Node

- Do not route any digital lines underneath or close to the SW node.
- Keep the switch node (SW) away from the feedback (FB) pin.

6.4 Output Capacitor

- Use a copper island to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.5 Thermal Measurements

Measuring the IC’s case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

For more information about the Evaluation board layout, please contact Microchip sales.

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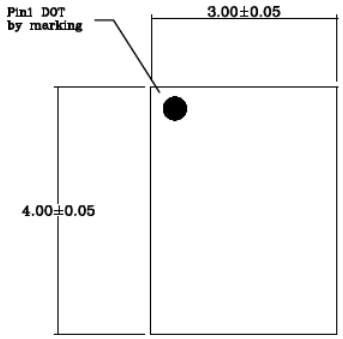
7.0 PACKAGING INFORMATION

24-Lead FQFN 3 mm x 4 mm Package Outline and Recommended Land Pattern

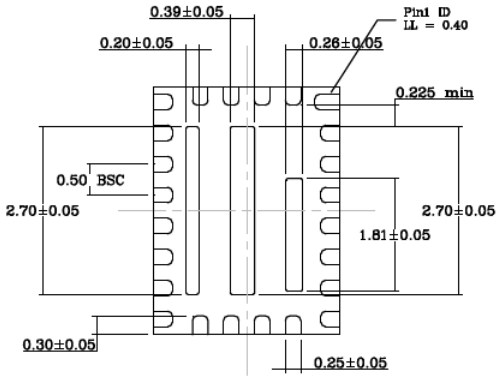
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TITLE
24 LEAD FQFN 3x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

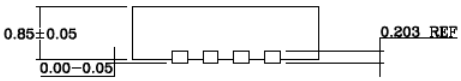
DRAWING #	FQFN34-24LD-PL-2	UNIT	MM
Lead Frame	Copper	Lead Finish	Matte Tin



Top View
Note 1,2,3



Bottom View
Note 1,2,3



Side View
Note 1,2,3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAs & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE. SIZE IS 0.30~0.35mm WITH 0.80mm PITCH.
5. SHADED AREA RECTANGLES REPRESENT SOLDER STENCIL OPENING ON EXPOSED METAL TRACE.
6. MAGENTA & BLUE COLORED RECTANGLES REPRESENT DIFFERENT POTENTIAL, DO NOT CONNECT TO GND.
7. BLACK COLORED RECTANGLES REPRESENT DIFFERENT IOs. DO NOT CONNECT TOGETHER.
8. RECOMMENDED LAND PATTERN TOLERANCE IS 0.02mm UNLESS SPECIFIED.
9. SEE RECOMMENDED LAND PATTERN ON PAGE 2.

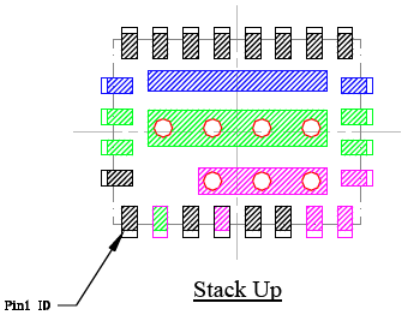
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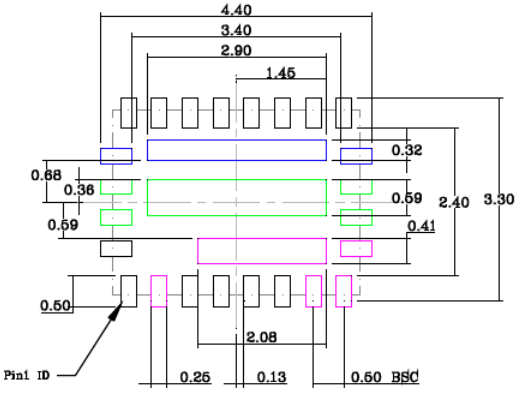
POD-Land Pattern Doc #: FQFN34-24LD-PL-2-E

Recommended Land Pattern

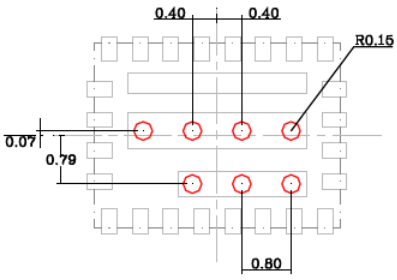
Note: 4,5,6,7



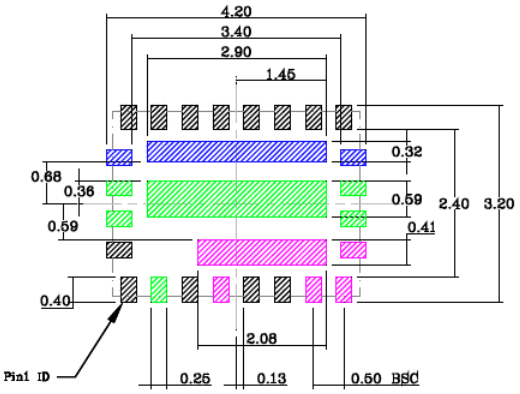
Stack Up



Exposed Metal



Thermal (filled) VIA



Solder Stencil Opening

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APPENDIX A: REVISION HISTORY

Revision A (May 2016)

- Converted Micrel document MIC28511 to Microchip data sheet template DS20005520A.
- Minor text changes throughout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO. —	X	X	XX
Device	Architecture	Temperature	Package

Device:	MIC28511:	$60V_{IN}$, 3A Synchronous Buck Regulator	
Architecture:	1	=	HyperLight Load
	2	=	Hyper Speed Control
Temperature:	Y	=	–40°C to +125°C
Package:	FL	=	24-Pin 3 mm x 4 mm FQFN; Note 1

Examples:

a) MIC28511-1YFL: $60V_{IN}$, 3A Synchronous Buck Regulator, HyperLight Load, –40°C to +125°C Junction Temperature Range, 24LD FQFN

b) MIC28511-2YFL: $60V_{IN}$, 3A Synchronous Buck Regulator, Hyper Speed Control, –40°C to +125°C Junction Temperature Range, 24LD FQFN

Note 1: FQFN is a lead-free package. Pb-Free lead finish is Matte Tin.

NOTES:

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Note the following details of the code protection feature on Microchip devices:

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