MIC2807

RF PA Power Management IC
2MHz, 600mA DC/DC w/DAC Input and Bypass Switch, Dual Low Noise 200mA/30mA LDO Regulators

General Description

The MIC2807 integrates a high performance 600mA DC/DC converter intended for powering a power amplifier (PA) in a mobile phone with dual low noise low dropout (LDO) regulators for the rest of the RF section. Optimized for low noise performance, the MIC2807 improves efficiency in the handset without compromising quality.

The MIC2807 has a 2MHz, constant frequency pulse width modulated (PWM) DC/DC converter designed for low noise operation and high efficiency. The output voltage (V_{OUT}) is variable from 0.3V to the input voltage (V_{IN}), adjustable from 0.3V to 3.6V through a DAC input when $V_{IN} > V_{OUT}$. The converter will work in a 100% duty cycle mode to offer maximum power and efficiency in the application. In addition to 100% duty cycle, the DC/DC converter has a bypass mode of operation where the input voltage node (PVIN pin) is shorted to the output voltage node (OUT pin) through a 95mΩ switch.

The integrated dual low noise low dropout regulators are optimized for high PSRR capability and fast turn-on times. The constant frequency DC/DC converter along with dual low noise LDO regulators enables a very quiet and efficient solution for mobile applications.

The MIC2807 is a µCap design, operating with small ceramic output capacitors and inductors for stability, reducing required board space and component cost and it is available in the tiny 2.5mm x 2.8mm MLF® package.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- 2.7V to 5.5V input voltage range
- Stable with ceramic output capacitors
- Tiny 17-pin 2.5mm x 2.8mm MLF® Package
- Thermal shutdown protection
- Current limit protection

RF PA Power Supply DC/DC Converter

- Adjustable output power supply – DAC controlled
  - $V_{OUT} = V_{DAC} \times 3$
- Bypass mode operation
  - Internal 95mΩ switch between PVIN and OUT pins
  - $V_{DAC} > 1.2V$
- Up to 600mA output current in PWM mode
- 100% duty cycle operation for maximum efficiency
- Tiny 4.7µH, 1µF output inductor and capacitor
- Low-noise 2MHz PWM operation
- >90% efficiency

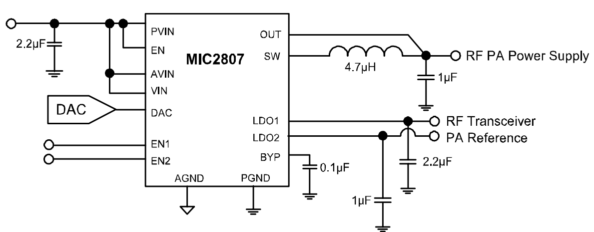
Dual Low Noise Low Dropout Regulators

- High accuracy – ±2% over temperature
- High PSRR – greater than 70dB
- Very low output noise – 32µVrms
- LDO1 – 200mA output current capability
- LDO2 – 30mA output current capability

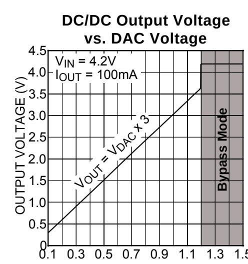
Applications

- CDMA2000 mobile phones
- UMTS/WCDMA mobile phones
- Wibro modules
- WiFi modules
- Power amplifier modules (PAMs) with linear PAs

Typical Application



CDMA2000/WCDMA RF Power Supply Circuit



Ordering Information

Part Number	Marking Code*	LDO1/LDO2 Voltage**	Junction Temp. Range	Package	Lead Finish
MIC2807-JJYML	$\overline{\text{Y}}$JJJ	2.5V/2.5V	–40°C to +125°C	17-Pin 2.5mm x 2.8mm MLF®	Pb-Free
MIC2807-MMYML	$\overline{\text{Y}}$JMM	2.8V/2.8V	–40°C to +125°C	17-Pin 2.5mm x 2.8mm MLF®	Pb-Free
MIC2807-NNYML	$\overline{\text{Y}}$JNN	2.85V/2.85V	–40°C to +125°C	17-Pin 2.5mm x 2.8mm MLF®	Pb-Free
MIC2807-OOYML	$\overline{\text{Y}}$JOO	2.9V/2.9V	–40°C to +125°C	17-Pin 2.5mm x 2.8mm MLF®	Pb-Free

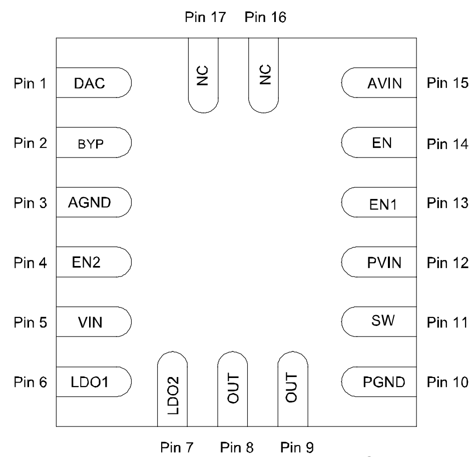
Notes:

MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

* Over bar (—) symbol may not be to scale.

** Other voltage options available. Please contact Micrel for details.

Pin Configuration



17-Pin 2.5mm x 2.8mm MLF® (ML)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	DAC	DAC Control Input (Analog Voltage Input). Provides control of output voltage of DC/DC converter. The output voltage is 3x's the DAC voltage (Ex. $0.5V_{DAC} = 1.5V_{OUT}$) when $V_{IN} > V_{OUT}$. Bypass mode is enabled when the DAC voltage exceeds 1.2V or $V_{IN} \le V_{OUT}$. $V_{OUT} = V_{DAC} \times 3$.
2	BYP	Filter capacitor for LDO1 and LDO2 internal voltage reference, connect capacitor to ground.
3	AGND	Signal ground of chip.
4	EN2	Enables the LDO2 regulator.
5	VIN	LDO1 and LDO2 Supply Voltage. Must be connected to PIN 15.
6	LDO1	Output of the LDO1.
7	LDO2	Output of the LDO2.
8, 9	OUT	Drain of internal bypass switch, also serves as feedback for the internal regulator.
10	PGND	Power ground.
11	SW	Switch: Internal power MOSFET output switches of DC/DC converter.
12	PVIN	Supply Voltage: Requires bypass capacitor to ground.
13	EN1	Enables LDO1 Regulator.
14	EN	Enables the DC/DC Converter.
15	AVIN	Supply voltage for DC/DC converter control circuitry and reference voltage circuit. Must be connected to PIN 5.
16, 17	NC	No Connect.

Absolute Maximum Ratings[1]

Supply Voltage (PV_{IN}, AV_{IN}, V_{IN}) .... 0V to 6V
Output Switch Voltage (V_{SW}). 6V
DAC Input Voltage (V_{DAC})....................................... 0V to V_{IN}
Logic Input Voltage (V_{EN}, V_{EN1}, V_{EN2}) .... 0V to V_{IN}
Power Dissipation[3]..................................Internally Limited
Storage Temperature (T_s) ....–65°C to +150°C
ESD Rating[4]..±2kV

Operating Ratings[2]

Supply Voltage (PV_{IN}, AV_{IN}, V_{IN}) .... 2.7V to 5.5V
Output Voltage (V_{OUT}) .... 0V to V_{IN}
Enable Voltage (V_{EN}, V_{EN1}, V_{EN2})............................ 0V to V_{IN}
DAC Input Voltage (V_{DAC})................................... 0.1V to V_{IN}
Junction Temperature (T_J) ....–40°C to +125°C
Thermal Resistance
2.5x2.8mm MLF-17 (θ_{JA})..................................70°C/W

Electrical Characteristics[5]

DC/DC Converter

$V_{IN} = PV_{IN} = AV_{IN} = V_{EN} = 3.6V$; $V_{DAC} = 0.6V$; $V_{EN1} = V_{EN2} = 0V$; L = 4.7µH; $C_{OUT} = 1µF$; $T_A = 25°C$, **bold** values indicate –40°C≤ T_J ≤ +125°C, unless noted.

LDO1/LDO2

$V_{IN} = V_{EN1} = V_{EN2} = 3.6V$; $C_{OUTLDO1} = 2.2µF$; $V_{EN} = 0V$; $C_{OUTLDO2} = 1µF$; $I_{OUT} = 100µA$; $T_A = 25°C$, **bold** values indicate –40°C≤ T_J ≤ +125°C, unless noted.

Parameter	Condition	Min	Typ	Max	Units
MIC2807					
Supply Voltage Range		**2.7**		**5.5**	V
Total Quiescent Current	$V_{EN} = V_{EN1} = V_{EN2} = 3.6V$ $V_{DAC} = 0.6V$ (DC/DC: not switching)		480		µA
Enable Pin Threshold	Logic Low			**0.4**	V
	Logic High	**1.3**			V
Enable Pin Hysteresis			30		mV
Enable Pin Input Current			0.01	**1**	µA
Under-Voltage Lockout Threshold	(turn-on)		2.6	**2.7**	V
UVLO Hysteresis			85		mV
Shutdown Temperature			160		ºC
Shutdown Temperature Hysteresis			20		ºC
Total Shutdown Current	$V_{EN} = V_{EN1} = V_{EN2} = 0V$		1	5	µA
DC/DC Converter [$V_{EN1} = V_{EN2} = 0V$]					
Maximum Duty Cycle		100			%
Bypass Quiescent Current	$V_{DAC} = 1.3V$		490	650	µA
Quiescent Current	$V_{DAC} = 0.6V$ (regulator on, not switching)		360	450	µA
Output Voltage	$V_{DAC} = 0.6V$, $I_{LOAD} = 0mA$	**1.746**	1.8	**1.854**	V
Output Voltage Line Regulation	3.0V≤ V_{IN} ≤ 4.5, $I_{LOAD} = 10mA$		0.05	0.5	%/V
Output Voltage Load Regulation	0mA < I_{OUT} < 400mA		0.2	1	%
Switch On-Resistance	I_{SW} = -100mA, High-Side Switch I_{SW} = 100mA, Low-Side Switch		0.55 0.6	0.75 0.85	Ω Ω
Current Limit (Peak SW Current)		0.65	0.85	1.6	A
Frequency		**1.8**	2	**2.2**	MHz

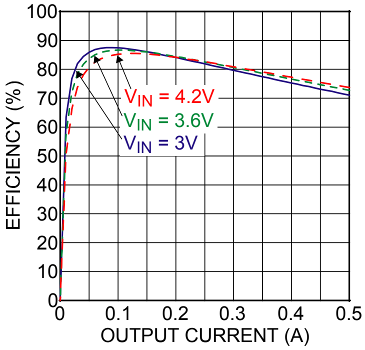
Parameter	Condition	Min	Typ	Max	Units
Turn-On Time	I_{OUT} = 100µA		25	**50**	µs
DAC Input Current			0.15	**2**	µA
Output Voltage/ DAC Voltage	(internally set)		3		V/V
Bypass Switch Threshold	DAC Voltage required to enable bypass mode	**1.176**	1.2	**1.224**	V
Bypass Switch Hysteresis			35		mV
Bypass Transition Time	Delay from V_{DAC} = 1.3V to V_{OUT} = 0.90V_{IN}		10	**40**	µs
Bypass Switch On-Resistance	V_{IN} = 3.0V, I_{BYPASS} = 100mA		95	150	mΩ
Bypass Switch Leakage				**5**	µA
Bypass Over-Current Limit		**1**	1.4	**2.5**	A
Current Limit Retry Time			32		µs
Current Limit Retry Duty Cycle			12.5		%
LDO1/LDO2 [V_{EN} = 0V]					
Total Ground Current[8]	V_{EN1} = V_{EN2} = 3.6V		220		µA
Turn-on Time	LDO1 or LDO2; C_{BYP} = 0.1µF		30	**100**	µs
LDO1 [V_{EN} = 0V]					
Output Voltage Accuracy	Variation from nominal V_{OUT}	–1		+1	%
	–40°C to +125°C	**–2**		**+2**	%
Line Regulation	V_{IN} = V_{OUT} +1V to 5.5V		0.02	**0.3**	%/V
Load Regulation[6]	I_{OUT} = 100µA to 200mA		0.2	**0.5**	%
Dropout Voltage[7]	I_{OUT} = 50mA; V_{OUT} > 2.8V		20		mV
	I_{OUT} = 150mA; V_{OUT} > 2.8V		55		mV
	I_{OUT} = 200mA; V_{OUT} > 2.8V		70	**120**	mV
Ground Pin Current[8]	I_{OUT} = 0mA; EN2 = GND		190	**300**	µA
Ripple Rejection	f = up to 1kHz; C_{BYP} = 0.1µF		70		dB
	f = 1kHz – 20kHz; C_{BYP} = 0.1µF		45		dB
Current Limit	V_{OUT} = 0V	225	300	700	mA
Output Voltage Noise	C_{BYP}=0.1µF, 10Hz to 100kHz		32		µV_{RMS}
LDO2 [V_{EN} = 0V]					
Output Voltage Accuracy	Variation from nominal V_{OUT}	–1		+1	%
	–40°C to +125°C	**–2**		**+2**	%
Line Regulation	V_{IN} = V_{OUT} +1V to 5.5V		0.02	**0.3**	%/V
Load Regulation[6]	I_{OUT} = 100µA to 30mA		0.2	**0.5**	%
Dropout Voltage[7]	I_{OUT} = 10mA; V_{OUT} > 2.8V		10		mV
	I_{OUT} = 30mA; V_{OUT} > 2.8V		30	**70**	mV
Ground Pin Current[8]	I_{OUT} = 0mA; EN1 = GND		190	**300**	µA
Ripple Rejection	f = up to 1kHz; C_{BYP} = 0.1µF		65		dB
	f = 1kHz – 20kHz; C_{BYP} = 0.1µF		40		dB
Current Limit	V_{OUT} = 0V	40	60	150	mA
Output Voltage Noise	C_{BYP} = 0.1µF, 10Hz to 100kHz		32		µV_{RMS}

Notes:

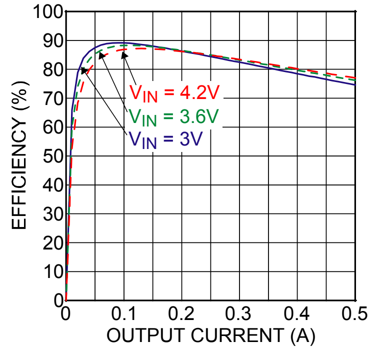
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended.
5. Specification for packaged product only.
6. Regulation is measured at constant junction temperature using low duty cycle pulse testing, changes in output voltage due to heating effects are covered by the thermal regulation specification.
7. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.
8. Ground pin current is the regulator quiescent current.

Typical Characteristics (DC/DC)

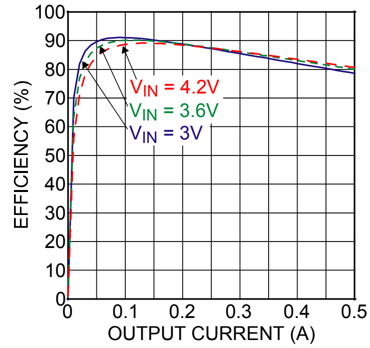
1V$_{OUT}$ DC/DC Efficiency



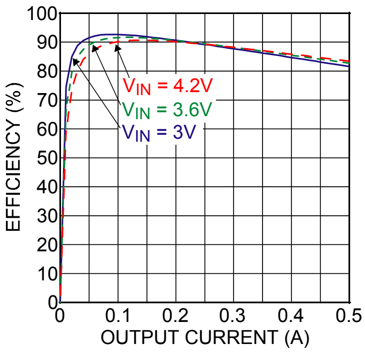
1.2V$_{OUT}$ DC/DC Efficiency



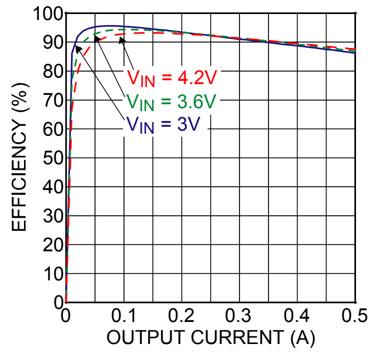
1.5V$_{OUT}$ DC/DC Efficiency



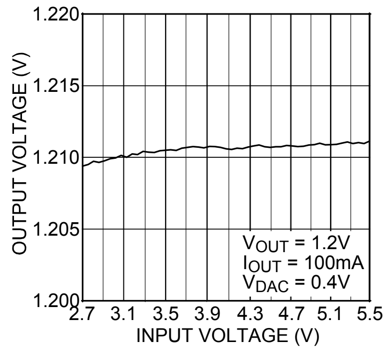
1.8V$_{OUT}$ DC/DC Efficiency



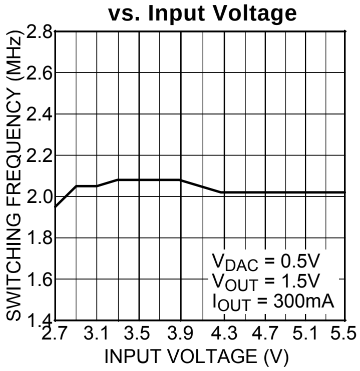
2.5V$_{OUT}$ DC/DC Efficiency



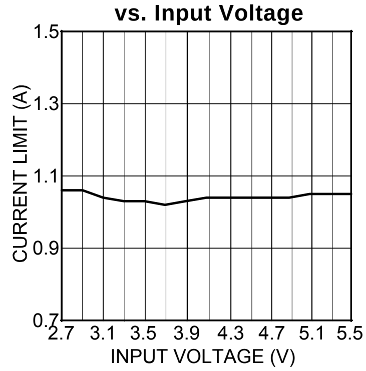
DC/DC Line Regulation



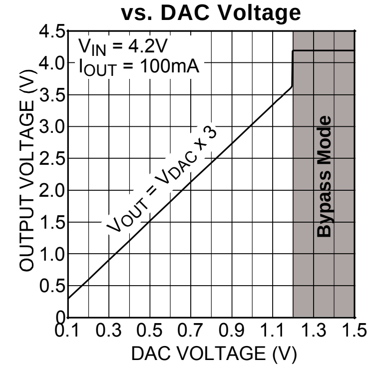
DC/DC Switching Frequency vs. Input Voltage



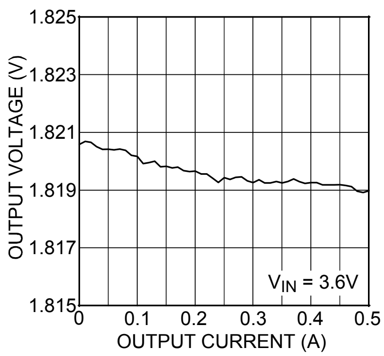
DC/DC Current Limit vs. Input Voltage



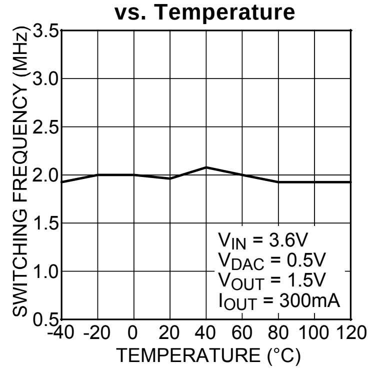
DC/DC Output Voltage vs. DAC Voltage



DC/DC Load Regulation

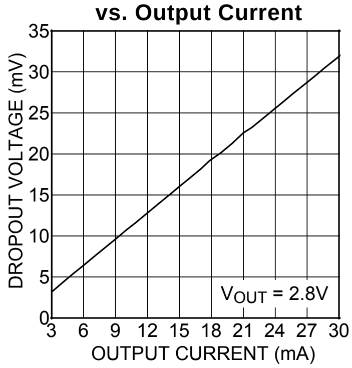


DC/DC Switching Frequency vs. Temperature

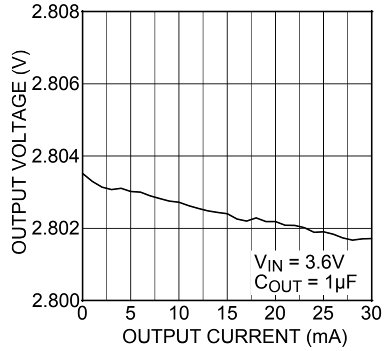


Typical Characteristics (LDO1/LDO2)

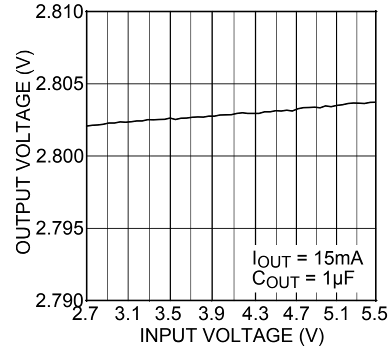
LDO2 Dropout Voltage vs. Output Current



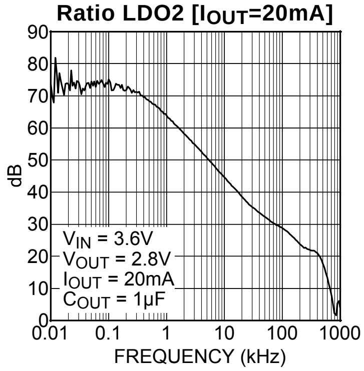
LDO2 Load Regulation



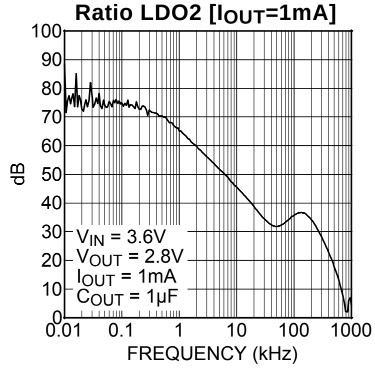
LDO2 Line Regulation



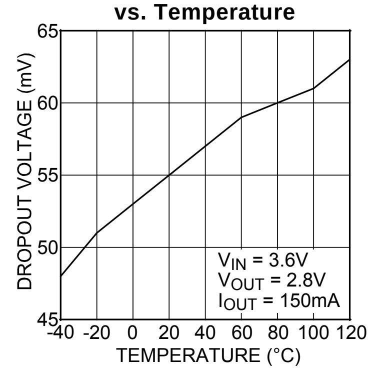
Power Supply Rejection Ratio LDO2 [I_{OUT}=20mA]



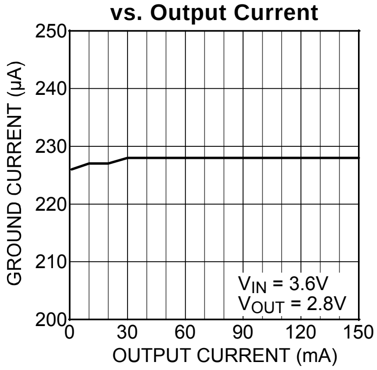
Power Supply Rejection Ratio LDO2 [I_{OUT}=1mA]



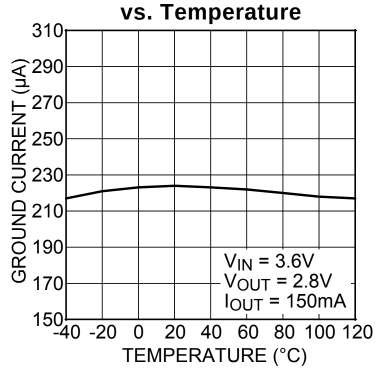
LDO1 Dropout Voltage vs. Temperature



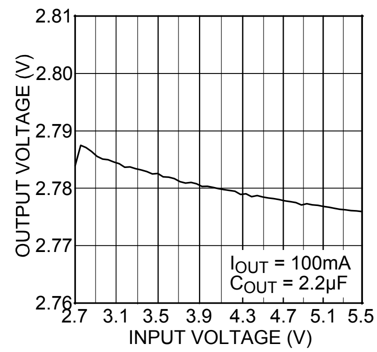
LDO1 Ground Current vs. Output Current



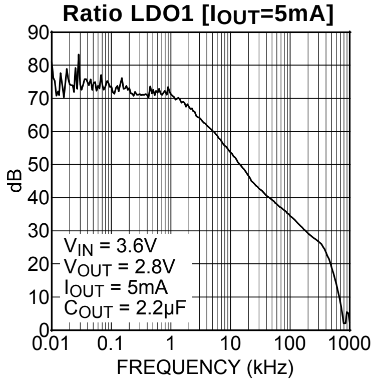
LDO1 Ground Current vs. Temperature



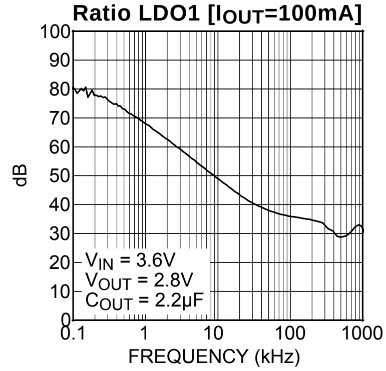
LDO1 Line Regulation



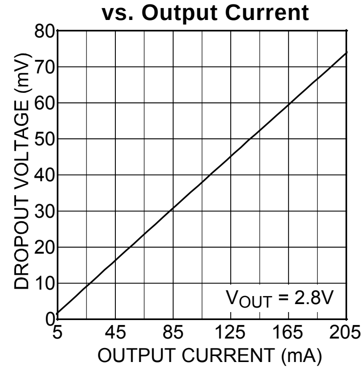
Power Supply Rejection Ratio LDO1 [I_{OUT}=5mA]



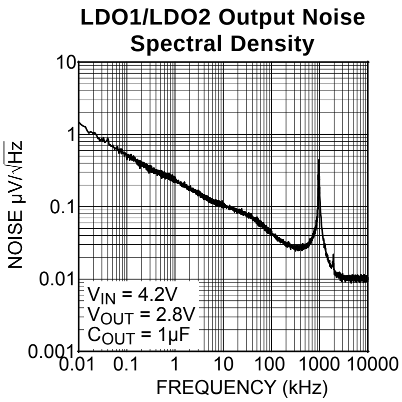
Power Supply Rejection Ratio LDO1 [I_{OUT}=100mA]



LDO1 Dropout Voltage vs. Output Current

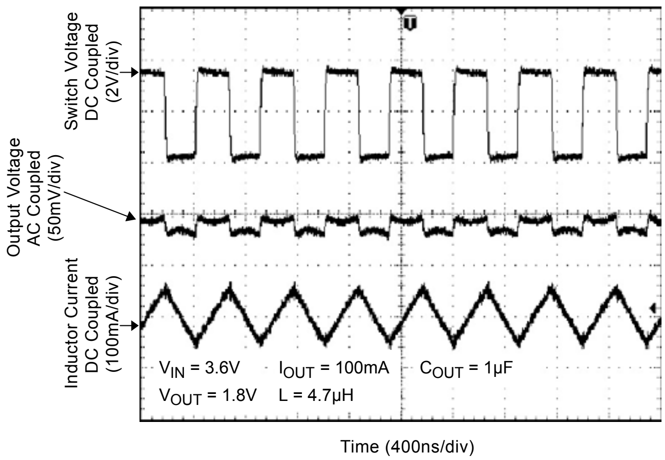


Typical Characteristics (LDO1/LDO2 cont.)

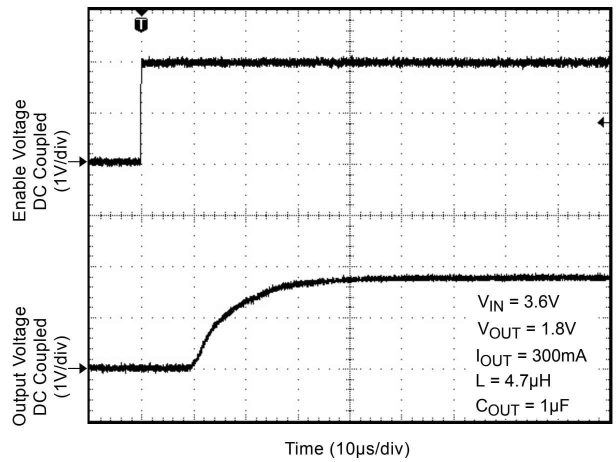


Functional Characteristics

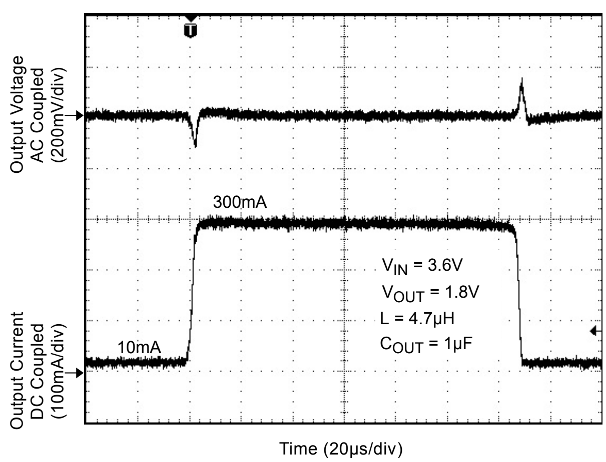
DC/DC PWM Waveforms



DC/DC Start-Up Waveforms

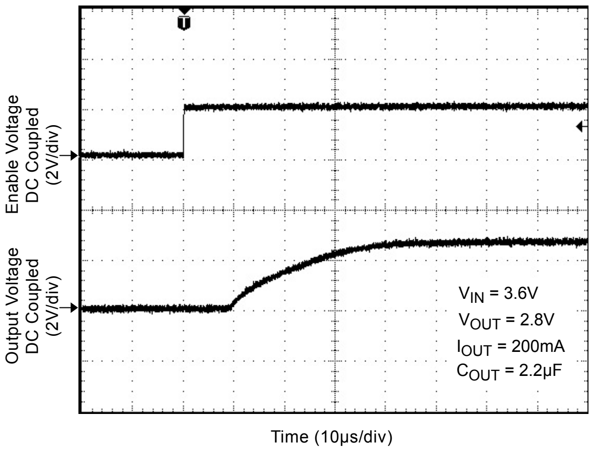


DC/DC Load Transient

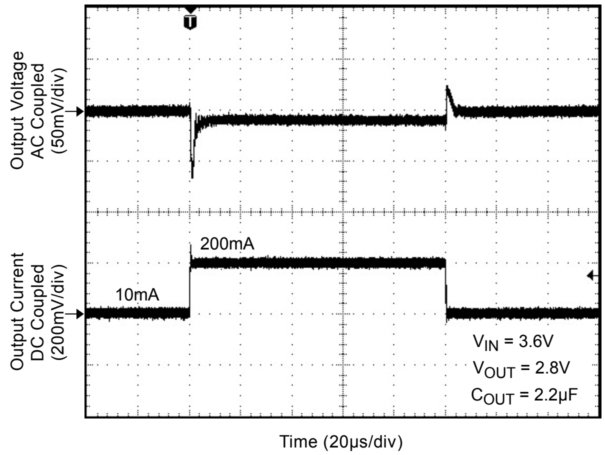


Functional Characteristics (cont.)

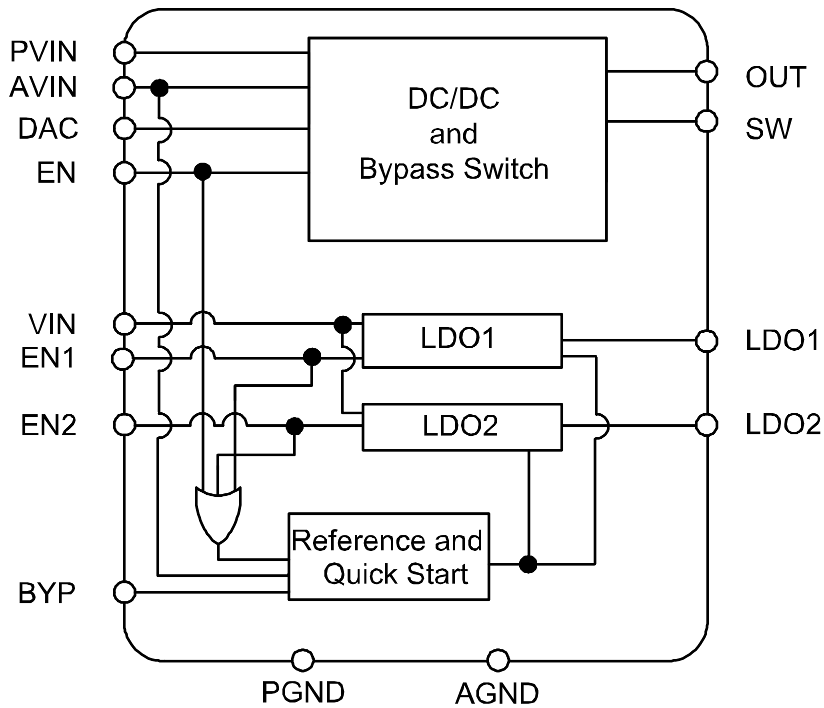
LDO1 Start-Up Waveforms



LDO1 Load Transient



Functional Diagram



MIC2807 Block Diagram

Device Functional Description

The MIC2807 is a power management IC with a single integrated step-down regulator and two low dropout regulators. LDO1 is a 200mA low dropout regulator and LDO2 is a 30mA low dropout regulator. The 500mA pulse-width-modulated (PWM) step-down regulator utilizes a dynamically adjustable output voltage for powering RF power amplifiers. By dynamically adjusting the output power as necessary, battery life can be dramatically improved in battery powered RF power amplifier applications. Also where high power is required, the step-down PWM regulator has a bypass mode where an internal 95mΩ switch shorts the OUT and PVIN pins together.

Pin Functional Description

PVIN

PVIN (Power VIN) provides power to the MOSFETs for the step-down switching regulator section of the MIC2807, along with the current limit sensing circuitry. Due to the high switching speeds, a minimum 1µF capacitor is recommended close to PVIN and the power ground (PGND) pin for bypassing*.

AVIN

AVIN (Analog VIN) provides power to the internal reference and control section of the step-down regulator. AVIN, VIN, and PVIN must all be tied together. Careful layout should be considered to ensure high frequency switching noise caused by PVIN is reduced before reaching AVIN*.

DAC

The DAC pin is the control pin that sets the output voltage of the step-down regulator. The Output voltage is 3X the voltage set on the DAC pin ($V_{OUT} = V_{DAC} \times 3$). When 1.2V or greater is applied to the DAC pin, the MIC2807's step-down regulator enters bypass mode. In bypass mode, the input supply is connected to the output through a 95mΩ P-Channel MOSFET.

EN/EN1/EN2

The EN pin provides a logic level control of the step-down regulator output. In the off state, supply current of the device is greatly reduced (typically ≤1µA). Also, in the off state, the output drive and bypass switch are placed in a "tri-stated" condition, where both the high side P-channel MOSFET and the low-side N-channel are in an off or non-conducting state. EN1 provides logic control for LDO1, and EN2 provides logic control for LDO2. Placing a logic high voltage on any one of the respective enable pins (EN, EN1 or EN2) will turn-on (powering up the bias and control circuitry) that respective regulator (DC/DC, LDO1 or LDO2). Do not drive the enable pins above the supply voltage (AVIN and VIN).

VIN

VIN provides power to the LDO1 and the LDO2 control sections of the MIC2807. A minimum 1µF capacitor, 2.2µF recommended, should be placed as close as possible between the VIN and AGND pins. VIN must have the same voltage as AVIN*.

OUT

The OUT pin connects the internal bypass drain and the feedback signal to the output. The bypass applies the input voltage through a low resistance (95mΩ typical) P-Channel MOSFET switch. The feedback signal provides the control path to set the output at 3 times the DAC voltage.

SW

The SW pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

PGND

PGND (Power GND) is the ground path for the MOSFETs in the step-down regulator section. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop*.

AGND

AGND (Analog GND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop*.

LDO1

Regulated output voltage of the LDO1. Power is provided by VIN. Recommended output capacitance is 2.2µF.

LDO2

Regulated output voltage of the LDO2. Power is provided by VIN. Recommended output capacitance is 1µF.

BYP

Filter capacitor for the voltage reference for the LDO1 and the LDO2. A 100nF capacitor is recommended from the BYP pin to ground.

*** Refer to PCB layout section of this data sheet for optimal layout principles.**

Component Selection

Output Capacitor

LDO1 output requires a 2.2µF ceramic capacitor, while the LDO2 and DC/DC regulator outputs require a 1µF ceramic capacitor. All output capacitor values can be increased to improve transient response, but performance has been optimized for a 2.2µF ceramic capacitor for LDO1 and 1µF ceramic capacitors for both the DC/DC regulator and LDO2. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X5R/X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% to 60% respectively over their operating temperature ranges.

Input Capacitor

For optimal bypassing a minimum 1µF ceramic, 2.2µF recommended, should be placed as close as possible to the VIN pin. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended. For high frequency filtering a minimum 1µF is recommended close to the VIN and PGND pins. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to the PCB layout section for an example of an appropriate circuit layout.

Inductor Selection

The MIC2807 is designed for use with a 4.7µH inductor. Proper selection should ensure that the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin, so that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

$$I_{PK} = I_{OUT} + \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \times f \times L}$$

I_{PK}: Peak Inductor Current

I_{OUT}: Output/Load Current

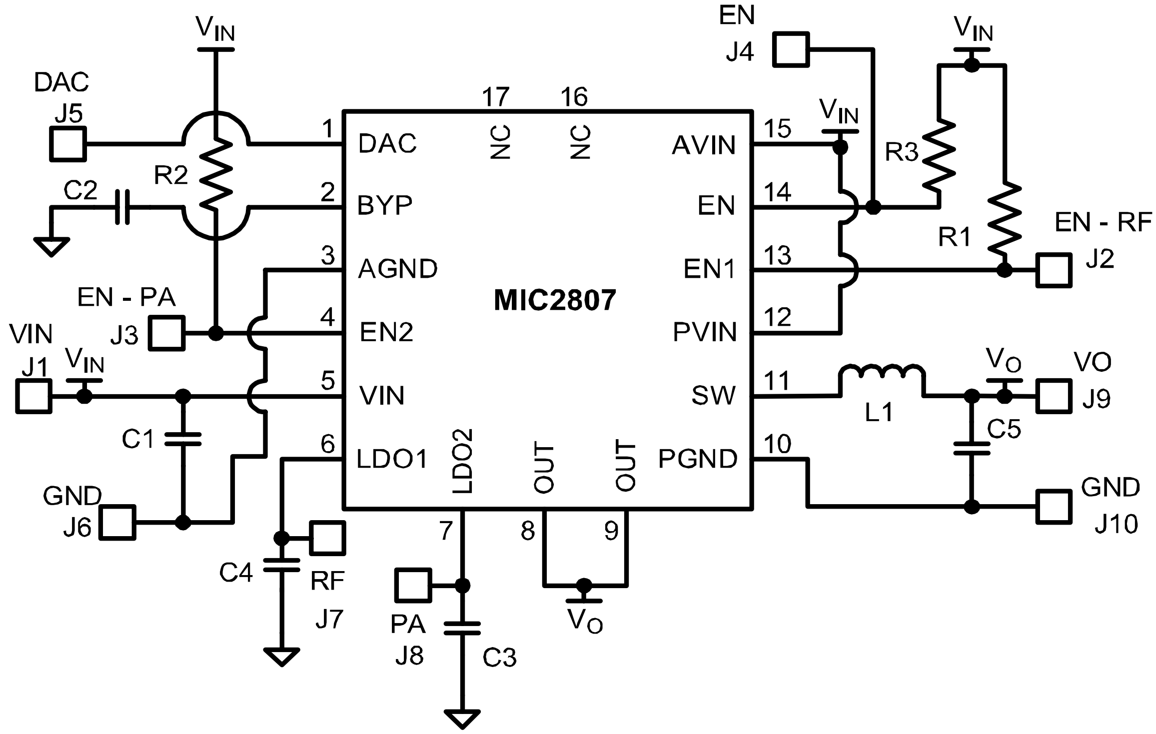
V_{IN}: Input Voltage

V_{OUT}: Output Voltage

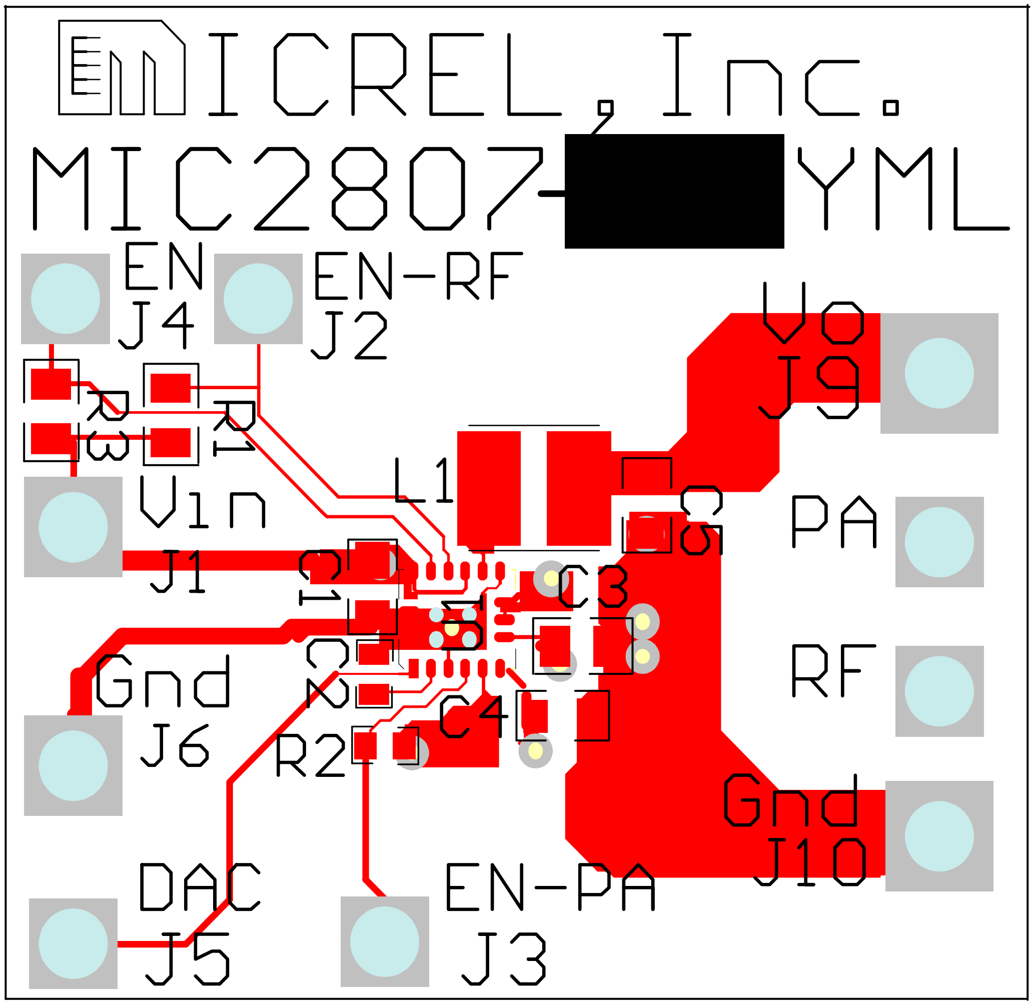
f: Switching Frequency of PWM Regulator

L: Inductor Value

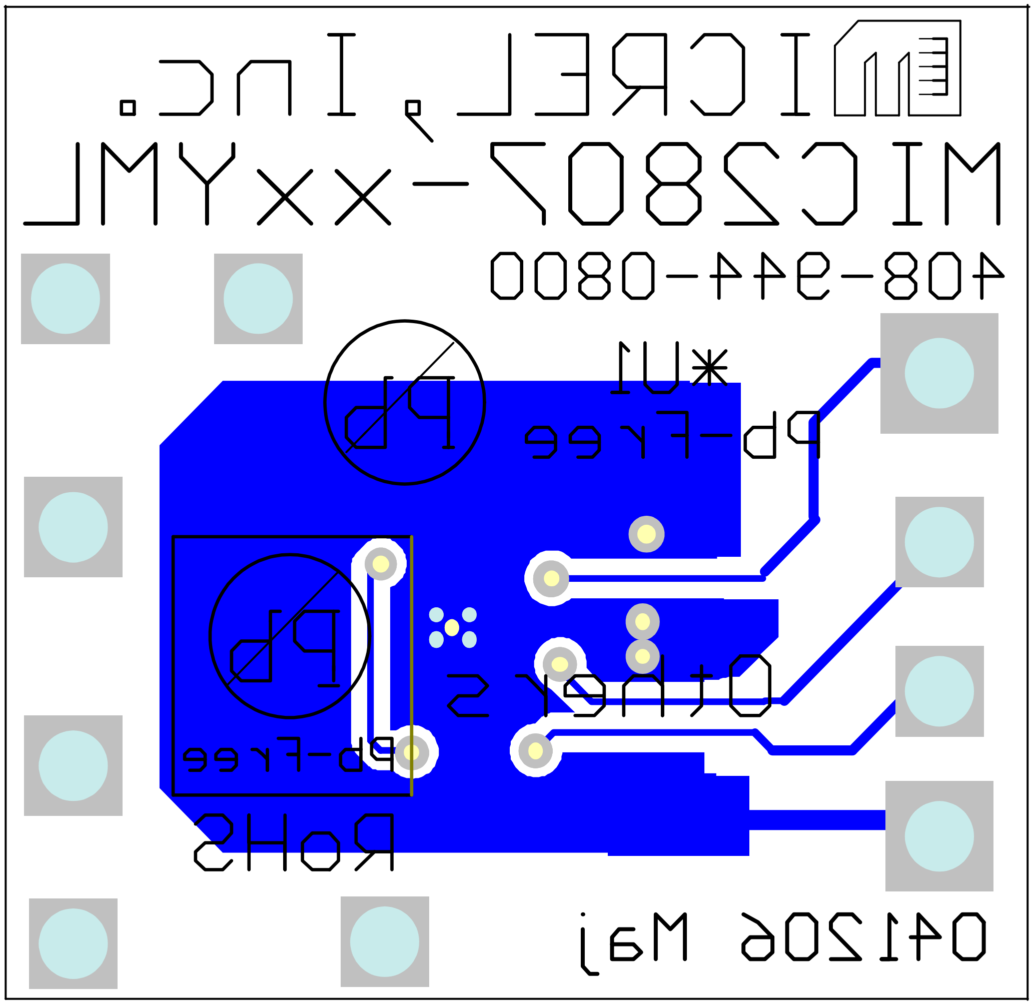
PCB Layout



Layout Schematic

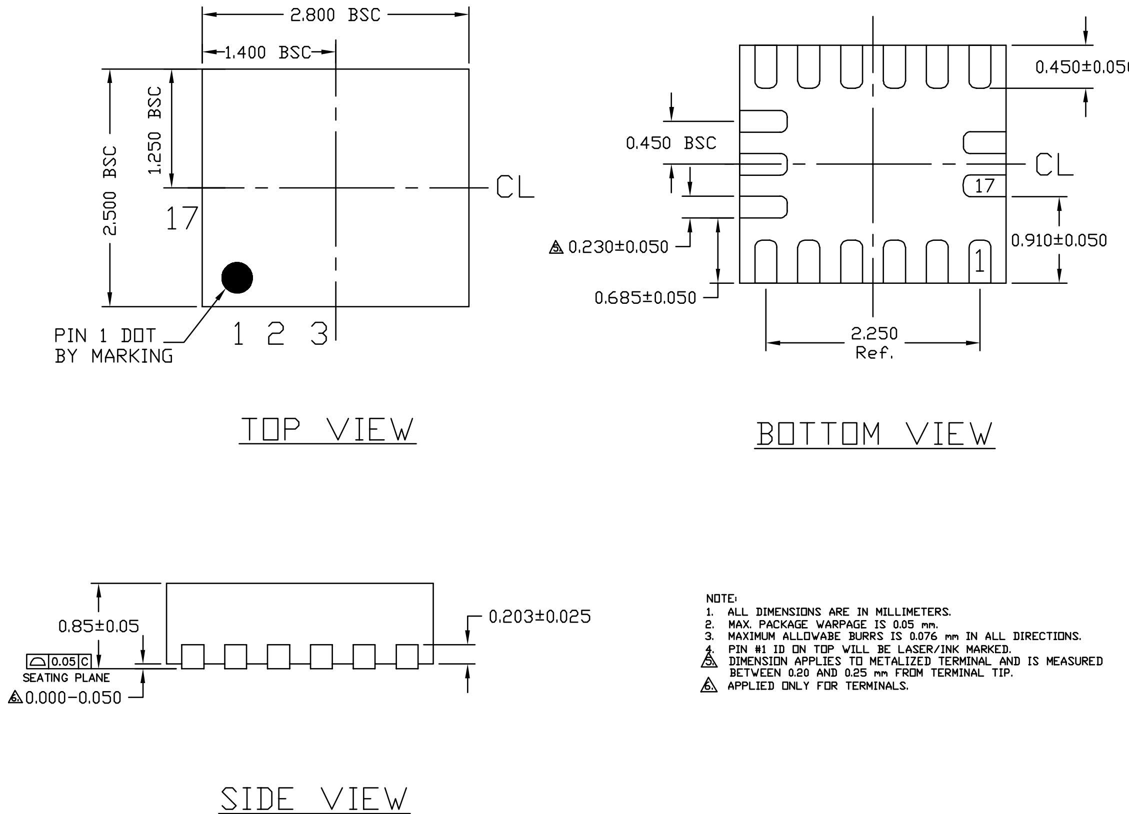

MICREL, Inc.
MIC2807-[redacted]YML
EN
J4
EN-RF
J2
Vo
J9
R3
R1
L1
Vin
J1
C1
C6
C3
PA
RF
C2
Gnd
J6
C4
R2
Gnd
J10
DAC
J5
EN-PA
J3

Top Layer



Bottom Layer

Package Information



17-Pin 2.5mm x 2.8mm MLF® (ML)

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