MH4S72CMA-10,-12,-15

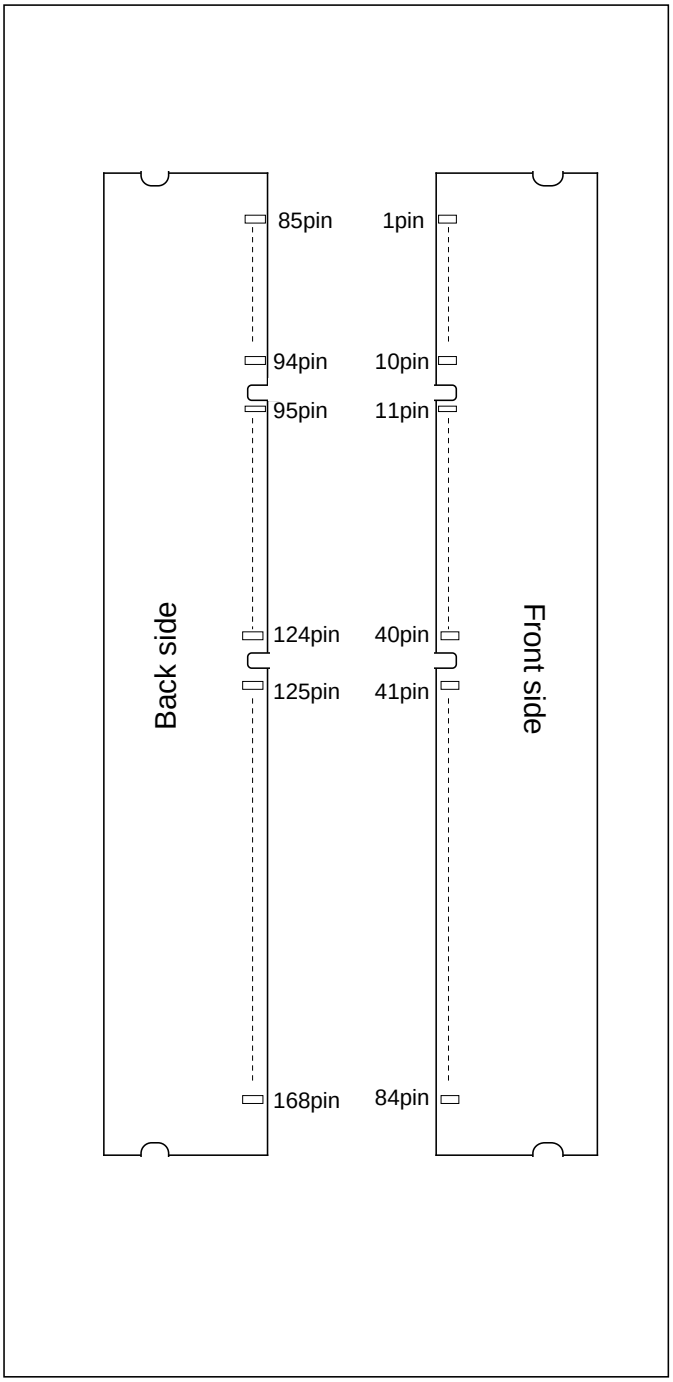
301989888-BIT (4194304-WORD BY 72-BIT)SynchronousDRAM

DESCRIPTION

The MH4S72CMA is 4194304-word by 72-bit Synchronous DRAM module. This consists of eighteen industry standard 2Mx8 Synchronous DRAMs in TSOP and one industory standard EEPROM in TSSOP.

The mounting of TSOP on a card edge Dual Inline package provides any application where high densities and large quantities of memory are required.

This is a socket type - memory modules, suitable for easy interchange or addition of modules.



FEATURES

	Frequency	CLK Access Time (Component SDRAM)
-10	100MHz	8ns(CL=3)
-12	83MHz	8ns (CL=3)
-15	67MHz	9ns (CL=3)

- Utilizes industry standard 2M x 8 Synchronous DRAMs TSOP and industry standard EEPROM in TSSOP
- 168-pin (84-pin dual in-line package)
- single 3.3V±0.3V power supply
- Clock frequency 100MHz/83MHz/67MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA(Bank Address)
- /CAS latency- 1/2/3(programmable)
- Burst length- 1/2/4/8(programmable)
- Burst type- sequential / interleave(programmable)
- Column access - random
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycle /64ms
- LVTTL Interface

APPLICATION

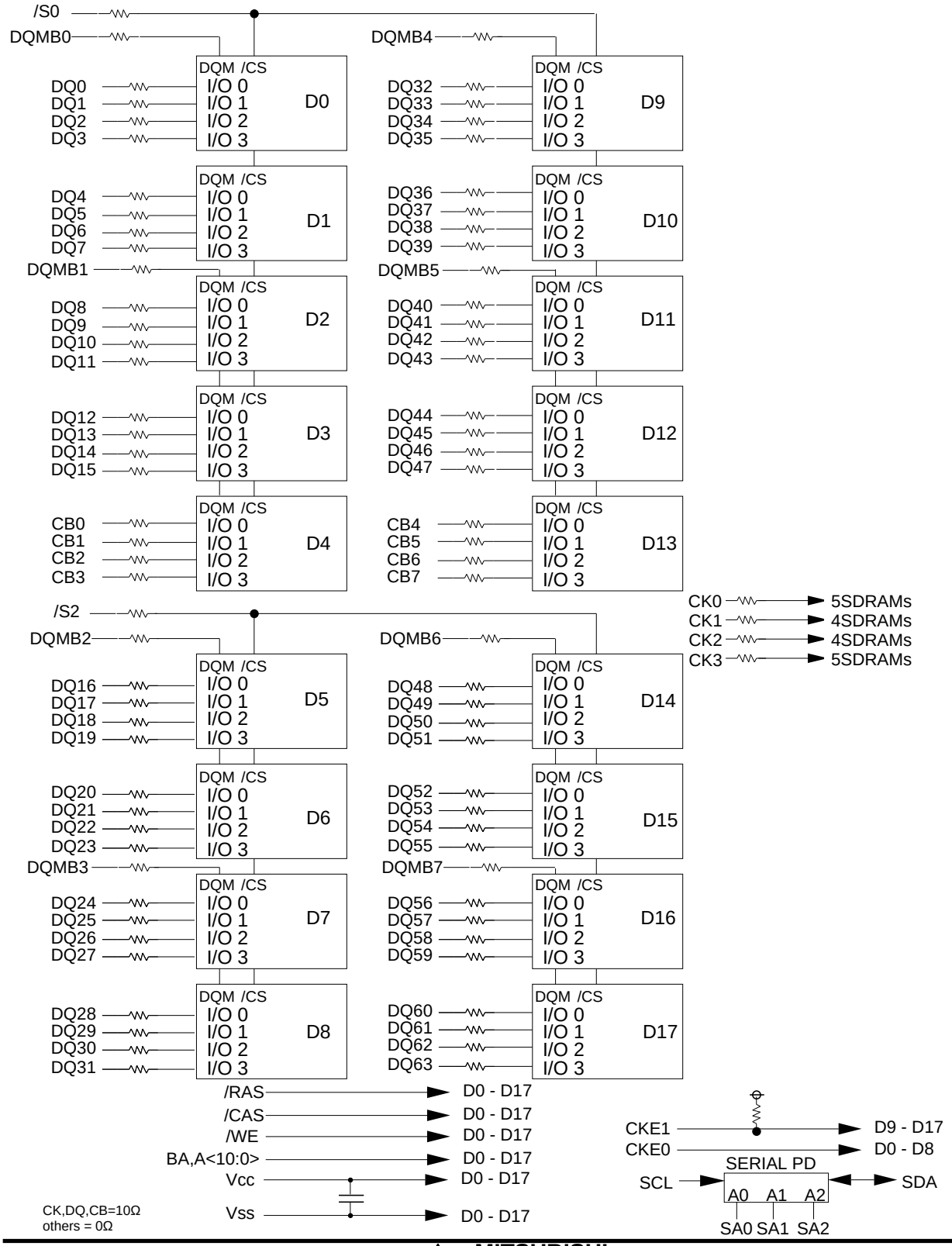
main memory or graphic memory in computer systems

Module item "-10","-12" , and "-15" show mounted SDRAM devices Cycle time(min.).

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	NC	90	VDD	132	NC
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	/WE0	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	NC	156	DQ59
31	NC	73	VDD	115	/RAS	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA	164	NC
39	NC	81	NC	123	NC	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	NC	168	VDD

NC = No Connection

Block Diagram



Serial Presence Detect Table

Byte	Function described		SPD enrty data	SPD DATA(hex)
0	Defines # bytes written into serial memory at module mfgr		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		SDRAM	04
3	# Row Addresses on this assembly		A0-A10	0B
4	# Column Addresses on this assembly		A0-A9	0A
5	# Module Banks on this assembly		1BANK	01
6	Data Width of this assembly...		x72	48
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		LVTTL	01
9	SDRAM Cycletime at Max. Supported CAS Latency (CL).	-10	10ns	A0
	Cycle time for CL=3	-12	12ns	C0
		-15	15ns	F0
10	SDRAM Access from Clock	-10	8ns	80
	tAC for CL=3	-12	8ns	80
		-15	9ns	90
11	DIMM Configuration type (Non-parity,Parity,ECC)		ECC	02
12	Refresh Rate/Type		self refresh(15.625uS)	80
13	SDRAM width,Primary DRAM		x4	04
14	Error Checking SDRAM data width		x4	04
15	Minimum Clock Delay,Back to Back Random Column Addresses		1	01
16	Burst Lengths Supported		1/2/4/8	0F
17	# Banks on Each SDRAM device		2bank	02
18	CAS# Latency		CL=1/2/3	06
19	CS# Latency		0	01
20	Write Latency		0	01
21	SDRAM Module Attributes		non-buffered,non-registered	00
22	SDRAM Device Attributes:General		Precharge All,Auto precharge	06
23	SDRAM Cycle time(2nd highest CAS latency)	-10	15ns	F0
	Cycle time for CL=2	-12	15ns	F0
		-15	20ns	FF
24	SDRAM Access form Clock(2nd highest CAS latency)	-10	9ns	90
	tAC for CL=2	-12	9.5ns	95
		-15	12ns	C0
25	SDRAM Cycle time(3rd highest CAS latency)	-10	30ns	78
	Cycle time for CL=1	-12	30ns	78
		-15	30ns	78
26	SDRAM Access form Clock(3rd highest CAS latency)	-10	27ns	6C
	tAC for CL=1	-12	27ns	6C
		-15	30ns	78
27	Precharge to Active Minimum	-10	30ns	1E
		-12	30ns	1E
		-15	40ns	28
28	Row Active to Row Active Min.	-10	20ns	14
		-12	24ns	18
		-15	30ns	1E

Serial Presence Detect Table

29	RAS to CAS Delay Min	-10	30ns	1E
		-12	30ns	1E
		-15	30ns	1E
30	Active to Precharge Min	-10	60ns	3C
		-12	70ns	46
		-15	80ns	50
31	Density of each bank on module		32MByte	08
32-61	Superset Information (may be used in future)		option	00
62	SPD Revision		rev 1	01
63	Checksum for bytes 0-62		Check sum for -10	AE
			Check sum for -12	E1
			Check sum for -15	81
64-71	Manufactures Jedec ID code per JEP-108E		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufactures Part Number		MH4S72CMA-10	4D4834533732434D412D3130202020202020
			MH4S72CMA-12	4D4834533732434D412D3132202020202020
			MH4S72CMA-15	4D4834533732434D412D3135202020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yyww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacture Specific Data		option	00
126	Intetl specification frequency		66MHz	66
127	Intel specification CAS# Latency support		CL=3: 04H, CL=2/3: 06H	06
128+	Unused storage locations		open	00

PIN FUNCTION

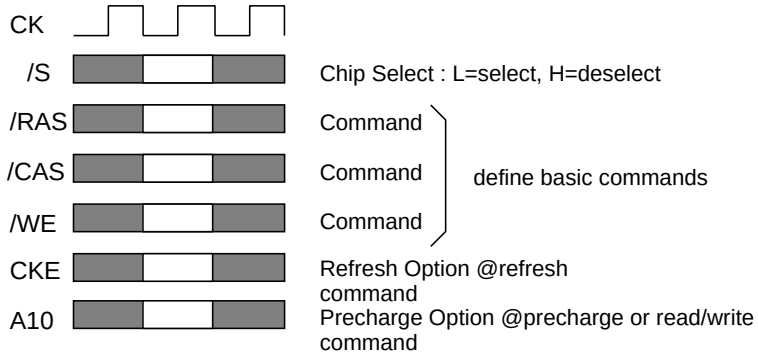
CK (CK0 ~ CK3)	Input	Master Clock:All other inputs are referenced to the rising edge of CK
CKE0,1	Input	Clock Enable:CKE controls internal clock.When CKE is low,internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE E becomes asynchronous input.Self refresh is maintained as long as CKE is low.
/S (/S0 & /S2)	Input	Chip Select: When /S is high,any command means No Operation.
/RAS,/CAS,/WE	Input	Combination of /RAS,/CAS,/WE defines basic commands.
A0-10	Input	A0-10 specify the Row/Column Address in conjunction with BA.The Row Address is specified by A0-10.The Column Address is specified by A0-9.A10 is also used to indicate precharge option.When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, both banks are precharged.
BA	Input	Bank Address:BA is not simply BA.BA specifies the bank to which a command is applied.BA must be set with ACT,PRE,READ,WRITE commands
DQ0-63	Input/Output	Data In and Data out are referenced to the rising edge of CK
CB0-7	Input/Output	Check bit data In and Check bit data out are referenced to the rising edge of CK
DQMB0-7	Input	Din Mask/Output Disable:When DQMB is high in burst write.Din for the current cycle is masked.When DQMB is high in burst read,Dout is disabled at the next but one cycle.
Vdd,Vss	Power Supply	Power Supply for the memory mounted module.
SCL	Input	Serial clock for serial PD
SDA	Output	Serial data for serial PD
SA0-3	Input	Address input for serial PD

BASIC FUNCTIONS

The MH4S72CMA provides basic functions,bank(row)activate,burst read / write, bank(row)precharge,and auto / self refresh.

Each command is defined by control signals of /RAS,/CAS and /WE at CK rising edge. In addition to 3 signals,/S,CKE and A10 are used as chip select,refresh option,and precharge option,respectively.

To know the detailed definition of commands please see the command truth table.



Activate(ACT) [/RAS =L, /CAS = /WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read(READ) [/RAS =H,/CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA.First output data appears after /CAS latency. When A10 =H at this command,the bank is deactivated after the burst read(auto-precharge,**READA**).

Write(WRITE) [/RAS =H, /CAS = /WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write(auto-precharge,**WRITEA**).

Precharge(PRE) [/RAS =L, /CAS =H,/WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated(precharge all, **PREA**).

Auto-Refresh(REFA) [/RAS =/CAS =L, /WE =CKE =H]

PEFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CK n-1	CK n	/S	/RAS	/CAS	/WE	BA	A10	A0-9
Deselect	DESEL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Row Adress Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X
Precharge All Bank	PREA	H	X	L	L	H	L	V	H	X
Column Address Entry & Write	WRITE	H	X	L	LH	H	L	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V
Column Address Entry & Read with Auto Precharge	READA	H	X	L	H	L	H	V	H	V
Auto-Refresh	REFA	H	H	L	HL	L	H	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X
Self-Refresh Exit	REFSX	L	H	H	LX	X	X	X	X	X
		L	H	L	H	H	H	X	X	X
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V*1

H =High Level, L = Low Level, V = Valid, X = Don't Care, n = CK cycle number

NOTE:
1.A7-9 = 0, A0-6 = Mode Address

FUNCTION TRUTH TABLE

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	Bank Active,Latch RA
	L	L	H	L	BA,A10	PRE/PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA,CA,A10	READ/READA	Begin Read,Latch CA, Determine Auto-Precharge
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	Begin Write,Latch CA, Determine Auto-Precharge
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA,CA,A10	READ/READA	Terminate Burst,Latch CA, Begin New Read,Determine Auto-Precharge*3
	L	H	L	L	BA,CA,A10	WRITE/WRITEA	Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Terminate Burst,Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA,CA,A10	READ/READA	Terminate Burst,Latch CA, Begin Read,Determine Auto-Precharge*3
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Terminate Burst,Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP(Idle after tRP)
	L	H	H	H	X	NOP	NOP(Idle after tRP)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP(Row Active after tRCD
	L	H	H	H	X	NOP	NOP(Row Active after tRCD
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
RE-	H	X	X	X	X	DESEL	NOP(Idle after tRC)
FRESHING	L	H	H	H	X	NOP	NOP(Idle after tRC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE	H	X	X	X	X	DESEL	NOP(Idle after tRSC)
REGISTER	L	H	H	H	X	NOP	NOP(Idle after tRSC)
SETTING	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:
H = Hige Level, L = Low Level, X = Don't Care
BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state.May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and / or date-integrity are not guaranteed.

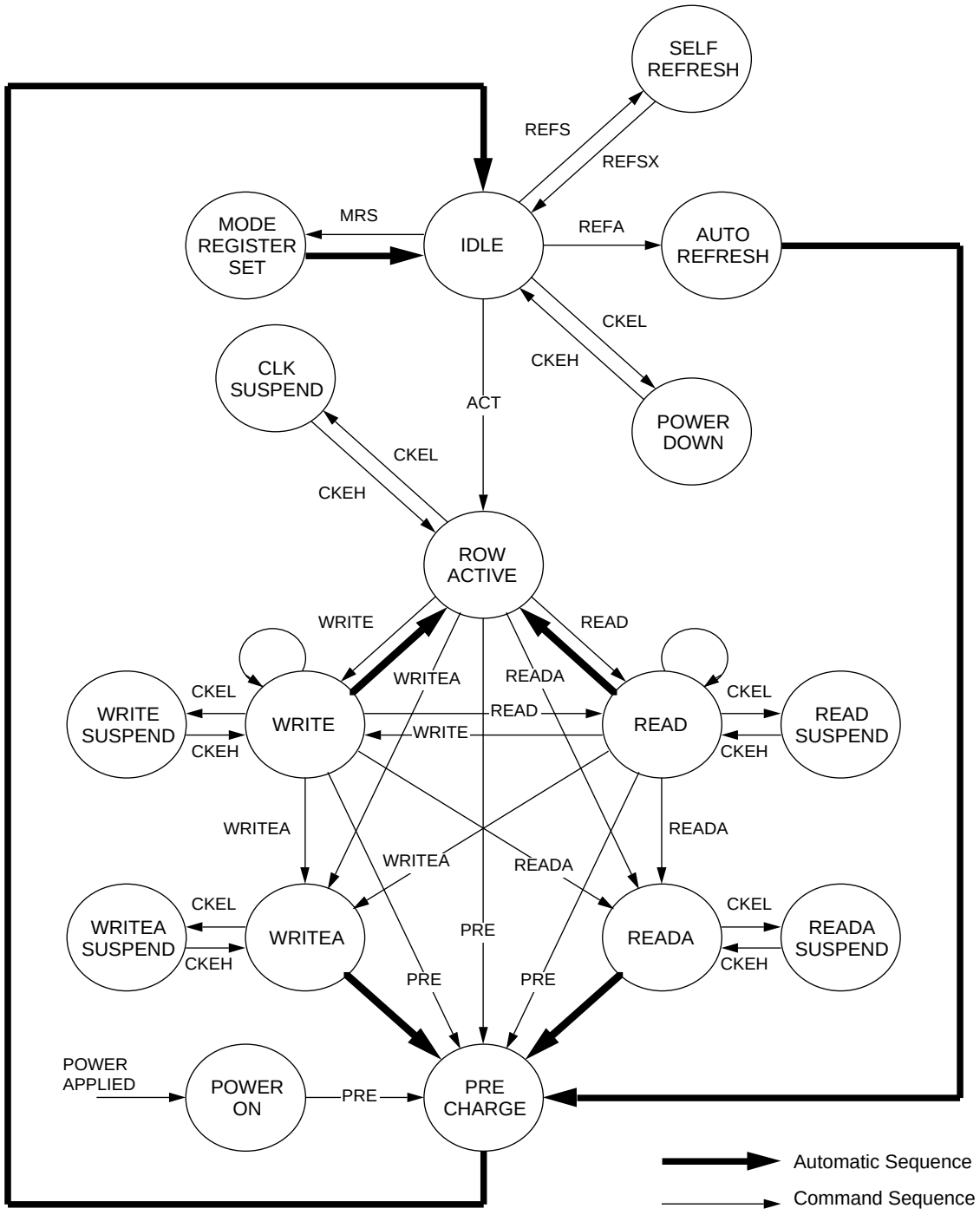
FUNCTION TRUTH TABLE FOR CKE

Current State	CK n-1	CK n	/S	/RAS	/CAS	/WE	Add	Action
SELF - REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh(Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh(Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State = Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CK0 Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CK0 Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CK0 Suspend

ABBREVIATIONS:
H = High Level, L = Low Level, X = Don't Care

NOTES:
1. CKE Low to High transition will re-enable CK and other inputs **asynchronously**.
   A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only form the All banks idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

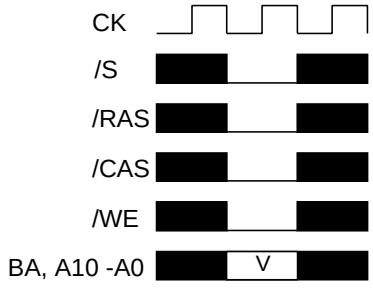
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQMB0-7 high and NOP condition at the inputs.
2. Maintain stable power, stable cock, and NOP input conditions for a minimum of 500É s.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register(MRS). The mode register stores these date until the next MRS command, which may be issue when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



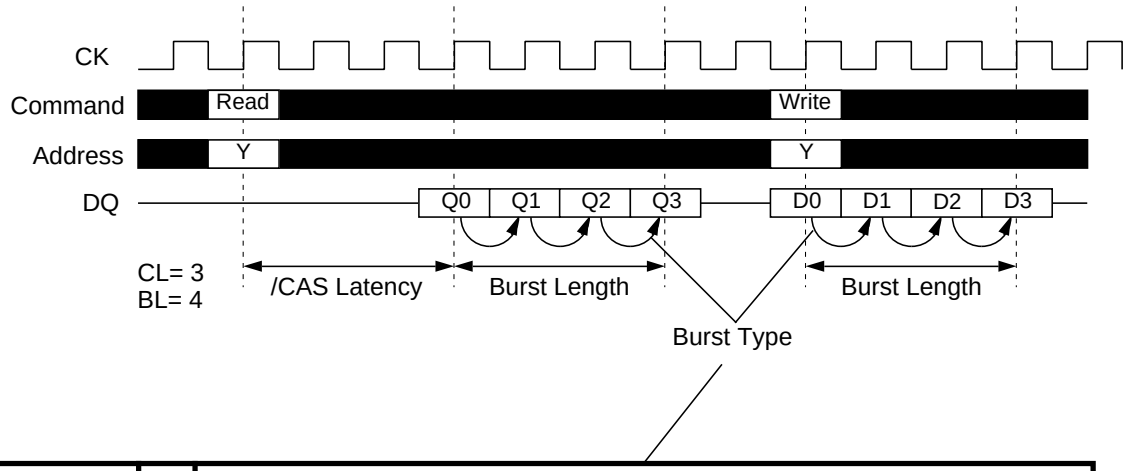
BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	LTMODE			BT	BL		

	CL	/CAS LATENCY
LATENCY MODE	0 0 0	R
	0 0 1	1
	0 1 0	2
	0 1 1	3
	1 0 0	4
	1 0 1	R
	1 1 0	R
	1 1 1	R

	BL	BT= 0	BT= 1
BURST LENGTH	0 0 0	1	1
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	R	R

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

R:Reserved for Future Use



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATION DESCRIPTION

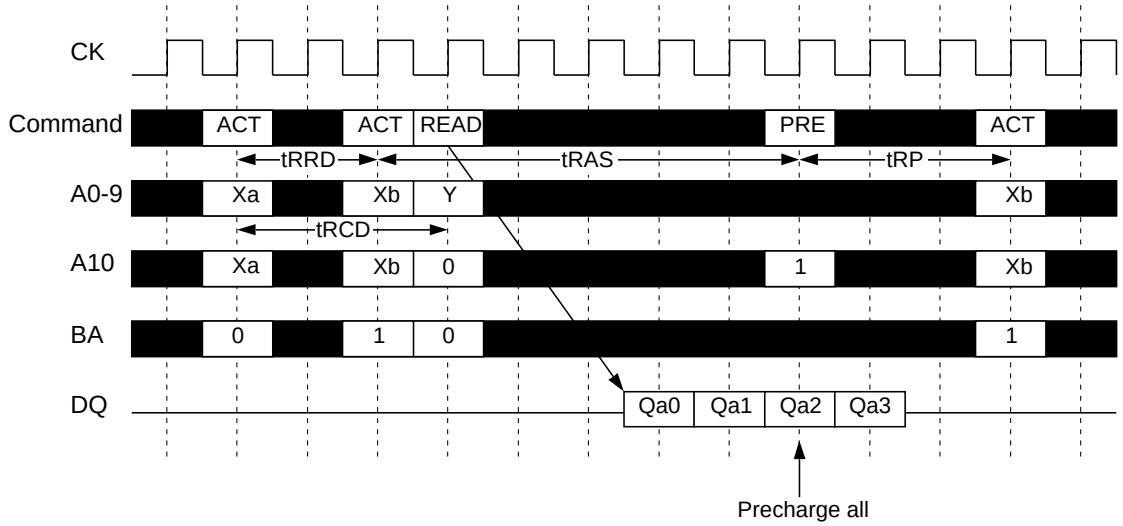
BANK ACTIVATE

The SDRAM has two independent banks. Each bank is activated by the ACT command with the bank address(BA). A row is indicated by the row address A10-0. The minimum activation interval between one bank and the other bank is tRRD.

PRECHARGE

The PRE command deactivates indicated by BA. When both banks are active, the precharge all command(PREA,PRE + A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command can be issued.

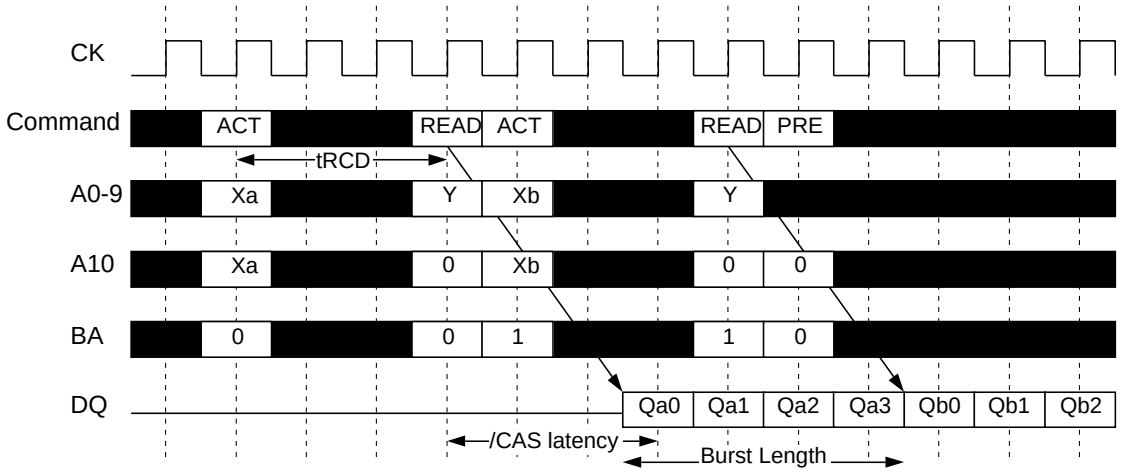
Bank Activation and Precharge All (BL=4, CL=3)



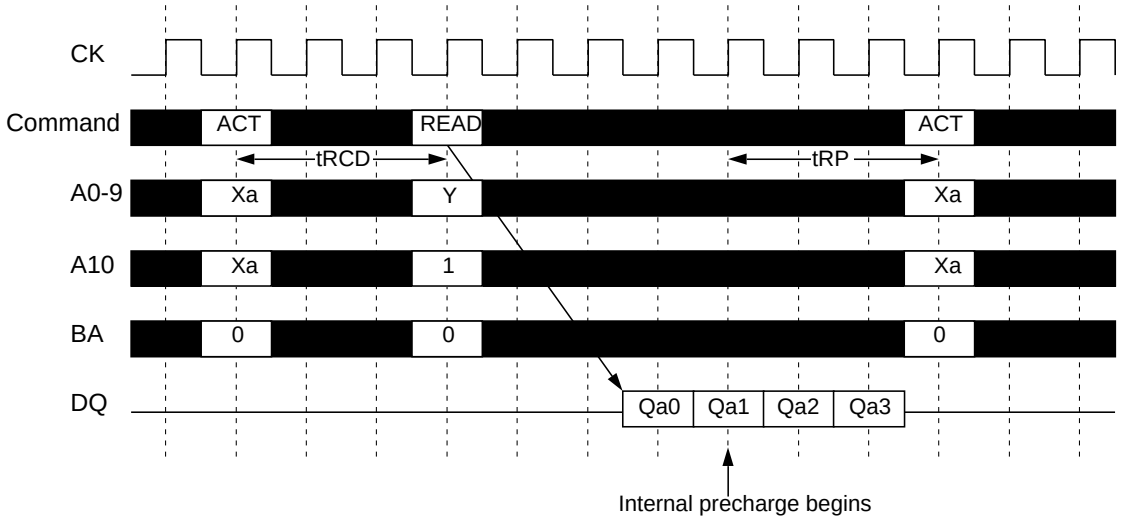
READ

After tRCD from the bank activation, a READ command can be issued. 1st output date is available after the /CAS Latency from the READ, followed by (BL-1) consecutive date when the Burst Length is BL. The start address is specified by A8-0, and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time(tRP) can be hidden behind continuous output data(in case of BL=8) by interleaving the dual banks. When A10 is high at a READ command, the auto-precharge(READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge start timing depends on /CAD Latency. The next ACT command can be issued after tRP from the internal precharge timing.

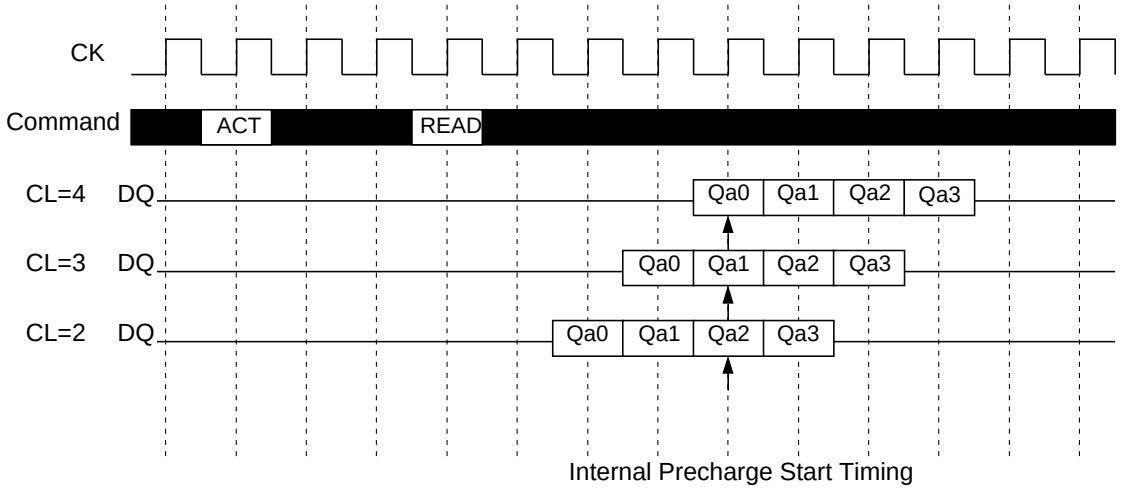
Dual Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



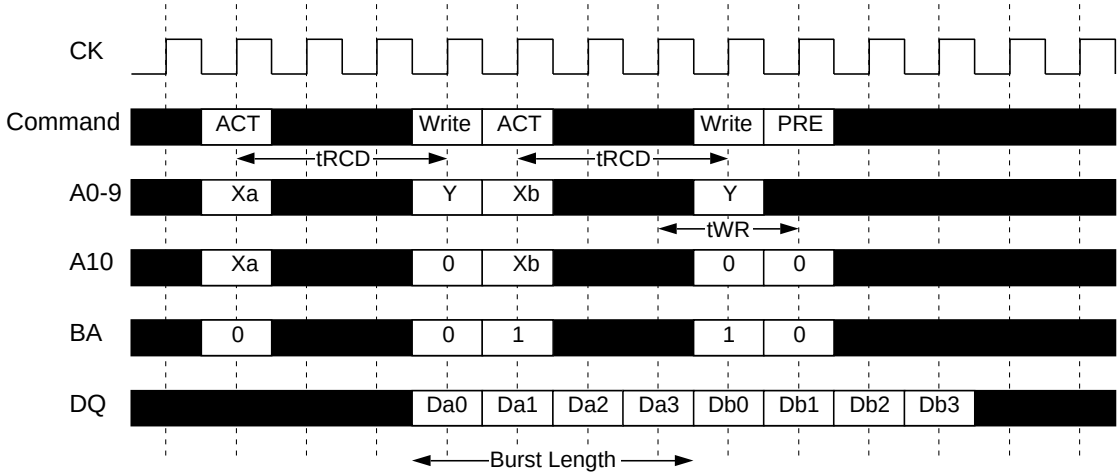
READ Auto-Precharge Timing (BL=4)



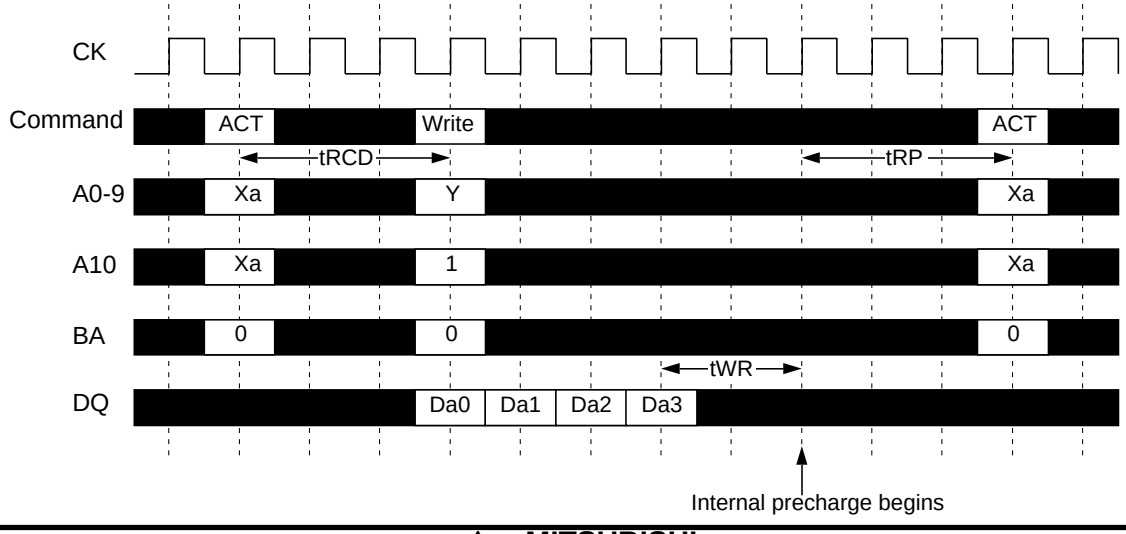
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following(BL-1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A8-0, and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time(tRP) can be hidden behind continuous input data (in case of BL=8) by interleaving the dual banks. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, the auto-precharge(WRITEA) is performed. Any command(READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. The next ACT command can be issued after tRP from the internal precharge timing.

Dual Bank Interleaving WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

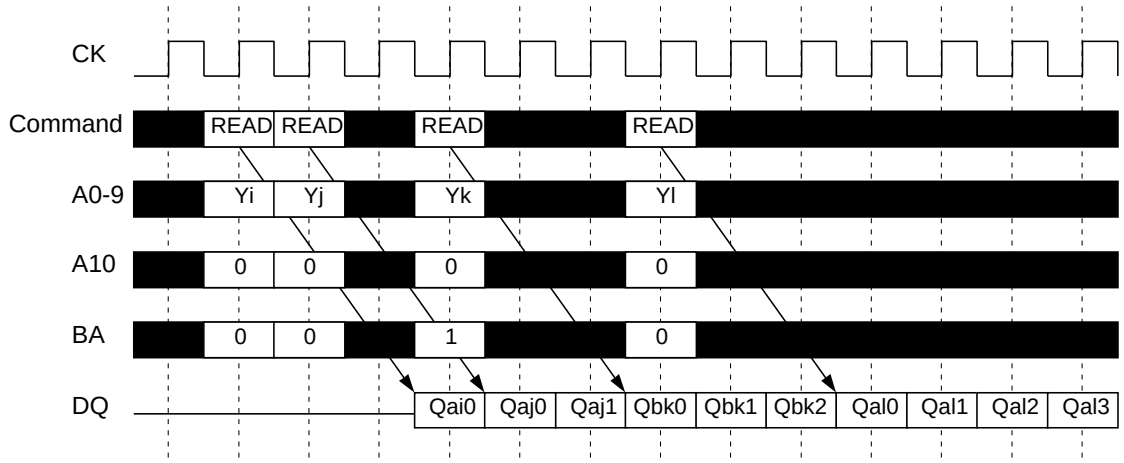


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read option can be interrupted by new read of the same or the other bank. MH4S72CMA allows random column access. READ to READ interval is minimum 1 CK

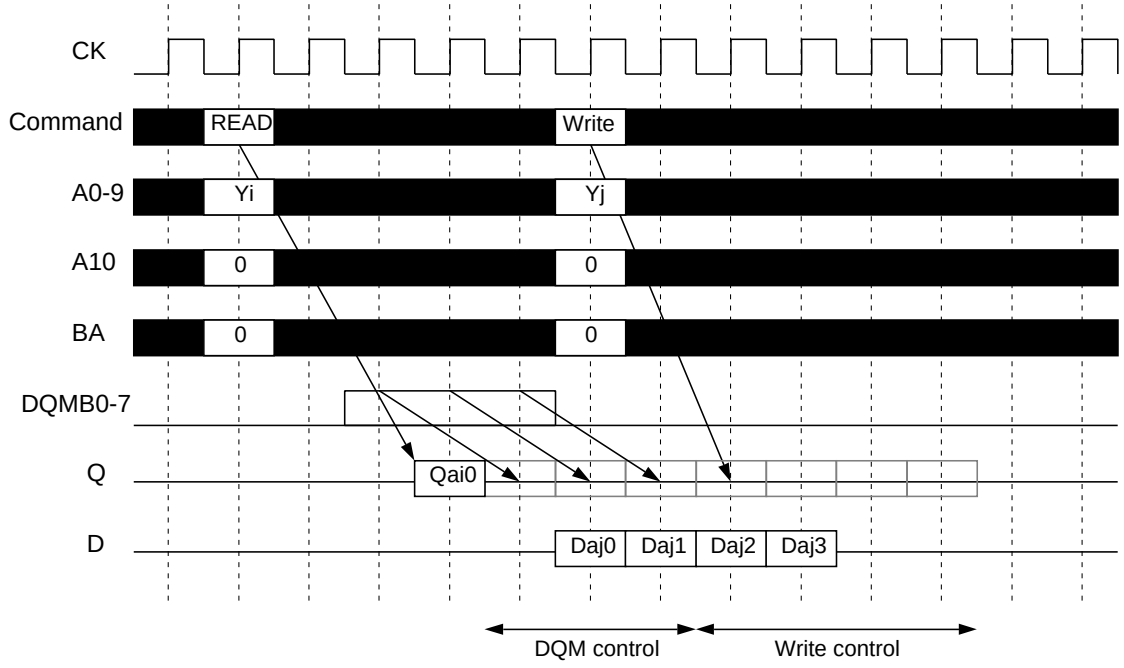
Read Interrupted by Read (BL=4, CL=3)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of the same or the other bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQMB0-7 to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.

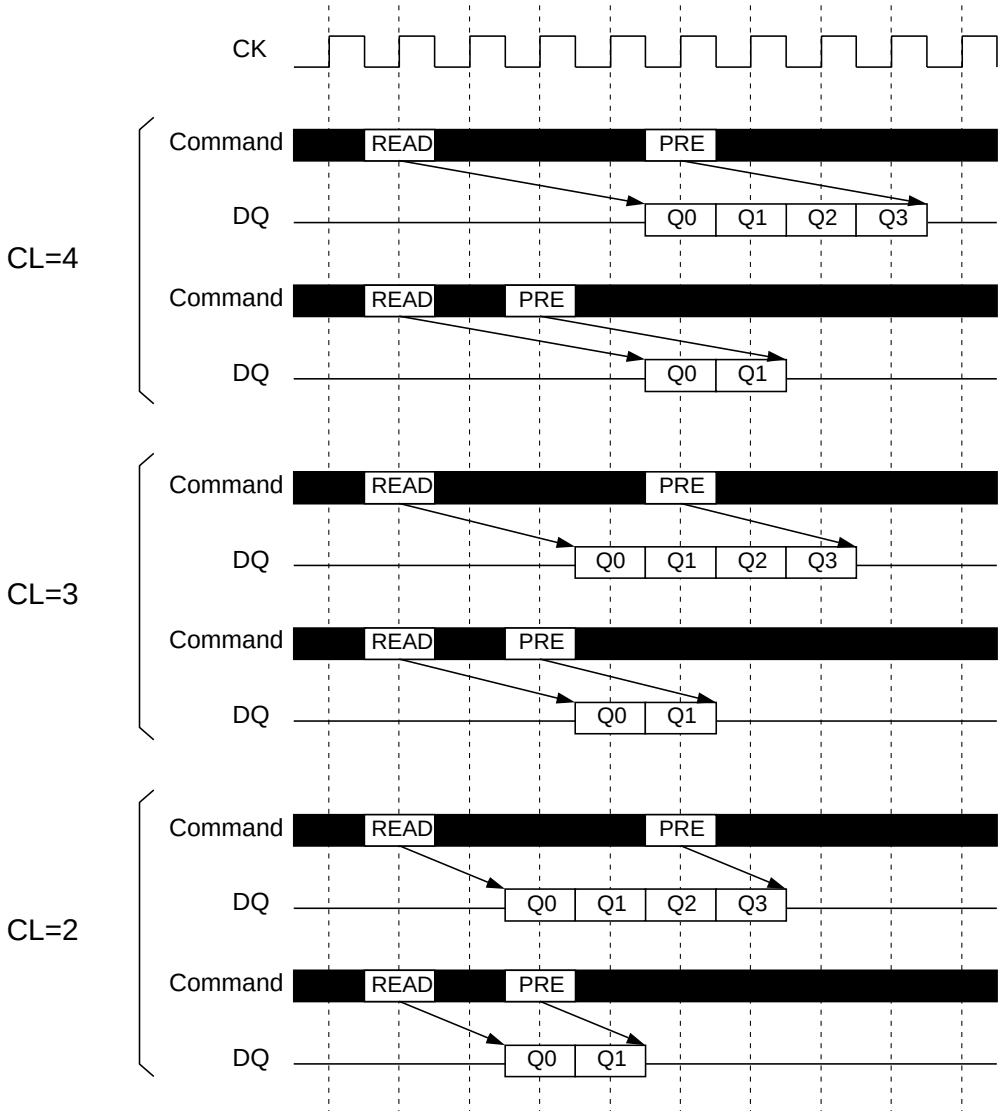
Read Interrupted by Write (BL=4, CL=3)



[Read Interrupted by Precharge]

Burst read operation can be interrupted by precharge of the same or the other bank. Read to PRE interval is minimum 1 CK. A PRE command disables the data output, depending on the /CAS Latency. The figure below shows examples, when the dataout is terminated.

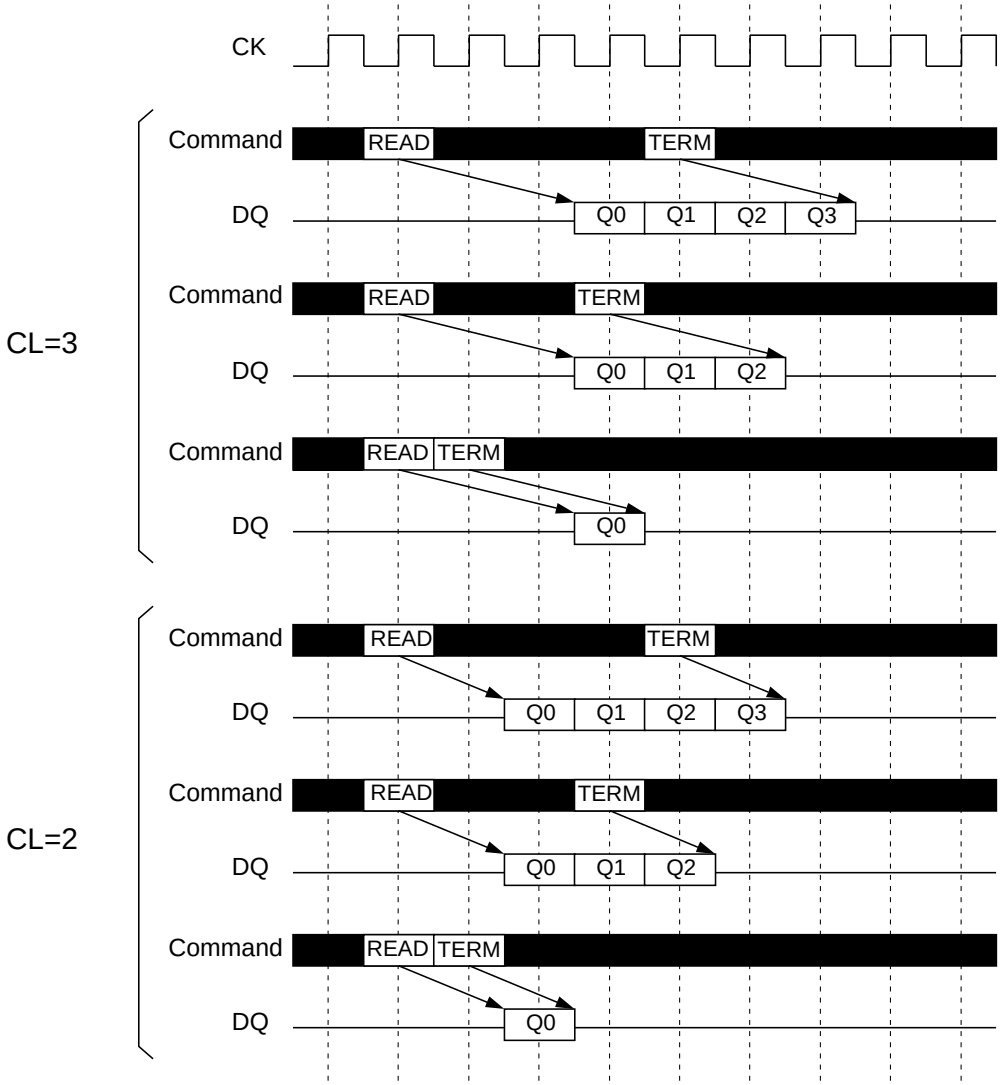
Read Interrupted by Precharge (BL=4)



[Read Interrupted by Burst Terminate]

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. READ to TERM interval is minimum 1 CK. The figure below shows examples, when the dataout is terminated.

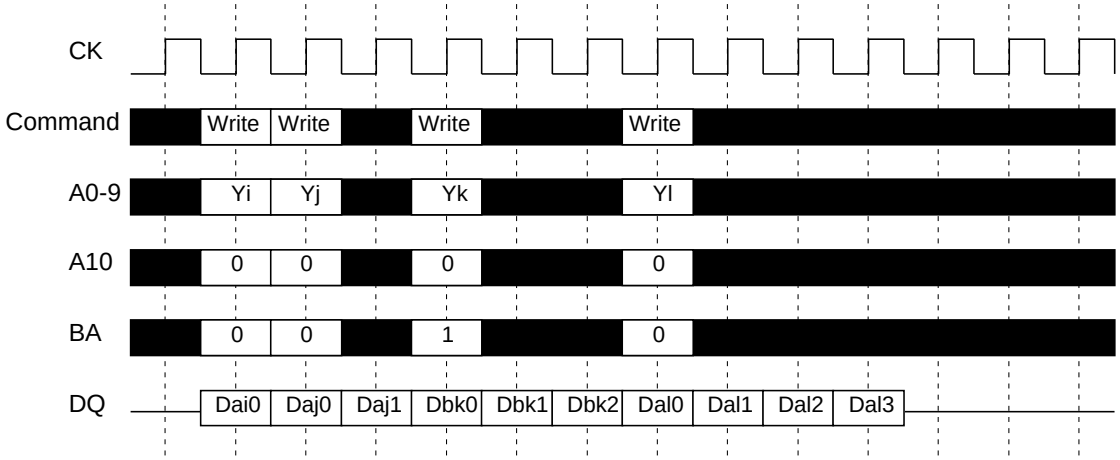
Read Interrupted by Burst Terminate (BL=4)



[Write Interrupted by Write]

Burst write operation can be interrupted by new write of the same or the other bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CK.

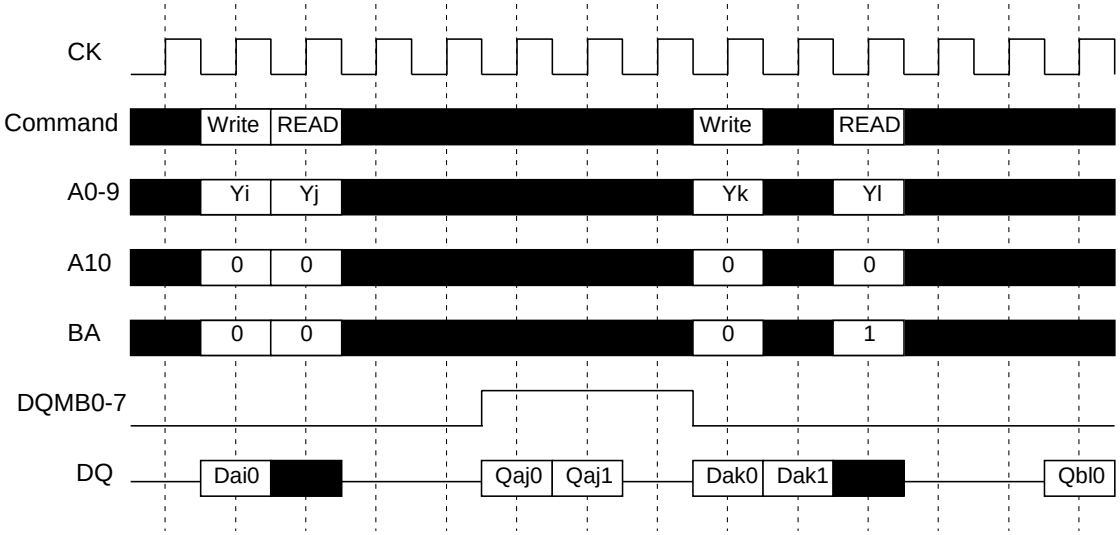
Write Interrupted by Write (BL=4)



[Write Interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CK. The input data on DQ at the interrupting READ cycle is "don't care".

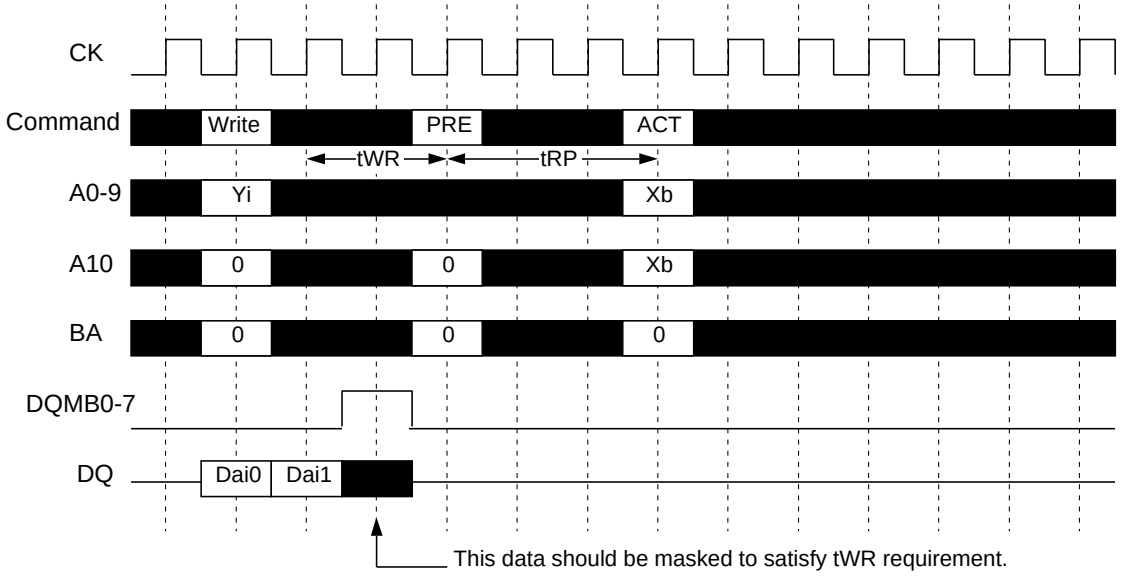
Write Interrupted by Read (BL=4, CL=3)



[Write Interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same bank. Random column access is allowed. Because the write recovery time(tWR) is required between the last input data and the next PRE, 3rd data should be masked with DQMB0-7 shown as below.

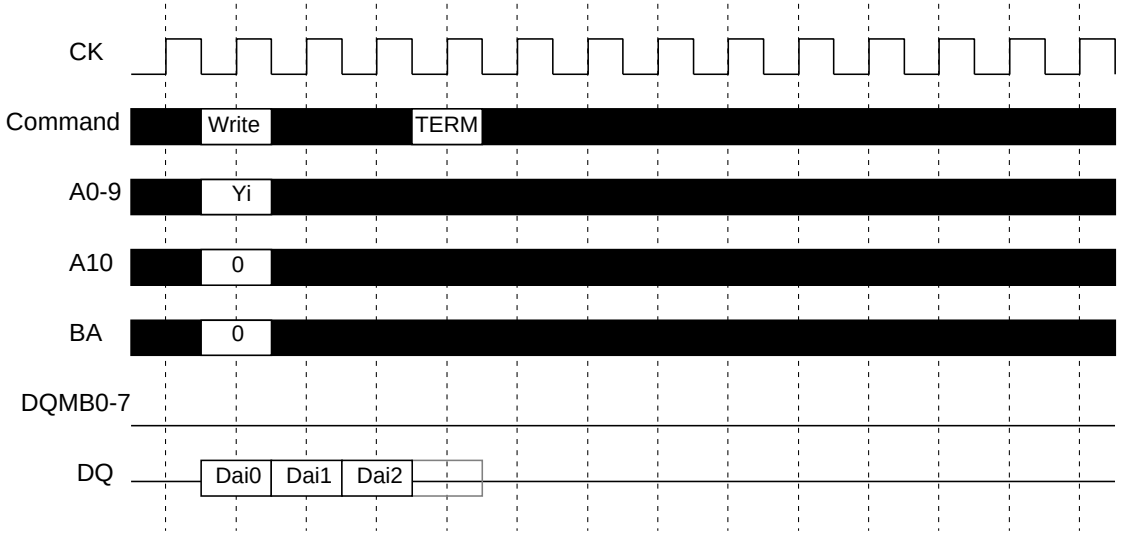
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case 3 words of data are written. Random column access is allowed. WRITE to TERM interval is minimum 1 CK.

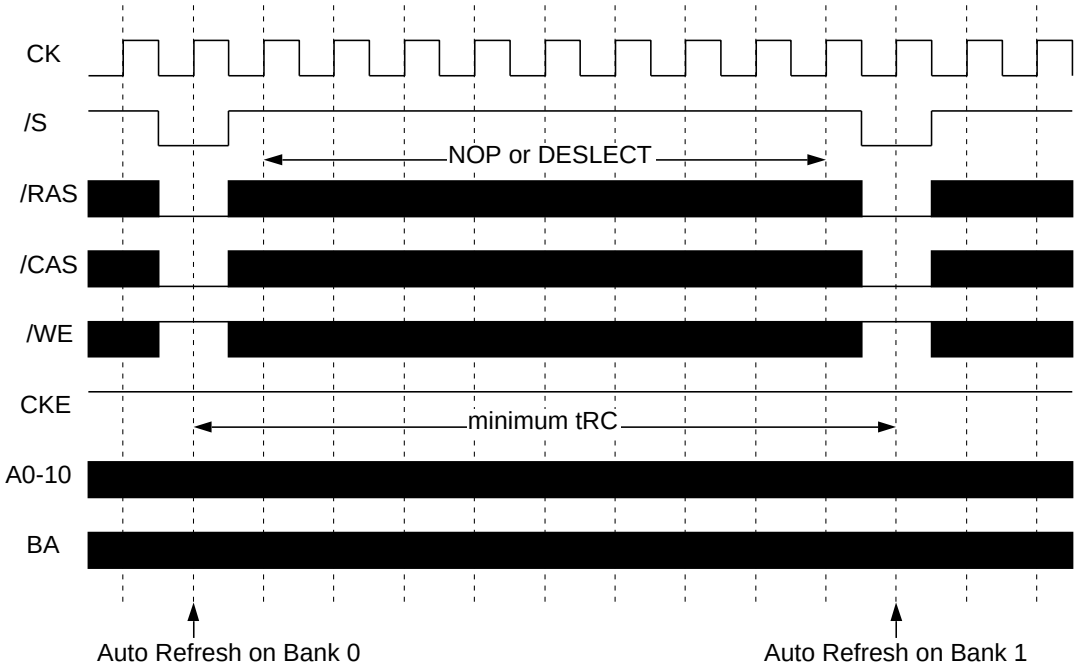
Write Interrupted by Burst Terminate (BL=4)



AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L, /WE=/CKE=H) command. The refresh address is generated internally. 4096 REFA cycle within 64ms refresh 16Mbit memory cells. The auto-refresh is performed on each bank alternately(ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before tRC from the REFA command.

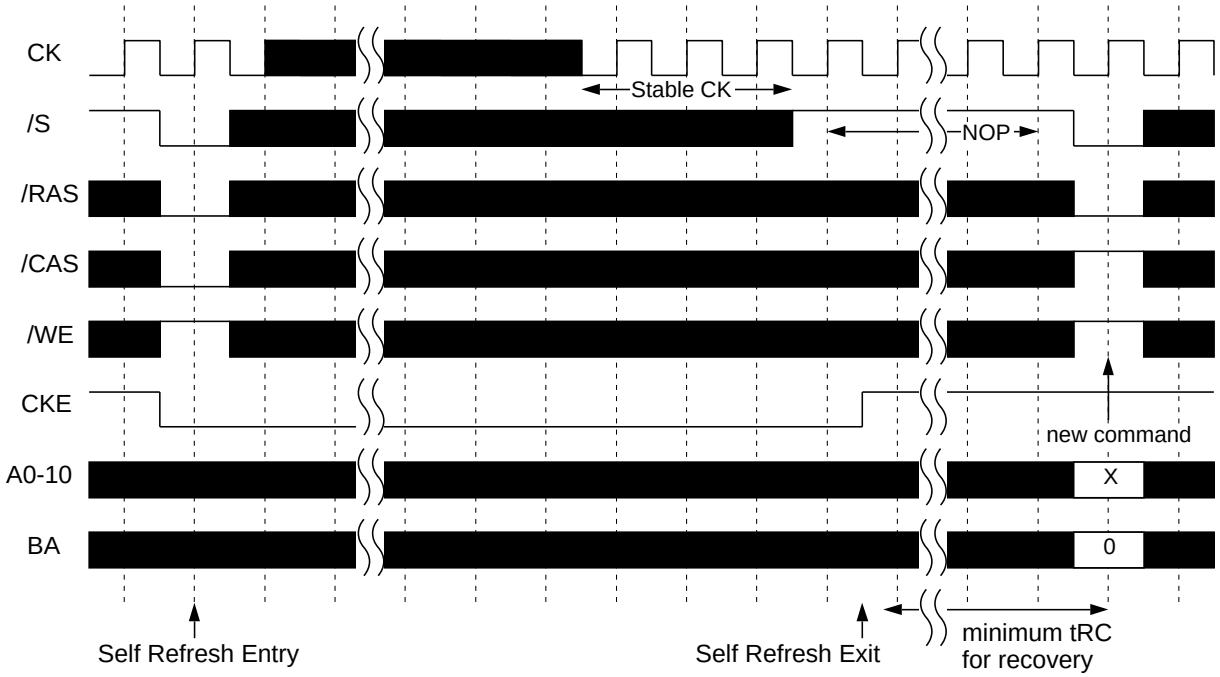
Auto-Refresh



SELF REFRESH

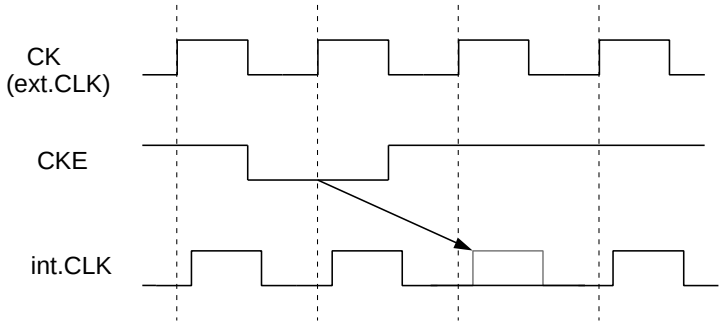
Self-refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L, /WE=H, CKE=L). Once the self-refresh is initiated, it is maintained as log as CKE is kept low.During the self-refresh mode, CKE is asynchronous and the only enabled input (but asynchronous), all other inputs including CK0 are disabled and ignored, and power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CK0 inputs, asserting DESEL or NOP command and then asserting CKE(REFSX). After tRC from REFSX both banks are in the idle state and a new command can be issued after tRC, but DESEL or NOP commands must be asserted till then.

Self-Refresh

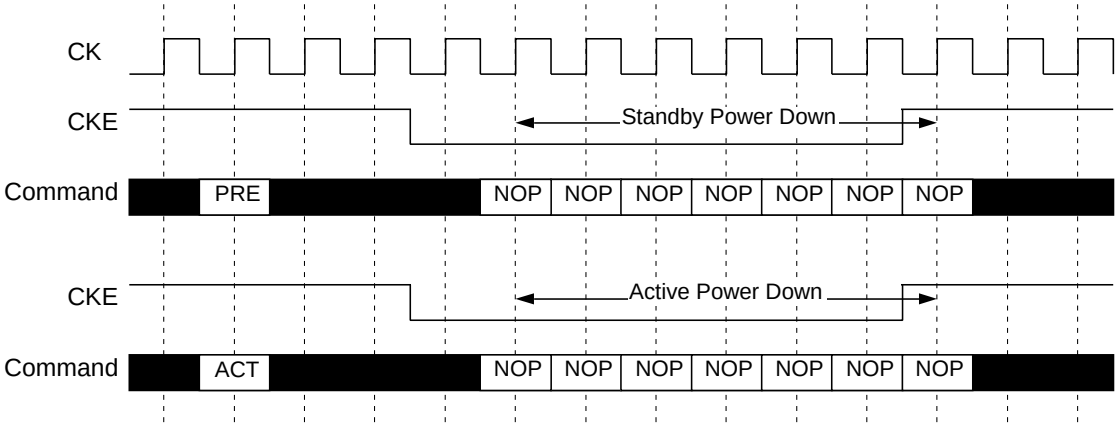


CLK SUSPEND

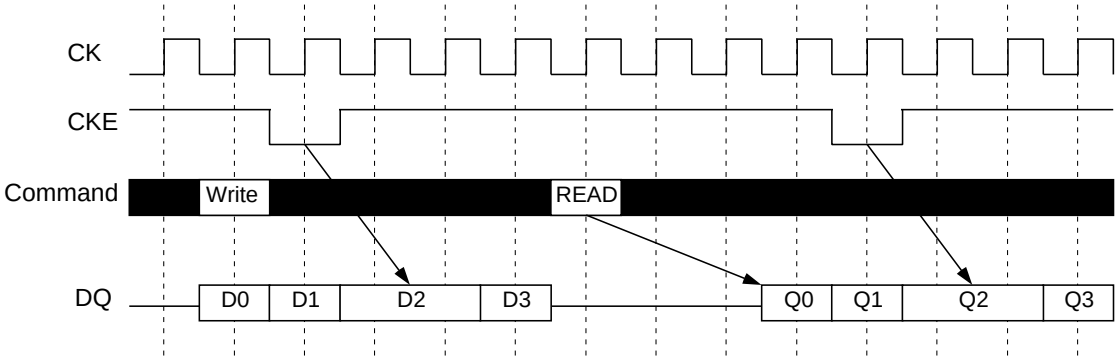
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.



Power Down by CKE



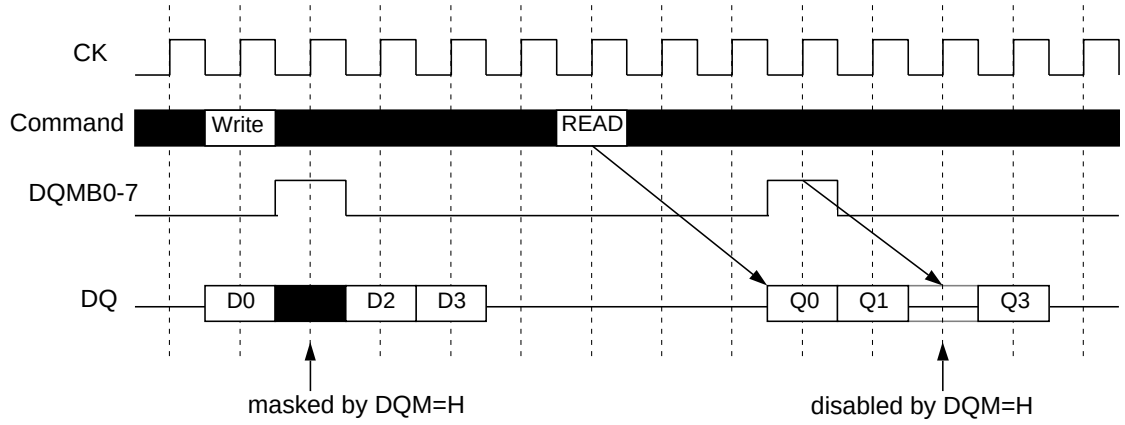
DQ Suspend by CKE



DQM CONTROL

DQMB0-7 is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQMB0-7 masks input data word by word. DQMB0-7 to write mask latency is 0.
During reads, DQMB0-7 forces output to Hi-Z word by word. DQMB0-7 to output Hi-Z latency is 2.

DQM Function



AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits(max)			Unit
			-10	-12	-15	
Icc1s	operating current, single bank (discrete)	tRC=min.tCLK=min, BL=1, CL=3	1440	1260	990	mA
Icc1d	operating current, dual bank (discrete)	tRC=min.tCLK=min, BL=1, CL=3	2160	1800	1440	mA
Icc2h	standby current, CKE=H	both banks idle, tCLK=min, CKE=H	360	324	288	mA
Icc2l	standby current, CKE=L	both banks idle, tCLK=min, CKE=L	36	36	36	mA
Icc3	active standby current	both banks active, tCLK=min, CKE=H	720	630	540	mA
Icc4	burst current	tCLK=min, BL=4, CL=3, 1 bank idle	1350	1080	900	mA
Icc5	auto-refresh current	tRC=min, tCLK=min	1170	1080	900	mA
Icc6	self-refresh current	CKE <0.2V	18	18	18	mA

AC OPERATING CONDITIONS AND CHARACTERISTICS

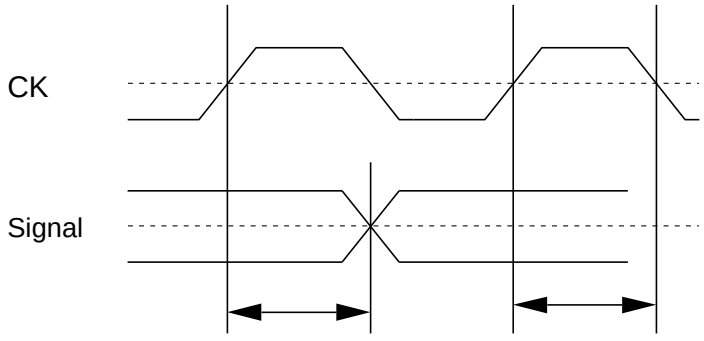
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Unit
			Min.	Max.	
VOH(DC)	High-Level Output Voltage(DC)	IOH=-2mA	2.4		V
VOL(DC)	Low-Level Output Voltage(DC)	IOL=2mA		0.4	V
IOZ	Off-stare Output Current	Q floating VO=0 ~ Vdd	-10	10	uA
Ii	Input Current	VIH=0 ~ Vdd+0.3V	-180	180	uA

AC TIMING REQUIREMENTS (SDRAM Component)

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)
Input Pulse Levels: 0.8V to 2.0V
Input Timing Measurement Level: 1.4V

Symbol	Parameter		Limits						Unit
			-10		-12		-15		
			Min.	Max.	Min.	Max.	Min.	Max.	
tCLK	CK cycle time	CL=1	30		30		30		ns
		CL=2	15		15		20		ns
		CL=3	10		12		15		ns
tCH	CK High pulse width		4		4		4		ns
tCL	CK Low pilse width		4		4		4		ns
tT	Transition time of CK		1	10	1	10	1	10	ns
tIS	Input Setup time(all inputs)		3		3		3		ns
tIH	Input Hold time(all inputs)		1		1		1.5		ns
tRC	Row cycle time		90		100		120		ns
tRCD	Row to Column Delay		30		30		30		ns
tRAS	Row Active time		60	10000	70	10000	80	10000	ns
tRP	Row Precharge time		30		30		40		ns
tWR	Write Recovery time		12		12		15		ns
tRRD	Act to Act Deley time		20		24		30		ns
tRSC	Mode Register Set Cycle time		20		24		30		ns
tSRX	Self Refresh Exit time		10		12		15		ns
tREF	Refresh Interval time			65.6		65.6		65.6	ms



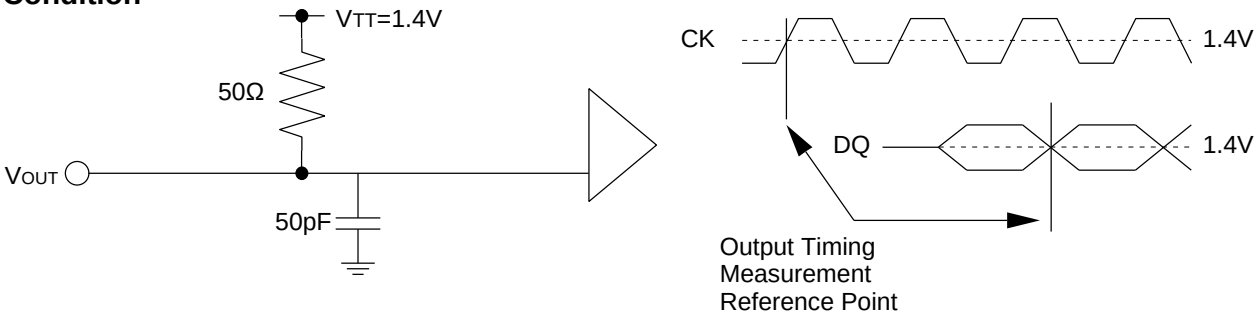
Any AC timing is referenced to the input signal crossing through 1.4V.

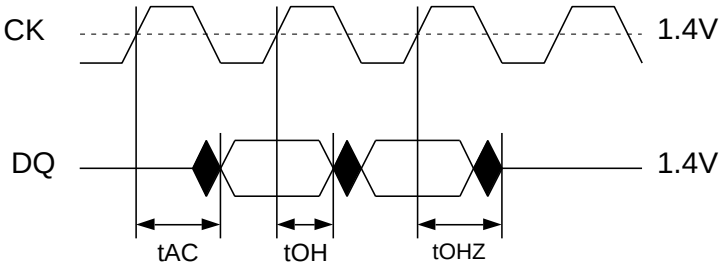
SWITCHING CHARACTERISTICS (SDRAM Component)

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

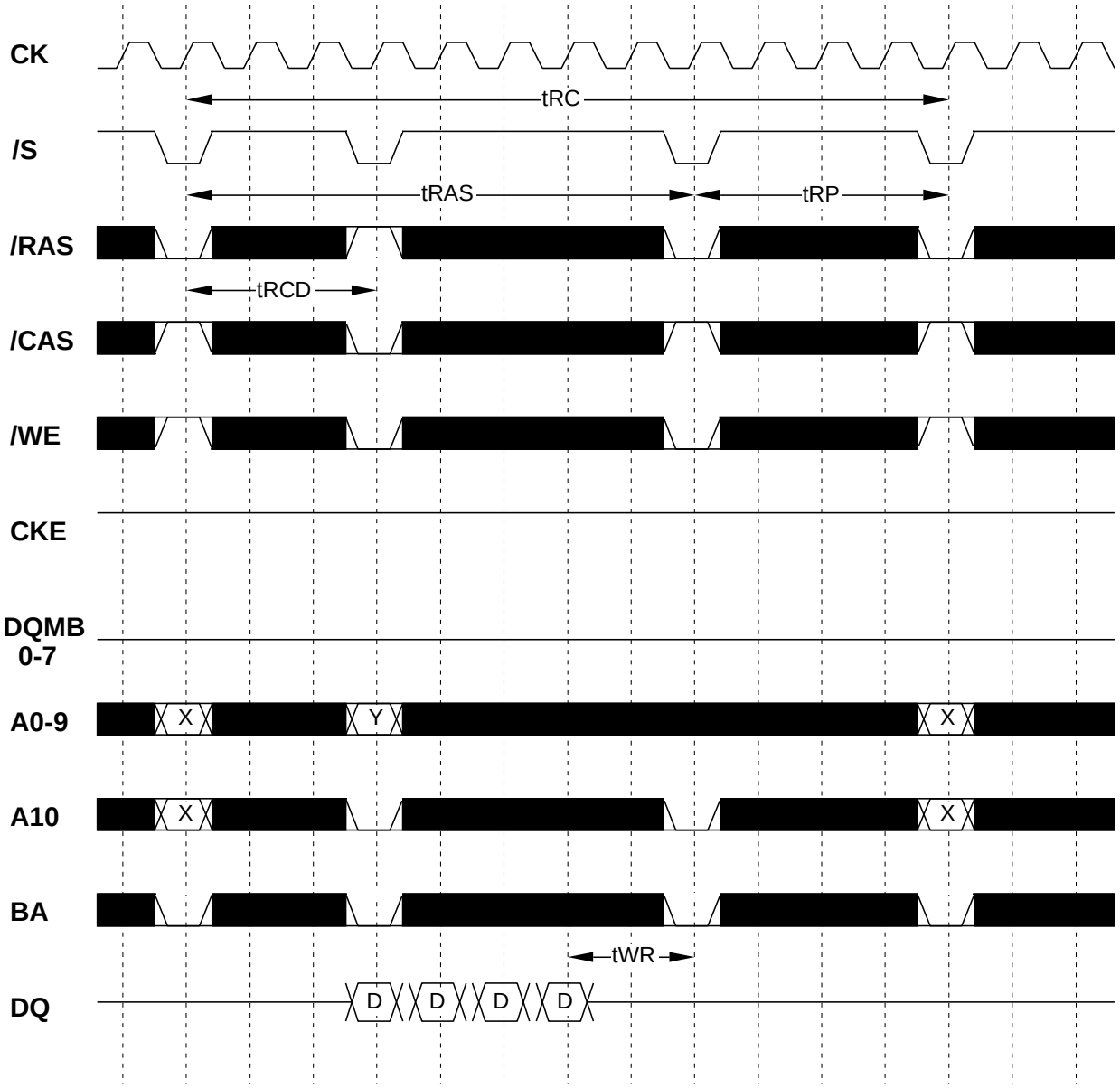
Symbol	Parameter		Limits						Unit
			-10		-12		-15		
			Min.	Max.	Min.	Max.	Min.	Max.	
tAC	Access time from CK	CL=1		27		27		30	ns
		CL=2		9		9.5		12	ns
		CL=3		8		8		9	ns
tOH	Output Hold time from CK		3		3		3		ns
tOLZ	Delay time, output low impedance from CK		0		0		0		ns
tOHZ	Delay time, output high impedance from CK		3	8	3	8	3	10	ns

Output Load Condition

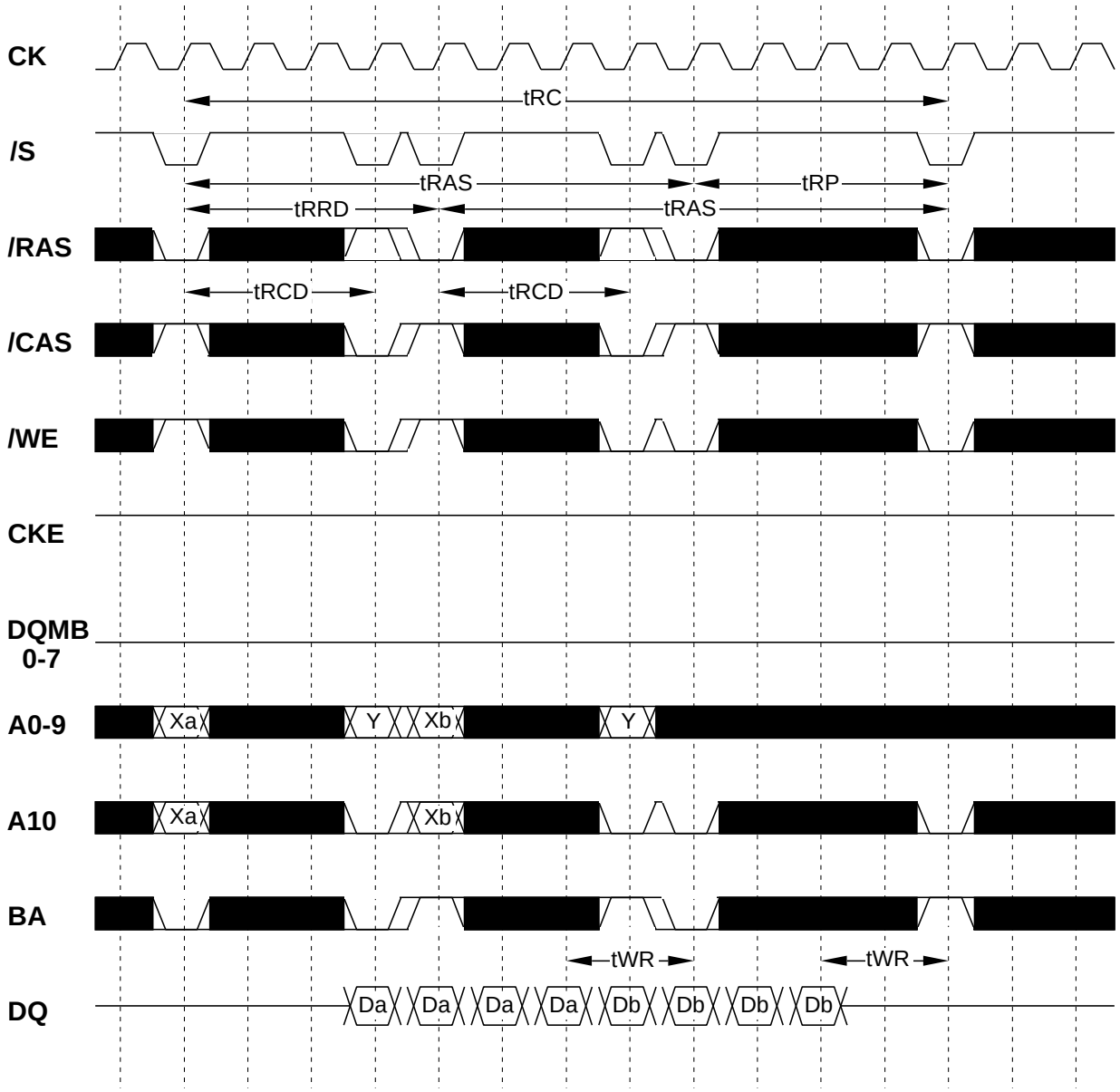




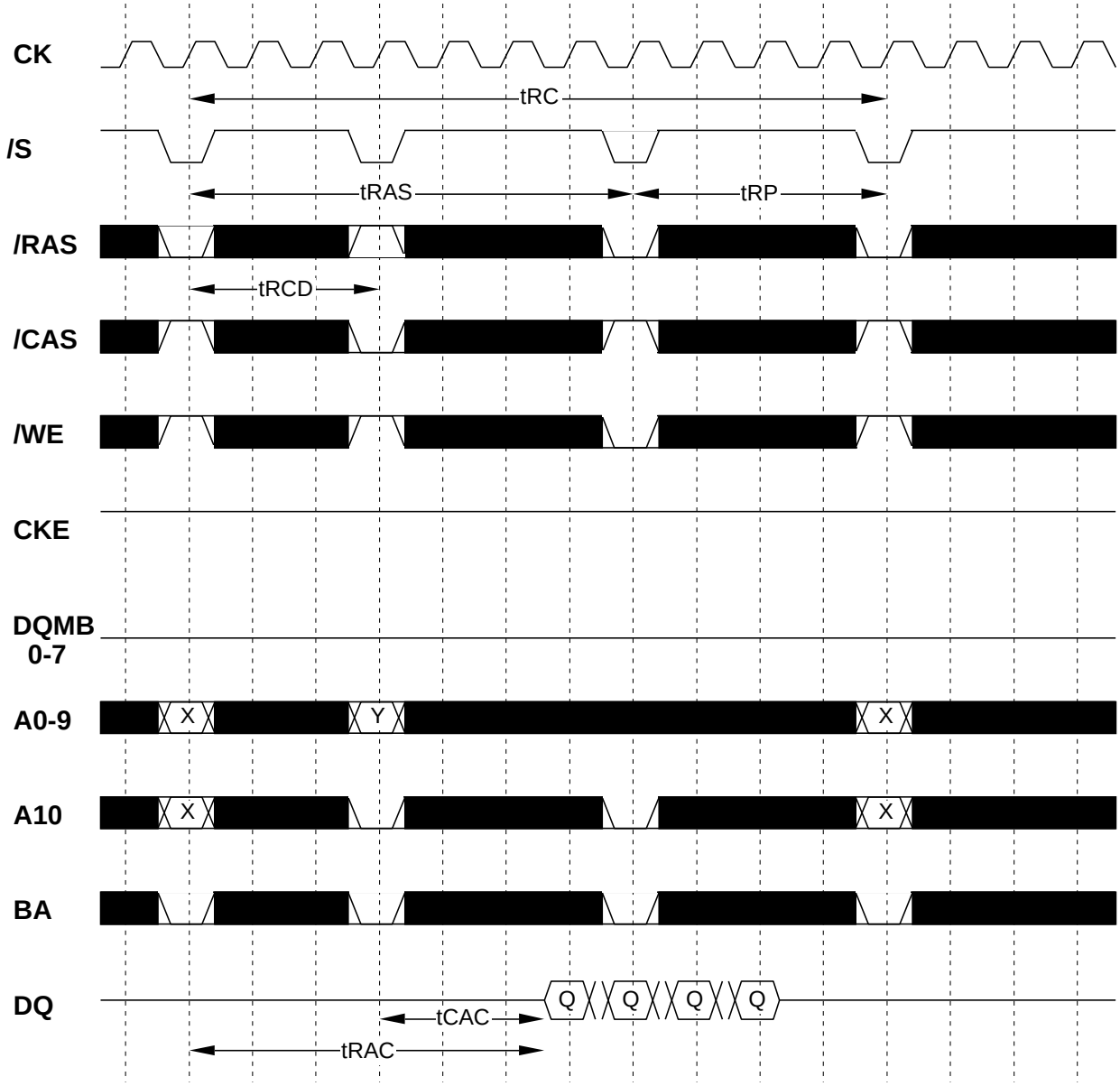
WRITE CYCLE (single bank) BL=4



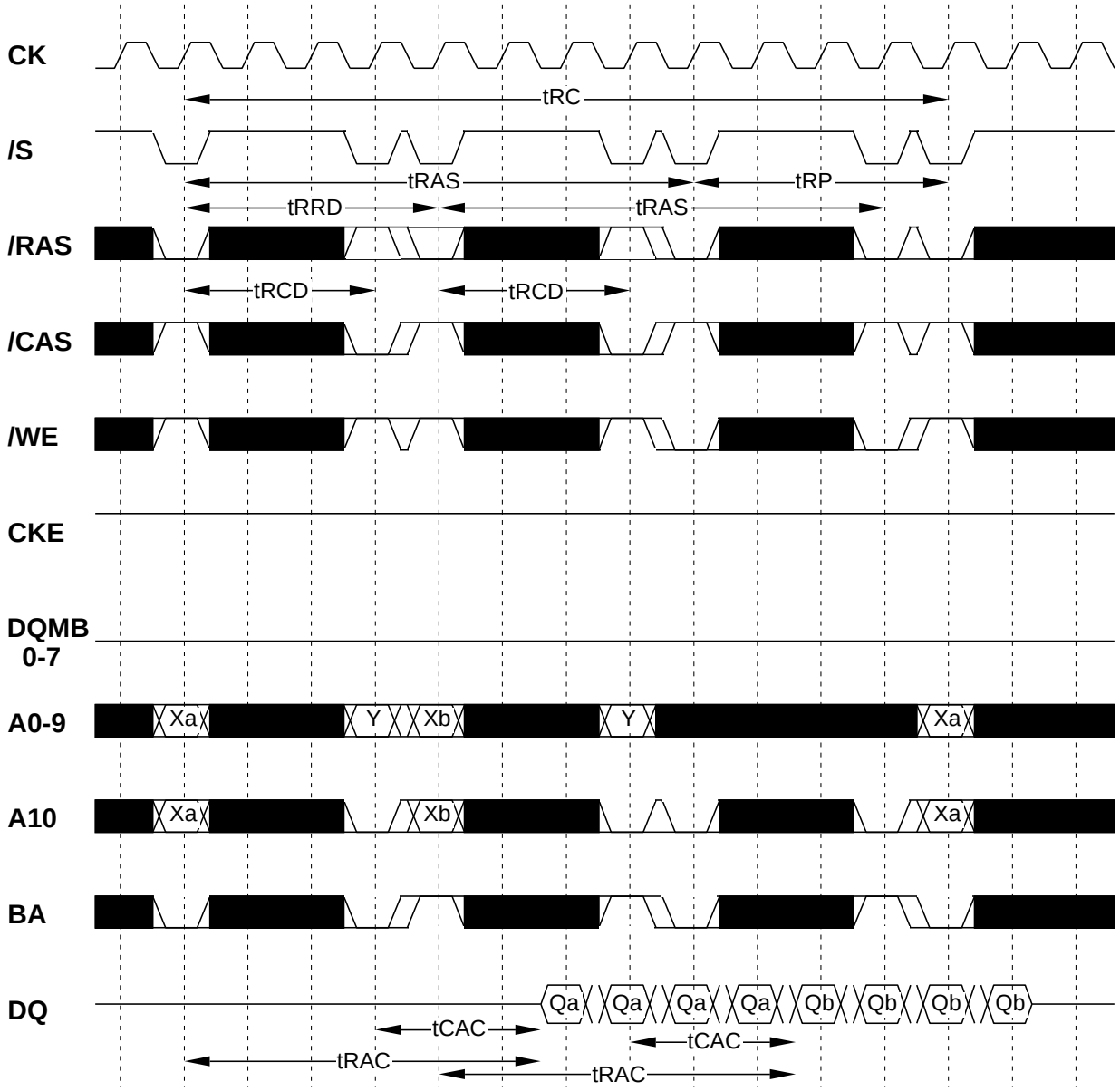
WRITE CYCLE (dual bank) BL=4



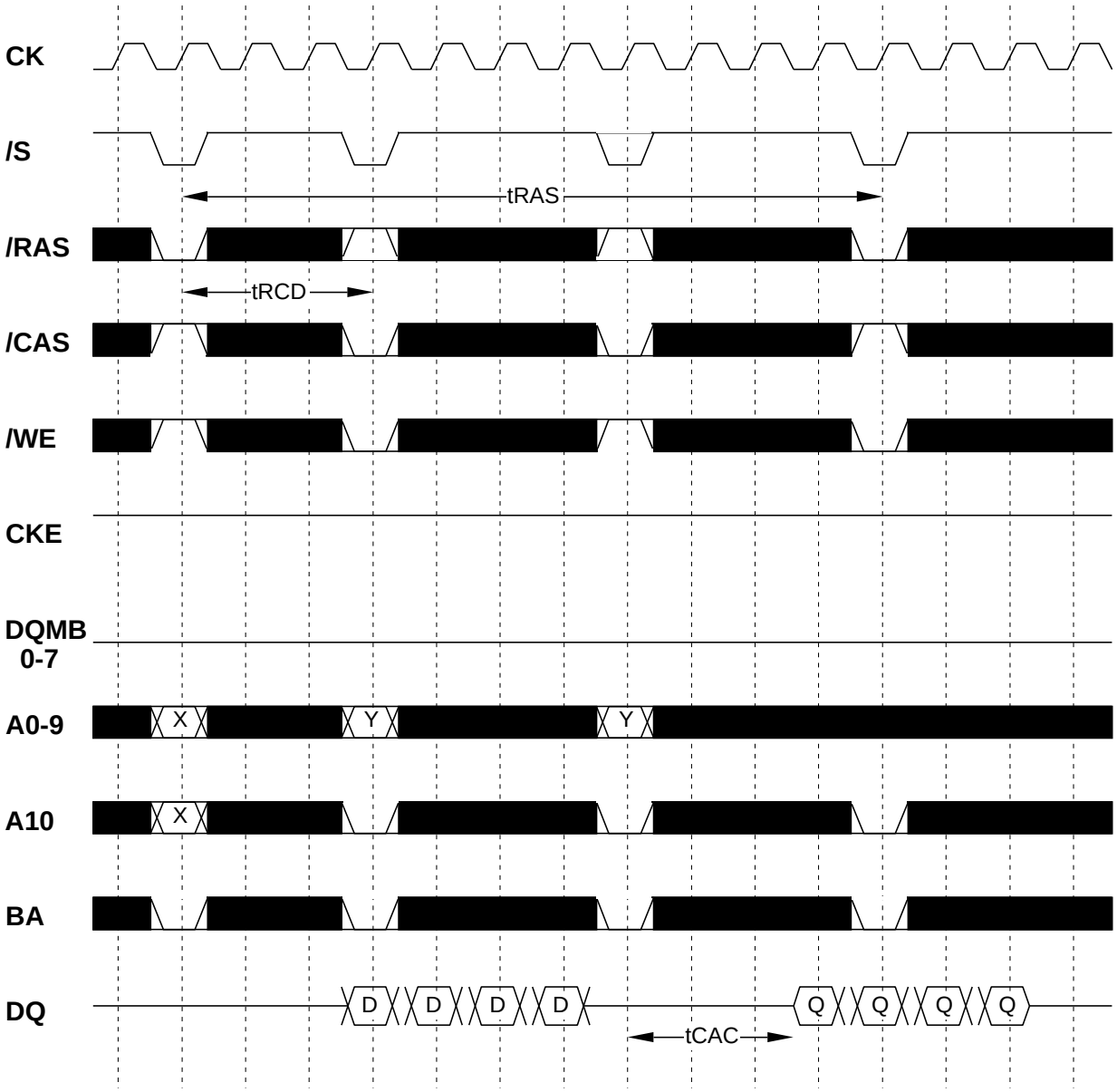
READ CYCLE (single bank) BL=4, CL=3



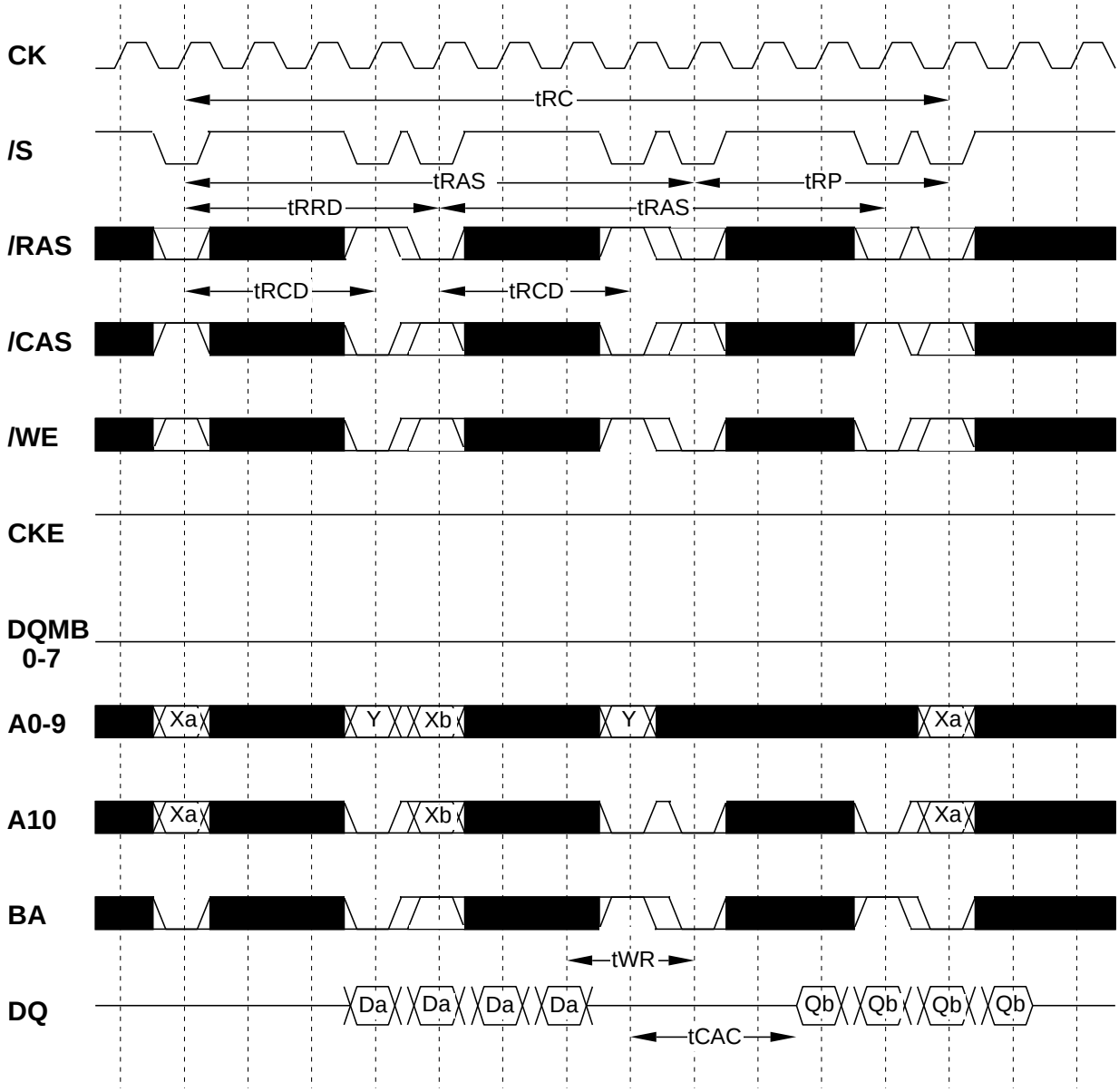
READ CYCLE (dual bank) BL=4, CL=3



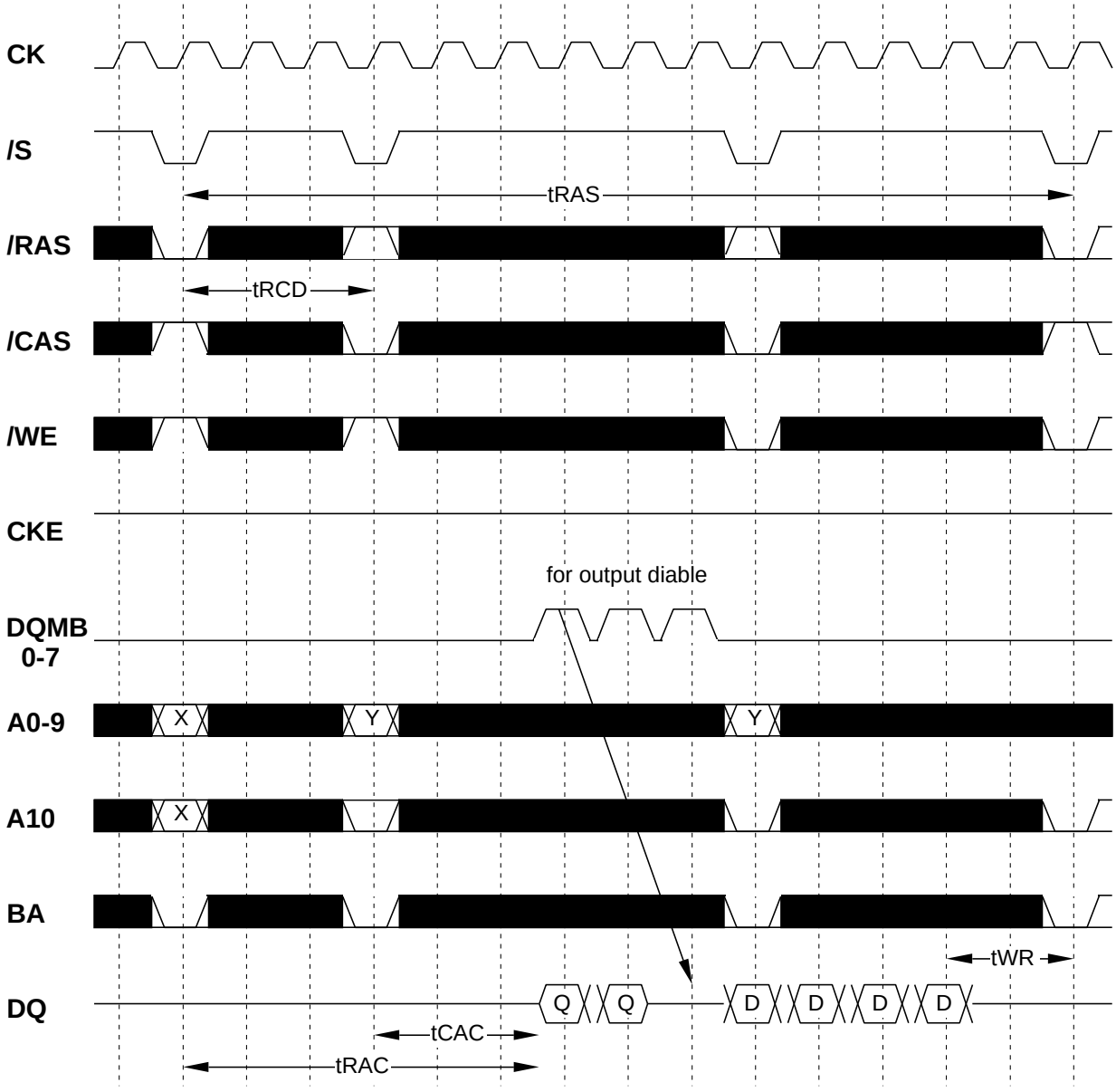
WRITE to READ (single bank) BL=4, CL=3



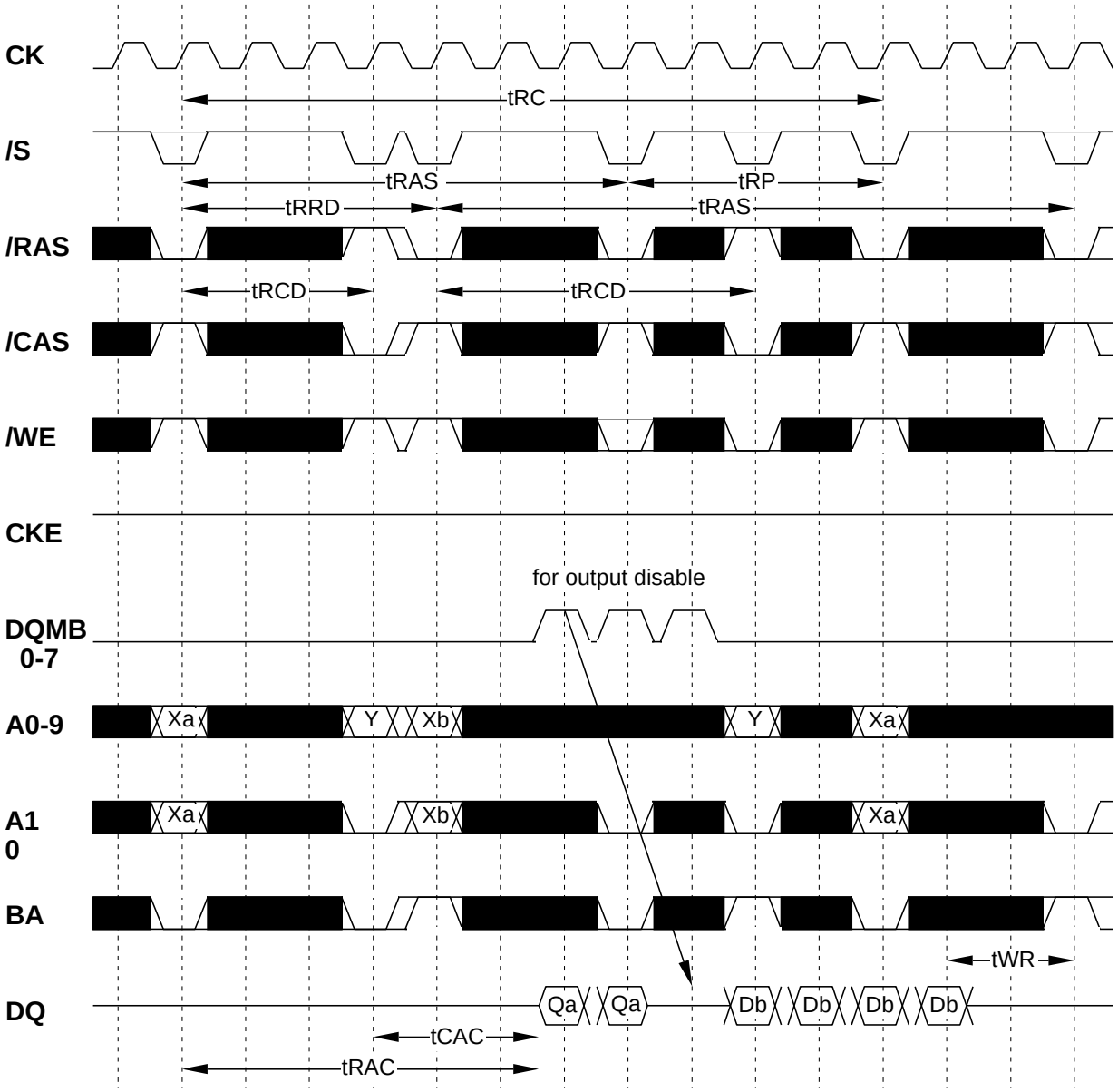
WRITE to READ (dual bank) BL=4, CL=3



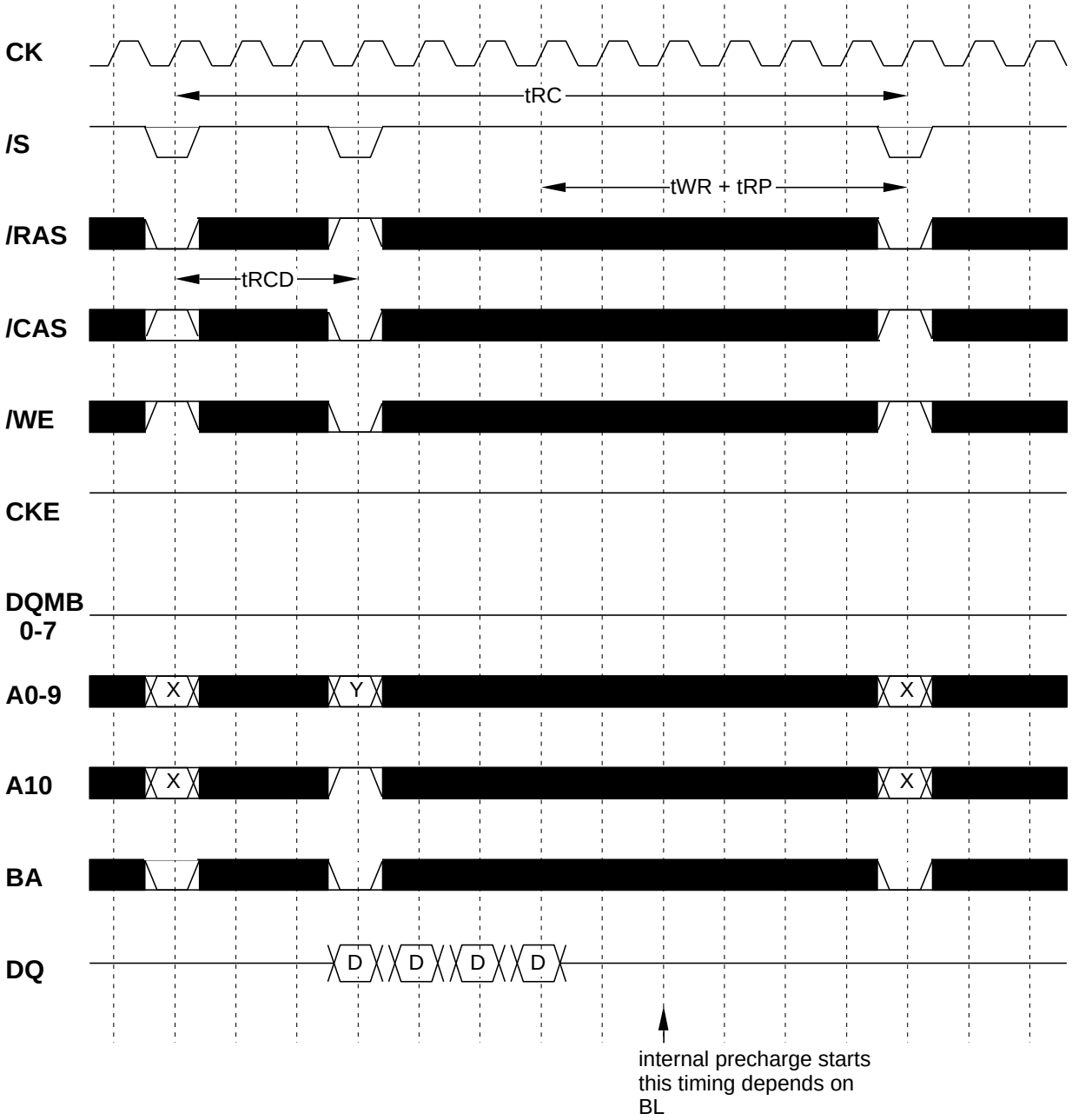
READ to WRITE (single bank) BL=4, CL=3



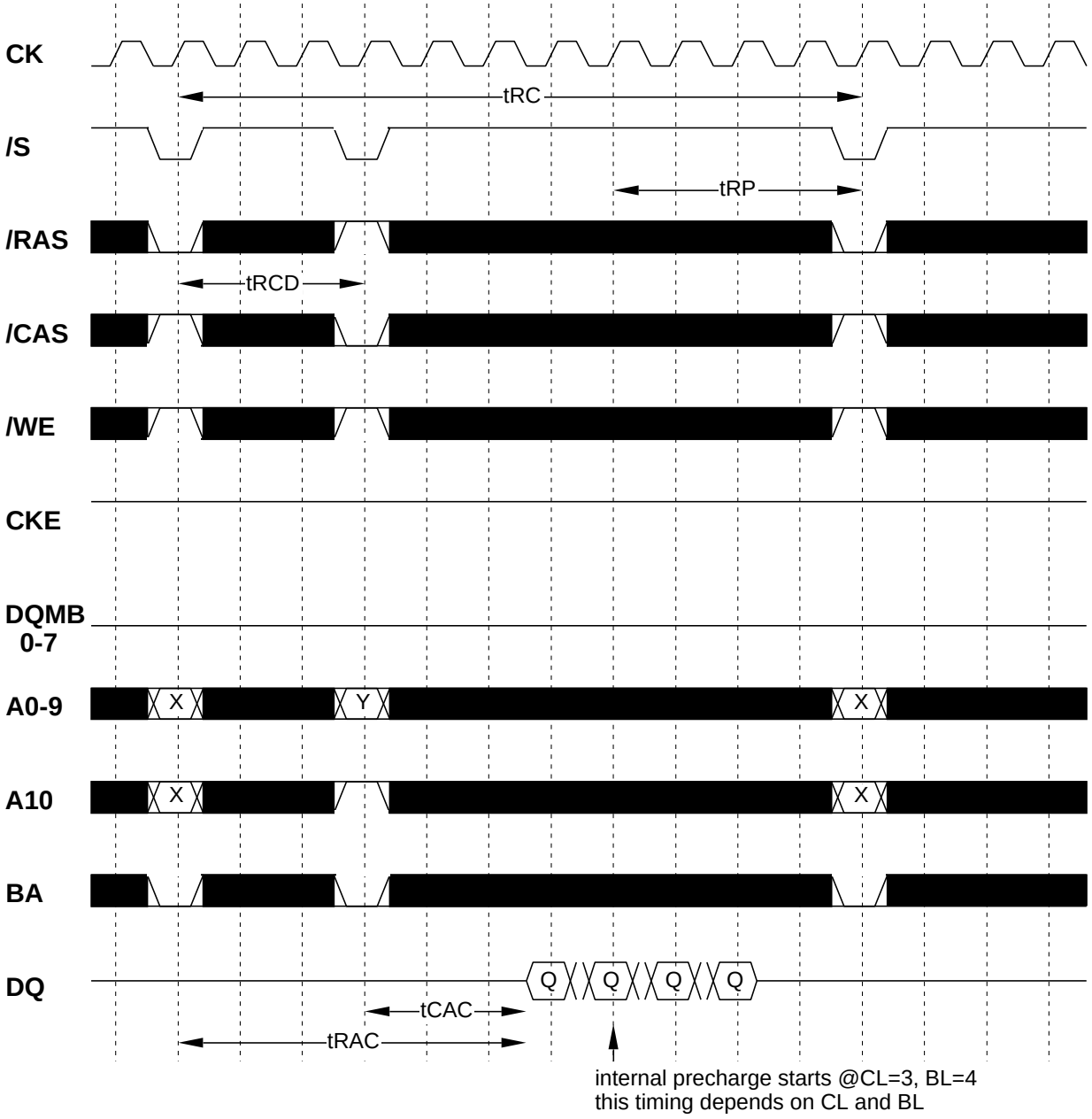
READ to WRITE (dual bank) BL=4, CL=3



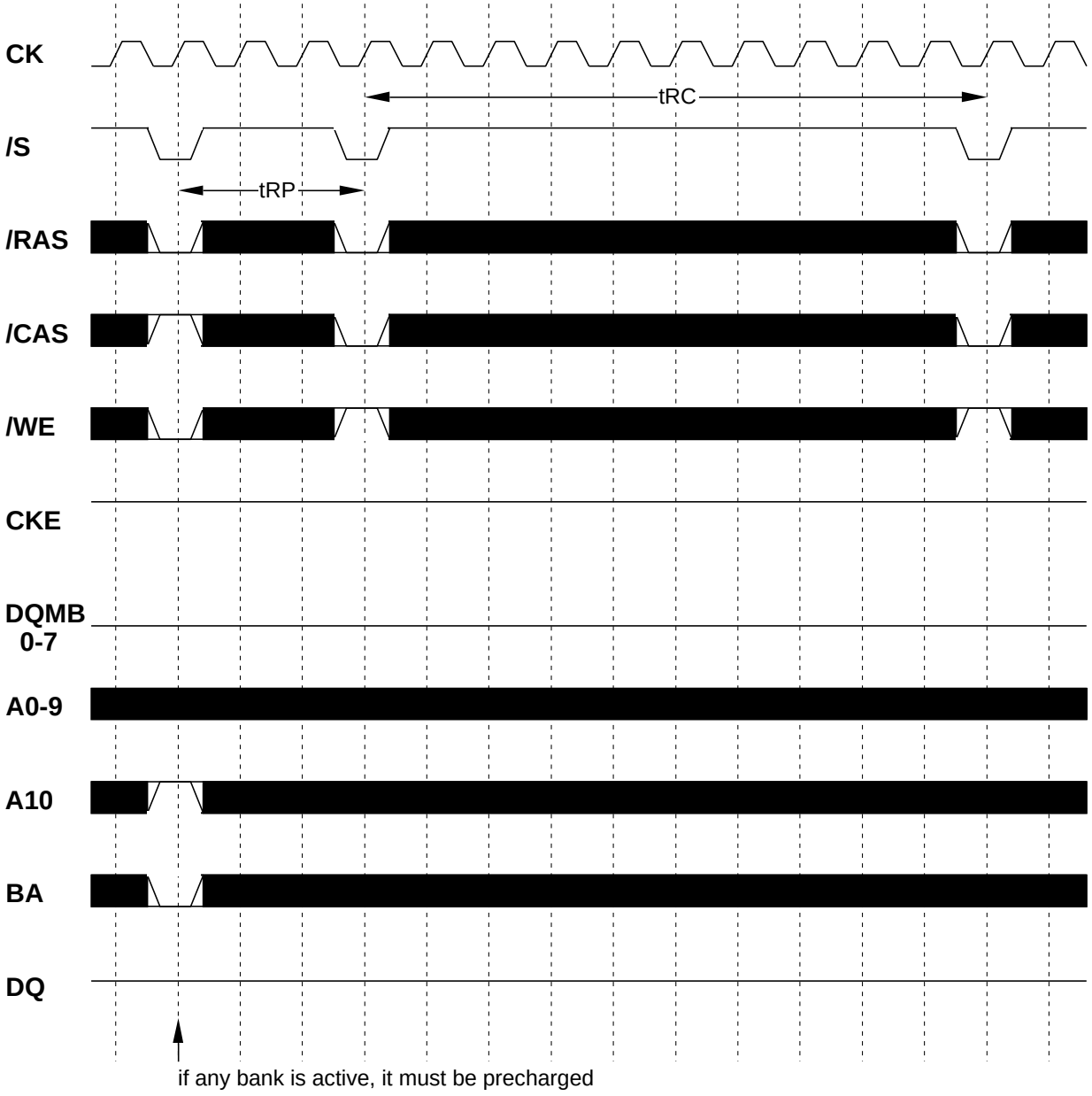
WRITE with AUTO-PRECHARGE BL=4



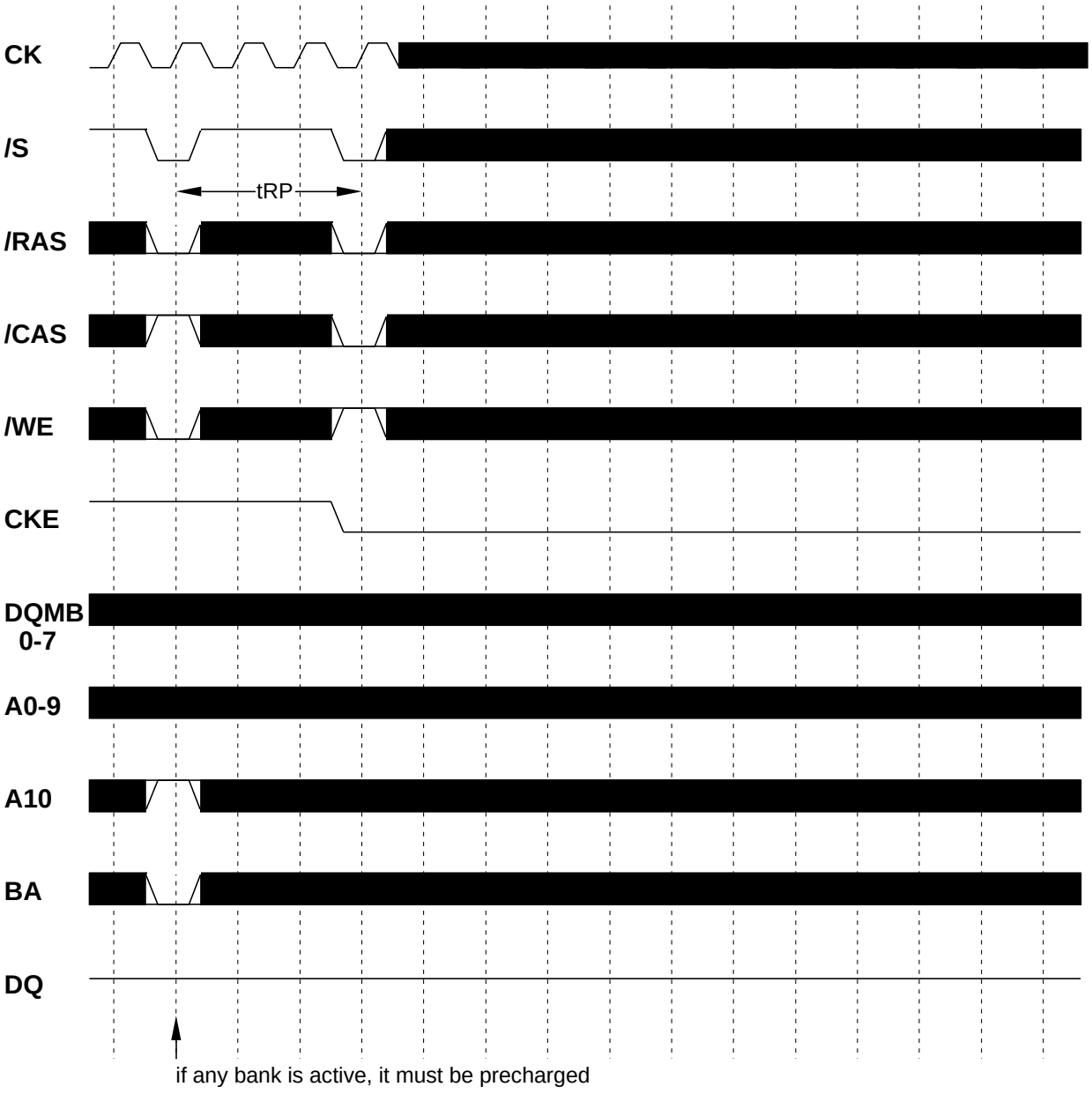
READ with AUTO-PRECHARGE BL=4, CL=3



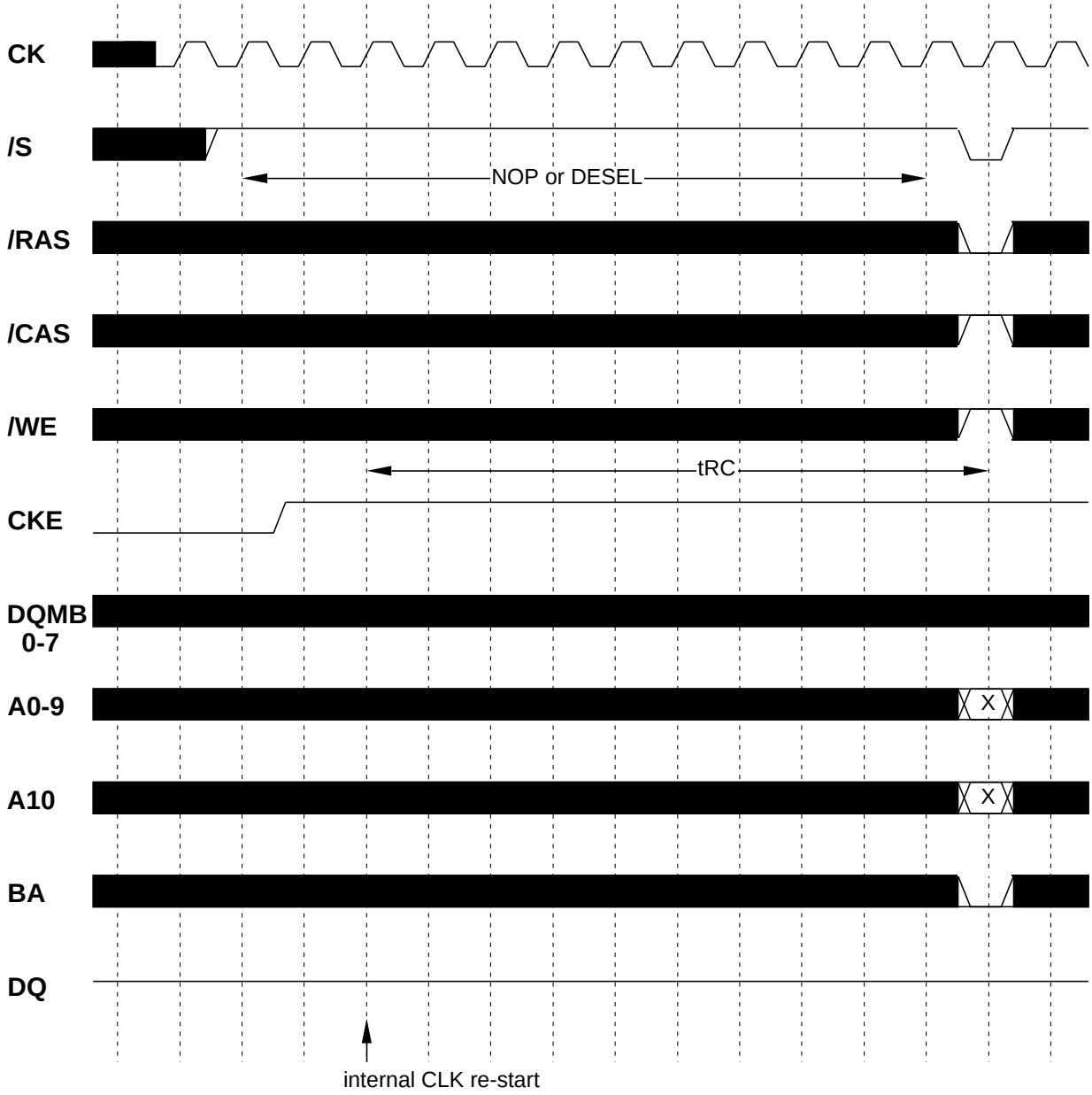
AUTO-REFRESH



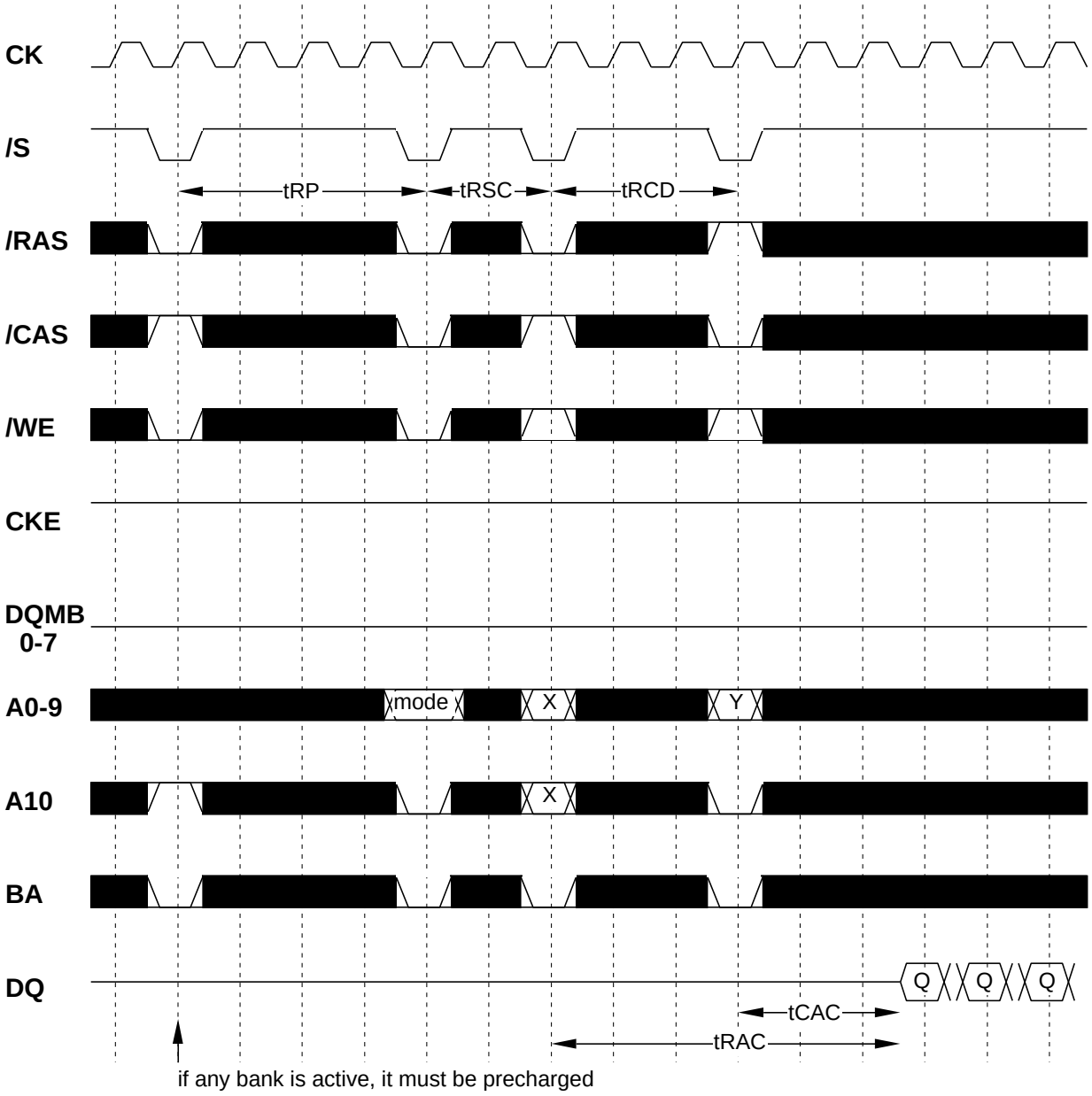
SELF-REFRESH ENTRY



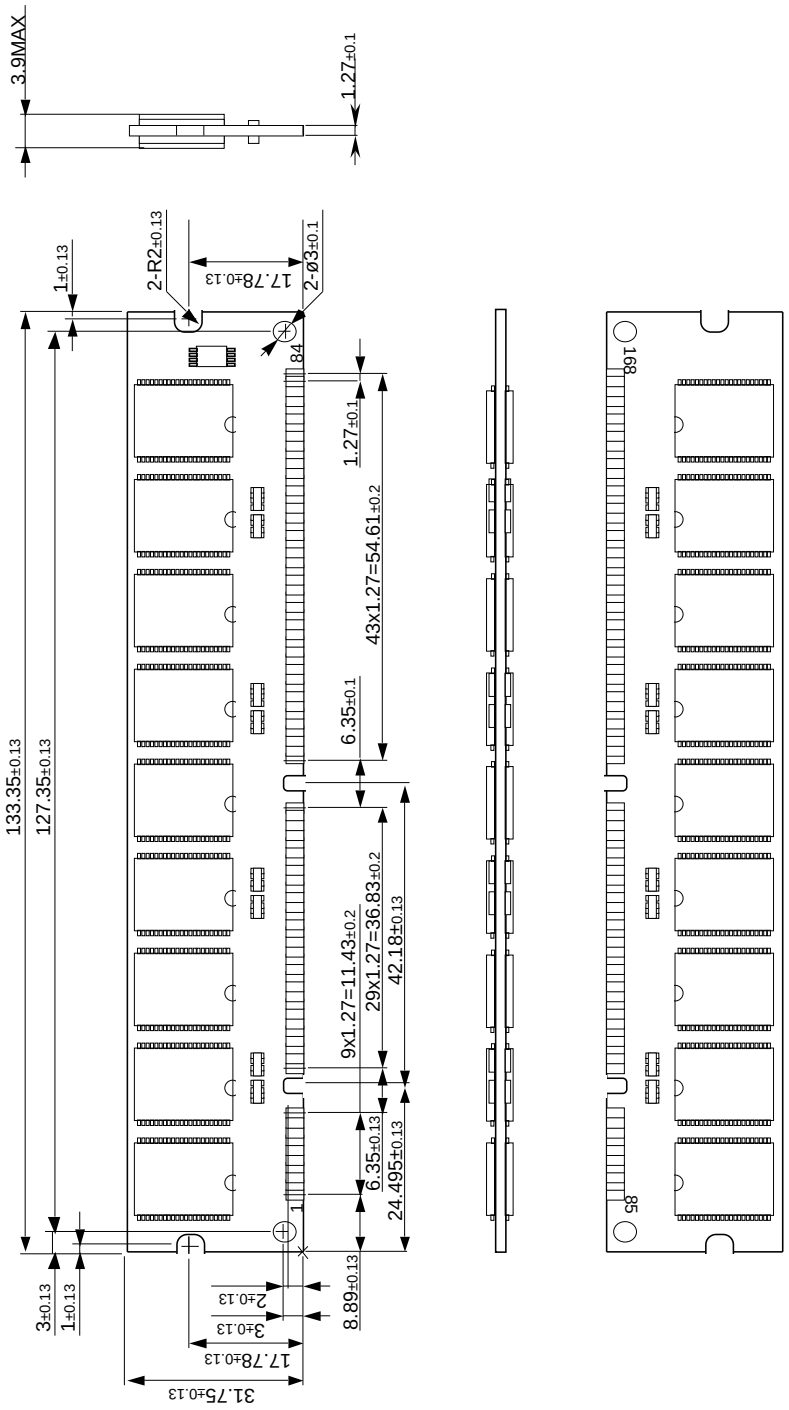
SELF-REFRESH EXIT



MODE REGISTER SET BL=4, CL=3



OUTLINE


3.9MAX
1.27±0.1
2-R2±0.13
2-ø3±0.1
17.78±0.13
1±0.13
84
1
168
85
1.27±0.1
43x1.27=54.61±0.2
6.35±0.1
133.35±0.13
127.35±0.13
9x1.27=11.43±0.2
29x1.27=36.83±0.2
42.18±0.13
6.35±0.13
24.495±0.13
8.89±0.13
3±0.13
1±0.13
2±0.13
3±0.13
17.78±0.13
31.75±0.13