

MGM13P Wireless Gecko Module Data Sheet



The MGM13P is Silicon Labs' first PCB module solution for 802.15.4 Mesh and multi-protocol networking that supports Bluetooth 5.0 LE, including long range, high throughput, and regular BLE PHYs.

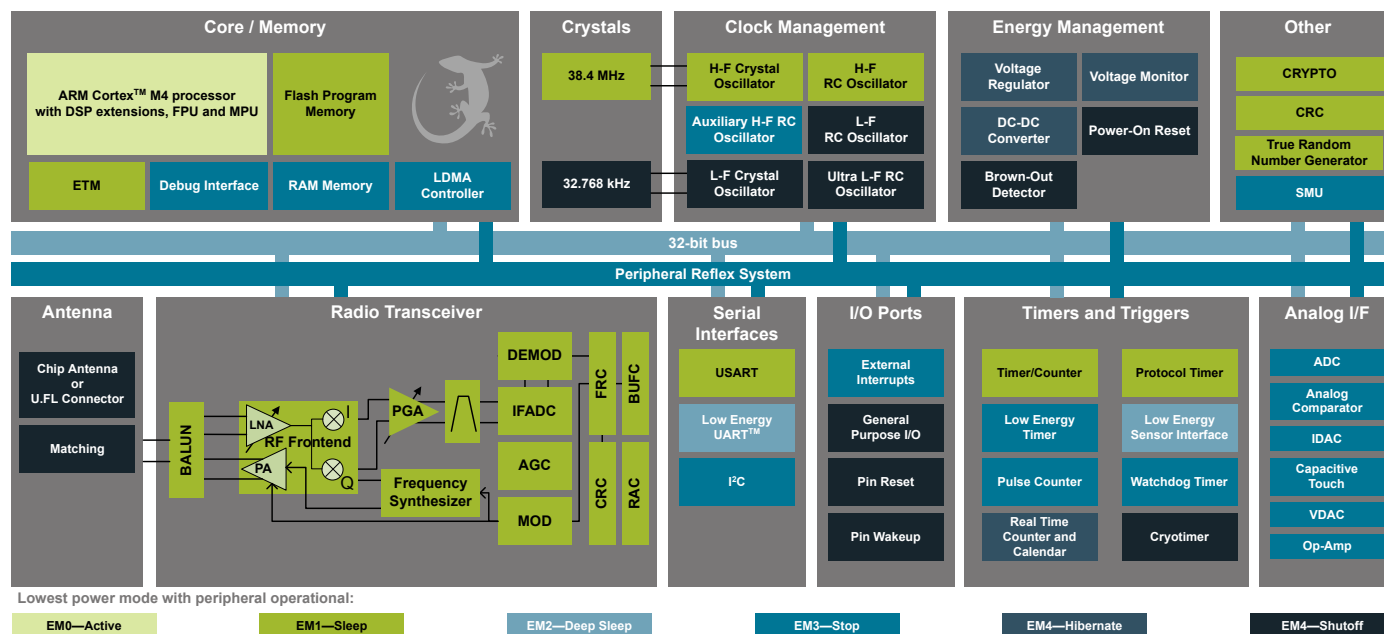
Based on the Silicon Labs EFR32MG13 Mighty Gecko SoC, the MGM13P delivers robust RF performance, low energy consumption, a wide selection of MCU peripherals, regulatory test certificates for various regions and countries, and a simplified development experience, all in a small form factor. Together with the certified software stacks and powerful tools also offered by Silicon Labs, the MGM13P can minimize the engineering efforts and development costs associated with adding Zigbee, Thread, Bluetooth 5.0 LE, or multi-protocol connectivity to any product, accelerating its time-to-market.

The MGM13P is intended for a broad range of applications, including:

- IoT multi-protocol end-node devices and gateways
- Connected home
- Lighting
- Metering
- Building automation and security
- Health and wellness

KEY FEATURES

- Zigbee, Thread, BLE, or multi-protocol connectivity
- Antenna or U.FL variants
- Up to +19 dBm TX power
- -94.6 dBm BLE RX sensitivity at 1 Mbps
- -102.1 dBm 802.15.4 RX sensitivity
- 32-bit ARM® Cortex®-M4 core at 38.4 MHz
- 512/64 kB of flash/RAM memory
- Robust security features
- Wide selection of MCU peripherals
- Integrated dc-dc converter
- 25 GPIO pins
- 12.9 × 17.8 × 2.3 mm



1. Feature List

- **Supported Protocols**
 - Zigbee
 - Thread
 - Bluetooth 5.0 LE
 - Multi-protocol
- **Wireless System-on-Chip.**
 - 2.4 GHz radio
 - TX power up to +19 dBm
 - High Performance 32-bit 38.4 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
 - 512 kB flash program memory
 - 64 kB RAM data memory
 - Embedded Trace Macrocell (ETM) for advanced debugging
 - Integrated dc-dc
- **High Receiver Performance**
 - -102.1 dBm sensitivity (1% PER) at 250 kbps DSSS-OQPSK
 - -102.8 dBm sensitivity (0.1% BER) at 125 kbit/s GFSK
 - -98.4 dBm sensitivity (0.1% BER) at 500 kbit/s GFSK
 - -94.6 dBm sensitivity (0.1% BER) at 1 Mbit/s GFSK
 - -91 dBm sensitivity (0.1% BER) at 2 Mbit/s GFSK
- **Low Energy Consumption**
 - 11 mA RX current at 250 kbps, DSSS-OQPSK
 - 9.9 mA RX current at 1 Mbps, GFSK
 - 8.5 mA TX current at 0 dBm output power
 - 87 μ A/MHz in Active Mode (EM0)
 - 1.4 μ A EM2 DeepSleep current (64 kB RAM retention and RTCC running from LFXO)
 - 1.3 μ A EM2 DeepSleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Regulatory Certifications**
 - FCC
 - CE
 - IC / ISERC
 - MIC / Telec
- **Wide Operating Range**
 - 1.8 V to 3.8 V single power supply
 - -40 °C to +85 °C
- **Dimensions**
 - 12.9 × 17.8 × 2.3 mm (W × L × H)
- **Support for Internet Security**
 - General Purpose CRC
 - True Random Number Generator (TRNG)
 - 2 × Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide Selection of MCU Peripherals**
 - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
 - 2 × Analog Comparator (ACMP)
 - 2 × Digital to Analog Converter (VDAC)
 - 3 × Operational Amplifier (Opamp)
 - Digital to Analog Current Converter (IDAC)
 - Low-Energy Sensor Interface (LESENSE)
 - Multi-channel Capacitive Sense Interface (CSEN)
 - 25 pins connected to analog channels (APORT) shared between analog peripherals
 - 25 General Purpose I/O pins with output state retention and asynchronous interrupts
 - 8 Channel DMA Controller
 - 12 Channel Peripheral Reflex System (PRS)
 - 2 × 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
 - 1 × 32-bit Timer/Counter
 - 3 Compare/Capture/PWM channels
 - 32-bit Real Time Counter and Calendar
 - 16-bit Low Energy Timer for waveform generation
 - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
 - 16-bit Pulse Counter with asynchronous operation
 - 2 × Watchdog Timer
 - 3 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I²S)
 - Low Energy UART (LEUART™)
 - 2 × I²C interface with SMBus support and address recognition in EM3 Stop

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	Antenna	Flash (kB)	RAM (kB)	GPIO	Packaging
MGM13P12F512GA-V2	Bluetooth LE Zigbee Thread	19 dBm	Built-in	512	64	25	Cut Tape
MGM13P12F512GA-V2R	Bluetooth LE Zigbee Thread	19 dBm	Built-in	512	64	25	Reel
MGM13P12F512GE-V2	Bluetooth LE Zigbee Thread	19 dBm	U.FL	512	64	25	Cut Tape
MGM13P12F512GE-V2R	Bluetooth LE Zigbee Thread	19 dBm	U.FL	512	64	25	Reel
MGM13P02F512GA-V2	Bluetooth LE Zigbee Thread	10 dBm	Built-in	512	64	25	Cut Tape
MGM13P02F512GA-V2R	Bluetooth LE Zigbee Thread	10 dBm	Built-in	512	64	25	Reel
MGM13P02F512GE-V2	Bluetooth LE Zigbee Thread	10 dBm	U.FL	512	64	25	Cut Tape
MGM13P02F512GE-V2R	Bluetooth LE Zigbee Thread	10 dBm	U.FL	512	64	25	Reel

End-product manufacturers must verify that the module is configured to meet regulatory limits for each region in accordance with the formal certification test reports.

Devices are not pre-programmed with a firmware image.

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3. System Overview

3.1 Introduction

The MGM13P product family combines an energy-friendly MCU with a highly integrated radio transceiver and a high performance, ultra robust antenna. The devices are well suited for any battery operated application, as well as other system where ultra-small size, reliable high performance RF, low-power consumption and easy application development are key requirements. This section gives a short introduction to the full radio and MCU system.

A detailed block diagram of the MGM13P module is shown in the figure below.

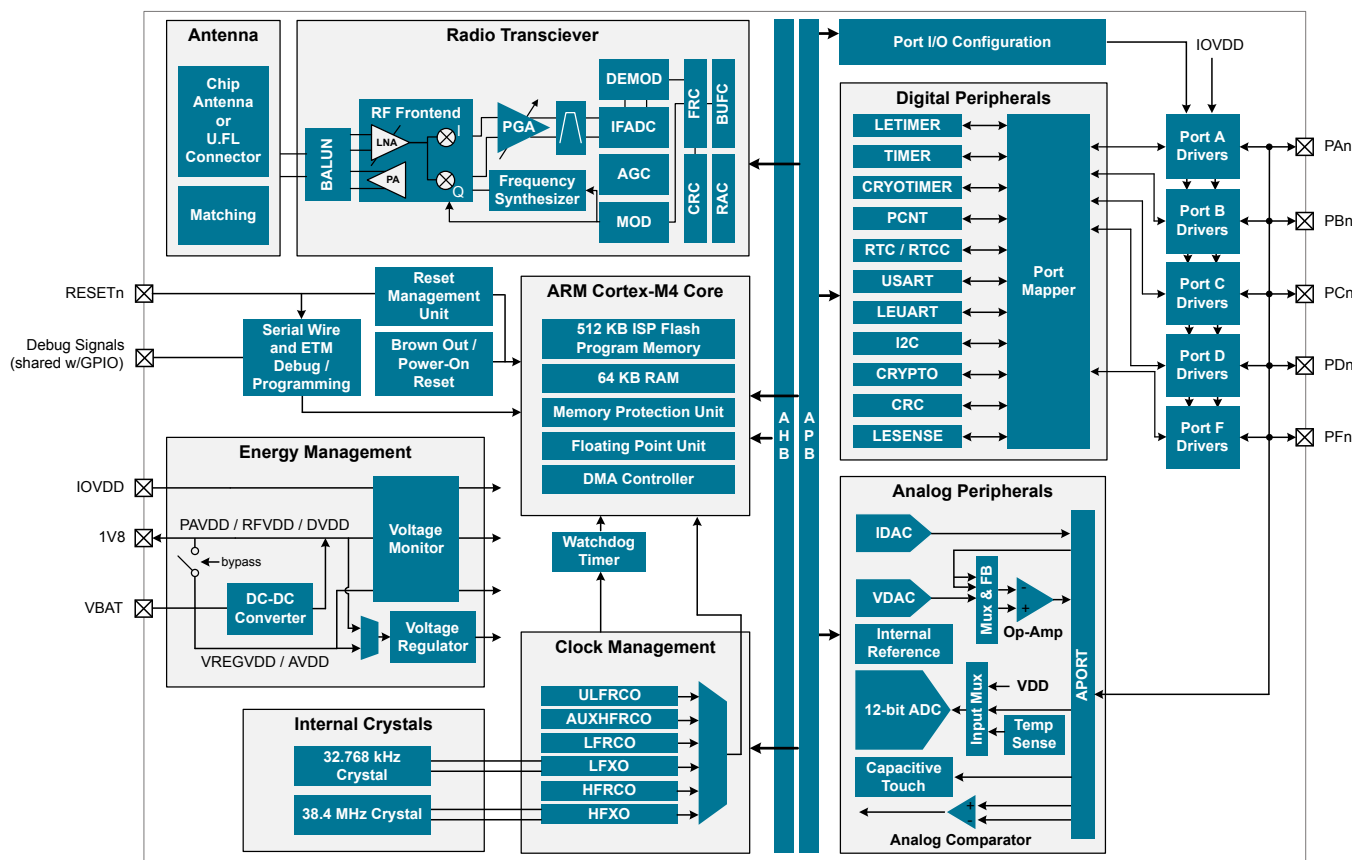


Figure 3.1. MGM13P Block Diagram

3.2 Radio

The MGM13P features a highly configurable radio transceiver supporting a wide range of wireless protocols including Zigbee, Thread, and Bluetooth Low Energy. It features a memory buffer and a low-voltage circuit that can withstand extremely high data rates.

3.2.1 Antenna Interface

The MGM13P has two antenna solution variants. One of them is a high-performance integrated chip antenna (MGM13PxxFxxxxA) and the other is a U.FL connector to attach an external antenna to the module (MGM13PxxFxxxxE).

Table 3.1. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1.5 to -3 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to 6. Layout Guidelines for PCB layout and antenna integration guidelines for optimal performance.
Peak gain	1 dBi	

3.2.2 RFSense

The RFSense block generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSense triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSense does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.3 Packet and State Trace

The MGM13P Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.4 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The MGM13P has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated dc-dc buck regulator is utilized to further reduce the current consumption. [Figure 3.2 Power Supply Configuration for +10 dBm Devices on page 9](#) and [Figure 3.3 Power Supply Configuration for +19 dBm Devices on page 9](#) show how the external and internal supplies of the module are connected for different part numbers.

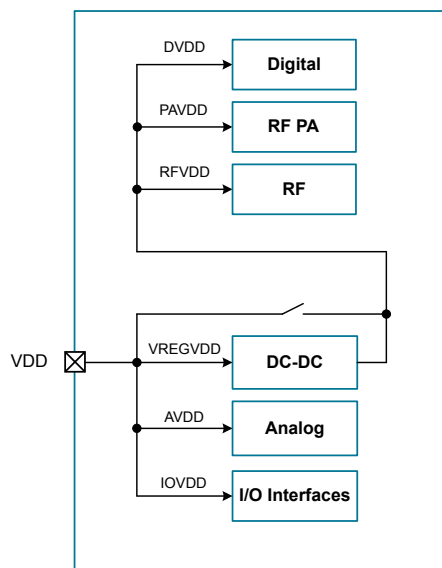


Figure 3.2. Power Supply Configuration for +10 dBm Devices

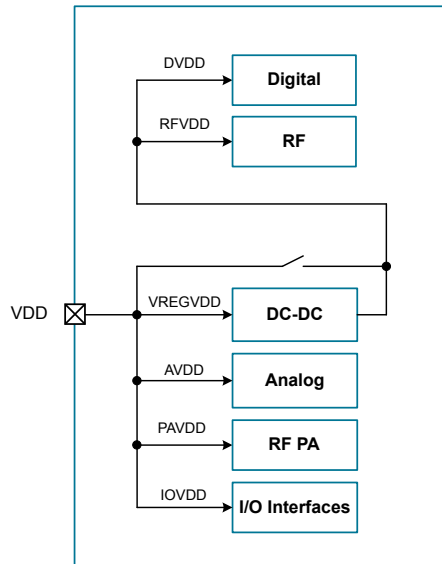


Figure 3.3. Power Supply Configuration for +19 dBm Devices

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The dc-dc buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the dc-dc converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The dc-dc converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the dc-dc input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The MGM13P has two peripheral power domains for operation in EM2 and EM3. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.2. Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	I2C0
APORT	I2C1
-	IDAC

3.4 General Purpose Input/Output (GPIO)

MGM13P has up to 25 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the MGM13P. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators and Crystals

The MGM13P fully integrates several oscillator sources and two crystals.

- The high-frequency crystal oscillator (HFXO) and integrated 38.4 MHz crystal provide a precise timing reference for the MCU and radio.
- The low-frequency crystal oscillator (LFXO) and integrated 32.768 kHz crystal provide an accurate timing reference for low energy modes and the real-time-clock circuits.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I²C)

The I²C interface enables communication between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSETM is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 General Purpose Cyclic Redundancy Check (GPCRC)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN peripheral is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN peripheral uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The peripheral can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.9.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC peripheral or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the MGM13P. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 512 kB flash program memory
- Up to 64 kB RAM data memory
- Configuration and event handling of all peripherals
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The MGM13P memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

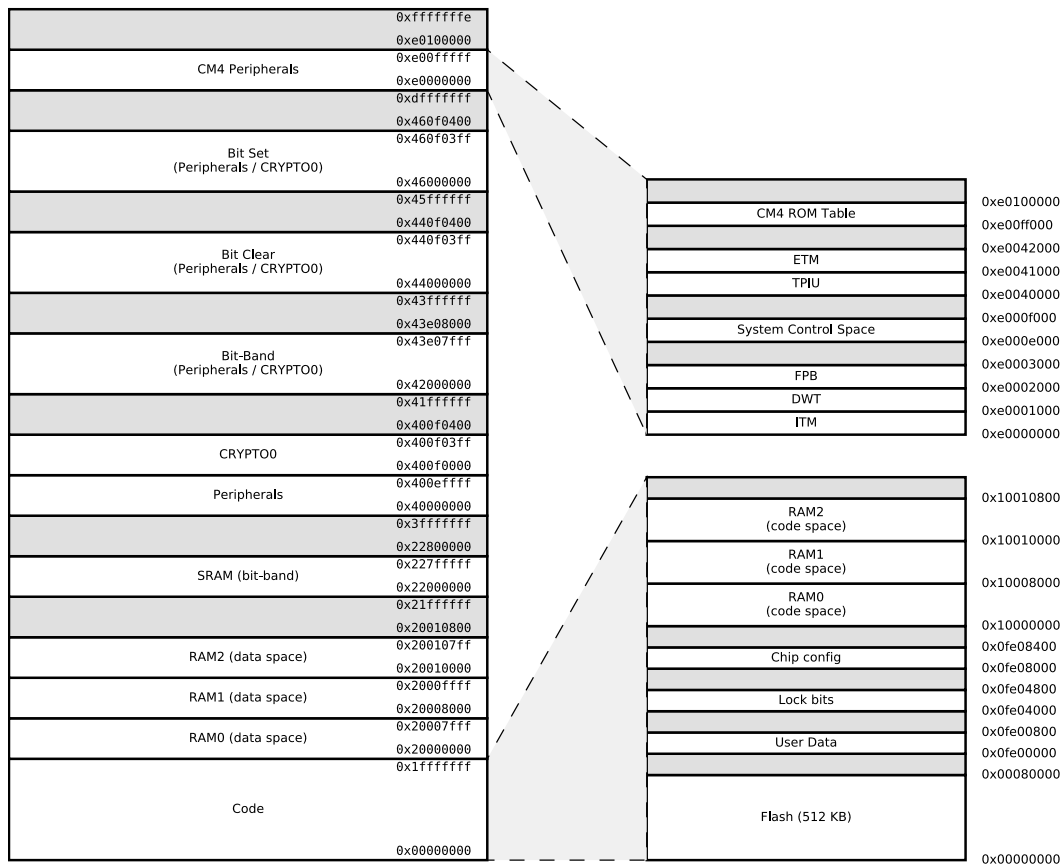


Figure 3.4. MGM13P Memory Map — Core Peripherals and Code Space

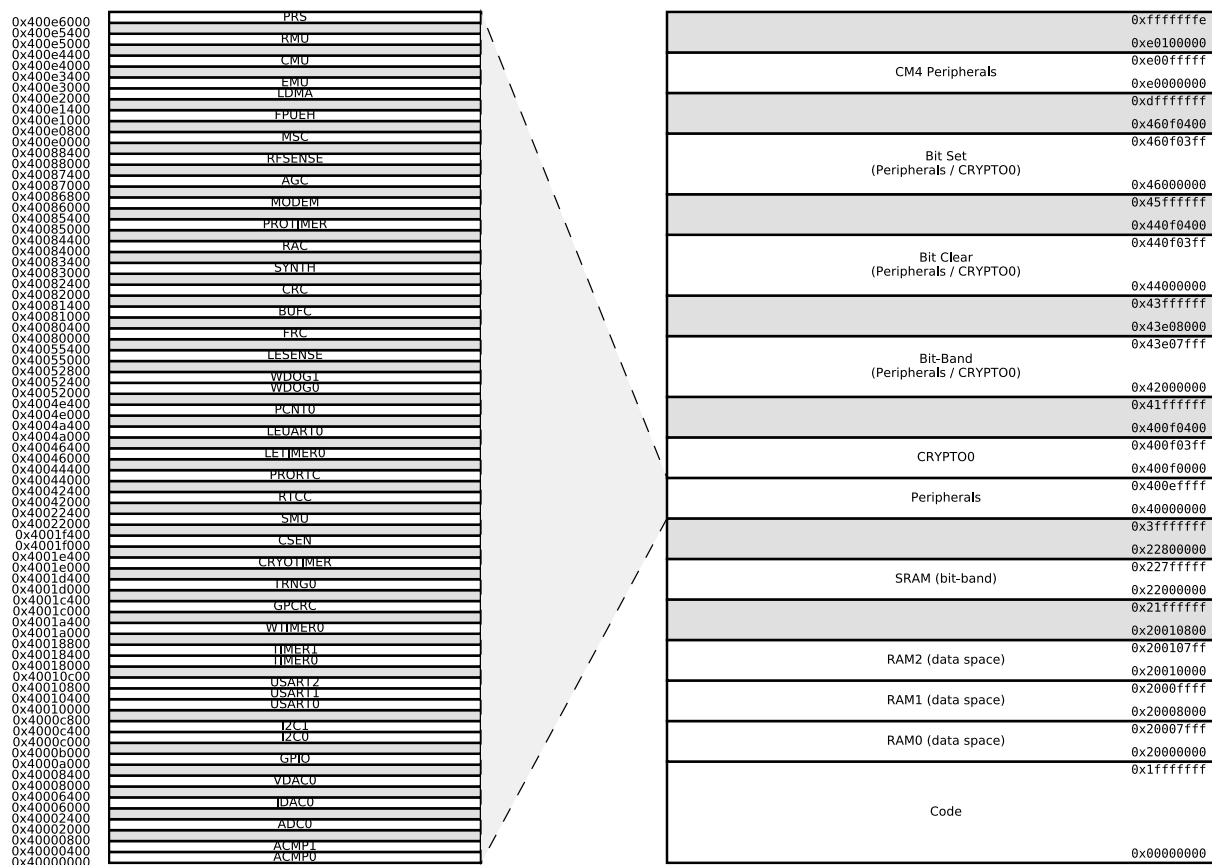


Figure 3.5. MGM13P Memory Map — Peripherals

3.13 Configuration Summary

Many peripherals on the MGM13P are available in multiple instances. However, certain USART, TIMER and WTIMER instances implement only a subset of the full features for that peripheral type. The table below describes the specific features available on these peripheral instances. All remaining peripherals support full configuration.

Table 3.3. Configuration Summary

Peripheral	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I ² S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA SmartCard	US2_TX, US2_RX, US2_CLK, US2_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a $50\ \Omega$ antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

The MGM13P module has only one external supply pin (VDD). There are several internal supply rails mentioned in the electrical specifications, whose connections vary based on transmit power configuration. Refer to [3.3 Power](#) for the relationship between the module's external VDD pin and internal voltage supply rails.

Refer to [Table 4.2 General Operating Conditions on page 19](#) for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stress levels beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T _{STG}		-40	—	85	°C
Voltage on any supply pin	V _{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	V _{DDRAMP} MAX		—	—	1	V / μ s
DC voltage on any GPIO pin	V _{DIGPIN}	5V tolerant GPIO pins ^{1 2 3}	-0.3	—	Min of 5.25 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Maximum RF level at input	P _{RFMAX2G4}		—	—	10	dBm
Total current into supply pins	I _{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I _{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I _{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	I _{IOALLMAX}	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T _J		-40	—	105	°C

Note:

1. When a GPIO pin is routed to the analog block through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

The following subsections define the recommended operating conditions for the module.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade	-40	25	85	°C
VDD operating supply voltage	V_{VDD}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS1	—	—	40	MHz
		VSCALE0, MODE = WS0	—	—	20	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	40	MHz
		VSCALE0	—	—	20	MHz

4.1.3 DC-DC Converter

Test conditions: $V_{\text{DCDC_I}}=3.3\text{ V}$, $V_{\text{DCDC_O}}=1.8\text{ V}$, $I_{\text{DCDC_LOAD}}=50\text{ mA}$, Heavy Drive configuration, $F_{\text{DCDC_LN}}=7\text{ MHz}$, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	$V_{\text{DCDC_I}}$	Bypass mode, $I_{\text{DCDC_LOAD}} = 50\text{ mA}$	1.8	—	$V_{\text{VREGVDD_MAX}}$	V
		Low noise (LN) mode, 1.8 V output, $I_{\text{DCDC_LOAD}} = 100\text{ mA}$, or Low power (LP) mode, 1.8 V output, $I_{\text{DCDC_LOAD}} = 10\text{ mA}$	2.4	—	$V_{\text{VREGVDD_MAX}}$	V
Output voltage programmable range ¹	$V_{\text{DCDC_O}}$		1.8	—	V_{VREGVDD}	V
Max load current	$I_{\text{LOAD_MAX}}$	Low noise (LN) mode, Medium or Heavy Drive ²	—	—	70	mA
		Low noise (LN) mode, Light Drive ²	—	—	50	mA
		Low power (LP) mode, $\text{LPCMPBIASEMxx}^3 = 0$	—	—	75	μA
		Low power (LP) mode, $\text{LPCMPBIASEMxx}^3 = 3$	—	—	10	mA

Note:

1. Due to internal dropout, the dc-dc output will never be able to reach its input voltage, V_{VREGVDD} .
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.

4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.4. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹	I _{ACTIVE_DCM}	38.4 MHz crystal, CPU running while loop from flash ²	—	87	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	69	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	70	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	82	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	615	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode ³	I _{ACTIVE_CCM}	38.4 MHz crystal, CPU running while loop from flash ²	—	97	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	80	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	92	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1145	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ³	I _{ACTIVE_CCM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	101	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1124	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹	I _{EM1_DCM}	38.4 MHz crystal ²	—	56	—	μA/MHz
		38 MHz HFRCO	—	39	—	μA/MHz
		26 MHz HFRCO	—	46	—	μA/MHz
		1 MHz HFRCO	—	588	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ¹	I _{EM1_DCM_VS}	19 MHz HFRCO	—	50	—	μA/MHz
		1 MHz HFRCO	—	572	—	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ⁴	I _{EM2_VS}	Full 64 kB RAM retention and RTCC running from LFXO	—	1.4	—	μA
		Full 64 kB RAM retention and RTCC running from LFRCO	—	1.5	—	μA
		1 bank RAM retention and RTCC running from LFRCO ⁵	—	1.3	—	μA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 64 kB RAM retention and CRYOTIMER running from ULFR-CO	—	1.14	—	μA
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.75	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.44	—	μA
		128 byte RAM retention, no RTCC	—	0.42	—	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.07	—	μA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
2. CMU_HFXOCTRL_LOWPOWER=0.
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
4. DCDC Low Power Mode = Medium Drive, LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.4.2 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T = 25 °C. DC-DC on. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.5. Current Consumption Using Radio

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I _{RX_ACTIVE}	125 kbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	10.5	—	mA
		500 kbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	10.4	—	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	9.9	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	10.6	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	11	—	mA
Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I _{RX_LISTEN}	125 kbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.5	—	mA
		500 kbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.5	—	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.9	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	11.6	—	mA
		802.15.4, F = 2.4 GHz, No radio clock prescaling	—	11.9	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I _{TX}	F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3	—	8.5	—	mA
		F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1	—	9.6	—	mA
		F = 2.4 GHz, CW, 10 dBm output power	—	38.2	—	mA
		F = 2.4 GHz, CW, 19 dBm output power	—	131	—	mA

4.1.5 Wake Up Times

Table 4.6. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.9	—	μs
		Code execution from RAM	—	3.8	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.9	—	μs
		Code execution from RAM	—	3.8	—	μs
Wake up from EM4H ¹	t_{EM4H_WU}	Executing from flash	—	90	—	μs
Wake up from EM4S ¹	t_{EM4S_WU}	Executing from flash	—	300	—	μs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	51	—	μs
		Any other reset released	—	358	—	μs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{2 3}	—	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ⁴	—	4.3	—	μs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.
3. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/ μs for approximately 20 μs . During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
4. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.

4.1.6 Brown Out Detector (BOD)

Table 4.7. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	1.53	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD_DELAY}$	Supply drops at 0.1V/ μs rate	—	2.4	—	μs
EM4 BOD threshold	V_{EM4BOD}	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/ μs rate	—	300	—	μs

4.1.7 Frequency Synthesizer

Table 4.8. Frequency Synthesizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF synthesizer frequency range	f_{RANGE}	2400 - 2483.5 MHz	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	f_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
Frequency deviation resolution with 38.4 MHz crystal	df_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	df_{MAX}	2400 - 2483.5 MHz	—	—	1677	kHz

4.1.8 2.4 GHz RF Transceiver Characteristics

4.1.8.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.9. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power ¹	POUT _{MAX}	19 dBm-rated part numbers.	—	19	—	dBm
		10 dBm-rated part numbers	—	10	—	dBm
Minimum active TX Power	POUT _{MIN}	CW		-27	—	dBm
Output power step size	POUT _{STEP}	-5 dBm < Output power < 0 dBm	—	0.5	—	dB
		0 dBm < output power < POUT _{MAX}	—	0.5	—	dB
Output power variation vs supply at POUT _{MAX}	POUT _{VAR_V}	1.8 V < V _{VDD} < 3.3 V, DCDC in bypass, MGM13P12	—	4.74	—	dB
		2.4 V < V _{VDD} < 3.3 V, MGM13P02	—	0	—	dB
		2.4 V < V _{VDD} < 3.3 V using DC-DC converter, MGM13P12	—	1.9	—	dB
Output power variation vs temperature at POUT _{MAX}	POUT _{VAR_T}	From -40 to +85 °C, MGM13P02	—	2.05	—	dB
		From -40 to +85 °C, MGM13P12	—	1.8	—	dB
Output power variation vs RF frequency at POUT _{MAX}	POUT _{VAR_F}	Over RF tuning frequency range	—	0.11	—	dB
RF tuning frequency range	F _{RANGE}		2400	—	2483.5	MHz

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.8.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.10. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F _{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	SPUR _{RX}	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm

4.1.8.3 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.11. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets. Using dc-dc converter.	—	-102.1	—	dBm
		Signal is reference signal. Packet length is 20 octets. Without dc-dc converter.	—	-102.1	—	dBm

4.1.8.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.12. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity, 0.1% BER	SENS	Signal is reference signal ¹ . Using dc-dc converter.	—	-102.8	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-102.4	—	dBm

Note:

1. Reference signal is defined 2GFSK at -79 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 125 kbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.8.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.13. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity, 0.1% BER	SENS	Signal is reference signal ¹ . Using dc-dc converter.	—	-98.4	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-97.4	—	dBm

Note:

1. Reference signal is defined 2GFSK at -72 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 500 kbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.8.6 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.14. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity, 0.1% BER	SENS	Signal is reference signal ¹ . Using dc-dc converter.	—	-94.6	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-94.4	—	dBm

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.8.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VDD = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.15. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity, 0.1% BER	SENS	Signal is reference signal ¹ . Using dc-dc converter.	—	-91	—	dBm
		With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.	—	-91	—	dBm

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 2 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.

4.1.9 Oscillators

4.1.9.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.16. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Overall frequency tolerance in all conditions ¹	FT_{LFXO}		-100	—	100	ppm
Note: 1. Nominal crystal frequency tolerance of ± 20 ppm.						

4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.17. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	38.4 MHz required for radio transceiver operation	—	38.4	—	MHz
Frequency tolerance for the crystal	FT_{HFXO}		-40	—	40	ppm

4.1.9.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.18. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f _{LFRCO}	ENVREF ¹ = 1	31.3	32.768	33.6	kHz
		ENVREF ¹ = 0	31.3	32.768	33.4	kHz
Startup time	t _{LFRCO}		—	500	—	μs
Current consumption ²	I _{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:

1. In CMU_LFRCOCTRL register.

2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.

4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.19. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{\text{HFRCO_ACC}}$	At production calibrated frequencies, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	$f_{\text{HFRCO}} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{\text{HFRCO}} < 19 \text{ MHz}$	—	1	—	μs
		$f_{\text{HFRCO}} \leq 4 \text{ MHz}$	—	2.5	—	μs
Current consumption on all supplies	I_{HFRCO}	$f_{\text{HFRCO}} = 38 \text{ MHz}$	—	267	299	μA
		$f_{\text{HFRCO}} = 32 \text{ MHz}$	—	224	248	μA
		$f_{\text{HFRCO}} = 26 \text{ MHz}$	—	189	211	μA
		$f_{\text{HFRCO}} = 19 \text{ MHz}$	—	154	172	μA
		$f_{\text{HFRCO}} = 16 \text{ MHz}$	—	133	148	μA
		$f_{\text{HFRCO}} = 13 \text{ MHz}$	—	118	135	μA
		$f_{\text{HFRCO}} = 7 \text{ MHz}$	—	89	100	μA
		$f_{\text{HFRCO}} = 4 \text{ MHz}$	—	34	44	μA
		$f_{\text{HFRCO}} = 2 \text{ MHz}$	—	29	40	μA
		$f_{\text{HFRCO}} = 1 \text{ MHz}$	—	26	36	μA
Coarse trim step size (% of period)	$SS_{\text{HFRCO_COARSE}}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{\text{HFRCO_FINE}}$		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS
Frequency limits	$f_{\text{HFRCO_BAND}}$	FREQRANGE = 0, FINETUNING = 0	3.47	—	6.15	MHz
		FREQRANGE = 3, FINETUNING = 0	6.24	—	11.45	MHz
		FREQRANGE = 6, FINETUNING = 0	11.3	—	19.8	MHz
		FREQRANGE = 7, FINETUNING = 0	13.45	—	22.8	MHz
		FREQRANGE = 8, FINETUNING = 0	16.5	—	29.0	MHz
		FREQRANGE = 10, FINETUNING = 0	23.11	—	40.63	MHz
		FREQRANGE = 11, FINETUNING = 0	27.27	—	48	MHz
		FREQRANGE = 12, FINETUNING = 0	33.33	—	54	MHz

4.1.9.5 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.20. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.10 Flash Memory Characteristics¹Table 4.21. Flash Memory Characteristics¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}		10	—	—	years
Word (32-bit) programming time	t_{W_PROG}	Burst write, 128 words, average time per word	20	26.3	30	μs
		Single word	62	68.9	80	μs
Page erase time ²	t_{PERASE}		20	29.5	40	ms
Mass erase time ³	t_{MERASE}		20	30	40	ms
Device erase time ^{4 5}	t_{DERASE}		—	56.2	70	ms
Erase current ⁶	I_{ERASE}	Page Erase	—	—	2.0	mA
Write current ⁶	I_{WRITE}		—	—	3.5	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	3.6	V

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- Mass erase is issued by the CPU and erases all flash.
- Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
- From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- Measured at 25 °C.

4.1.11 General-Purpose I/O (GPIO)

Table 4.22. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	$V_{DD} \cdot 0.3$	V
Input high voltage	V_{IH}	GPIO pins	$V_{DD} \cdot 0.7$	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, $V_{DD} \geq 3$ V, DRIVESTRENGTH ¹ = WEAK	$V_{DD} \cdot 0.8$	—	—	V
		Sourcing 1.2 mA, $V_{DD} \geq 1.62$ V, DRIVESTRENGTH ¹ = WEAK	$V_{DD} \cdot 0.6$	—	—	V
		Sourcing 20 mA, $V_{DD} \geq 3$ V, DRIVESTRENGTH ¹ = STRONG	$V_{DD} \cdot 0.8$	—	—	V
		Sourcing 8 mA, $V_{DD} \geq 1.62$ V, DRIVESTRENGTH ¹ = STRONG	$V_{DD} \cdot 0.6$	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = WEAK	—	—	$V_{DD} \cdot 0.2$	V
		Sinking 1.2 mA, $V_{DD} \geq 1.62$ V, DRIVESTRENGTH ¹ = WEAK	—	—	$V_{DD} \cdot 0.4$	V
		Sinking 20 mA, $V_{DD} \geq 3$ V, DRIVESTRENGTH ¹ = STRONG	—	—	$V_{DD} \cdot 0.2$	V
		Sinking 8 mA, $V_{DD} \geq 1.62$ V, DRIVESTRENGTH ¹ = STRONG	—	—	$V_{DD} \cdot 0.4$	V
Input leakage current	I_{IOLEAK}	GPIO $\leq V_{DD}$	—	0.1	30	nA
Input leakage current on 5VTOL pads above VDD	$I_{5VTOLLEAK}$	$V_{DD} < \text{GPIO} \leq V_{DD} + 2$ V	—	3.3	15	μ A
I/O pin pull-up/pull-down resistor	R_{PUD}		30	40	65	k Ω
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	45	ns
Output fall time, From 70% to 30% of V_{DD}	t_{IOOF}	$C_L = 50$ pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE ¹ = 0x6	—	1.8	—	ns
		$C_L = 50$ pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6	—	4.5	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output rise time, From 30% to 70% of V _{DD}	t _{IOOR}	C _L = 50 pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE = 0x6 ¹	—	2.2	—	ns
		C _L = 50 pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6	—	7.4	—	ns
Note: 1. In GPIO_Pn_CTRL register.						

4.1.12 Voltage Monitor (VMON)

Table 4.23. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_{SENSE})	I_{VMON}	In EM0 or EM1, 1 active channel	—	6.3	8	μA
		In EM0 or EM1, All channels active	—	12.5	15	μA
		In EM2, EM3 or EM4, 1 channel active and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 channel active and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, All channels active and above threshold	—	99	—	nA
		In EM2, EM3 or EM4, All channels active and below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at $1\text{V}/\mu\text{s}$ rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.24. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	V _{RESOLUTION}		6	—	12	Bits
Input voltage range ¹	V _{ADCIN}	Single ended	—	—	V _{FS}	V
		Differential	-V _{FS} /2	—	V _{FS} /2	V
Input range of external reference voltage, single ended and differential	V _{ADCREFIN_P}		1	—	V _{AVDD}	V
Power supply rejection ²	PSRR _{ADC}	At DC	—	80	—	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ³ = KEEPADC-WARM	I _{ADC_CONTINUOUS_LP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	270	290	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 ⁴	—	125	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 ⁴	—	80	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ³ = NORMAL	I _{ADC_NORMAL_LP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	45	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 ⁴	—	8	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEP-INSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_LP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	105	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	70	—	μA
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ³ = KEEPADC-WARM	I _{ADC_CONTINUOUS_HP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	325	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 ⁴	—	175	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 ⁴	—	125	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ³ = NORMAL	I _{ADC_NORMAL_HP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	85	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ⁴	—	16	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEP-INSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_HP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	160	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	125	—	μA
Current from HFPERCLK	I _{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	f_{ADCRATE}		—	—	1	Msp/s
Conversion time ⁵	t_{ADCCONV}	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	t_{ADCSTART}	WARMUPMODE ³ = NORMAL	—	—	5	μs
		WARMUPMODE ³ = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE ³ = KEEPINSLOWACC	—	—	1	μs
SNDR at 1Msp/s and f_{IN} = 10kHz	SNDR_{ADC}	Internal reference ⁶ , differential measurement	58	67	—	dB
		External reference ⁷ , differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	SFDR_{ADC}	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing codes	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Offset error	$V_{\text{ADCOFFSETERR}}$		-3	0	3	LSB
Gain error in ADC	V_{ADCGAIN}	Using internal reference	—	-0.2	3.5	%
		Using external reference	—	-1	—	%
Temperature sensor slope	$V_{\text{TS_SLOPE}}$		—	-1.84	—	mV/°C

Note:

1. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_CNTL register.
4. In ADCn_BIASPROG register.
5. Derived from ADCCLK.
6. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
7. External reference is 1.25 V applied externally to ADCn_EXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.

4.1.14 Analog Comparator (ACMP)

Table 4.25. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	$ACMPVDD = ACMPn_CTRL_PWRSEL^1$	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	$BIASPROG^2 \leq 0x10$ or FULL-BIAS ² = 0	1.8	—	$V_{VREGVDD_MAX}$	V
		$0x10 < BIASPROG^2 \leq 0x20$ and FULLBIAS ² = 1	2.1	—	$V_{VREGVDD_MAX}$	V
Active current not including voltage reference ³	I_{ACMP}	$BIASPROG^2 = 1$, FULLBIAS ² = 0	—	50	—	nA
		$BIASPROG^2 = 0x10$, FULLBIAS ² = 0	—	306	—	nA
		$BIASPROG^2 = 0x02$, FULLBIAS ² = 1	—	6.1	11	μA
		$BIASPROG^2 = 0x20$, FULLBIAS ² = 1	—	74	92	μA
Current consumption of internal voltage reference ³	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	—	2.4	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$)	$V_{ACMPHYST}$	$HYSTSEL^4 = HYST0$	-3	0	3	mV
		$HYSTSEL^4 = HYST1$	5	18	27	mV
		$HYSTSEL^4 = HYST2$	12	33	50	mV
		$HYSTSEL^4 = HYST3$	17	46	67	mV
		$HYSTSEL^4 = HYST4$	23	57	86	mV
		$HYSTSEL^4 = HYST5$	26	68	104	mV
		$HYSTSEL^4 = HYST6$	30	79	130	mV
		$HYSTSEL^4 = HYST7$	34	90	155	mV
		$HYSTSEL^4 = HYST8$	-3	0	3	mV
		$HYSTSEL^4 = HYST9$	-27	-18	-5	mV
		$HYSTSEL^4 = HYST10$	-50	-33	-12	mV
		$HYSTSEL^4 = HYST11$	-67	-45	-17	mV
		$HYSTSEL^4 = HYST12$	-86	-57	-23	mV
		$HYSTSEL^4 = HYST13$	-104	-67	-26	mV
		$HYSTSEL^4 = HYST14$	-130	-78	-30	mV
		$HYSTSEL^4 = HYST15$	-155	-88	-34	mV
Comparator delay ⁵	$t_{ACMPDELAY}$	$BIASPROG^2 = 1$, $FULLBIAS^2 = 0$	—	30	95	μs
		$BIASPROG^2 = 0x10$, $FULLBIAS^2 = 0$	—	3.7	10	μs
		$BIASPROG^2 = 0x02$, $FULLBIAS^2 = 1$	—	360	1000	ns
		$BIASPROG^2 = 0x20$, $FULLBIAS^2 = 1$	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	$BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$	-35	—	35	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	1.98	2.5	2.8	V
Capacitive sense internal resistance	R_{CSRES}	$CSRESSEL^6 = 0$	—	infinite	—	k Ω
		$CSRESSEL^6 = 1$	—	15	—	k Ω
		$CSRESSEL^6 = 2$	—	27	—	k Ω
		$CSRESSEL^6 = 3$	—	39	—	k Ω
		$CSRESSEL^6 = 4$	—	51	—	k Ω
		$CSRESSEL^6 = 5$	—	102	—	k Ω
		$CSRESSEL^6 = 6$	—	164	—	k Ω
		$CSRESSEL^6 = 7$	—	239	—	k Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. 2. In ACMPn_CTRL register. 3. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. 4. In ACMPn_HYSTERESIS registers. 5. ± 100 mV differential drive. 6. In ACMPn_INPUTSEL register.						

4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.26. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}	Single-Ended	0	—	V_{VREF}	V
		Differential ¹	$-V_{VREF}$	—	V_{VREF}	V
Current consumption including references (2 channels) ²	I_{DAC}	500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4	—	396	—	μA
		44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4	—	72	—	μA
		200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, REFSEL = 4, SETTLETIME = 0x02, WARMUP-TIME = 0x0A	—	1.2	—	μA
Current from HFPERCLK ³	I_{DAC_CLK}		—	5.8	—	$\mu A/MHz$
Sample rate	SR_{DAC}		—	—	500	ksps
DAC clock frequency	f_{DAC}		—	—	1	MHz
Conversion time	$t_{DACCONV}$	$f_{DAC} = 1MHz$	2	—	—	μs
Settling time	$t_{DACSETTLE}$	50% fs step settling to 5 LSB	—	2.5	—	μs
Startup time	$t_{DACSTARTUP}$	Enable to 90% fs output, settling to 10 LSB	—	—	12	μs
Output impedance	R_{OUT}	DRIVESTRENGTH = 2, $0.4 V \leq V_{OUT} \leq V_{OPA} - 0.4 V$, $-8 mA < I_{OUT} < 8 mA$, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, $0.4 V \leq V_{OUT} \leq V_{OPA} - 0.4 V$, $-400 \mu A < I_{OUT} < 400 \mu A$, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 2, $0.1 V \leq V_{OUT} \leq V_{OPA} - 0.1 V$, $-2 mA < I_{OUT} < 2 mA$, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, $0.1 V \leq V_{OUT} \leq V_{OPA} - 0.1 V$, $-100 \mu A < I_{OUT} < 100 \mu A$, Full supply range	—	2	—	Ω
Power supply rejection ratio ⁴	PSRR	$V_{out} = 50\% fs$. DC	—	65.5	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	SNDR _{DAC}	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	SNDR _{DAC_BAND}	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity ⁵	DNL _{DAC}		-0.99	—	1	LSB
Integral non-linearity	INL _{DAC}		-4	—	4	LSB
Offset error ⁶	V _{OFFSET}	T = 25 °C	-8	—	8	mV
		Across operating temperature range	-25	—	25	mV
Gain error ⁶	V _{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	-2.5	—	2.5	%
		T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5)	-5	—	5	%
		T = 25 °C, External reference (REFSEL = VDD or EXT)	-1.8	—	1.8	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	-3.5	—	3.5	%
		Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5)	-7.5	—	7.5	%
		Across operating temperature range, External reference (REFSEL = VDD or EXT)	-2.0	—	2.0	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External load capacitance, OUTSCALE=0	C _{LOAD}		—	—	75	pF

Note:

1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
3. Current from HUPERCLK is dependent on HUPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC peripheral is enabled in the CMU.
4. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$, VDAC output at 90% of full scale
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.

4.1.16 Current Digital to Analog Converter (IDAC)

Table 4.27. Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N _{IDAC_RANGES}		—	4	—	ranges
Output current	I _{IDAC_OUT}	RANGSEL ¹ = RANGE0	0.05	—	1.6	μA
		RANGSEL ¹ = RANGE1	1.6	—	4.7	μA
		RANGSEL ¹ = RANGE2	0.5	—	16	μA
		RANGSEL ¹ = RANGE3	2	—	64	μA
Linear steps within each range	N _{IDAC_STEPS}		—	32	—	steps
Step size	SS _{IDAC}	RANGSEL ¹ = RANGE0	—	50	—	nA
		RANGSEL ¹ = RANGE1	—	100	—	nA
		RANGSEL ¹ = RANGE2	—	500	—	nA
		RANGSEL ¹ = RANGE3	—	2	—	μA
Total accuracy, STEPSEL ¹ = 0x10	ACC _{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-3	—	3	%
		EM0 or EM1, Across operating temperature range	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t _{IDAC_SU}	Output within 1% of steady state value	—	5	—	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	μs
		Step value is changed	—	1	—	μs
Current consumption ²	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	15	μA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	18	μA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.023	—	μA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.041	—	μA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	μA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	μA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.11	—	%
		RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.06	—	%
		RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$	—	0.04	—	%
		RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.05	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.04	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.17 Capacitive Sense (CSEN)

Table 4.28. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	μs
		16-bit SAR Conversions	—	26.4	—	μs
		Delta Modulation Conversion (single comparison)	—	1.55	—	μs
Maximum external capacitive load	C_{EXTMAX}	IREFPROG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		IREFPROG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	k Ω
Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0	I_{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	25	—	nA
Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	57	—	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I _{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, IRE-FPROG=0 (Gain = 10x), always on	—	90.5	—	μA
HFPERCLK supply current	I _{CSEN_HFPERCLK}	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	μA/MHz

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the peripheral is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.18 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{1 2}.

Table 4.29. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply voltage (from AVDD)	V _{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	—	3.8	V
Input voltage	V _{IN}	HCMDIS = 0, Rail-to-rail input range	V _{VSS}	—	V _{OPA}	V
		HCMDIS = 1	V _{VSS}	—	V _{OPA} -1.2	V
Input impedance	R _{IN}		100	—	—	MΩ
Output voltage	V _{OUT}		V _{VSS}	—	V _{OPA}	V
Load capacitance ³	C _{LOAD}	OUTSCALE = 0	—	—	75	pF
		OUTSCALE = 1	—	—	37.5	pF
Output impedance	R _{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Buffer connection, Full supply range	—	0.25	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Buffer connection, Full supply range	—	0.6	—	Ω
		DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Buffer connection, Full supply range	—	0.4	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Buffer connection, Full supply range	—	1	—	Ω
Internal closed-loop gain	G _{CL}	Buffer connection	0.99	1	1.01	-
		3x Gain connection	2.93	2.99	3.05	-
		16x Gain connection	15.07	15.7	16.33	-
Active current ⁴	I _{OPA}	DRIVESTRENGTH = 3, OUTSCALE = 0	—	580	—	μA
		DRIVESTRENGTH = 2, OUTSCALE = 0	—	176	—	μA
		DRIVESTRENGTH = 1, OUTSCALE = 0	—	13	—	μA
		DRIVESTRENGTH = 0, OUTSCALE = 0	—	4.7	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G _{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency ⁵	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N _{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	μVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	μVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	μVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	μVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	μVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	μVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	μVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	μVrms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate ⁶	SR	DRIVESTRENGTH = 3, INCBW=1 ⁷	—	4.7	—	V/μs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/μs
		DRIVESTRENGTH = 2, INCBW=1 ⁷	—	1.27	—	V/μs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/μs
		DRIVESTRENGTH = 1, INCBW=1 ⁷	—	0.17	—	V/μs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/μs
		DRIVESTRENGTH = 0, INCBW=1 ⁷	—	0.044	—	V/μs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/μs
Startup time ⁸	T _{START}	DRIVESTRENGTH = 2	—	—	12	μs
Input offset voltage	V _{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	-2	—	2	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	-2	—	2	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	-12	—	12	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	-30	—	30	mV
DC power supply rejection ratio ⁹	PSRR _{DC}	Input referred	—	70	—	dB
DC common-mode rejection ratio ⁹	CMRR _{DC}	Input referred	—	70	—	dB
Total harmonic distortion	THD _{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V	—	90	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: - Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{\text{INPUT}} = 0.5 \text{ V}$, $V_{\text{OUTPUT}} = 0.5 \text{ V}$. - Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{\text{INPUT}} = 0.5 \text{ V}$, $V_{\text{OUTPUT}} = 1.5 \text{ V}$. Nominal voltage gain is 3. - If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information. - Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another $\sim 10 \mu\text{A}$ current when the OPAMP drives 1.5 V between output and ground. - In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network. - Step between 0.2V and $V_{\text{OPA}} - 0.2\text{V}$, 10%-90% rising/falling range. - When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable. - From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error $< 1\text{mV}$. - When HCMDIS=1 and input common mode transitions the region from $V_{\text{OPA}} - 1.4\text{V}$ to $V_{\text{OPA}} - 1\text{V}$, input offset will change. PSRR and CMRR specifications do not apply to this transition region.						

4.1.19 Pulse Counter (PCNT)

Table 4.30. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	10	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 Analog Port (APORT)

Table 4.31. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current ^{1 2}	I_{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	—	63	—	nA

Note:

- Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported peripheral currents. Additional peripherals requesting access to APORT do not incur further current.
- Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.

4.1.21 I2C

4.1.21.1 I2C Standard-mode (Sm)¹Table 4.32. I2C Standard-mode (Sm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	100	kHz
SCL clock low time	t _{LOW}		4.7	—	—	μs
SCL clock high time	t _{HIGH}		4	—	—	μs
SDA set-up time	t _{SU_DAT}		250	—	—	ns
SDA hold time ³	t _{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t _{SU_STA}		4.7	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		4	—	—	μs
STOP condition set-up time	t _{SU_STO}		4	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		4.7	—	—	μs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.21.2 I2C Fast-mode (Fm)¹Table 4.33. I2C Fast-mode (Fm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	400	kHz
SCL clock low time	t _{LOW}		1.3	—	—	μs
SCL clock high time	t _{HIGH}		0.6	—	—	μs
SDA set-up time	t _{SU_DAT}		100	—	—	ns
SDA hold time ³	t _{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t _{SU_STA}		0.6	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.6	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		1.3	—	—	μs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.21.3 I2C Fast-mode Plus (Fm+)¹Table 4.34. I2C Fast-mode Plus (Fm+)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	1000	kHz
SCL clock low time	t _{LOW}		0.5	—	—	μs
SCL clock high time	t _{HIGH}		0.26	—	—	μs
SDA set-up time	t _{SU_DAT}		50	—	—	ns
SDA hold time	t _{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.22 USART SPI

SPI Master Timing

Table 4.35. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		$2 * t_{HFERCLK}$	—	—	ns
CS to MOSI ^{1 2}	t_{CS_MO}		-12.5	—	14	ns
SCLK to MOSI ^{1 2}	t_{SCLK_MO}		-8.5	—	10.5	ns
MISO setup time ^{1 2}	t_{SU_MI}	IOVDD = 1.62 V	90	—	—	ns
		IOVDD = 3.0 V	42	—	—	ns
MISO hold time ^{1 2}	t_{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFERCLK}$ is one period of the selected HFERCLK.

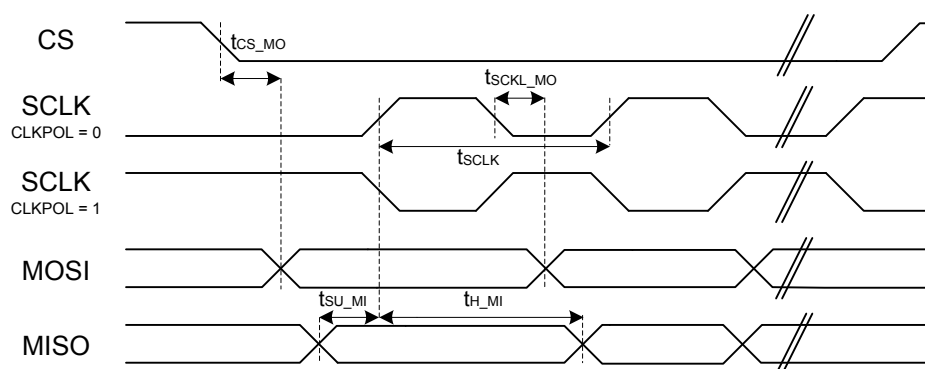


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.36. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		6 * $t_{HFERCLK}$	—	—	ns
SCLK high time ^{1 2 3}	t_{SCLK_HI}		2.5 * $t_{HFERCLK}$	—	—	ns
SCLK low time ^{1 2 3}	t_{SCLK_LO}		2.5 * $t_{HFERCLK}$	—	—	ns
CS active to MISO ^{1 2}	$t_{CS_ACT_MI}$		4	—	70	ns
CS disable to MISO ^{1 2}	$t_{CS_DIS_MI}$		4	—	50	ns
MOSI setup time ^{1 2}	t_{SU_MO}		12.5	—	—	ns
MOSI hold time ^{1 2 3}	t_{H_MO}		13	—	—	ns
SCLK to MISO ^{1 2 3}	t_{SCLK_MI}		6 + 1.5 * $t_{HFERCLK}$	—	45 + 2.5 * $t_{HFERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFERCLK}$ is one period of the selected HFERCLK.

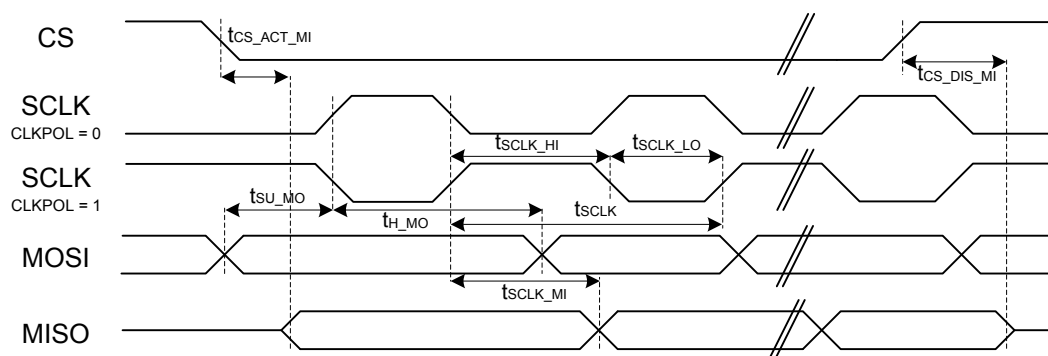


Figure 4.2. SPI Slave Timing Diagram

5. Typical Connection Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The MGM13P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug, and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

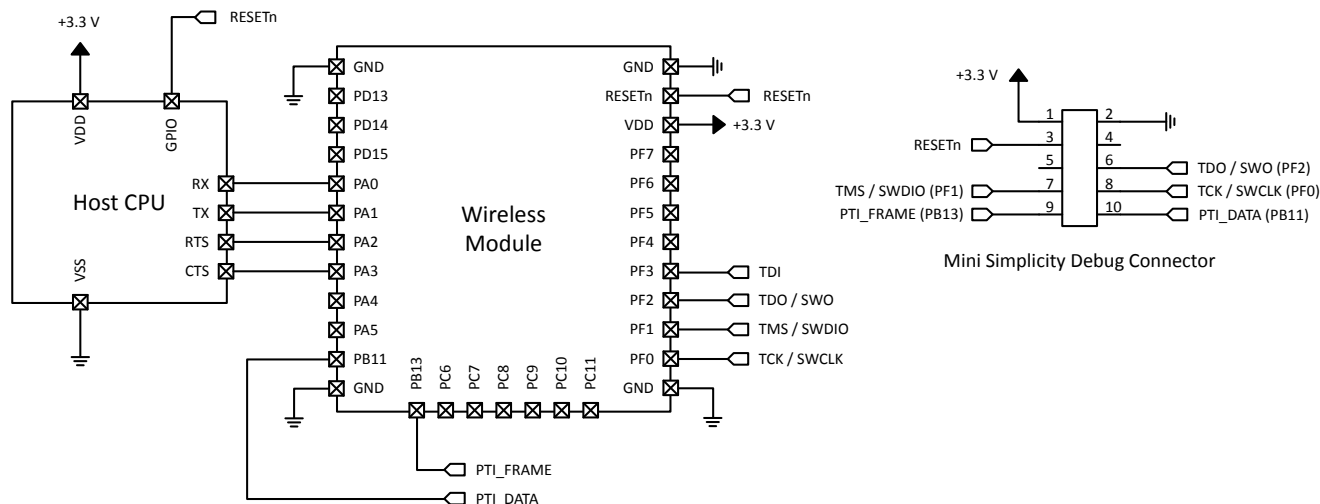


Figure 5.1. Connection Diagram: UART NCP Configuration

5.2 Network Co-Processor (NCP) Application with SPI Host

The MGM13P can be controlled over the SPI interface as a peripheral to an external host processor. Typical power supply, programming/debug and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

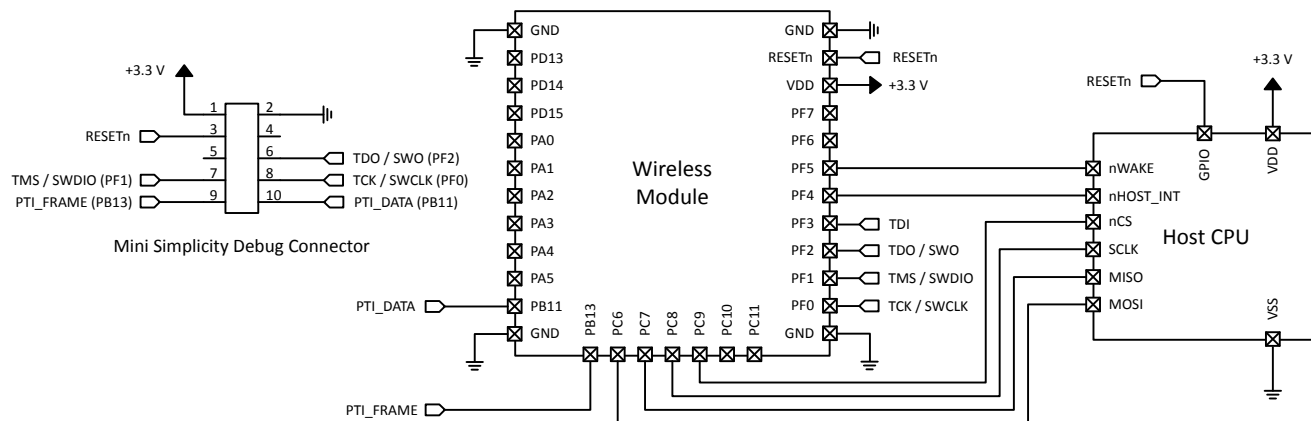


Figure 5.2. Connection Diagram: SPI NCP Configuration

5.3 SoC Application

The MGM13P can be used in a standalone SoC configuration with no external host processor. Typical power supply and programming/debug connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

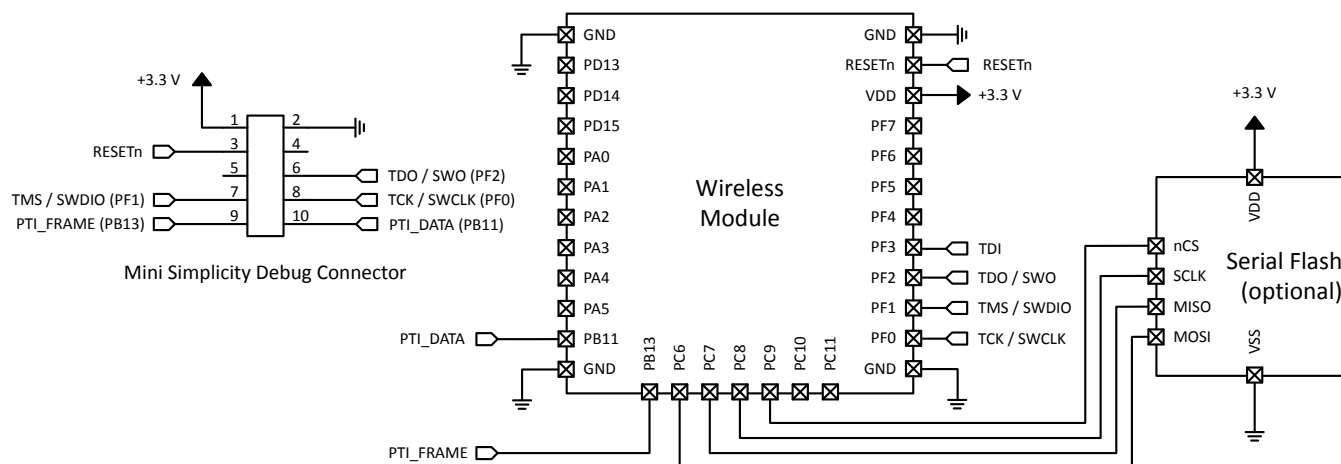


Figure 5.3. Connection Diagram: SoC Configuration

6. Layout Guidelines

For optimal performance of the MGM13P (with integrated antenna), please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

6.1 Module Placement and Application PCB Layout Guidelines

- Place the module at the edge of the PCB, as shown in [Figure 6.1 Recommended Application PCB Layout for MGM13P with Integrated Antenna on page 57](#).
- Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Do not place plastic or any other dielectric material in contact with the antenna.

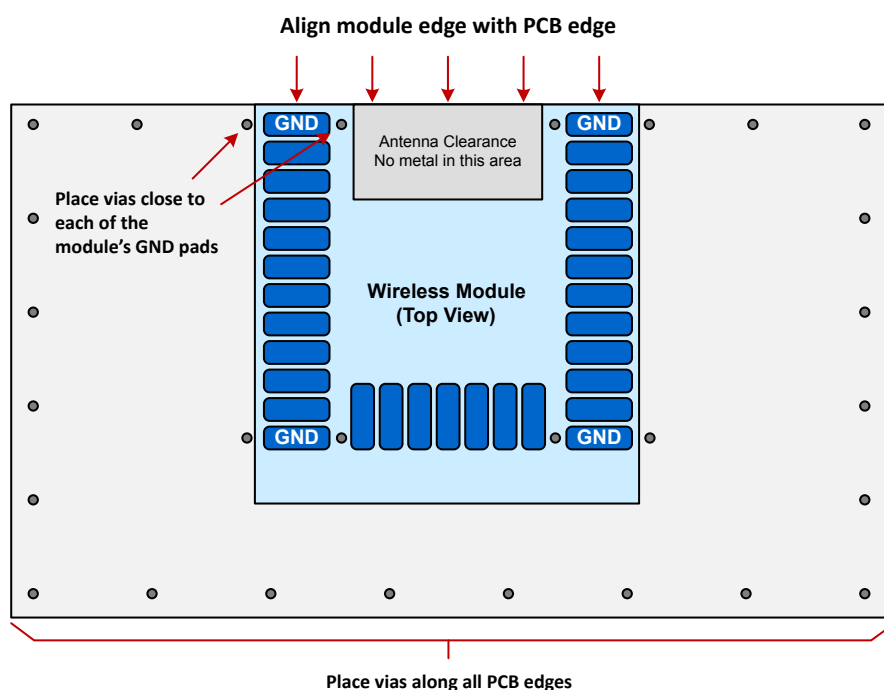


Figure 6.1. Recommended Application PCB Layout for MGM13P with Integrated Antenna

Figure 6.2 Non-optimal Module Placements for MGM13P with Integrated Antenna on page 58 shows examples of layouts that will result in severely degraded RF performance.

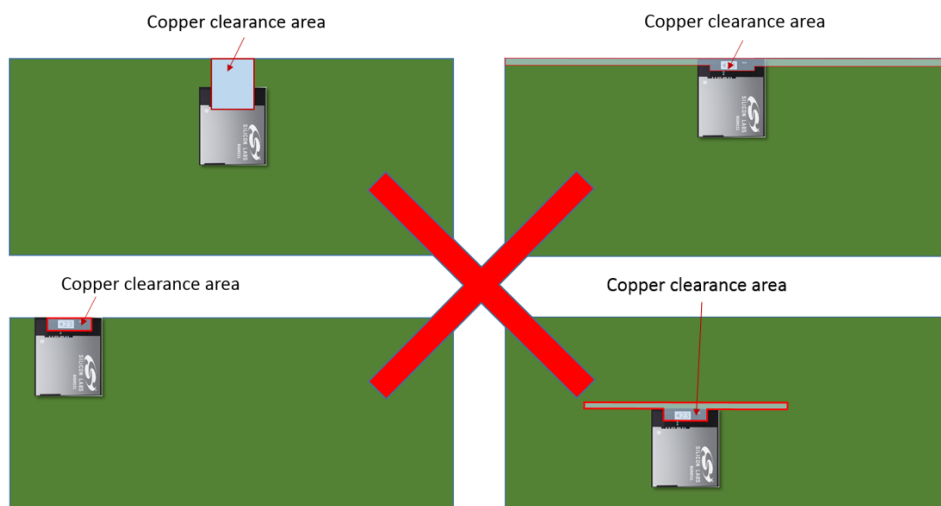


Figure 6.2. Non-optimal Module Placements for MGM13P with Integrated Antenna

The amount of ground plane surrounding the sides of the module will also impact the maximum RF range, as shown in Figure 6.3 Impact of GND Plane Size vs. Range for MGM13P on page 58.

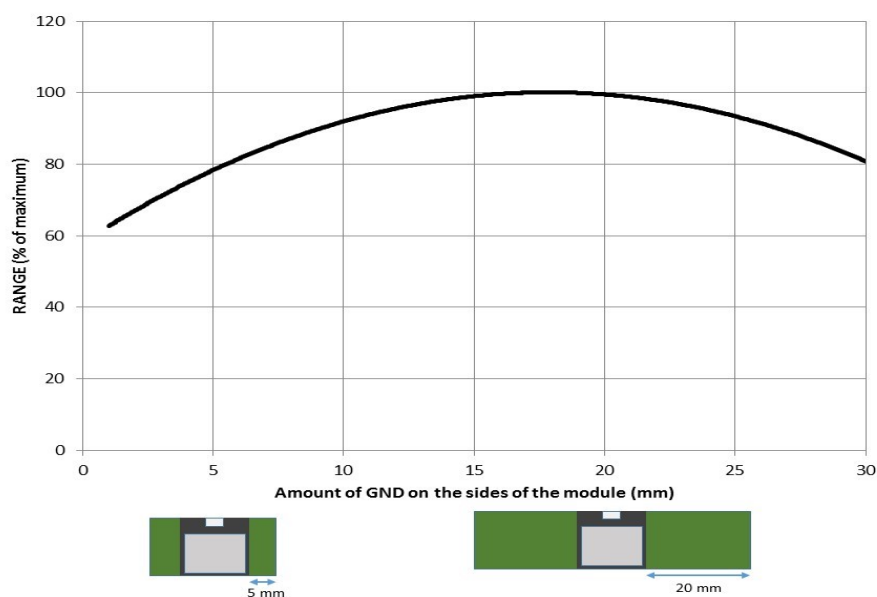


Figure 6.3. Impact of GND Plane Size vs. Range for MGM13P

6.2 Effect of Plastic and Metal Materials

Do not place plastic or any other dielectric material in close proximity to the antenna.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

6.3 Locating the Module Close to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

6.4 2D Radiation Pattern Plots

2D pattern, front view

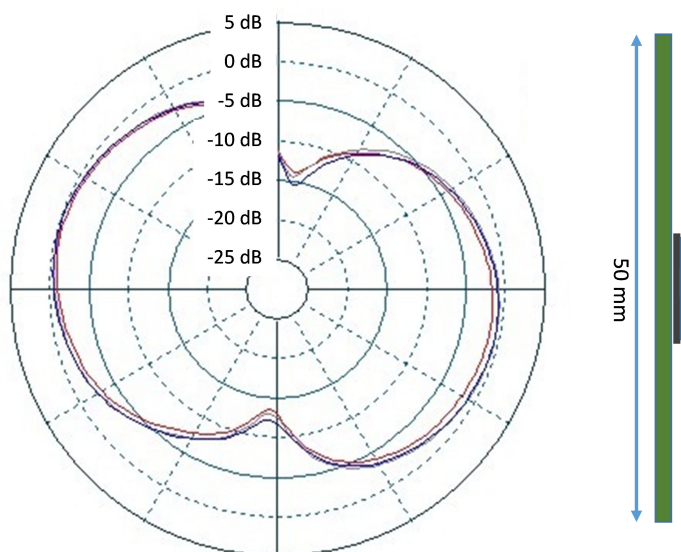


Figure 6.4. Typical 2D Radiation Pattern – Front View

2D pattern, side view

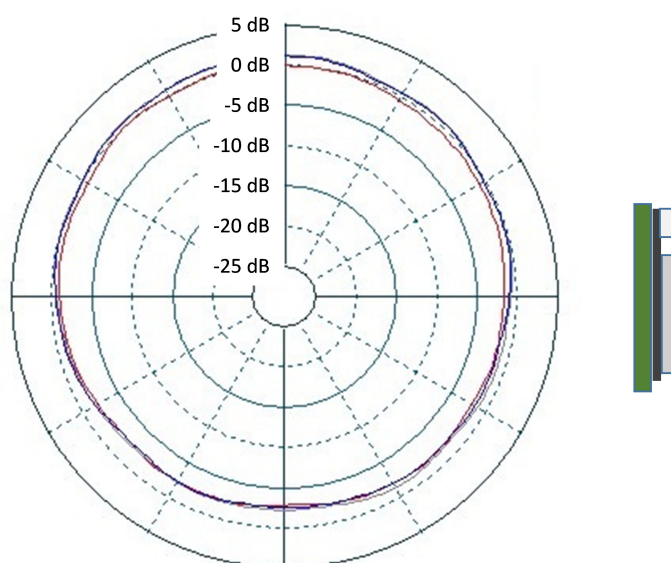


Figure 6.5. Typical 2D Radiation Pattern – Side View

2D pattern, top view

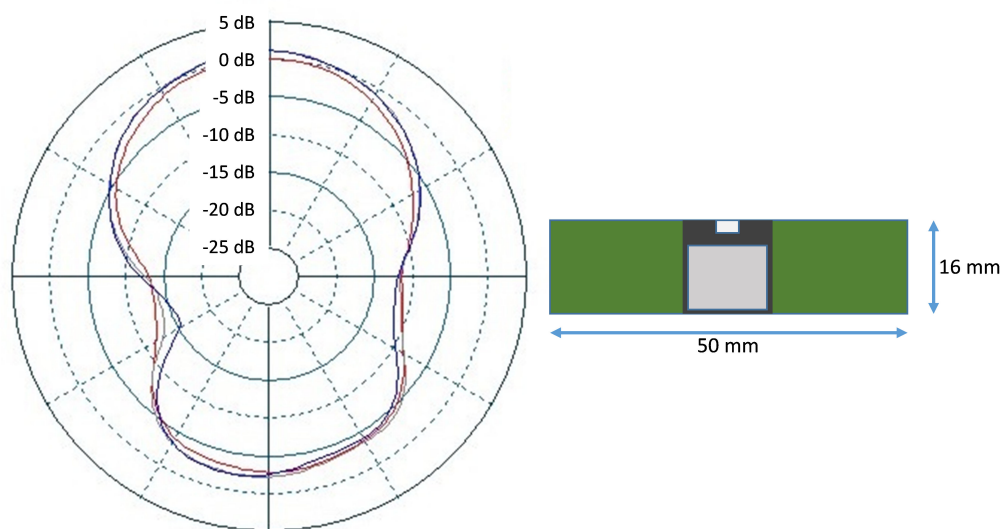


Figure 6.6. Typical 2D Radiation Pattern – Top View

7. Hardware Design Guidelines

The MGM13P is an easy-to-use module with regard to hardware application design. The guidelines in this section should be followed to guarantee optimal performance.

7.1 Power Supply Requirements

Coin cell batteries cannot withstand high peak currents (e.g. higher than 15 mA). If the peak current exceeds 15 mA it is recommended to place a 47 - 100 μ F capacitor in parallel with the coin cell battery to improve battery life time. Note that the total current consumption of the application is a combination of the radio, peripherals and MCU current consumption, and all power consumers must be taken into account. MGM13P should be powered by a unipolar supply voltage with nominal value of 3.3 V.

7.2 Reset Functions

The MGM13P can be reset by three different methods: by pulling the RESET line low, by the internal watchdog timer or by software command. The reset state in MGM13P does not provide any power saving functionality and is not recommended as a means to conserve power. MGM13P has an internal system power-up reset function. The RESET pin includes an on-chip pull-up resistor and can be left unconnected if no external reset switch or source is used.

7.3 Debug and Firmware Updates

Refer to the following application note: *AN958: Debugging and Programming Interfaces for Custom Designs*.

7.3.1 Programming and Debug Connections

It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes. The following table lists the required pins for JTAG connection and SWD connections.

Certain debug pins have internal pull-down or pull-ups enabled by default, and leaving them enabled may increase current consumption if left connected to supply or ground. If the JTAG pins are enabled, the module must be power cycled to return to a SWD debug configuration.

Table 7.1. Debug Pins

Pin Name	Pin Number	JTAG Signal	SWD Signal	Comments
PF3	24	TDI	N/A	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PF2	23	TDO	N/A	This pin is disabled after reset.
PF1	22	TMS	SWDIO	Pin is enabled after reset and has a built-in pull-up.
PF0	21	TCK	SWCLK	Pin is enabled after reset and has a built-in pull-down.

7.3.2 Packet Trace Interface (PTI)

The MGM13P integrates a true PHY-level packet trace interface (PTI) with the MAC, allowing complete, non-intrusive capture of all packets to and from the EFR32 Wireless STK development tools. The PTI_DATA and PTI_FRAME signals are configurable via software. Refer to for pin availability.

8. Pin Definitions

8.1 MGM13P Device Pinout

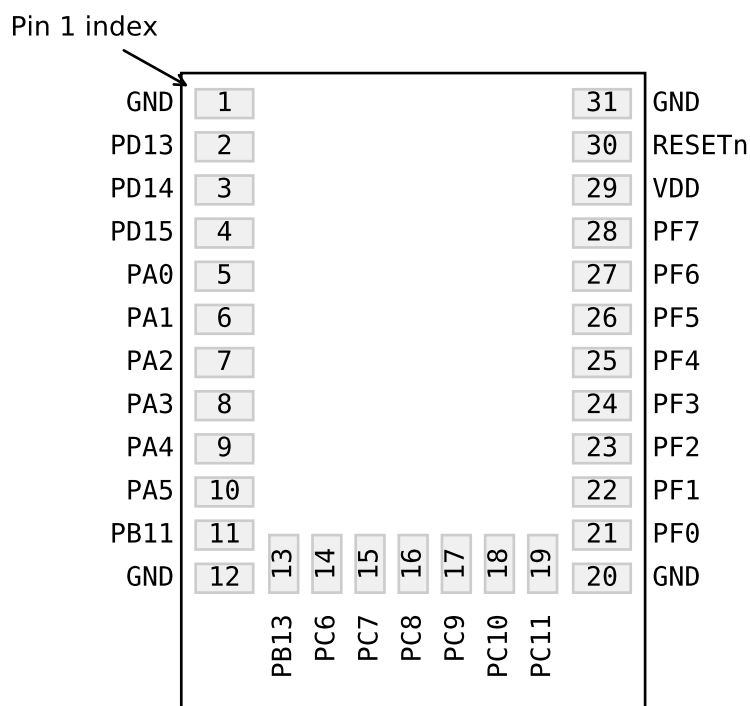


Figure 8.1. MGM13P Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [8.2 GPIO Functionality Table](#) or [8.3 Alternate Functionality Overview](#).

Table 8.1. MGM13P Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
GND	1 12 20 31	Ground	PD13	2	GPIO
PD14	3	GPIO	PD15	4	GPIO
PA0	5	GPIO	PA1	6	GPIO
PA2	7	GPIO	PA3	8	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA4	9	GPIO	PA5	10	GPIO (5V)
PB11	11	GPIO	PB13	13	GPIO
PC6	14	GPIO (5V)	PC7	15	GPIO (5V)
PC8	16	GPIO (5V)	PC9	17	GPIO (5V)
PC10	18	GPIO (5V)	PC11	19	GPIO (5V)
PF0	21	GPIO (5V)	PF1	22	GPIO (5V)
PF2	23	GPIO (5V)	PF3	24	GPIO (5V)
PF4	25	GPIO (5V)	PF5	26	GPIO (5V)
PF6	27	GPIO (5V)	PF7	28	GPIO (5V)
VDD	29	Module Power Supply	RESETn	30	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.

Note:

1. GPIO with 5V tolerance are indicated by (5V).

8.2 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [8.3 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 8.2. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8
PA1	BUSCY BUSDX ADC0_EXTP VDAC0_EXT	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 LES_CH9
PA2	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 WTIM0_CC0 #2 WTIM0_CC1 #0 LE- TIM0_OUT0 #2 LE- TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 LES_CH10

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA3	BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 WTIM0_CC0 #3 WTIM0_CC1 #1 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 LES_CH11 GPIO_EM4WU8
PA4	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 WTIM0_CC0 #4 WTIM0_CC1 #2 WTIM0_CC2 #0 LE- TIM0_OUT0 #4 LE- TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 LES_CH12
PA5	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 WTIM0_CC0 #5 WTIM0_CC1 #3 WTIM0_CC2 #1 LE- TIM0_OUT0 #5 LE- TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 US2_TX #0 US2_RX #31 US2_CLK #30 US2_CS #29 US2_CTS #28 US2_RTS #27 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3	CMU_CLKI0 #4 PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 LES_CH13 ETM_TCLK #1

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB11	BUSCY BUSDX OPA2_P	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LETIM0_OUT0 #6 LETIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 LETIM0_OUT0 #8 LETIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 WTIM0_CC0 #26 WTIM0_CC1 #24 WTIM0_CC2 #22 WTIM0_CDTI0 #18 WTIM0_CDTI1 #16 WTIM0_CDTI2 #14 LETIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MODEM_DOUT #9	CMU_CLK0 #2 CMU_CLKI0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 ETM_TCLK #3

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 WTIM0_CC0 #27 WTIM0_CC1 #25 WTIM0_CC2 #23 WTIM0_CDTI0 #19 WTIM0_CDTI1 #17 WTIM0_CDTI2 #15 LETIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MODEM_DOUT #10	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 ETM_TD0
PC8	BUSBY BUSAX	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 WTIM0_CC0 #28 WTIM0_CC1 #26 WTIM0_CC2 #24 WTIM0_CDTI0 #20 WTIM0_CDTI1 #18 WTIM0_CDTI2 #16 LETIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MODEM_DOUT #11	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13 ETM_TD1
PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 WTIM0_CC0 #29 WTIM0_CC1 #27 WTIM0_CC2 #25 WTIM0_CDTI0 #21 WTIM0_CDTI1 #19 WTIM0_CDTI2 #17 LETIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MODEM_DOUT #12	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14 ETM_TD2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC10	BUSBY BUSAX	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 WTIM0_CC0 #30 WTIM0_CC1 #28 WTIM0_CC2 #26 WTIM0_CDTI0 #22 WTIM0_CDTI1 #20 WTIM0_CDTI2 #18 LETIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 I2C1_SDA #19 I2C1_SCL #18	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 ETM_TD3 GPIO_EM4WU12
PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 LETIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3
PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 LETIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 LETIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 LETIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2
PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 LETIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK BOOT_TX

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 LETIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX
PF2	BUSBY BUSAX	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 WTIM0_CDTI2 #30 LETIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO DBG_SWO #0 GPIO_EM4WU0
PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 WTIM0_CDTI2 #31 LETIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF4	BUSBY BUSAX	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 US2_TX #17 US2_RX #16 US2_CLK #15 US2_CS #14 US2_CTS #13 US2_RTS #12 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LE- TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MODEM_DOUT #28	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE- TIM0_OUT0 #31 LE- TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MODEM_DOUT #29	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1

8.3 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [8.2 GPIO Functionality Table](#) for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 8.3. Alternate Functionality Overview

Alternate	LOCATION								Description
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin.
BOOT_RX	0: PF1								Bootloader RX.
BOOT_TX	0: PF0								Bootloader TX.
CMU_CLK0	0: PA1 2: PC6 3: PC11	5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 2: PC7 3: PC10	5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
CMU_CLKI0	0: PB13 1: PF7 2: PC6	4: PA5							Clock Management Unit, clock input number 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
ETM_TCLK	1: PA5 3: PC6								Embedded Trace Module ETM clock .
ETM_TDO	3: PC7								Embedded Trace Module ETM data 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ETM_TD1	3: PC8								Embedded Trace Module ETM data 1.
ETM_TD2	3: PC9								Embedded Trace Module ETM data 2.
ETM_TD3	3: PC10								Embedded Trace Module ETM data 3.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
I2C1_SCL					18: PC10 19: PC11				I2C1 Serial Clock Line input / output.
I2C1_SDA					19: PC10	20: PC11			I2C1 Serial Data input / output.
LES_CH5	0: PD13								LESENSE channel 5.
LES_CH6	0: PD14								LESENSE channel 6.
LES_CH7	0: PD15								LESENSE channel 7.
LES_CH8	0: PA0								LESENSE channel 8.
LES_CH9	0: PA1								LESENSE channel 9.
LES_CH10	0: PA2								LESENSE channel 10.
LES_CH11	0: PA3								LESENSE channel 11.
LES_CH12	0: PA4								LESENSE channel 12.
LES_CH13	0: PA5								LESENSE channel 13.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.
OPA0_N	0: PA4								Operational Amplifier 0 external negative input.
OPA0_P	0: PA2								Operational Amplifier 0 external positive input.
OPA1_N	0: PD15								Operational Amplifier 1 external negative input.
OPA1_P	0: PD13								Operational Amplifier 1 external positive input.
OPA2_N	0: PB13								Operational Amplifier 2 external negative input.
OPA2_P	0: PB11								Operational Amplifier 2 external positive input.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7 14: PC10 15: PC11	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input num- ber 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, chan- nel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, chan- nel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, chan- nel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2		12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, chan- nel 3.
PRS_CH4		4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, chan- nel 4.
PRS_CH5	3: PD13	4: PD14 5: PD15							Peripheral Reflex System PRS, chan- nel 5.
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13	15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, chan- nel 6.
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PA0						Peripheral Reflex System PRS, chan- nel 7.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PA5 2: PB11	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM0_CDTI2	0: PA5 1: PB11 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6 14: PC9 15: PC10	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7 14: PC10 15: PC11	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7 14: PC10 15: PC11	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6 14: PC9 15: PC10	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 6: PB13	9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	5: PB13	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11	4: PB13 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PA5 1: PB11 3: PB13	6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 7: PB13	10: PC6 11: PC7 14: PC10 15: PC11	12: PC8 13: PC9 14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11	8: PB13 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK				12: PF0 13: PF1 14: PF3 15: PF4	16: PF5 17: PF6 18: PF7			30: PA5	USART2 clock input / output.
US2_CS			11: PF0	12: PF1 13: PF3 14: PF4 15: PF5	16: PF6 17: PF7			29: PA5	USART2 chip select input / output.
US2_CTS			10: PF0 11: PF1	12: PF3 13: PF4 14: PF5 15: PF6	16: PF7			28: PA5	USART2 Clear To Send hardware flow control input.
US2_RTS			9: PF0 10: PF1 11: PF3	12: PF4 13: PF5 14: PF6 15: PF7			27: PA5		USART2 Request To Send hardware flow control output.
US2_RX				13: PF0 14: PF1 15: PF3	16: PF4 17: PF5 18: PF6 19: PF7			31: PA5	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PA5			14: PF0 15: PF1	16: PF3 17: PF4 18: PF5 19: PF6	20: PF7			USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
VDAC0_EXT	0: PA1								Digital to analog converter VDAC0 external reference input pin.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
VDAC0_OUT0 / OPA0_OUT	0: PA3								Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUT-ALT	0: PA5 1: PD13 2: PD15								Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PD14								Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUT-ALT	1: PA2 2: PA4								Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5		15: PB11	17: PB13		26: PC6 27: PC7	28: PC8 29: PC9 30: PC10 31: PC11	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PA2 1: PA3 2: PA4 3: PA5			13: PB11 15: PB13			24: PC6 25: PC7 26: PC8 27: PC9	28: PC10 29: PC11	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PA4 1: PA5		11: PB11	13: PB13		22: PC6 23: PC7	24: PC8 25: PC9 26: PC10 27: PC11		Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0		7: PB11	9: PB13		18: PC6 19: PC7	20: PC8 21: PC9 22: PC10 23: PC11		29: PD13 30: PD14 31: PD15	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1		5: PB11 7: PB13			16: PC6 17: PC7 18: PC8 19: PC9	20: PC10 21: PC11	27: PD13	28: PD14 29: PD15 30: PF0 31: PF1	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	3: PB11	5: PB13		14: PC6 15: PC7	16: PC8 17: PC9 18: PC10 19: PC11		25: PD13 26: PD14 27: PD15	28: PF0 29: PF1 30: PF2 31: PF3	Wide timer 0 Complimentary Dead Time Insertion channel 2.

8.4 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. [Figure 8.2 APORT Connection Diagram on page 84](#) shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

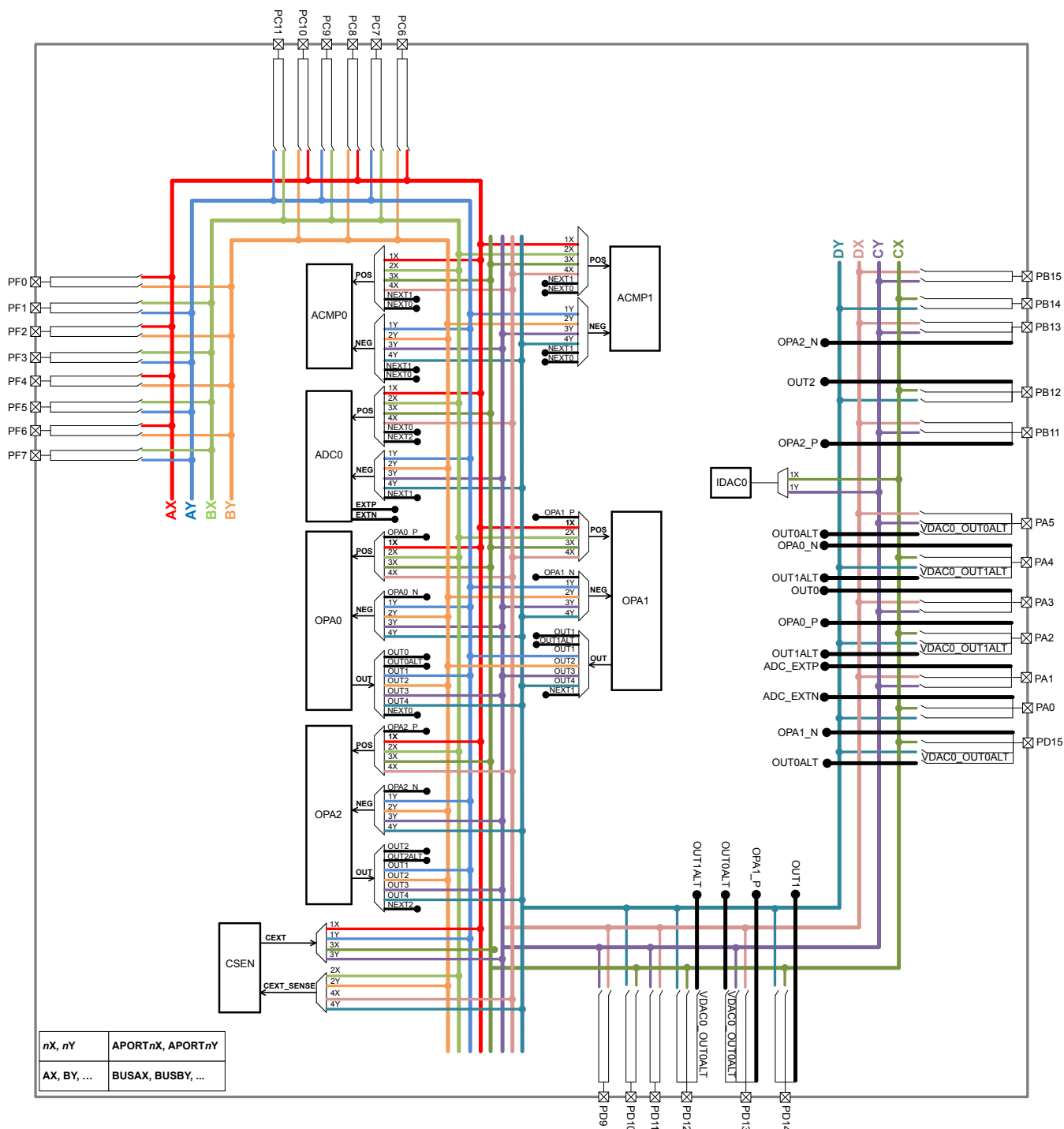


Figure 8.2. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 8.4. ACMP0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	Bus
								CH31
								CH30
	PB13	PB13						CH29
								CH28
	PB11	PB11						CH27
								CH26
								CH25
								CH24
					PF7	PF7		CH23
				PF6			PF6	CH22
					PF5	PF5		CH21
				PF4			PF4	CH20
					PF3	PF3		CH19
				PF2			PF2	CH18
					PF1	PF1		CH17
				PF0			PF0	CH16
								CH15
								CH14
	PA5	PA5						CH13
PA4			PA4					CH12
	PA3	PA3			PC11	PC11		CH11
PA2			PA2	PC10			PC10	CH10
	PA1	PA1			PC9	PC9		CH9
PA0			PA0	PC8			PC8	CH8
	PD15	PD15			PC7	PC7		CH7
PD14			PD14	PC6			PC6	CH6
	PD13	PD13						CH5
								CH4
								CH3
								CH2
								CH1
								CH0

Table 8.5. ACMP1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	Bus
								CH31
								CH30
	PB13	PB13						CH29
								CH28
	PB11	PB11						CH27
								CH26
								CH25
								CH24
					PF7	PF7		CH23
				PF6			PF6	CH22
					PF5	PF5		CH21
				PF4			PF4	CH20
					PF3	PF3		CH19
				PF2			PF2	CH18
					PF1	PF1		CH17
				PF0			PF0	CH16
								CH15
								CH14
	PA5	PA5						CH13
PA4			PA4					CH12
	PA3	PA3			PC11	PC11		CH11
PA2			PA2	PC10			PC10	CH10
	PA1	PA1			PC9	PC9		CH9
PA0			PA0	PC8			PC8	CH8
	PD15	PD15			PC7	PC7		CH7
PD14			PD14	PC6			PC6	CH6
	PD13	PD13						CH5
								CH4
								CH3
								CH2
								CH1
								CH0

Table 8.6. ADC0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	Bus
								CH31
								CH30
	PB13	PB13						CH29
								CH28
	PB11	PB11						CH27
								CH26
								CH25
								CH24
					PF7	PF7		CH23
				PF6			PF6	CH22
					PF5	PF5		CH21
				PF4			PF4	CH20
					PF3	PF3		CH19
				PF2			PF2	CH18
					PF1	PF1		CH17
				PF0			PF0	CH16
								CH15
								CH14
	PA5	PA5						CH13
PA4			PA4					CH12
	PA3	PA3			PC11	PC11		CH11
PA2			PA2	PC10			PC10	CH10
	PA1	PA1			PC9	PC9		CH9
PA0			PA0	PC8			PC8	CH8
	PD15	PD15			PC7	PC7		CH7
PD14			PD14	PC6			PC6	CH6
	PD13	PD13						CH5
								CH4
								CH3
								CH2
								CH1
								CH0

Table 8.7. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	APORT1Y	APORT3X	APORT3Y	BUSCY	BUSCX	BUSAY	BUSAX																										

Table 8.8. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
		CH31
		CH30
PB13		CH29
		CH28
PB11		CH27
		CH26
		CH25
		CH24
		CH23
		CH22
		CH21
		CH20
		CH19
		CH18
		CH17
		CH16
		CH15
		CH14
PA5		CH13
	PA4	CH12
PA3		CH11
	PA2	CH10
PA1		CH9
	PA0	CH8
PD15		CH7
	PD14	CH6
PD13		CH5
		CH4
		CH3
		CH2
		CH1
		CH0

Table 8.9. VDAC0 / OPA Bus and Pin Mapping

[illegible]

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA1_N																																	
APORT1Y	BUSAY																						PC11		PC9		PC7						
APORT2Y	BUSBY										PF6		PF4		PF2		PF0							PC10		PC8		PC6					
APORT3Y	BUSCY			PB13		PB11														PA5			PA3		PA1		PD15		PD13				
APORT4Y	BUSDY																				PA4		PA2		PA0		PD14						
OPA1_P																																	
APORT1X	BUSAX																							PC10		PC8		PC6					
APORT2X	BUSBX									PF7		PF5		PF3		PF1							PC11		PC9		PC7						
APORT3X	BUSCX																				PA4		PA2		PA0		PD14						
APORT4X	BUSDX		PB13		PB11															PA5		PA3		PA1		PD15		PD13					
OPA2_N																																	
APORT1Y	BUSAY																						PC11		PC9		PC7						
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY			PB13		PB11														PA5		PA3		PA1		PD15		PD13					
APORT4Y	BUSDY																				PA4		PA2		PA0		PD14						

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA2_OUT																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1							PC11		PC9		PC7						
APORT2Y	BUSBY										PF6		PF4		PF2		PF0							PC10		PC8		PC6					
APORT3Y	BUSCY			PB13		PB11														PA5			PA3		PA1		PD15		PD13				
APORT4Y	BUSDY																			PA4			PA2		PA0		PD14						
OPA2_P																																	
APORT1X	BUSAX										PF7	PF6		PF4		PF2								PC10		PC8		PC6					
APORT2X	BUSBX											PF5		PF4		PF3		PF1						PC11		PC9		PC7					
APORT3X	BUSCX																			PA4			PA2		PA0		PD14						
APORT4X	BUSDX		PB13		PB11															PA5			PA3		PA1		PD15		PD13				
VDAC0_OUT0 / OPA0_OUT																																	
APORT1Y	BUSAY									PF7		PF5		PF3		PF1							PC11		PC9		PC7						
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3Y	BUSCY			PB13		PB11														PA5			PA3		PA1		PD15		PD13				
APORT4Y	BUSDY																			PA4			PA2		PA0		PD14						

APORT4Y	APORT3Y	APORT2Y	APORT1Y	Port
BUSDY	BUSCY	BUSBY	BUSAY	Bus
				CH31
				CH30
	PB13			CH29
				CH28
	PB11			CH27
				CH26
				CH25
				CH24
			PF7	CH23
		PF6		CH22
			PF5	CH21
		PF4		CH20
			PF3	CH19
		PF2		CH18
			PF1	CH17
		PF0		CH16
				CH15
				CH14
	PA5			CH13
PA4				CH12
	PA3		PC11	CH11
PA2		PC10		CH10
	PA1		PC9	CH9
PA0		PC8		CH8
	PD15		PC7	CH7
PD14		PC6		CH6
	PD13			CH5
				CH4
				CH3
				CH2
				CH1
				CH0
VDA0_OUT1 / OPA1_OUT				

9. Package Specifications

9.1 Package Outline

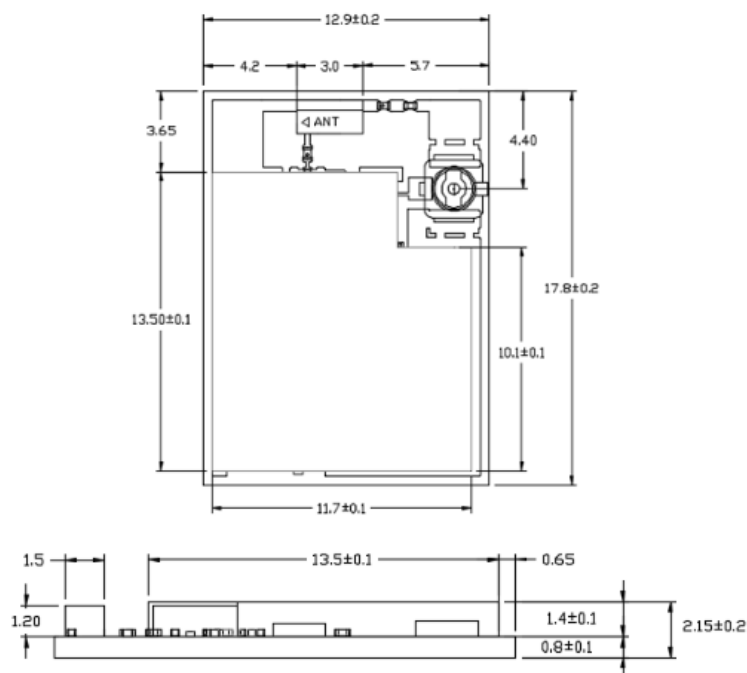


Figure 9.1. MGM13P with Antenna - Top and Side View

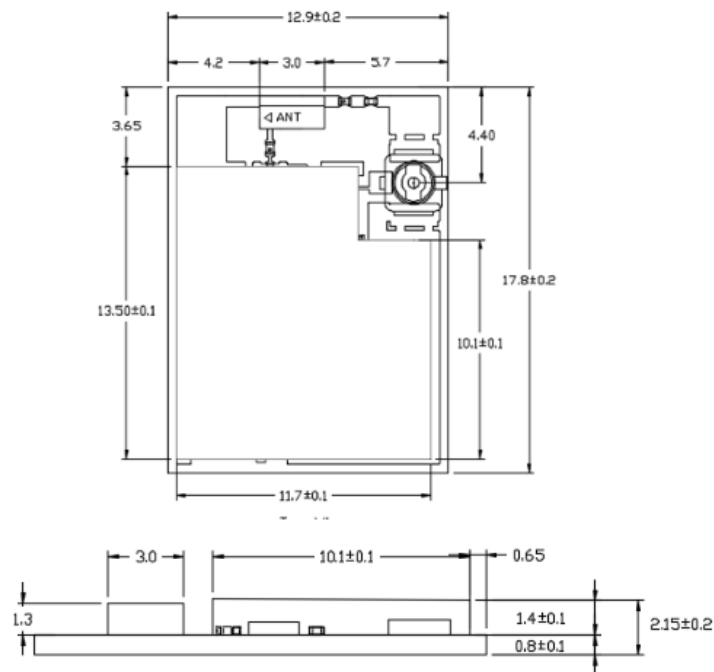


Figure 9.2. MGM13P with U.FL - Top and Side View

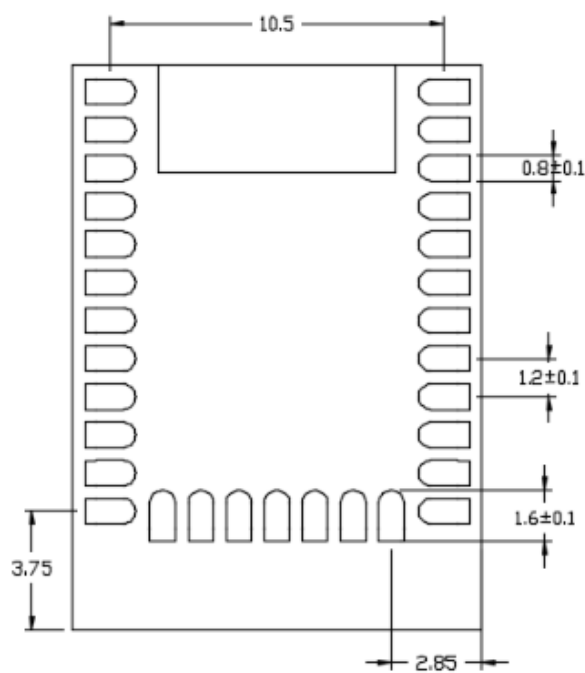


Figure 9.3. MGM13P Bottom View

9.2 Recommended PCB Land Pattern

The figure below shows the recommended land pattern. The antenna clearance section is not required for MGM13P module versions with a U.FL connector.

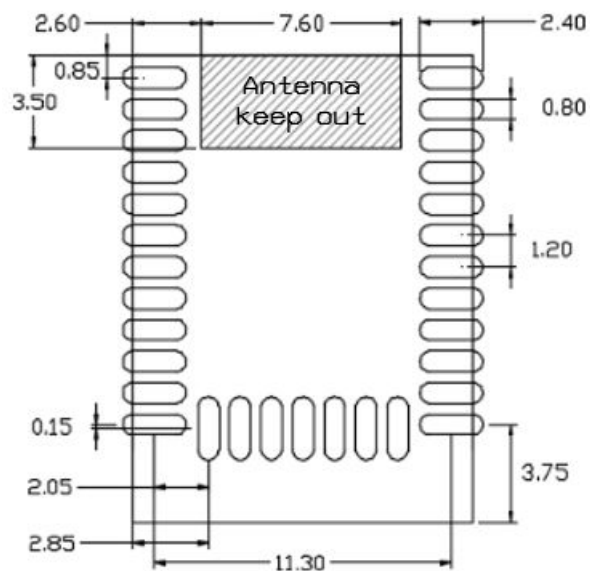


Figure 9.4. MGM13P Recommended PCB Land Pattern

9.3 Package Marking

The figure below shows the module markings printed on the RF-shield.

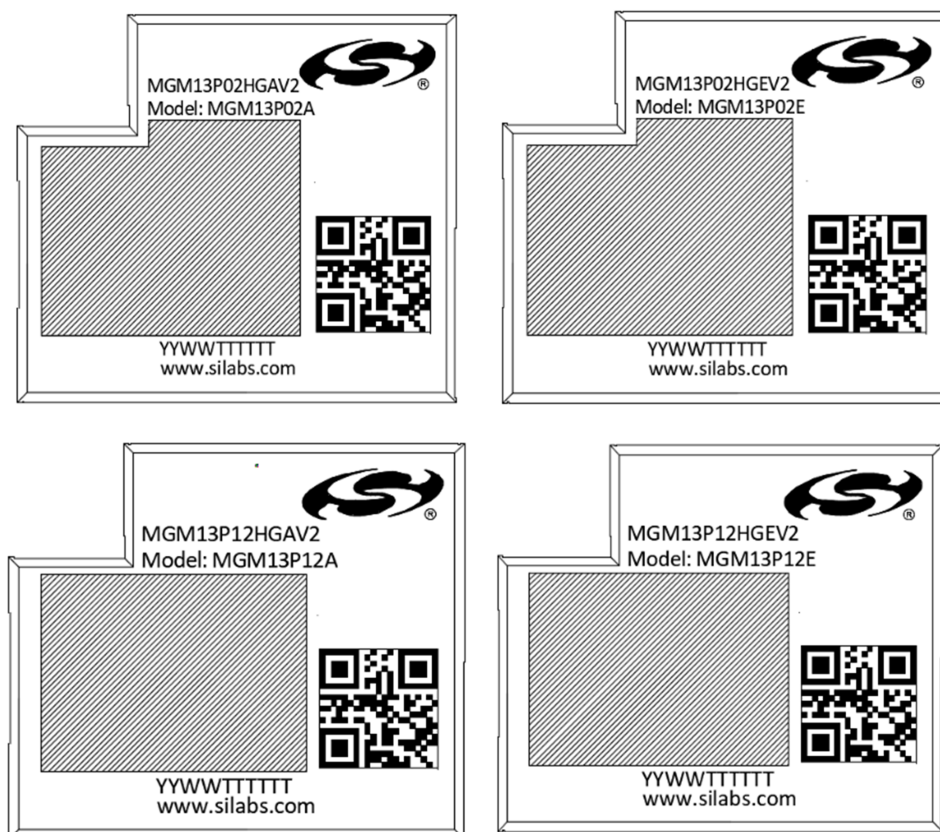


Figure 9.5. MGM13P Package Marking

Note: Module memory size in the Ordering Code (F512) is encoded as "H" in the package top mark.

Mark Description

The package marking consists of:

- MGM13Pxxxxxx - Part number designation.
- Model: MGM13Pxxxx - Model number designation.
- QR Code: YYWMMABCDE
 - YY - Last two digits of the assembly year.
 - WW - Two-digit workweek when the device was assembled.
 - MMABCDE - Silicon Labs unit code.
- YYWWTTTTTT
 - YY – Last two digits of the assembly year.
 - WW – Two-digit workweek when the device was assembled.
 - TTTTTT – Manufacturing trace code. The first letter is the device revision.
- Certification marks such as the CE logo, FCC and IC IDs, etc. will be engraved on the grayed out area, according to regulatory body requirements.

10. Soldering Recommendations

The MGM13P is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

- Refer to technical documentations of particular solder paste for profile configurations.
- Avoid using more than two reflow cycles.
- A no-clean, type-3 solder paste is recommended.
- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- Recommended stencil thickness is 0.100mm (4 mils).
- Refer to the recommended PCB land pattern for an example stencil aperture size.
- For further recommendation, please refer to the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines.
- Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

11. Certifications

11.1 Qualified Antenna Types

The MGM13P variants supporting an external antenna have been designed to operate with a standard 2.14 dBi dipole antenna. Any antenna of a different type or with a gain higher than 2.14 dBi is strictly prohibited for use with this device. Using an antenna of a different type or gain more than 2.14 dBi will require additional testing for FCC, CE and IC. The required antenna impedance is 50 Ω .

Table 11.1. Qualified Antennas for MGM13P

Antenna Type	Maximum Gain
Dipole	2.14 dBi

11.2 Bluetooth

The MGM13P is pre-qualified as a Low Energy RF-PHY tested component, having Declaration ID of D037287 and QDID of 101562. For the qualification of an end product embedding the MGM13P, the above should be combined with the most up to date Wireless Gecko Link Layer and Host components.

11.3 CE

The MGM13P02 module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) (2014/53/EU). Please note that every application using the MGM13P02 will need to perform the radio EMC tests on the end product, according to EN 301 489-17. It is ultimately the responsibility of the manufacturer to ensure the compliance of the end-product. The specific product assembly may have an impact to RF radiated characteristics, and manufacturers should carefully consider RF radiated testing with the end-product assembly. A formal DoC is available via www.silabs.com

The MGM13P12 module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) at up to 10 dBm RF transmit power when not using Adaptive Frequency Hopping (AFH). With early module firmware versions that do not support AFH and that do not have built-in functionality to limit the max RF transmit power to 10 dBm automatically, it is responsibility of the end-product's manufacturer to limit output power accordingly. With newer firmware versions supporting AFH, the end-product's manufacturer has the option to enable AFH and transmit at full output power while the module remains compliant or, alternatively, to disable AFH in which case the max RF transmit power will be automatically limited to 10 dBm, making the module compliant in all cases. Please refer to the firmware change log to verify which version introduced AFH.

11.4 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations:

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

- With MGM13P12 the antenna(s) must be installed such that a minimum separation distance of 50.5 mm is maintained between the radiator (antenna) and all persons at all times.
- With MGM13P02 the antenna(s) must be installed such that a minimum separation distance of 7.7 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

Important Note:

In the event that the above conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The variants of MGM13P Modules are labeled with their own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQMGM13P"

Or

"Contains FCC ID: QOQMGM13P"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

11.5 ISED Canada

ISED

This radio transmitter (IC: 5123A-MGM13P) has been approved by Industry Canada to operate with the antenna types listed above, with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The models MGM13P12A and MGM13P12E meet the given requirements when the minimum separation distance to human body is 35 mm.

The models MGM13P02A and MGM13P02E meet the given requirements when the minimum separation distance to human body is 20 mm.

RF exposure or SAR evaluation is not required when the separation distance is same or more than stated above. If the separation distance is less than stated above the OEM integrator is responsible for evaluating the SAR.

OEM Responsibilities to comply with IC Regulations

The MGM13P modules have been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE

In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the ISED authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate ISED authorization.

End Product Labeling

The MGM13P module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module IC: 5123A-MGM13P "

or

"Contains IC: 5123A-MGM13P"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

ISED (Français)

Industrie Canada a approuvé l'utilisation de cet émetteur radio (IC: 5123A-MGM13P) en conjonction avec des antennes de type dipolaire à 2.14dBi ou des antennes embarquées, intégrée au produit. L'utilisation de tout autre type d'antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'Industrie Canada. Son mode de fonctionnement est soumis aux deux conditions suivantes:

1. Ce composant ne doit pas générer d'interférences.
2. Ce composant doit pouvoir est soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

Déclaration d'exposition RF

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Les modules MGM13P12A and MGM13P12E répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 35 mm.

Les modules MGM13P02A and MGM13P02E répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 20 mm.

La déclaration d'exposition RF ou l'évaluation SAR n'est pas nécessaire lorsque la distance de séparation est identique ou supérieure à celle indiquée ci-dessus. Si la distance de séparation est inférieure à celle mentionnées plus haut, il incombe à l'intégrateur OEM de procéder à une évaluation SAR.

Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré

Le module MGM13P a été approuvé pour l'intégration dans des produits finaux exclusivement réalisés par des OEM sous les conditions suivantes:

- L'antenne (s) doit être installée de sorte qu'une distance de séparation minimale indiquée ci-dessus soit maintenue entre le radiateur (antenne) et toutes les personnes avoisinante, ce à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner avec une autre antenne ou un autre transmetteur que celle indiquée plus haut.

Tant que les deux conditions ci-dessus sont respectées, il n'est pas nécessaire de tester ce transmetteur de façon plus poussée. Cependant, il incombe à l'intégrateur OEM de s'assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l'utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

REMARQUE IMPORTANTE

ans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l'autorisation ISED n'est plus considérée comme valide et le numéro d'identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera responsable de la réévaluation du produit final (y compris le transmetteur) et de l'obtention d'une autorisation ISED distincte.

Étiquetage des produits finis

Les modules MGM13P sont étiquetés avec leur propre ID IC. Si l'ID IC n'est pas visible lorsque le module est intégré au sein d'un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaître les référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes:

“Contient le module transmetteur: 5123A-MGM13P ”

or

“Contient le circuit: 5123A-MGM13P”

L'intégrateur OEM doit être conscient qu'il ne doit pas fournir, dans le manuel d'utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.

11.6 Japan

The MGM13P02A and MGM13P02E are certified in Japan with certification number 209-J00283.

Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment can place the certification mark and certification number (the same marking/number as depicted on the label of the radio module) on the outside of the host equipment. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

"This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

The "Giteki" marking shown in the figures below must be affixed to an easily noticeable section of the specified radio equipment. Note that additional information may be required if the device is also subject to a telecom approval.



Figure 11.1. GITEKI Mark and ID

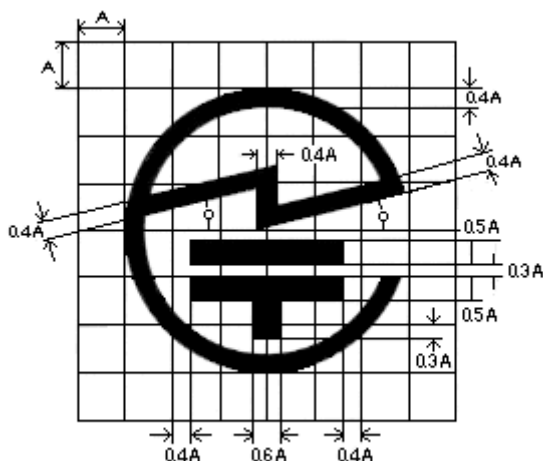


Figure 11.2. GITEKI Mark

11.7 KC South Korea

The MGM13P02A and MGM13P02E have certification in South-Korea.

Certification number: R-CRM-BGT-MGM13P02

12. Revision History

Revision 1.2

April, 2020

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Removed Wake On Radio references wherever applicable since this feature is not supported by the software.
- Removed multiprotocol from protocol stack [Table 2.1 Ordering Information on page 3](#).
- Updated [3.2 Radio](#) overview.
- Updated [3.6.4 Low Energy Timer \(LETIMER\)](#) lowest energy mode.
- Updated DCDC Low Power Mode configuration note in [Table 4.4 Current Consumption 3.3 V using DC-DC Converter on page 21](#).
- Updated wording in [Table 4.23 Voltage Monitor \(VMON\) on page 33](#).
- Updated VDAC test conditions for EM2 current consumption [Table 4.26 Digital to Analog Converter \(VDAC\) on page 39](#).
- Updated register name IREFPROG for CSEN test conditions [Table 4.28 Capacitive Sense \(CSEN\) on page 44](#).
- Updated PTI description [7.3.2 Packet Trace Interface \(PTI\)](#).
- Updated package drawing and specifications in [9.1 Package Outline](#).
- Updated dimensions [9.2 Recommended PCB Land Pattern](#).
- Updated [9.3 Package Marking](#) images and description.
- Additional text regarding [10. Soldering Recommendations](#).
- Updated text in [11.3 CE](#).
- Added [11.7 KC South Korea](#).
- Minor wording change regarding peripheral modules.

Revision 1.1

September 2018

- Added 19 dBm part numbers (MGM13P12) and associated specifications and details.

Revision 1.01

August 2018

- Added Electrical Specifications Tables for VDAC, CSEN, OPAMP, PCNT and APORT.
- [Table 8.2 GPIO Functionality Table on page 64](#): Sorted by GPIO name.
- Removed unbonded I/O from APORT mapping tables.
- Removed tape and reel specifications section.

Revision 1.0

February 2018

- Added V2 part numbers to [Table 2.1 Ordering Information on page 3](#).
- Updated with latest characterization data and test limits.
- Added certification details.

Revision 0.1

September 15, 2017

- Initial Release.

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