



MF520

3-Phase Brushless DC Motor Controller

Data Sheet

Version 0.01 – Apr. 14, 2020

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Revision History:

Revision	Date	Description
0.00	2020/01/07	Preliminary version
0.01	2020/04/14	1. Amend Chapter 1 and Section 3.1: Operating Temperature 2. Update DC/AC Characteristics: V_{DD} , f_{SYS} , R_{PH} , f_{IHRC} , f_{ILRC} , $ADoS$

1. Key Features

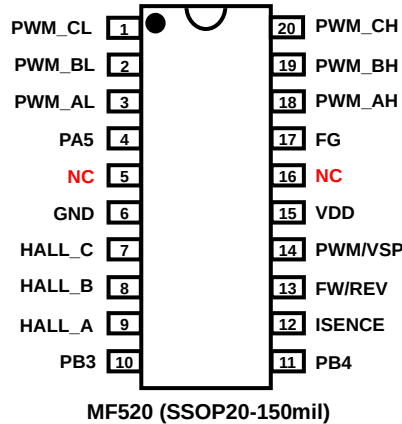
- 3-Phase brushless DC motor with hall IC interface
- Sine wave / square wave
- PWM or voltage control input
- FG output
- Software hall degree forward
- Close loop or/and open loop control
- Current limit and over-current protection
- Lock-protect and auto-restart
- System protection
 - Low-voltage detection with reset
 - Illegal opcode detection with reset
- MTP Programming
 - Support 6-wire factory programming mode
 - Support 4-wire in-system programming mode
- BLDC Applications
 - Operating voltage range: 3.5V~5.5V
 - Operating temperature range: -40°C~85°C
- 20-pin SSOP20 package

MF520 is a 3-phase BLDC motor controller based on 8-bit 8-FPPA MCU which can be programmed by 6-wire factory mode or 4-wire ISP mode. MF520 receives motor position signal from Hall IC and can control the sine wave or six step square wave flexibly to make the best efficiency of the motor. Through the PADAUK patented AP development system, it can easily set any speed curve, output signal and protection parameters etc., and it can observe the motor response online immediately. Using the MF520's development system, it's much easier and adjustable for application.

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2. Pin Diagram and Pin Description



Pin No.	Pin Name	I/O	Description
1	PWM_CL	Output	C output signal to control the low side of motor driver
2	PWM_BL	Output	B output signal to control the low side of motor driver
3	PWM_AL	Output	A output signal to control the low side of motor driver
4	PA5	I/O	Digital input / digital output / analog input
5	NC	-	NA
6	GND	-	Ground
7	HALL_C	Input	Digital input to sense motor position C
8	HALL_B	Input	Digital input to sense motor position B
9	HALL_A	Input	Digital input to sense motor position A
10	PB3	I/O	Digital input / digital output / analog input
11	PB4	I/O	Digital input / digital output / analog input
12	ISENSE	Input	Analog input to sense motor current
13	FW/REV	Input	Forward / Reverse control input
14	PWM_IN	Input	PWM control input
15	VDD	-	Positive power
16	NC	-	NA
17	FG	Output	Rotation speed detection
18	PWM_AH	Output	A output signal to control the high side of motor driver
19	PWM_BH	Output	B output signal to control the high side of motor driver
20	PWM_CH	Output	C output signal to control the high side of motor driver

3. Device Characteristics

3.1. Absolute Maximum Ratings

Name	Min	Typ.	Max	Unit	Notes
Supply Voltage (VDD)	3.5		5.5	V	Exceed the maximum rating may cause permanent damaged !!
Input Voltage	-0.3		$V_{DD} + 0.3$	V	
Operating Temperature	-40		85	°C	
Storage Temperature	-50		125	°C	
Junction Temperature		150		°C	

3.2. DC/AC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25°C)
V_{DD}	Operating Voltage	3.5	5.0	5.5	V	-40 °C < Ta < 85 °C
V_{FSV}	Forbidden V_{DD} startup voltage range	0.7		1.6	V	
V_{PORV}	V_{DD} power down release voltage			0.7	V	
T_{POR}	V_{DD} power on time (V_{DD} from 0V to 5V)			50	ms	
T_{FSV}	V_{DD} power on time during V_{FSV} range			10	ms	
f_{SYS}	System clock IHRC IHRC Internal low RC oscillator	0 0	33.8K	8M 4M	Hz	$V_{DD} = 3.3V$ $V_{DD} = 2.5V$ $V_{DD} = 5.0V$
I_{OP}	Operating Current		1.8 3.5 150 8		mA mA uA uA	$f_{SYS}=1MIPS@5.0V$ $f_{SYS}=8MIPS@5.0V$ $f_{SYS}=ILRC \sim 32KHz@5.0V$ $f_{SYS}=ILRC \sim 12KHz@3.3V$
I_{PD}	Power Down Current (by stopsys command)		3 1		uA uA	$V_{DD}=5.0V$ $V_{DD}=3.3V$
I_{PS}	Power Save Current (by stopexe command)		0.4		mA	$V_{DD}=5.0V$; Band-gap, LVD, IHRC, ILRC, Timer16 modules are ON.
V_{IL}	Input low voltage for IO lines	0		$0.2V_{DD}$	V	
V_{IH}	Input high voltage for IO lines	$0.8 V_{DD}$		V_{DD}	V	
I_{OL}	IO lines sink current	11	14	17	mA	$V_{DD}=5.0V$, $V_{OL}=0.5V$
I_{OH}	IO lines drive current	-8	-10	-12	mA	$V_{DD}=5.0V$, $V_{OH}=4.5V$
R_{PH}	Pull-high Resistance		90 170		K Ω	$V_{DD}=5.0V$ $V_{DD}=3.3V$
V_{BRD}	Low Voltage Detect Voltage *	4.2	4.5	4.8	V	

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Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25°C)
	(Brown-out voltage)	3.7 3.35 3.25 3.05 2.9 2.75 2.47	4 3.75 3.5 3.3 3.15 3 2.7	4.3 4.05 3.75 3.55 3.4 3.25 2.93		
V _{BG}	Band-gap Reference Voltage (before calibration)	1.12	1.20	1.28	V	V _{DD} =5V, 25°C
	Band-gap Reference Voltage * (after calibration)	1.17*	1.20*	1.23*		V _{DD} =2.5V ~ 5.5V, -40°C < Ta < 85°C*
f _{IHRC}	Frequency of IHRC after calibration *	15.52*	16*	16.48*1 6.32*	MHz	25°C, V _{DD} =3V~5.5V
		15*	16*	17.28*		V _{DD} =3V~5.5V, -40°C < Ta < 105°C*
f _{ILRC}	Frequency of ILRC *	20.4*	24*	27.6*	KHz	V _{DD} =5.0V, Ta=25°C
		15.6*	24*	32.4*		V _{DD} =5.0V, -40°C < Ta < 85°C*
		10.2*	12*	13.8*		V _{DD} =3.3V, Ta=25°C
		7.8*	12*	16.2*		V _{DD} =3.3V, -40°C < Ta < 85°C*
V _{ADC}	Workable ADC operating Voltage	2.5		5.0	V	
V _{AD}	AD Input Voltage	0		V _{DD}	V	
ADrs	ADC resolution			11	bit	
ADclk	ADC clock period		2		us	2.5V ~ 5.5V
t _{ADCONV}	ADC conversion time (T _{ADCLK} is the period of the selected AD conversion clock)		14		T _{ADCLK}	
AD DNL	ADC Differential NonLinearity		±3*		LSB	
AD INL	ADC Integral NonLinearity		±3*		LSB	
ADos	ADC offset*		3 4		LSB	-40°C < Ta < 85°C* -40°C < Ta < 105°C*
t _{INT}	Interrupt pulse width	30			ns	V _{DD} = 5.0V
V _{DR}	RAM data retention voltage*	1.5			V	In power-down mode.
	Watchdog timeout period (T _{ILRC} is the clock period of ILRC)		4096			misc[1:0]=01
			16384			misc[1:0]=10
t _{SBP}	System boot-up period from power-on		1024		T _{ILRC}	Where T _{ILRC} is the clock period of ILRC

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Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25°C)
t _{WUP}	System wake-up period					
	Fast wake-up by IO toggle from STOPEXE suspend		128		T _{SYS}	Where T _{SYS} is the time period of system clock
	Fast wake-up by IO toggle from STOPSYS suspend, IHRC is the system clock		128 T _{SYS} + T _{SIHRC}			Where T _{SIHRC} is the stable time of IHRC from power-on.
	Fast wake-up by IO toggle from STOPSYS suspend, ILRC is the system clock		128 T _{SYS} + T _{SILRC}			Where T _{SILRC} is the stable time of ILRC from power-on.
	Normal wake-up from STOPEXE or STOPSYS suspend		1024		T _{ILRC}	Where T _{ILRC} is the clock period of ILRC
HCPos	Comparator offset*	-	±10	±20	mV	
HCPcm	Comparator input common mode*	0		V _{DD} -1.5	V	
HCPspt	Comparator response time**		100	500	ns	Both Rising and Falling
HCPmc	Stable time to change comparator mode		2.5	7.5	us	

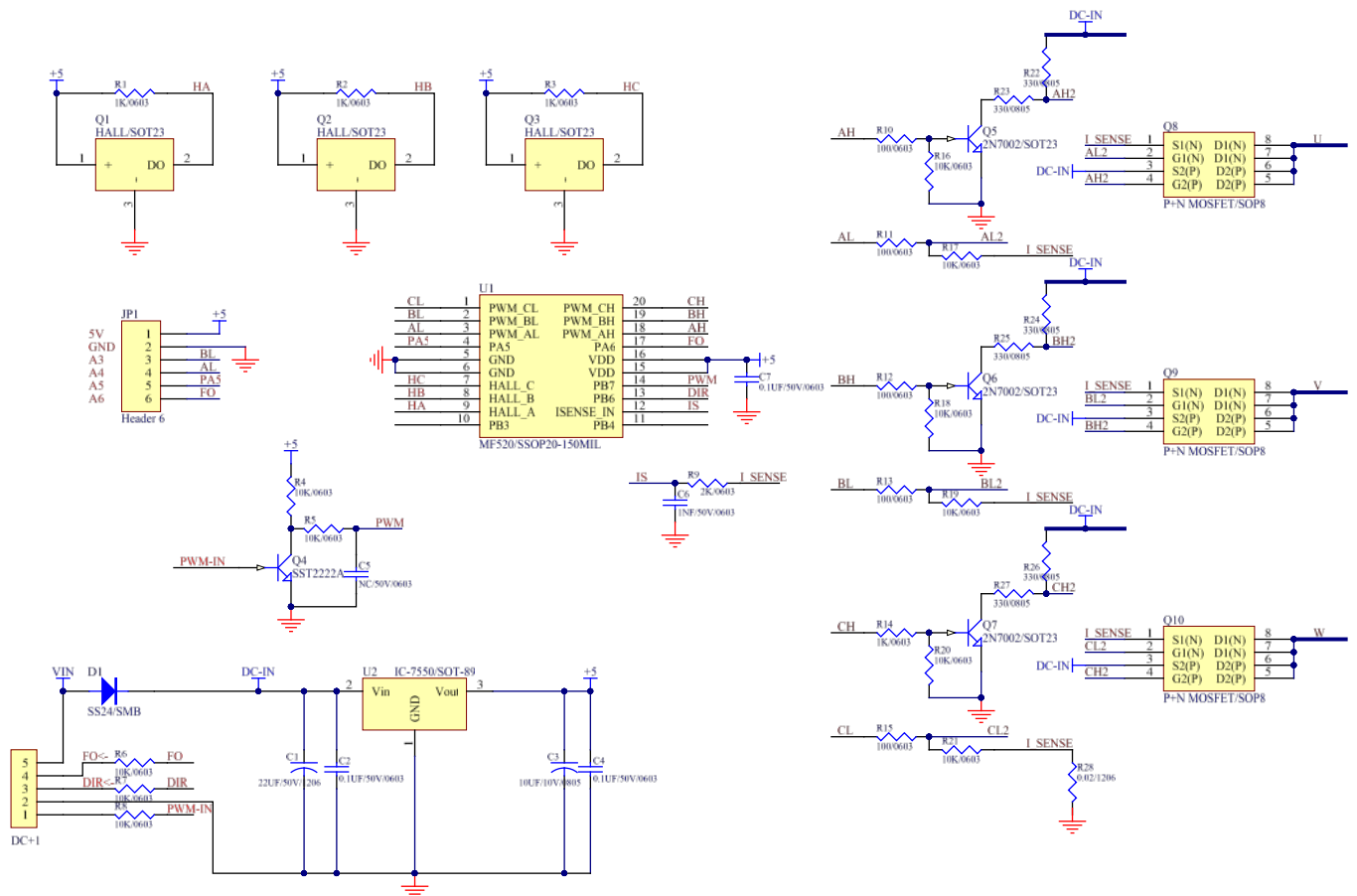
*These parameters are for design reference, not tested for every chip.

** Response time is measured with comparator input at (V_{DD}-1.5)/2 -100mV, and (V_{DD}-1.5)/2+100mV

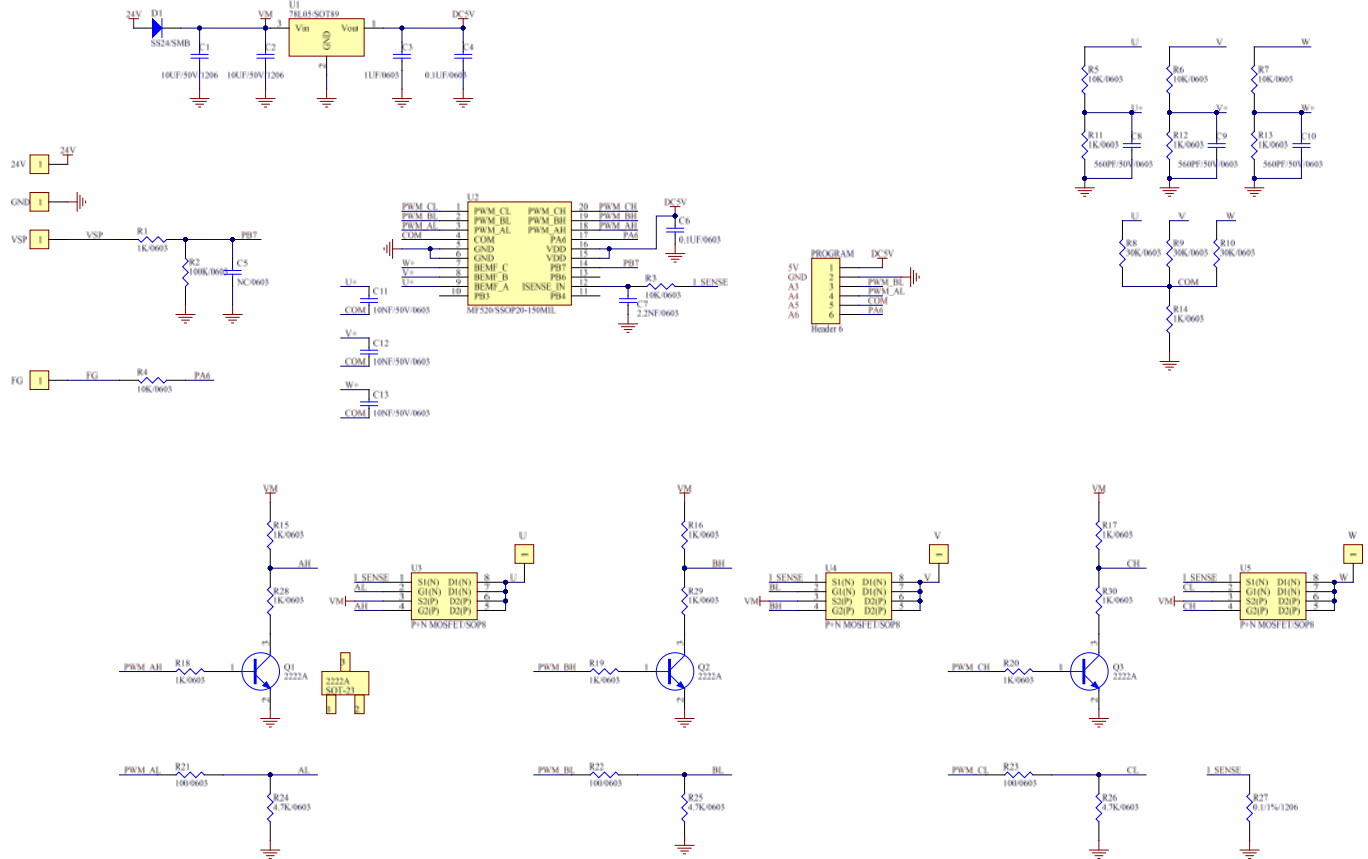
The characteristic diagrams are the actual measured values. Considering the influence of production drift and other factors, the data in the table are within the safety range of the actual measured values.

4. Reference Application Circuit

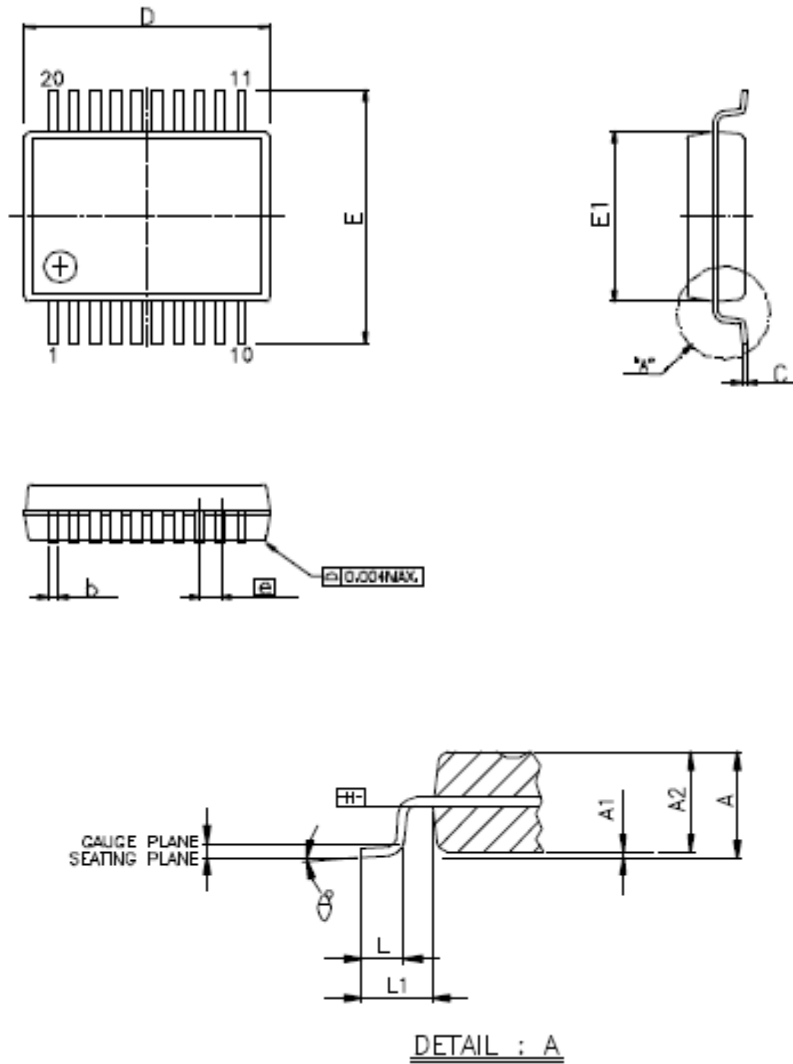
4.1. 3HALL



4.2. Sensor-less



5. Package Information: SSOP20 (150mil)



SYMBOLS	INCH		
	MIN	TYP	MAX
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.059
b	0.008	-	0.012
C	0.007	-	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BSC		
L	0.016	0.025	0.050
L1	0.041 BSC		
θ°	0	-	8