High Speed Ultrasound Beamforming Source Driver

Features

- Multiple-level ultrasound pulser
- Fast switching current source for push-pull topology
- 250MHz maximum frequency, 4.0ns input to output delay
- 15 independent programmable output level registers
- Pulse amplitude modulation (PAM) with 8-bit resolution
- 8-bit apodization DAC for peak output current via SPI
- Very low second order harmonic distortion
- Picoseconds time-jitter from input to output
- Fast SPI write and read-back of level & DAC registers
- +5.0V power supply, 2.5V CMOS logic interface
- Drives DN2625 MOSFETs output up to $230V_{P-P}$
- Programmable aperture windowing

Applications

- Medical imaging ultrasound beamforming transmitter
- Dynamic focusing B-scan CW PW Doppler & FM chirp
- Ultrasonic phase array focusing transmitter
- Piezoelectric & MEMS transducer waveform drivers
- High speed arbitrary waveform generator
- High resolution NDT phase array ultrasound pulser

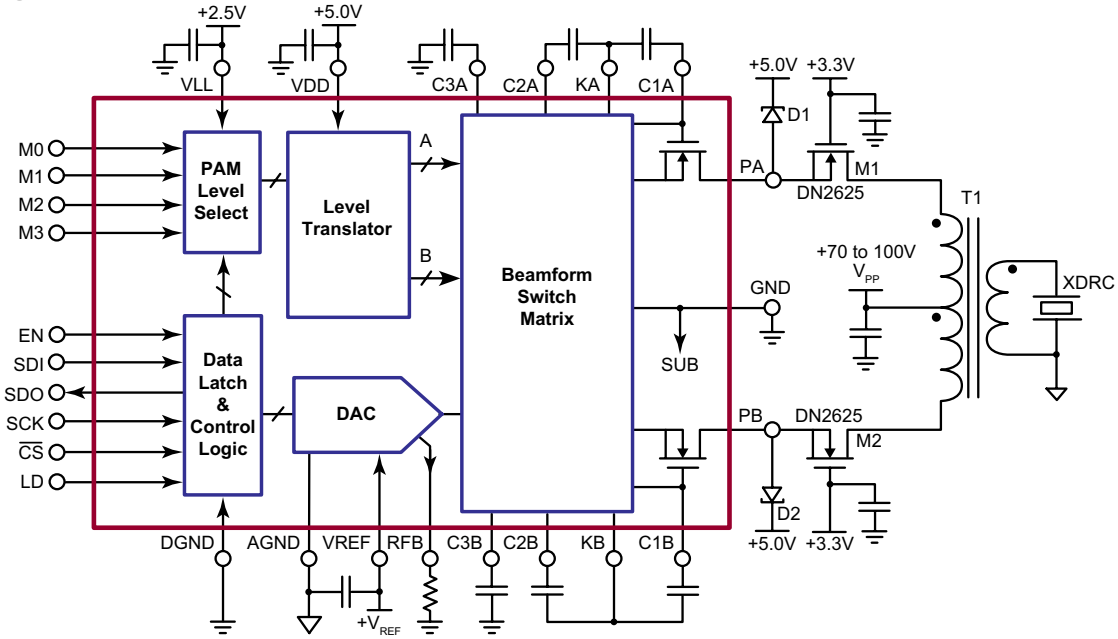
General Description

The MD2134 is a high-speed source driver for use in a pulsed current waveform generator. This programmable, fast, arbitrary current level driver is designed for medical ultrasound imaging beamforming applications. It also can be used in HIFU, NDT ultrasound and other instrument applications.

The MD2134 consists of CMOS digital logic input circuits, an eight-bit current DAC for aperture weighting amplitude control, and a programmable 15-level pulse amplitude modulation (PAM) current-source that does not include a zero level. The fast current sources are constructed with current-switch array, controlled by the LV0~LV15 level-register as the waveform data points. Four logic inputs M[3:0] are used for transmit data level selecting, as well as the transmitting timing control pins. Each level can be programmed to a resolution of +/-127 including zero (8-bit) in addition to an 8-bit SPI apodization DAC. The outputs PA and PB are controlled by M[3:0] pins directly, as well as the polarity-flip bit S1 in the SPI register. The high-speed SPI interface will achieve per-scan-line fast data updating for dynamically changing delay time, weighting and waveforms.

The MD2134 outputs are designed to drive two very low-threshold, high-voltage depletion N-MOSFETs, such as Supertex's DN2625s, as source drivers. The two DN2625 drains are connected to a center-tap RF pulse transformer. The transformer's secondary output connects to a cable and piezoelectric or capacitive transducer as a load with a good impedance match.

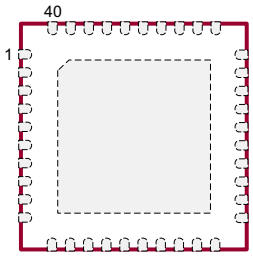
Block Diagram



Ordering Information

Part Number	Package	Packing
MD2134K7-G	40-Lead (5x5) QFN	490/ Tray

Pin Configuration



40-Lead QFN (K7)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{LL}, Logic supply	-0.5V to +3.5V
V_{DD}, Positive supply	-0.5V to +6V
V_{PA}, V_{PB} Driver outputs	-0.5V to +6V
V_{SUB}, Ground	0V
Operating temperature	0°C to +70°C
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Package Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

Package may or may not include the following marks: Si or

40-Lead QFN (K7)

Typical Thermal Resistance

Package	θ_{ja}
40-Lead QFN	26°C/W

Operating Supply Voltages

(Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, V_{REF} = 2.5V, R_{FB} = 71.1kΩ, T_A = 25°C, DAC = 0)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic supply	2.25	-	2.75	V	T_A = 0 to 70°C
V_{DD}	Power supply	4.75	5.0	5.25	V	
I_{LLQ}	V_{LL} supply current EN = 0	-	0.1	1.0	µA	Standby condition
I_{DDQ}	V_{DD} supply current EN = 0	-	0.2	1.0		
I_{LLEN}	V_{LL} supply current EN = 1	-	5.0	20	µA	f_{SCK} = 0, all logic input, no transit
I_{DDEN}	V_{DD} supply current EN = 1	-	5.0	12	mA	
I_{LL50}	V_{LL} supply current EN = 1	-	1.0	3.0	mA	f_{SCK} = 50MHz, CW, M[0:3] = 0
I_{DD50}	V_{DD} supply current EN = 1	-	40	85	mA	f_{SCK} = 0 , Input = 50MHz, CW

Output Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, V_{REF} = 2.5V, R_{FB} = 71.1kΩ, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{MAX-A/B}$	Full scale output peak current	2.88	-	3.52	A	*DAC = 255, Level = 127*
$I_{OO-A/B}$	Output current offset	-	0.5	2.0	mA	*DAC = 0*
$V_{PA/B}$	Output voltage range, +10% of $I_{PA/B}$	5.3	5.8	-	V	$I_{PA/B}$ = 1.0A
		5.0	5.5	-		$I_{PA/B}$ = 1.5A
		4.5	5.0	-		$I_{PA/B}$ = 3.0A
	Output voltage range, -10% of $I_{PA/B}$	-	1.0	1.5		$I_{PA/B}$ = 1.0A
		-	1.2	1.7		$I_{PA/B}$ = 1.5A
		-	1.8	2.3		$I_{PA/B}$ = 3.0A

Aperture DAC Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, R_{FB} = 71.1kΩ, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
Reso	Resolution	-	8	8	Bits	---
E_{LINEAR}	Linearity error	-	1.0	3.0	%	±% of FSR
E_{DIFF}	Differential nonlinearity error	-	0.6	1.0	%	±% of FSR
MON	Monotonicity	-	8	8	Bits	---
V_{REF}	External reference voltage	1.25	-	2.5	V	---

Clock and Data Input/Output Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, R_{FB} = 71.1kΩ, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	$0.8V_{LL}$	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	$0.2V_{LL}$	V	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---
C_{IN}	Input capacitance	-	2.0	-	pF	---
I_{OH}	Output logic high current	-	-	-5.0	mA	---
I_{OL}	Output logic low current	-	-	5.0	mA	---
V_{OH}	Output logic high voltage	1.95	-	-	V	I_{OH} = -5.0mA
V_{OL}	Output logic low voltage	-	-	0.35	V	I_{OL} = 5.0mA

AC Electrical Characteristics

(Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, R_{FB} = 71.1kΩ, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{ST}	DAC to output setup time	-	-	10	µs	All caps 10nF, DAC = 0 to 255, settle to 1LSB,
t_r	Output current rise time	-	2.0	3.0	ns	With 1.0Ω resistor load to V_{DD}, DAC = 85, V_{REF} = 2.5V, LV=127
t_f	Output current fall time	-	2.0	3.0		
t_{dr}	Input to output delay on rise	-	4.0	5.0		
t_{df}	Input to output delay on fall	-	4.0	5.0		
t_M	Delay time matching	-	±2.0	±3.0	ns	From PA to PB and device to device
t_J	Output jitter	-	50	-	ps	---
t_1	SDI valid to SCK setup time	0	2.0	-	ns	See serial interface timing diagram
t_2	SDI valid to SCK hold time	4.0	-	-		
t_3	SCK high time % of $1/f_{CLK}$	45	-	55	%	See serial interface timing diagram
t_4	SCK low time % of $1/f_{CLK}$	45	-	55		
t_5	CS pulse width	4.0	-	-	ns	See serial interface timing diagram
t_6	LSB SCK high to CS high	7.0	-	-		
t_7	CS low to SCK high	7.0	-	-		
t_8	SDO propagation delay from SCK failing edge	-	-	10		
t_9	CS high to SCK rising edge	7.0	-	-		
t_{10}	CS high to LD rising edge	10	-	-		

AC Electrical Characteristics

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{SCK}	Serial clock maximum frequency	40	50	-	MHz	---
t_{CSR}	Clock input slew rate	1.0	-	-	V/ns	---
t_{DSR}	Control / data input slew rate	1.0	-	-	V/ns	---
THD	Total harmonic distortion	-	-45	-40	dB	---
t_{EN-Off}	EN fall to PA/PB turn-off time	-	5.0	8.0	ns	50% to 90%
t_{EN-On}	EN rise to PA/PB turn-on time	-	13.5	20.0	µs	50% to 10%

DAC Input and Output Description

MSB	DAC Value Register						LSB	PA or PB Output Current
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	$(0/255)I_{MAX-A/B} + I_{OO-A/B}$
0	0	0	0	0	0	0	1	$(1/255)I_{MAX-A/B} + I_{OO-A/B}$
0	1	1	1	1	1	1	1	$(127/255)I_{MAX-A/B} + I_{OO-A/B}$
1	0	0	0	0	0	0	0	$(128/255)I_{MAX-A/B} + I_{OO-A/B}$
1	1	1	1	1	1	1	0	$(254/255)I_{MAX-A/B} + I_{OO-A/B}$
1	1	1	1	1	1	1	1	$(255/255)I_{MAX-A/B} + I_{OO-A/B}$

Output Current Level Control Data Register LAx or LBx

MSB	Current Level Data Register LAx or LBx					LSB	Ratio of full scale	Output Polarity Control
D6	D5	D4	D3	D2	D1	D0		
1	1	1	1	1	1	1	127/127	M3 = 0 output to PA M3 = 1 output to PB
1	1	1	1	1	1	0	126/127	
...							...	
0	0	0	0	0	0	1	1/127	
0	0	0	0	0	0	0	0	

Fast Output Current Level Control Pin Description

Input Control Pin Name				PAM Current Level	Description
M3	M2	M1	M0		
0	0	0	0	LV0	PA & PB Both Off, Zero Current
0	0	0	1	LV1	Select LV1 Current Magnitude to PA
0	0	1	0	LV2	Select LV2 Current Magnitude to PA
0	0	1	1	LV3	Select LV3 Current Magnitude to PA
0	1	0	0	LV4	Select LV4 Current Magnitude to PA
0	1	0	1	LV5	Select LV5 Current Magnitude to PA
0	1	1	0	LV6	Select LV6 Current Magnitude to PA
0	1	1	1	LV7	Select LV7 Current Magnitude to PA
1	0	0	0	LV8	Select LV8 Current Magnitude to PB
1	0	0	1	LV9	Select LV9 Current Magnitude to PB
1	0	1	0	LV10	Select LV10 Current Magnitude to PB
1	0	1	1	LV11	Select LV11 Current Magnitude to PB
1	1	0	0	LV12	Select LV12 Current Magnitude to PB
1	1	0	1	LV13	Select LV13 Current Magnitude to PB
1	1	1	0	LV14	Select LV14 Current Magnitude to PB
1	1	1	1	LV15	Select LV15 Current Magnitude to PB

Note:

Turning on PA & PB simultaneously can cause over-current and permanent damage to the IC, high voltage MOSFETs, or to the transformer.

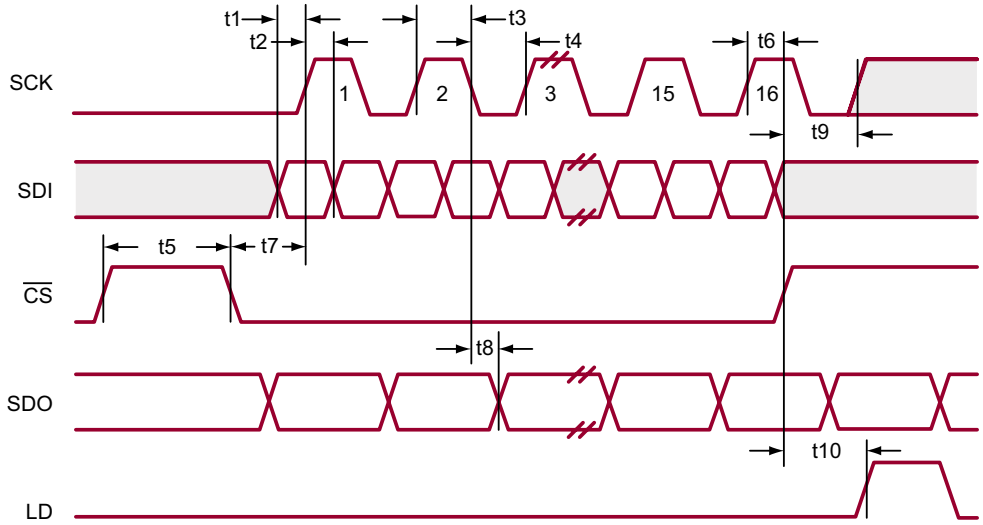
SPI Control Registers Description

Data	C1	C0	RA3	RA2	RA1	RA0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Write Data	0	0	0	0	0	0	x	S1	DAC[7:0] Data Write							
	0	0	0	0	0	1	x	x	x	LV1[6:0] PAM current Level Data Write						
	0	0	0	0	1	0	x	x	x	LV2[6:0] PAM current Level Data Write						
	0	0	0	0	1	1	x	x	x	LV3[6:0] PAM current Level Data Write						
	0	0	0	1	0	0	x	x	x	LV4[6:0] PAM current Level Data Write						
	0	0	0	1	0	1	x	x	x	LV5[6:0] PAM current Level Data Write						
	0	0	0	1	1	0	x	x	x	LV6[6:0] PAM current Level Data Write						
	0	0	0	1	1	1	x	x	x	LV7[6:0] PAM current Level Data Write						
	0	0	1	0	0	0	x	x	x	LV8[6:0] PAM current Level Data Write						
	0	0	1	0	0	1	x	x	x	LV9[6:0] PAM current Level Data Write						
	0	0	1	0	1	0	x	x	x	LV10[6:0] PAM current Level Data Write						
	0	0	1	0	1	1	x	x	x	LV11[6:0] PAM current Level Data Write						
	0	0	1	1	0	0	x	x	x	LV12[6:0] PAM current Level Data Write						
	0	0	1	1	0	1	x	x	x	LV13[6:0] PAM current Level Data Write						
	0	0	1	1	1	0	x	x	x	LV14[6:0] PAM current Level Data Write						
	0	0	1	1	1	1	x	x	x	LV15[6:0] PAM current Level Data Write						
Read Back Data	0	1	0	0	0	0	x	S1	DAC[7:0] Data Read							
	0	1	0	0	0	1	x	x	x	LV1[6:0] PAM current Level Data Read						
	0	1	0	0	1	0	x	x	x	LV2[6:0] PAM current Level Data Read						
	0	1	0	0	1	1	x	x	x	LV3[6:0] PAM current Level Data Read						
	0	1	0	1	0	0	x	x	x	LV4[6:0] PAM current Level Data Read						
	0	1	0	1	0	1	x	x	x	LV5[6:0] PAM current Level Data Read						
	0	1	0	1	1	0	x	x	x	LV6[6:0] PAM current Level Data Read						
	0	1	0	1	1	1	x	x	x	LV7[6:0] PAM current Level Data Read						
	0	1	1	0	0	0	x	x	x	LV8[6:0] PAM current Level Data Read						
	0	1	1	0	0	1	x	x	x	LV9[6:0] PAM current Level Data Read						
	0	1	1	0	1	0	x	x	x	LV10[6:0] PAM current Level Data Read						
	0	1	1	0	1	1	x	x	x	LV11[6:0] PAM current Level Data Read						
	0	1	1	1	0	0	x	x	x	LV12[6:0] PAM current Level Data Read						
	0	1	1	1	0	1	x	x	x	LV13[6:0] PAM current Level Data Read						
	0	1	1	1	1	0	x	x	x	LV14[6:0] PAM current Level Data Read						
	0	1	1	1	1	1	x	x	x	LV15[6:0] PAM current Level Data Read						
PWDN	1	0	X	X	X	X	D[9:0] = X Power Down State									
N.A.	1	1	X	X	X	X	(Reserved, Do Not Use)									

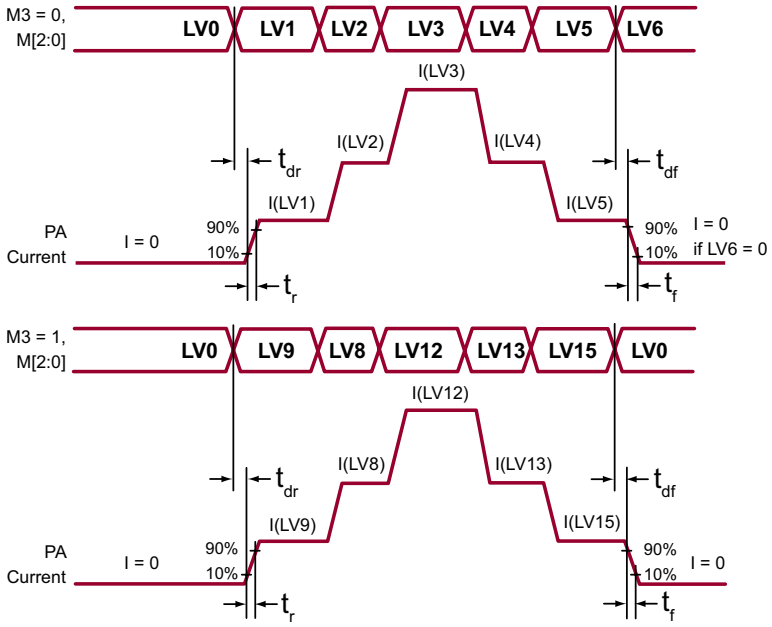
Note:

S1 is Tx polarity swapping control bit. When S1 = 0 LV1~7 output to PA and LV8~15 output to PB, when S1 = 1 LV1~7 output to PB and LV8~15 output to PA.

Serial Port Interface (SPI) Read Write Timing for Control Register



Tx Output Timing Diagram



PA and PB Output Current Equations

The in-phase PA and 180^{O} PB output sinking current magnitudes I_A and I_B can be calculated by the following equations.

$$I_A = \frac{48 \bullet V_{REF} \bullet DAC \bullet (2^6 - 1) \bullet \frac{LAx}{127}}{9 \bullet R_{FB}}$$

$$I_B = \frac{48 \bullet V_{REF} \bullet DAC \bullet (2^6 - 1) \bullet \frac{LBx}{127}}{9 \bullet R_{FB}}$$

Where the V_{REF} is the voltage reference, DAC is the decimal value of the data in the DAC register, R_{FB} is the setting resistor value in ohms, LAx or LBx is the decimal value of the data in the level register.

The values of the results from the equations represent the magnitude of the output current. The current flow into the port PA or PB is controlled by M0, M1, M2 or M3 are turned on. Note that the maximum full scale peak current at PA or PB port only can be obtained at DAC = 255, V_{REF} = 2.5V, R_{FB} = 71.1kΩ, LAx[6:0] = 127 for PA or LBx[6:0] = 127 for PB.

Pin Description

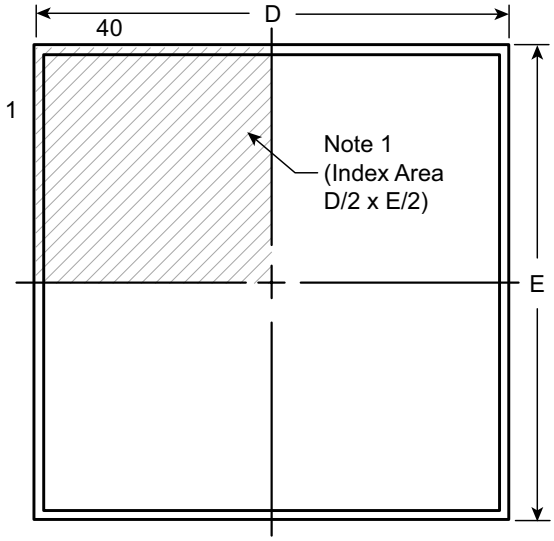
Pin	Name	Description
1	KA	Kelvin connection A
2	GND	High current output ground
3	C1A	Bypass cap to KA, 10nF low ESR X7R ceramic cap.
4	GND	High current output ground
5	VDD	Supplies voltage of the gate driver and internal analog circuit.
6	C3A	Bypass cap to GND of Pin #7, 10nF low ESR X7R ceramic cap.
7	GND	High current output ground
8	VLL	Supply voltage of logic circuit.
9	DGND	Digital logic ground.
10	SCK	Serial clock input.
11	SDI	Serial data input.
12	M3	Control logic for selecting output current level. See “Fast Output Current Level Control Pin Description”
13	M2	Control logic for selecting output current level. See “Fast Output Current Level Control Pin Description”
14	M1	Control logic for selecting output current level. See “Fast Output Current Level Control Pin Description”
15	M0	Control logic for selecting output current level. See “Fast Output Current Level Control Pin Description”
16	VDD	Supplies voltage of the gate driver and internal analog circuit.
17	AGND	Analog reference ground.
18	SDO	Serial data output.
19	CS	Serial chip select, active low, and buffer register loading clock on rising edge.
20	LD	DAC data register loading clock on rising edge.
21	EN	Enable, EN = Low, PA = PB = Hi-Z and all internal registers freeze until next clock rising edge.
22	VREF	External reference voltage input.
23	RFB	Resistor to GND, 71.1kΩ 0.1% for the best accuracy.
24	GND	High current output ground.
25	C3B	Bypass cap to GND of Pin #24, 10nF low ESR X7R ceramic cap.
26	VDD	Supplies voltage of the gate driver and internal analog circuit.
27	GND	High current output ground.
28	C1B	Bypass cap to KB, 10nF low ESR X7R ceramic cap.
29	GND	High current output ground.
30	KB	Kelvin connection B.
31	C2B	Bypass cap to KB, 10nF low ESR X7R ceramic cap.
32	PB	Current sinking source driver output B, external Schottky diode to VDD.
33	PB	Current sinking source driver output B, external Schottky diode to VDD.
34	PB	Current sinking source driver output B, external Schottky diode to VDD.
35	VSUB	Substrate voltage must connect to the lowest potential of the IC, the ground.
36	VSUB	Substrate voltage must connect to the lowest potential of the IC, the ground.
37	PA	Current sinking source driver output A, external Schottky diode to VDD.
38	PA	Current sinking source driver output A, external Schottky diode to VDD.
39	PA	Current sinking source driver output A, external Schottky diode to VDD.
40	C2A	Bypass cap to KA, 10nF low ESR X7R ceramic cap.

Notes:

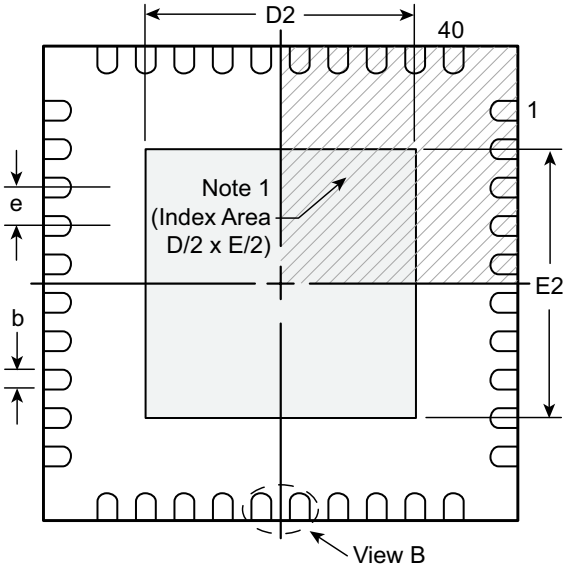
1. *Pin # 35 & #36 are V_{SUB} connected to the center thermal pad internally in the package.*
2. *All bypass capacitors need be very close to the pins*

40-Lead QFN Package Outline (K7)

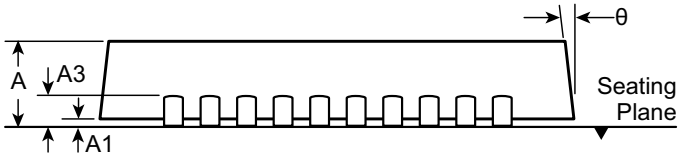
5.00x5.00mm body, 0.80mm height (max), 0.40mm pitch



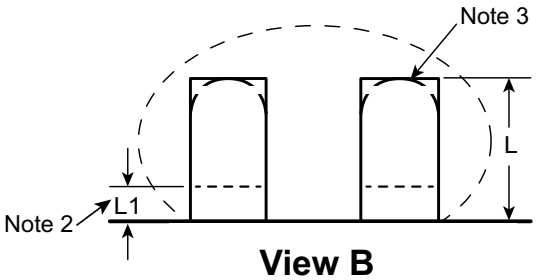
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.15	4.85*	3.45	4.85*	3.45	0.40 BSC	0.25†	0.00	0°
	NOM	0.75	0.02		0.20	5.00	3.60	5.00	3.60		0.35†	-	-
	MAX	0.80	0.05		0.25	5.15*	3.70†	5.15*	3.70†		0.45†	0.15	14°

JEDEC Registration MO-220, Variation WHHE-1, Issue K, June 2006
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-40QFNK75X5P040, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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