# MD1821

## High-Speed 4-Channel MOSFET Driver with Inverting Outputs

### Features

- Inverting MOSFET Driver
- 6 ns Rise and Fall Time
- 2A Peak Output Source and Sink Currents
- 1.8V to 5V Input CMOS Compatible
- 5V to 10V Total Supply Voltage
- Smart Logic Threshold
- Low-jitter Design
- Four Matched Channels
- Drives Two P-channel and Two N-channel MOSFETs
- Outputs can Swing below Ground
- Low-inductance Quad Flat No-lead Package
- High-performance, Thermally Enhanced Package

### Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-destructive Testing (NDT)
- PIN Diode Driver
- CCD Clock Driver/buffer
- High-speed Level Translator

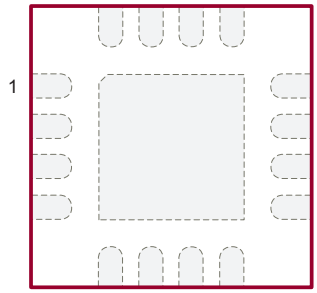
### General Description

The MD1821 is a high-speed, 4-channel MOSFET driver designed to drive high-voltage P-channel and N-channel MOSFETs for medical ultrasound applications and other applications requiring a high output current for a capacitive load. The high-speed input stage of the MD1821 can operate from a 1.8V to 5V logic interface with an optimum operating input signal range of 1.8V to 3.3V. An adaptive threshold circuit is used to set the level translator switch threshold to the average of the input logic `0` and logic `1` levels. The input logic levels may be ground referenced even though the driver is putting out bipolar signals. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

The output stage of the MD1821 has separate power connections, enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5 and –5V and the output L and H levels may be varied anywhere over the range of –5 to +5V. The output stage is capable of peak currents of up to ±2A, depending on the supply voltages used and load capacitance present. The PE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Second, when PE is low, the outputs are disabled, with the A and C outputs high and the B and D outputs low. This assists in properly precharging the AC coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS transistor pair.

### Package Type

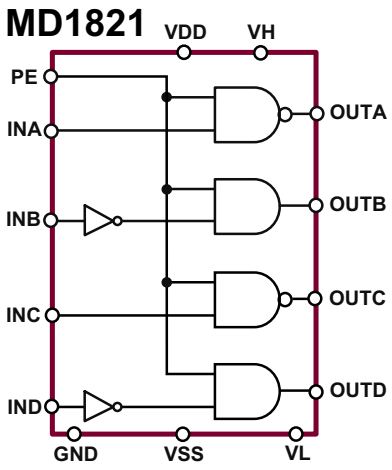
**16-lead QFN**
(Top view)



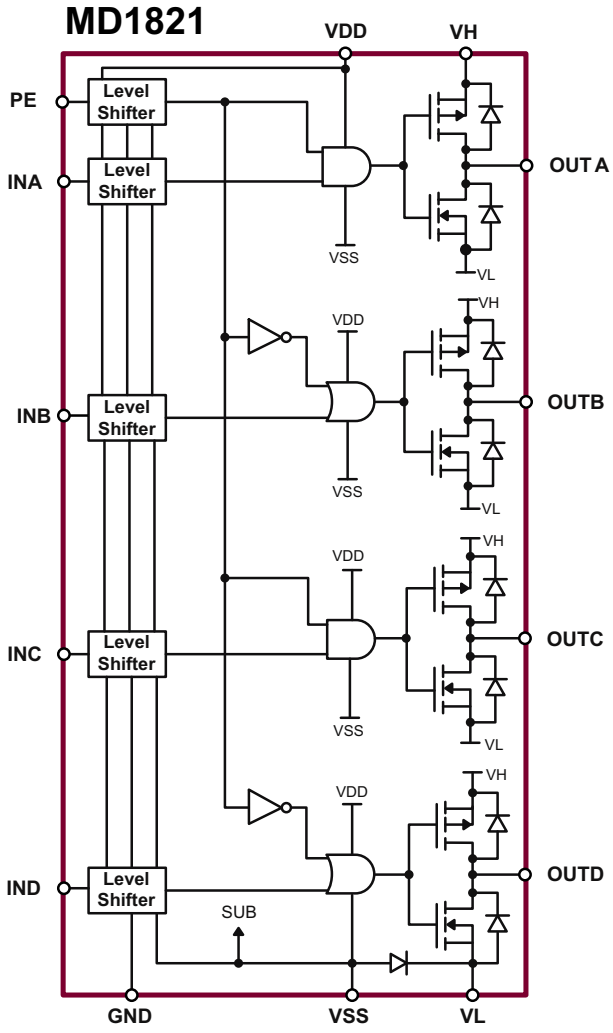

See Table 2-1 for pin information.

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## Functional Block Diagrams



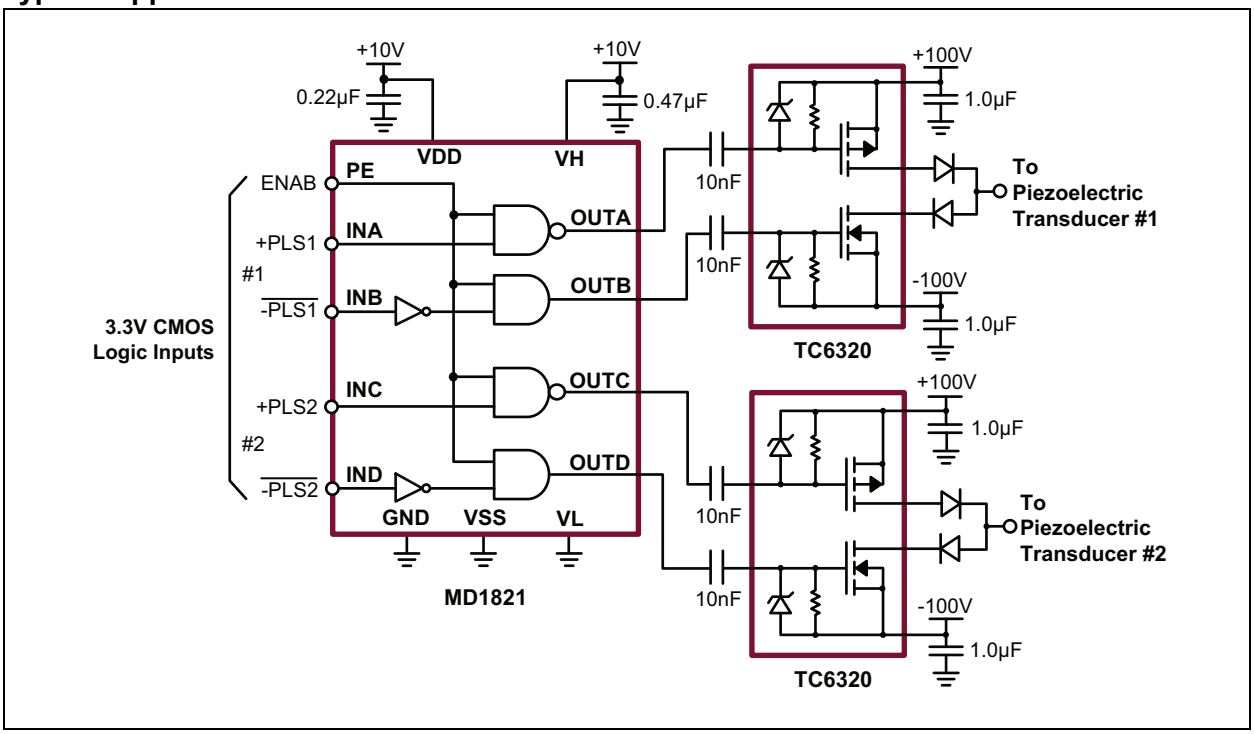

**Simplified Block Diagram**




**Detailed Block Diagram**


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## Typical Application Circuit



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Logic Supply Voltage, $V_{DD}$–$V_{SS}$ ..... –0.5V to +12.5V
Output High Supply Voltage, $V_H$ ..... $V_L$–0.5V to $V_{DD}$ +0.5V
Output Low Supply Voltage, $V_L$ ..... $V_{SS}$–0.5V to $V_H$ +0.5V
Low-side Supply Voltage, $V_{SS}$ ..... –6V to +0.5V
Logic Input Levels ..... $V_{SS}$–0.5V to GND +5.5V
Maximum Junction Temperature, $T_J$ ..... +125°C
Operating Ambient Temperature, $T_A$ ..... –20°C to +85°C
Storage Temperature, $T_S$ ..... –65°C to +150°C
Package Power Dissipation:
16-lead QFN ..... 2.2W
ESD Rating (**Note 1**) ..... ESD Sensitive

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Device is ESD sensitive. Handling precautions are recommended.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications**: $V_H$ = $V_{DD}$ = 10V, $V_L$ = $V_{SS}$ = GND = 0V, $V_{PE}$ = 3.3V, $T_A$ = 25°C

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{DD}$–$V_{SS}$ | 4.75 | — | 11.5 | V | 4V ≤ $V_{DD}$ ≤ 11.5V |
| Low-side Supply Voltage | $V_{SS}$ | –5.5 | — | 0 | V | |
| Output High Supply Voltage | $V_H$ | $V_{SS}$+2 | — | $V_{DD}$ | V | |
| Output Low Supply Voltage | $V_L$ | $V_{SS}$ | — | $V_{DD}$–4 | V | |
| $V_{DD}$ Quiescent Current | $I_{DDQ}$ | — | 60 | | µA | No input transitions, PE = 0 |
| $V_H$ Quiescent Current | $I_{HQ}$ | — | 2 | — | µA | |
| $V_{DD}$ Quiescent Current | $I_{DDQ}$ | — | 1.3 | — | mA | No input transitions, PE = 1 |
| $V_H$ Quiescent Current | $I_{HQ}$ | — | 2 | — | µA | |
| $V_{DD}$ Average Current | $I_{DD}$ | — | 3.5 | — | mA | One channel on at 5 MHz, no load |
| $V_H$ Average Current | $I_H$ | — | 10 | — | mA | |
| Input Logic Voltage High | $V_{IH}$ | $V_{PE}$–0.3 | — | $V_{PE}$ | V | For logic inputs INA, INB, INC and IND |
| Input Logic Voltage Low | $V_{IL}$ | 0 | — | 0.3 | V | |
| Input Logic Current High | $I_{IH}$ | — | — | 1 | µA | |
| Input Logic Current Low | $I_{IL}$ | — | — | 1 | µA | |
| PE Input logic Voltage High | $V_{IH}$ | 1.7 | 3.3 | 5.25 | V | For logic input PE |
| PE Input Logic Voltage Low | $V_{IL}$ | 0 | — | 0.3 | V | |
| PE Input Resistance | $R_{IN_PE}$ | 100 | — | — | kΩ | |
| Logic Input Capacitance | $C_{IN}$ | — | 5 | 10 | pF | |
| Output Sink Resistance | $R_{SINK}$ | — | 1.5 | — | Ω | $I_{SINK}$ = 50 mA |
| Output Source Resistance | $R_{SOURCE}$ | — | 2 | — | Ω | $I_{SOURCE}$ = 50 mA |
| Peak Output Sink Current | $I_{SINK}$ | — | 2 | — | A | |
| Peak Output Source Current | $I_{SOURCE}$ | — | 2 | — | A | |


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## AC ELECTRICAL CHARACTERISTICS

| **Electrical Specifications**: $V_H = V_{DD}$ = 10V, $V_L = V_{SS}$ = GND = 0V, $V_{PE}$ = 3.3V, $T_A$ = 25°C | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Unit** | **Conditions** |
| Input or PE Rise and Fall Time | $t_{irf}$ | — | — | 10 | ns | Logic input edge speed requirement |
| Propagation Delay when Output is from Low to High | $t_{PLH}$ | — | 6.5 | — | ns | $C_{LOAD}$ = 1000 pF (See **Timing Diagram**.), input signal rise/fall time 2 ns |
| Propagation Delay when Output is from High to Low | $t_{PHL}$ | — | 6.5 | — | ns | |
| Output Rise Time | $t_r$ | — | 7 | — | ns | |
| Output Fall Time | $t_f$ | — | 7 | — | ns | |
| Rise and Fall Time Matching | $\lvert t_r - t_f \rvert$ | — | 1 | — | ns | For each channel |
| Propagation Low to High and High to Low Matching | $\lvert t_{PLH} - t_{PHL} \rvert$ | — | 1 | — | ns | |
| Propagation Delay Matching | $\Delta t_{dm}$ | — | ±2 | — | ns | Device-to-device delay match |
| PE On Time | $t_{PE-ON}$ | — | — | 5 | µs | $V_{PE}$ = 1.7V~5.25V, $V_{DD}$ = 7.5V~11.5V, –20°C~85°C |
| PE Off-time | $t_{PE-OFF}$ | — | — | 4 | µs | |

## TEMPERATURE SPECIFICATIONS

| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Unit** | **Conditions** |
|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | |
| Maximum Junction Temperature | $T_J$ | — | — | +125 | °C | |
| Operating Ambient Temperature | $T_A$ | –20 | — | +85 | °C | |
| Storage Temperature | $T_S$ | –65 | — | +150 | °C | |
| **PACKAGE THERMAL RESISTANCE** | | | | | | |
| 16-lead QFN | $\theta_{JA}$ | — | 55 | — | °C/W | **Note 1** |

**Note 1:** 1 oz four-layer 3” x 4” PCB

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## Timing Diagram

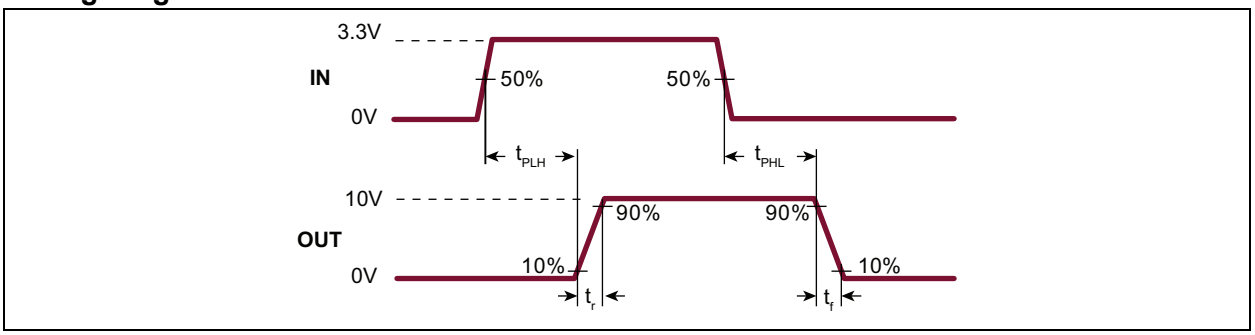



**TABLE 1-1: TRUTH FUNCTION TABLE**

| Logic Inputs | | | Outputs | |
|---|---|---|---|---|
| **PE** | **INA** | **INB** | **OUTA** | **OUTB** |
| H | L | L | $V_H$ | $V_H$ |
| H | L | H | $V_H$ | $V_L$ |
| H | H | L | $V_L$ | $V_H$ |
| H | H | H | $V_L$ | $V_L$ |
| L | X | X | $V_H$ | $V_L$ |
| **PE** | **INC** | **IND** | **OUTC** | **OUTD** |
| H | L | L | $V_H$ | $V_H$ |
| H | L | H | $V_H$ | $V_L$ |
| H | H | L | $V_L$ | $V_H$ |
| H | H | H | $V_L$ | $V_L$ |
| L | X | X | $V_H$ | $V_L$ |


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## 2.0 PIN DESCRIPTION

The details on the pins of MD1821 are listed on Table 2-1. See **Package Type** for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | INB | Logic input |
| 2 | VDD | High-side supply voltage |
| 3 | VSS | Low-side supply voltage. VSS is also connected to the IC substrate. It is required to connect to the most negative potential of voltage supplies. |
| 4 | INC | Logic input |
| 5 | IND | |
| 6 | GND | Logic input ground reference |
| 7 | VL | Supply voltage for N-channel output stage |
| 8 | OUTC | Output drivers |
| 9 | OUTD | |
| 10, 11 | VH | Supply voltage for P-channel output stage |
| 12 | OUTA | Output drivers |
| 13 | OUTB | |
| 14 | VL | Supply voltage for N-channel output stage |
| 15 | PE | Power enable logic input. When PE is high, the input logic threshold is set. When PE is low, all outputs are at default state and the IC is in Standby mode. (See Table 1-1 and Figure 3-1.) |
| 16 | INA | Logic input |
| Substrate | | The IC substrate is internally connected to the thermal pad. The thermal pad and VSS must be connected externally. |

## 3.0 APPLICATION INFORMATION

For proper operation of the MD1821, low-inductance bypass capacitors should be used in the various supply pins. The GND pin should be connected to the logic ground. The INA, INB, INC, IND and PE pins should be connected to a logic source with a swing of GND to PE, where PE is 1.8V to 5V. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1821 is capable of operating up to 100 MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents due to capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the $V_{SS}$ and $V_L$ pins should have a low-inductance bypass capacitor to GND and supply power connections. If these voltages are not zero, they need bypass capacitors similar to the positive power supplies. The power connection $V_{DD}$ should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the powerleads.

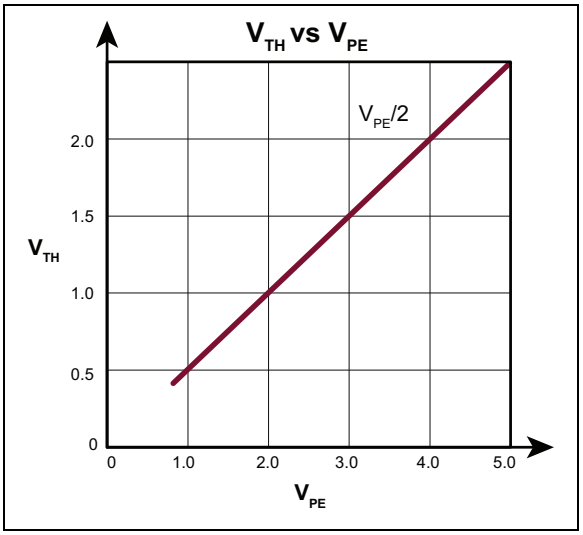



***FIGURE 3-1:*** *$V_{TH}/V_{PE}$ Curve.*

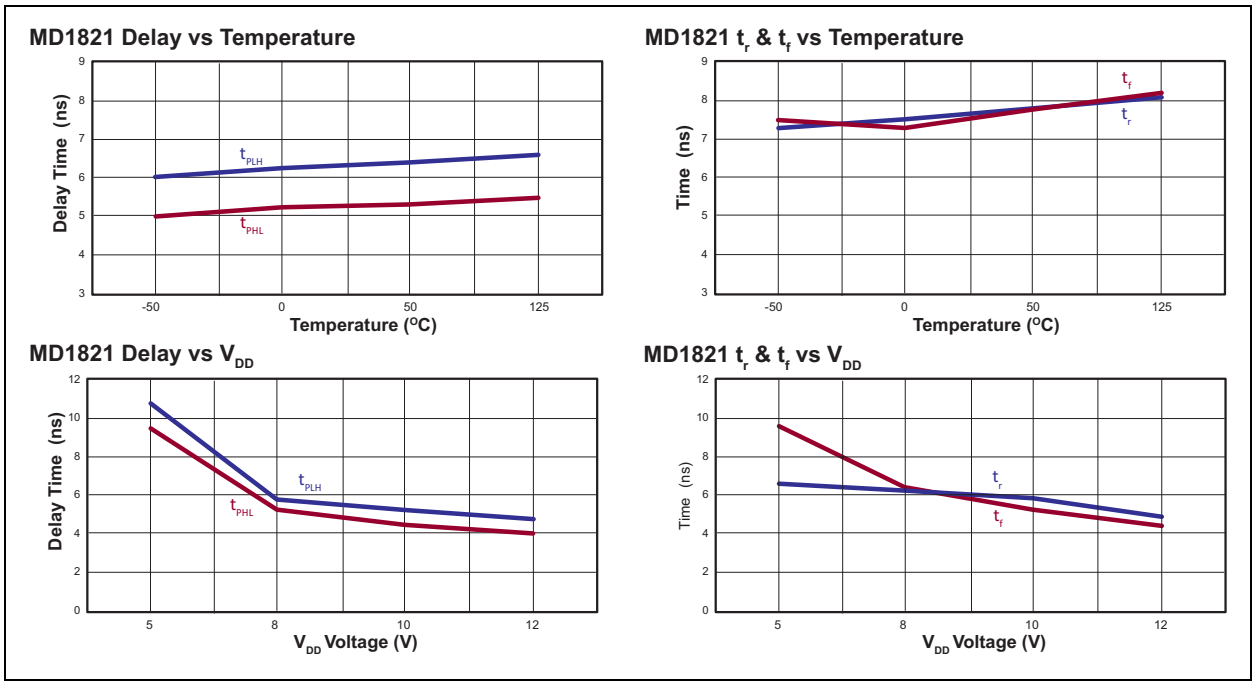



***FIGURE 3-2:*** *Timing Characteristics vs. Temperature and $V_{DD}$.*

The voltages of $V_H$ and $V_L$ decide the output signal levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1 µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead going to the capacitor. Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface-mount components are highly recommended. Since the output impedance of this driver is very low, in some cases, it may be desirable to add a small series resistor in series with the output signal to obtain better waveform transitions at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.


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Make sure that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupled voltages may cause problems. The use of a solid ground plane and good power and signal layout practices will prevent this problem. Make sure that the circulating ground return current from a capacitive load will not react with common inductance to cause noise voltages in the input logic circuitry.

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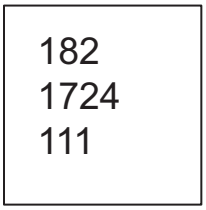
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

16-lead QFN




Example



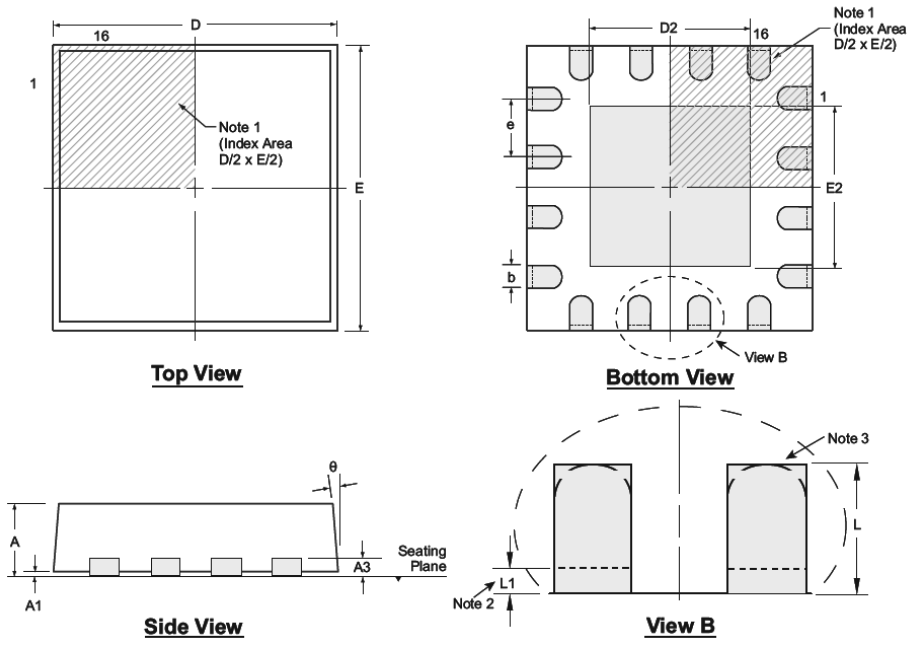

| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.


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## 16-Lead QFN Package Outline (K6)

***3.00x3.00mm body, 1.00mm height (max), 0.50mm pitch***




Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

***Notes:***

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

| Symbol | | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 2.85* | 1.50 | 2.85* | 1.50 | 0.50 BSC | 0.20† | 0.00 | 0° |
| | NOM | 0.90 | 0.02 | | 0.25 | 3.00 | 1.65 | 3.00 | 1.65 | | 0.30† | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 3.15* | 1.80 | 3.15* | 1.80 | | 0.45 | 0.15 | 14° |

*JEDEC Registration MO-220, Variation VEED-4, Issue K, June 2006.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***

**NOTES:**


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# APPENDIX A: REVISION HISTORY

## Revision A (May 2017)

- Converted Supertex Doc# DSFP-MD1821 to Microchip DS20005768A
- Changed the package marking format
- Changed the quantity of the K6 package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| Device | Package Options | | Environmental | | Media Type |

| | | | |
|---|---|---|---|
| Device: | MD1821 | = | High-Speed 4-Channel MOSFET Driver with Inverting Outputs |
| Package: | K6 | = | 16-lead QFN |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package |
| Media Type: | (blank) | = | 3300/Reel for a K6 Package |

**Example:**

a) MD1821K6-G: High-Speed 4-Channel MOSFET Driver with Inverting Outputs, 16-lead QFN, 3300/Reel


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