

1、Description

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic **TO-92** package which is readily adaptable for use in automatic insertion equipment.

2、Features

- Sensitive gate allows triggering by micro-controllers and other logic circuits
- Blocking voltage to 800 volts
- On-state RMS current to 1.0A RMS at 50°C
- Ultra low gate trigger current
- Glass-Passivated Surface for Reliability and Uniformity

3、Pinning information

PIN	Description	Simplified outline	Symbol
1	Cathode (K)	 TO-92	
2	Gate (G)		
3	Anode (A)		

4、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages	800	V
$I_{T(RMS)}$	RMS on-state current	1.0	A
I_{TSM}	Non-repetitive peak on-state current	10	A
I_{GT}	Gate trigger current	100	uA

5、Thermal characteristics

SYMBOL	PARAMETER		Value	UNIT
$R_{th(j-c)}$	junction to case(AC)	TO-92	75	°C/W

6、Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages		-	800	V
$I_{T(RMS)}$	RMS on-state current	Full Cycle Sine Wave 50 to 60 Hz (TC = 50°C)	-	1.0	A
I_{TSM}	Non-repetitive peak Surge current	One Full cycle, 60 Hz, $T_J = +110^{\circ}\text{C}$	-	10	A
I^2t	I^2t for fusing	$t = 8.3\text{ms}$	-	0.32	A^2s
V_{GM}	Peak gate voltage	Pulse Width $\leq 1.0 \mu\text{s}$, TC = 85°C	-	5	V
P_{GM}	Peak gate power	Pulse Width $\leq 1.0 \mu\text{s}$, TC = 85°C	-	0.5	W
$P_{G(AV)}$	Average gate power	Pulse Width $\leq 1.0 \mu\text{s}$, TC = 85°C	-	0.1	W
T_{stg}	Storage temperature		-40	150	$^{\circ}\text{C}$
T_J	Operating junction temperature		-40	110	$^{\circ}\text{C}$

7、Characteristics

$T_J = 25^{\circ}\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	$V_D = 12 \text{ V}$; $R_L = 33\Omega$	-	50	100	μA
I_L	Latching current	$I_G = 1.2 I_{GT}$	-	-	5	mA
I_H	Holding current	$I_T = 0.05\text{mA}$	-	-	3	mA
V_{TM}	On-state voltage	$I_{TM} = 1.1\text{A}$ $t_p = 380\mu\text{s}$	-	-	1.50	V
V_{GT}	Gate trigger voltage	$V_D = 12 \text{ V}$; $R_L = 33\Omega$	-	-	0.8	V
V_{GD}	Gate Non-Trigger Voltage	$V_D = V_{DRM}$; $T_J = 110^{\circ}\text{C}$	0.2	-	-	V
I_{DRM} I_{RRM}	$V_D = V_{DRM}$ $V_R = V_{RRM}$	$T_J = 25^{\circ}\text{C}$	-	-	5	μA
		$T_J = 110^{\circ}\text{C}$	-	-	500	μA
Dynamic Characteristics						
dV/dt	Critical rate of rise of off-state voltage	$V_D = 2/3 V_{DRM}$ Gate Open $T_J = 110^{\circ}\text{C}$	10	-	-	$\text{V}/\mu\text{s}$

8. Electrical Characteristics Curve

FIG.1 Maximum power dissipation versus RMS on-state current

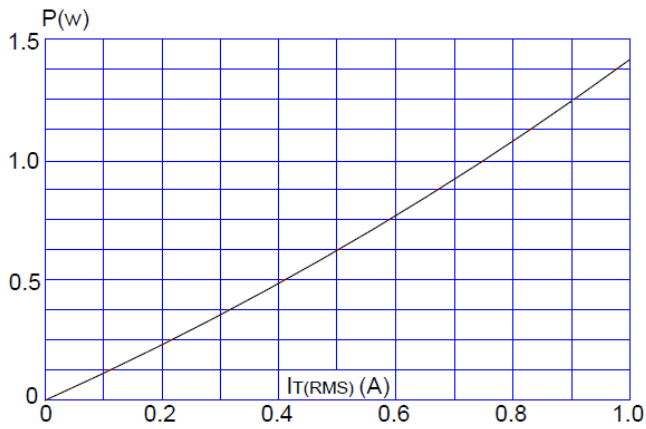


FIG.2: RMS on-state current versus case temperature

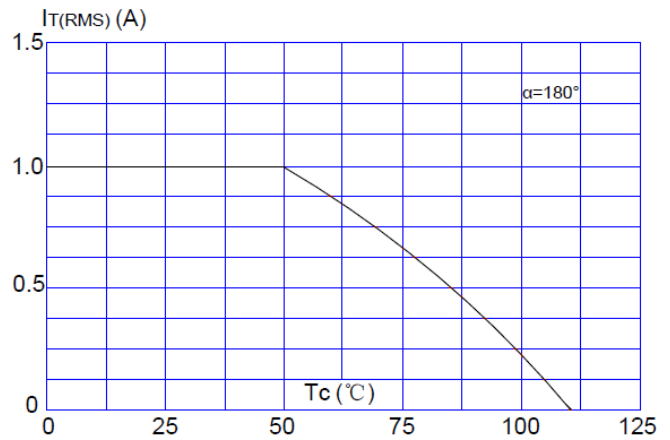


FIG.3: Surge peak on-state current versus number of cycles

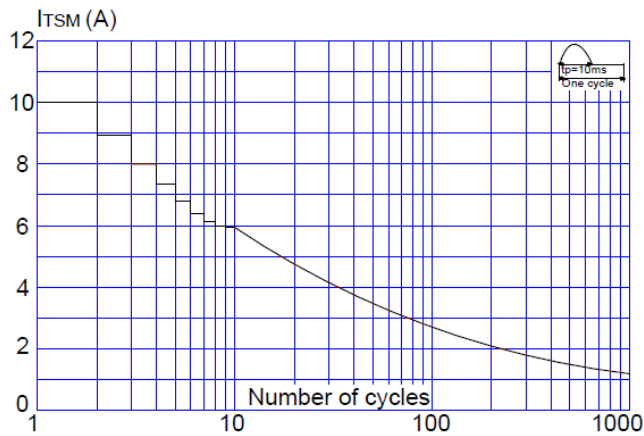


FIG.4: On-state characteristics (maximum values)

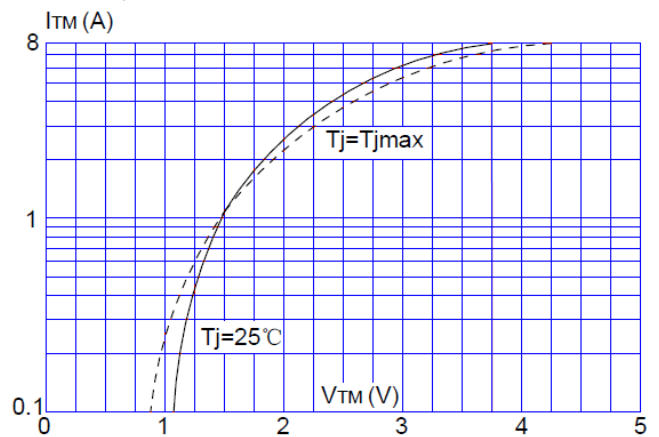


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10ms$, and corresponding value of I^2t

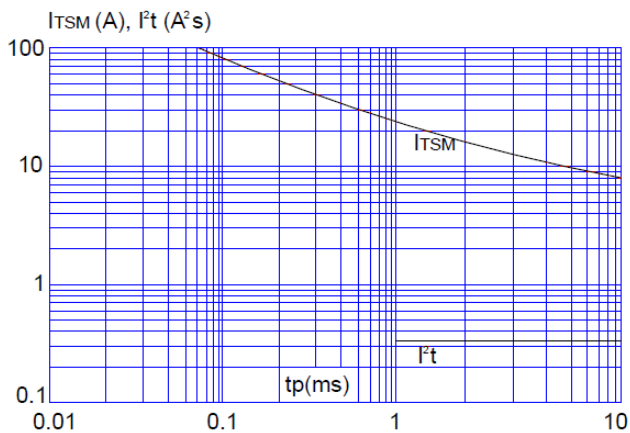
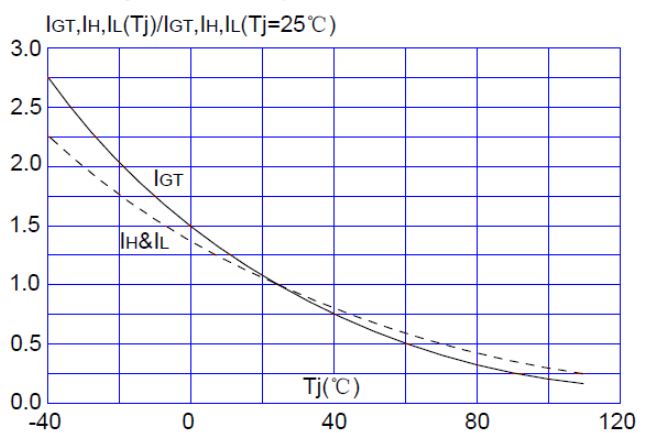
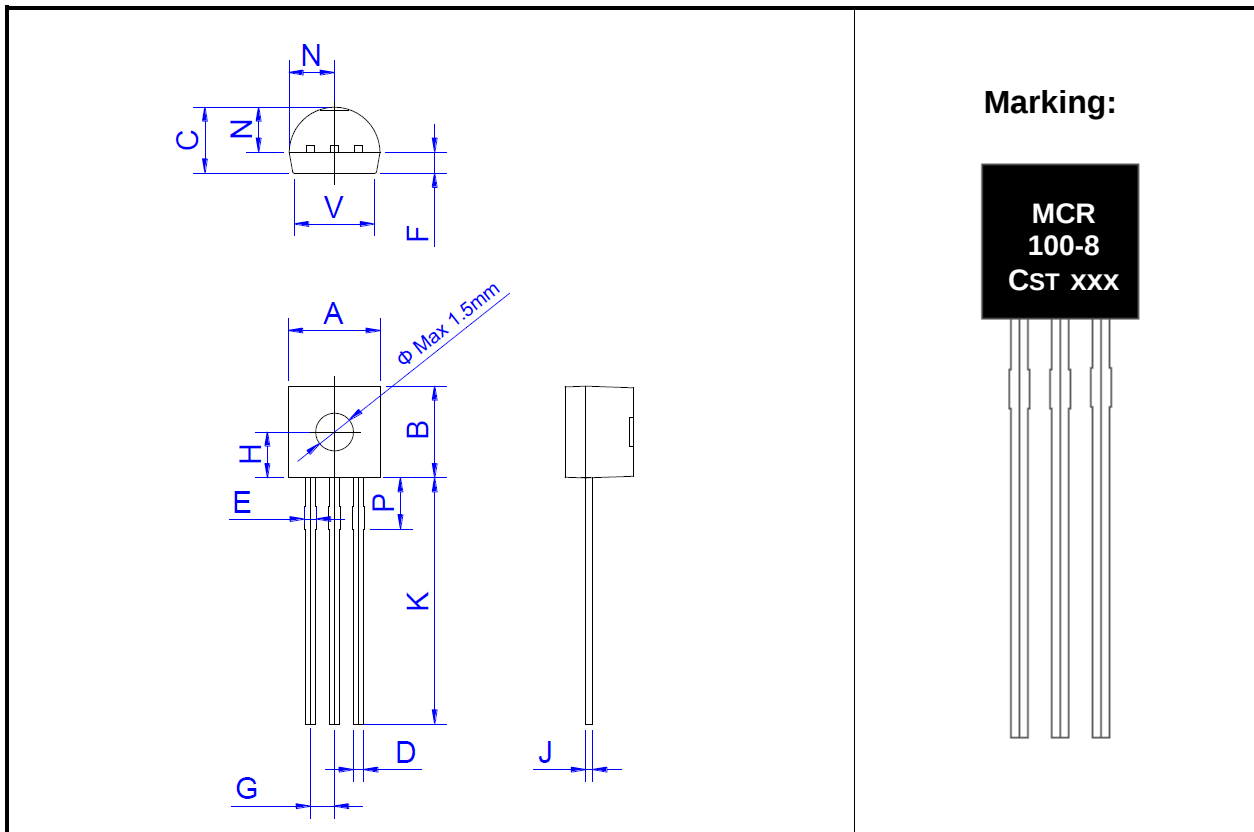


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



9、Package outline(TO-92)



DIM	Inches			Millimeters		
	Min	Type	Max	Min	Type	Max
A	0.175	-	0.205	4.45	-	5.20
B	0.170	-	0.210	4.32	-	5.33
C	0.125	-	0.165	3.18	-	4.19
D	0.016	-	0.021	0.407	-	0.533
E	0.016	-	0.028	0.40	-	0.70
F	-	0.043	-	-	1.10	-
G	-	0.050	-	-	1.27	-
H	-	0.091	-	-	2.30	-
J	0.013	-	0.018	0.32	-	0.45
K	0.500	-	0.591	12.7	-	15.0
N	0.080	-	0.105	2.04	-	2.66
P	0.073	-	0.081	1.86	-	2.06
V	-	-	0.177	-	-	4.50