# MCP6N11

## 500 kHz, 800 µA Instrumentation Amplifier

### Features

- Rail-to-Rail Input and Output
- Gain Set by 2 External Resistors
- Minimum Gain ($G_{MIN}$) Options:
  1, 2, 5, 10 or 100 V/V
- Common Mode Rejection Ratio (CMRR): 115 dB (typical, $G_{MIN}$ = 100)
- Power Supply Rejection Ratio (PSRR): 112 dB (typical, $G_{MIN}$ = 100)
- Bandwidth: 500 kHz (typical, Gain = $G_{MIN}$)
- Supply Current: 800 µA/channel (typical)
- Single Channel
- Enable/$V_{OS}$ Calibration pin: (EN/$\overline{CAL}$)
- Power Supply: 1.8V to 5.5V
- Extended Temperature Range: -40°C to +125°C

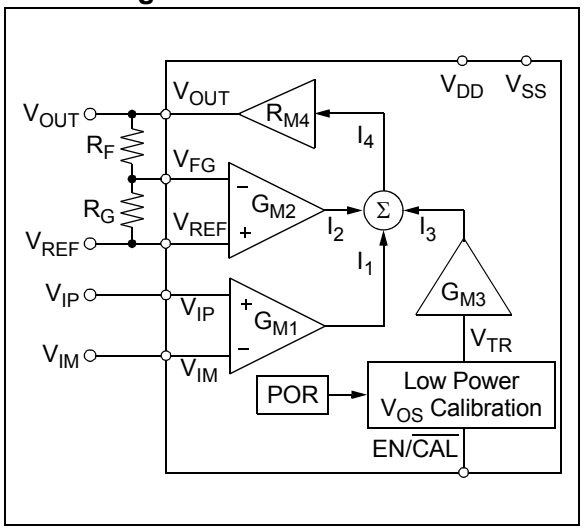
### Typical Applications

- High Side Current Sensor
- Wheatstone Bridge Sensors
- Difference Amplifier with Level Shifting
- Power Control Loops

### Design Aids

- Microchip Advanced Part Selector (MAPS)
- Demonstration Board
- Application Notes

### Block Diagram




### Description

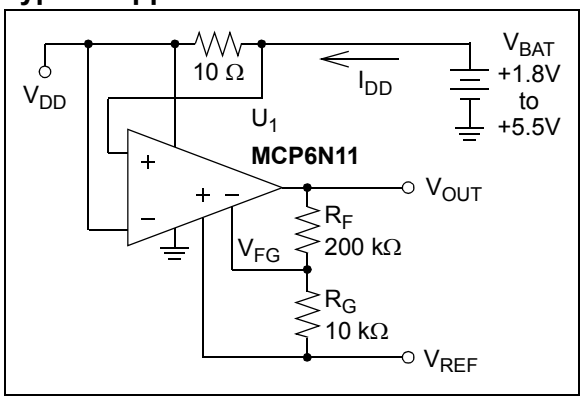
Microchip Technology Inc. offers the single MCP6N11 instrumentation amplifier (INA) with Enable/$V_{OS}$ Calibration pin (EN/$\overline{CAL}$) and several minimum gain options. It is optimized for single-supply operation with rail-to-rail input (no common mode crossover distortion) and output performance.

Two external resistors set the gain, minimizing gain error and drift-over temperature. The reference voltage ($V_{REF}$) shifts the output voltage ($V_{OUT}$).

The supply voltage range (1.8V to 5.5V) is low enough to support many portable applications. All devices are fully specified from -40°C to +125°C.

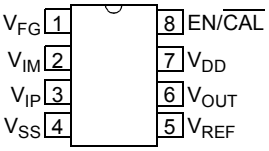
These parts have five minimum gain options (1, 2, 5, 10 and 100 V/V). This allows the user to optimize the input offset voltage and input noise for different applications.

### Typical Application Circuit

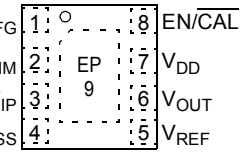



### Package Types

**MCP6N11**
SOIC




**MCP6N11**
2×3 TDFN *




* Includes Exposed Thermal Pad (EP); see Table 3-1.

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## Minimum Gain Options

Table 1 shows key specifications that differentiate between the different minimum gain ($G_{MIN}$) options. See **Section 1.0 "Electrical Characteristics"**, **Section 6.0 "Packaging Information"** and **Product Identification System** for further information on $G_{MIN}$.

**TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS**

| Part No. | $G_{MIN}$ (V/V) Nom. | $V_{OS}$ (±mV) Max. | $\Delta V_{OS}/\Delta T_A$ (±µV/°C) Typ. | CMRR (dB) Min. $V_{DD}$ = 5.5V | PSRR (dB) Min. | $V_{DMH}$ (V) Max. | GBWP (MHz) Nom. | $E_{ni}$ ($\mu V_{P-P}$) Nom. (f = 0.1 to 10 Hz) | $e_{ni}$ (nV/√Hz) Nom. (f = 10 kHz) |
|---|---|---|---|---|---|---|---|---|---|
| MCP6N11-001 | 1 | 3.0 | 90 | 70 | 62 | 2.70 | 0.50 | 570 | 950 |
| MCP6N11-002 | 2 | 2.0 | 45 | 78 | 68 | 1.35 | 1.0 | 285 | 475 |
| MCP6N11-005 | 5 | 0.85 | 18 | 80 | 75 | 0.54 | 2.5 | 114 | 190 |
| MCP6N11-010 | 10 | 0.50 | 9.0 | 81 | 81 | 0.27 | 5.0 | 57 | 95 |
| MCP6N11-100 | 100 | 0.35 | 2.7 | 88 | 86 | 0.027 | 35 | 18 | 35 |


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# 1.0 ELECTRICAL CHARACTERISTICS

## 1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....6.5V
Current at Input Pins †† .....±2 mA
Analog Inputs ($V_{IP}$ and $V_{IM}$) †† ..... $V_{SS}$ – 1.0V to $V_{DD}$ + 1.0V
All Other Inputs and Outputs ..... $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V
Difference Input Voltage..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, CDM, MM).≥ 2 kV, 1.5 kV, 300V

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.1.2 "Input Voltage Limits"** and **Section 4.2.1.3 "Input Current Limits"**.

## 1.2 Specifications

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$ and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

| Parameters | Sym | Min | Typ | Max | Units | $G_{MIN}$ | Conditions |
|---|---|---|---|---|---|---|---|
| **Input Offset** | | | | | | | |
| Input Offset Voltage, Calibrated | $V_{OS}$ | -3.0 | — | +3.0 | mV | 1 | **(Note 2)** |
| | | -2.0 | — | +2.0 | mV | 2 | |
| | | -0.85 | — | +0.85 | mV | 5 | |
| | | -0.50 | — | +0.50 | mV | 10 | |
| | | -0.35 | — | +0.35 | mV | 100 | |
| Input Offset Voltage Trim Step | $V_{OSTRM}$ | — | 0.36 | — | mV | 1 | |
| | | — | 0.21 | — | mV | 2 | |
| | | — | 0.077 | — | mV | 5 | |
| | | — | 0.045 | — | mV | 10 | |
| | | — | 0.014 | — | mV | 100 | |
| Input Offset Voltage Drift | $\Delta V_{OS}/\Delta T_A$ | — | $\pm 90/G_{MIN}$ | — | µV/°C | 1 to 10 | $T_A$= -40°C to +125°C **(Note 3)** |
| | | — | ±2.7 | — | µV/°C | 100 | |
| Power Supply Rejection Ratio | PSRR | 62 | 82 | — | dB | 1 | |
| | | 68 | 88 | — | dB | 2 | |
| | | 75 | 96 | — | dB | 5 | |
| | | 81 | 102 | — | dB | 10 | |
| | | 86 | 112 | — | dB | 100 | |

**Note 1:** $V_{CM} = (V_{IP} + V_{IM}) / 2$, $V_{DM} = (V_{IP} - V_{IM})$ and $G_{DM} = 1 + R_F/R_G$.
**2:** The $V_{OS}$ spec limits include 1/f noise effects.
**3:** This is the input offset drift without $V_{OS}$ re-calibration; toggle EN/$\overline{CAL}$ to minimize this effect.
**4:** These specs apply to both the $V_{IP}$, $V_{IM}$ input pair (use $V_{CM}$) and to the $V_{REF}$, $V_{FG}$ input pair ($V_{REF}$ takes $V_{CM}$'s place).
**5:** This spec applies to the $V_{IP}$, $V_{IM}$, $V_{REF}$ and $V_{FG}$ pins individually.
**6:** Figure 2-11 and Figure 2-19 show the $V_{IVR}$ and $V_{DMR}$ variation over temperature.
**7:** See **Section 1.5 "Explanation of DC Error Specs"**.

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**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}/2$, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

| Parameters | Sym | Min | Typ | Max | Units | $G_{MIN}$ | Conditions |
|---|---|---|---|---|---|---|---|
| **Input Current and Impedance (Note 4)** | | | | | | | |
| Input Bias Current | $I_B$ | — | 10 | — | pA | all | |
| Across Temperature | | — | 80 | — | pA | | $T_A$= +85°C |
| Across Temperature | | 0 | 2 | 5 | nA | | $T_A$= +125°C |
| Input Offset Current | $I_{OS}$ | — | ±1 | — | pA | | |
| Across Temperature | | — | ±5 | — | pA | | $T_A$= +85°C |
| Across Temperature | | -1 | ±0.05 | +1 | nA | | $T_A$= +125°C |
| Common Mode Input Impedance | $Z_{CM}$ | — | $10^{13}$\|\|6 | — | Ω\|\|pF | | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$\|\|3 | — | Ω\|\|pF | | |
| **Input Common Mode Voltage ($V_{CM}$ or $V_{REF}$) (Note 4)** | | | | | | | |
| Input Voltage Range | $V_{IVL}$ | — | — | $V_{SS}$ – 0.2 | V | all | **(Note 5, Note 6)** |
| | $V_{IVH}$ | $V_{DD}$ + 0.15 | — | — | V | | |
| Common Mode Rejection Ratio | CMRR | 62 | 79 | — | dB | 1 | $V_{CM}$ = $V_{IVL}$ to $V_{IVH}$, $V_{DD}$ = 1.8V |
| | | 69 | 87 | — | dB | 2 | |
| | | 75 | 101 | — | dB | 5 | |
| | | 79 | 107 | — | dB | 10 | |
| | | 86 | 119 | — | dB | 100 | |
| | | 70 | 94 | — | dB | 1 | $V_{CM}$ = $V_{IVL}$ to $V_{IVH}$, $V_{DD}$ = 5.5V |
| | | 78 | 100 | — | dB | 2 | |
| | | 80 | 108 | — | dB | 5 | |
| | | 81 | 114 | — | dB | 10 | |
| | | 88 | 115 | — | dB | 100 | |
| Common Mode Non-Linearity | $INL_{CM}$ | -1000 | ±115 | +1000 | ppm | 1 | $V_{CM}$ = $V_{IVL}$ to $V_{IVH}$, $V_{DM}$ = 0V, $V_{DD}$ = 1.8V **(Note 7)** |
| | | -570 | ±27 | +570 | ppm | 2 | |
| | | -230 | ±11 | +230 | ppm | 5 | |
| | | -125 | ±6 | +125 | ppm | 10 | |
| | | -50 | ±2 | +50 | ppm | 100 | |
| | | -400 | ±42 | +400 | ppm | 1 | $V_{CM}$ = $V_{IVL}$ to $V_{IVH}$, $V_{DM}$ = 0V, $V_{DD}$ = 5.5V **(Note 7)** |
| | | -220 | ±10 | +220 | ppm | 2 | |
| | | -100 | ±4 | +100 | ppm | 5 | |
| | | -50 | ±2 | +50 | ppm | 10 | |
| | | -30 | ±1 | +30 | ppm | 100 | |

**Note 1:** $V_{CM}$ = ($V_{IP}$ + $V_{IM}$) / 2, $V_{DM}$ = ($V_{IP}$ – $V_{IM}$) and $G_{DM}$ = 1 + $R_F/R_G$.
**2:** The $V_{OS}$ spec limits include 1/f noise effects.
**3:** This is the input offset drift without $V_{OS}$ re-calibration; toggle EN/$\overline{CAL}$ to minimize this effect.
**4:** These specs apply to both the $V_{IP}$, $V_{IM}$ input pair (use $V_{CM}$) and to the $V_{REF}$, $V_{FG}$ input pair ($V_{REF}$ takes $V_{CM}$'s place).
**5:** This spec applies to the $V_{IP}$, $V_{IM}$, $V_{REF}$ and $V_{FG}$ pins individually.
**6:** Figure 2-11 and Figure 2-19 show the $V_{IVR}$ and $V_{DMR}$ variation over temperature.
**7:** See **Section 1.5 "Explanation of DC Error Specs"**.


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**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$ and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

| Parameters | Sym | Min | Typ | Max | Units | $G_{MIN}$ | Conditions |
|---|---|---|---|---|---|---|---|
| **Input Differential Mode Voltage ($V_{DM}$) (Note 4)** | | | | | | | |
| Differential Input Voltage Range | $V_{DML}$ | -2.7/$G_{MIN}$ | — | — | V | all | $V_{REF}$ = ($V_{DD}$ – $G_{DM}V_{DM}$)/2 **(Note 6)** |
| | $V_{DMH}$ | — | — | +2.7/$G_{MIN}$ | V | | |
| Differential Gain Error | $g_E$ | -1 | ±0.13 | +1 | % | | $V_{DM}$ = $V_{DML}$ to $V_{DMH}$, $V_{REF}$ = ($V_{DD}$ – $G_{DM}V_{DM}$)/2 |
| Differential Gain Drift | $\Delta g_E/\Delta T_A$ | — | ±0.0006 | — | %/°C | | |
| Differential Non-Linearity | $INL_{DM}$ | -500 | ±30 | +500 | ppm | 1 | **(Note 7)** |
| | | -800 | ±40 | +800 | ppm | 2, 5 | |
| | | -2000 | ±100 | +2000 | ppm | 10, 100 | |
| DC Open-Loop Gain | $A_{OL}$ | 61 | 84 | — | dB | 1 | $V_{DD}$ = 1.8V, $V_{OUT}$ = 0.2V to 1.6V |
| | | 68 | 90 | — | dB | 2 | |
| | | 76 | 98 | — | dB | 5 | |
| | | 78 | 104 | — | dB | 10 | |
| | | 86 | 116 | — | dB | 100 | |
| | | 70 | 94 | — | dB | 1 | $V_{DD}$ = 5.5V, $V_{OUT}$ = 0.2V to 5.3V |
| | | 77 | 100 | — | dB | 2 | |
| | | 84 | 108 | — | dB | 5 | |
| | | 90 | 114 | — | dB | 10 | |
| | | 97 | 125 | — | dB | 100 | |
| **Output** | | | | | | | |
| Minimum Output Voltage Swing | $V_{OL}$ | — | — | $V_{SS}$ + 15 | mV | all | $V_{DM}$ = -$V_{DD}$/(2$G_{DM}$), $V_{DD}$ = 1.8V, $V_{REF}$ = $V_{DD}$/2 – 1V |
| | | — | — | $V_{SS}$ + 25 | mV | | $V_{DM}$ = -$V_{DD}$/(2$G_{DM}$), $V_{DD}$ = 5.5V, $V_{REF}$ = $V_{DD}$/2 – 1V |
| Maximum Output Voltage Swing | $V_{OH}$ | $V_{DD}$ – 15 | — | — | mV | | $V_{DM}$ = $V_{DD}$/(2$G_{DM}$), $V_{DD}$ = 1.8V, $V_{REF}$ = $V_{DD}$/2 + 1V |
| | | $V_{DD}$ – 25 | — | — | mV | | $V_{DM}$ = $V_{DD}$/(2$G_{DM}$), $V_{DD}$ = 5.5V, $V_{REF}$ = $V_{DD}$/2 + 1V |
| Output Short Circuit Current | $I_{SC}$ | — | ±8 | — | mA | | $V_{DD}$ = 1.8V |
| | | — | ±30 | — | mA | | $V_{DD}$ = 5.5V |
| **Power Supply** | | | | | | | |
| Supply Voltage | $V_{DD}$ | 1.8 | — | 5.5 | V | all | |
| Quiescent Current per Amplifier | $I_Q$ | 0.5 | 0.8 | 1.1 | mA | | $I_O$ = 0 |
| POR Trip Voltage | $V_{PRL}$ | 1.1 | 1.4 | — | V | | |
| | $V_{PRH}$ | — | 1.4 | 1.7 | V | | |

**Note 1:** $V_{CM}$ = ($V_{IP}$ + $V_{IM}$) / 2, $V_{DM}$ = ($V_{IP}$ – $V_{IM}$) and $G_{DM}$ = 1 + $R_F/R_G$.
**2:** The $V_{OS}$ spec limits include 1/f noise effects.
**3:** This is the input offset drift without $V_{OS}$ re-calibration; toggle EN/$\overline{CAL}$ to minimize this effect.
**4:** These specs apply to both the $V_{IP}$, $V_{IM}$ input pair (use $V_{CM}$) and to the $V_{REF}$, $V_{FG}$ input pair ($V_{REF}$ takes $V_{CM}$'s place).
**5:** This spec applies to the $V_{IP}$, $V_{IM}$, $V_{REF}$ and $V_{FG}$ pins individually.
**6:** Figure 2-11 and Figure 2-19 show the $V_{IVR}$ and $V_{DMR}$ variation over temperature.
**7:** See **Section 1.5 "Explanation of DC Error Specs"**.

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**TABLE 1-2: AC ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = 25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

| Parameters | Sym | Min | Typ | Max | Units | $G_{MIN}$ | Conditions |
|---|---|---|---|---|---|---|---|
| **AC Response** | | | | | | | |
| Gain Bandwidth Product | GBWP | — | 0.50 $G_{MIN}$ | — | MHz | 1 to 10 | |
| | | — | 35 | — | MHz | 100 | |
| Phase Margin | PM | — | 70 | — | ° | all | |
| Open-Loop Output Impedance | $R_{OL}$ | — | 0.9 | — | kΩ | 1 to 10 | |
| | | — | 0.6 | — | kΩ | 100 | |
| Power Supply Rejection Ratio | PSRR | — | 94 | — | dB | all | f < 10 kHz |
| Common Mode Rejection Ratio | CMRR | — | 104 | — | dB | 1 to 10 | f < 10 kHz |
| | | — | 94 | — | dB | 100 | f < 10 kHz |
| **Step Response** | | | | | | | |
| Slew Rate | SR | — | 3 | — | V/µs | 1 to 10 | $V_{DD}$ = 1.8V |
| | | — | 9 | — | V/µs | | $V_{DD}$ = 5.5V |
| | | — | 2 | — | V/µs | 100 | $V_{DD}$ = 1.8V |
| | | — | 6 | — | V/µs | | $V_{DD}$ = 5.5V |
| Overdrive Recovery, Input Common Mode | $t_{IRC}$ | — | 10 | — | µs | all | $V_{CM}$ = $V_{SS}$ – 1V (or $V_{DD}$ + 1V) to $V_{DD}$/2, $G_{DM}V_{DM}$ = ±0.1V, 90% of $V_{OUT}$ change |
| Overdrive Recovery, Input Differential Mode | $t_{IRD}$ | — | 5 | — | µs | | $V_{DM}$ = $V_{DML}$ – (0.5V)/$G_{MIN}$ (or $V_{DMH}$ + (0.5V)/$G_{MIN}$) to 0V, $V_{REF}$ = ($V_{DD}$ – $G_{DM}V_{DM}$)/2, 90% of $V_{OUT}$ change |
| Overdrive Recovery, Output | $t_{OR}$ | — | 8 | — | µs | | $G_{DM}$ = 2$G_{MIN}$, $G_{DM}V_{DM}$ = 0.5$V_{DD}$ to 0V, $V_{REF}$ = 0.75$V_{DD}$ (or 0.25$V_{DD}$), 90% of $V_{OUT}$ change |
| **Noise** | | | | | | | |
| Input Noise Voltage | $E_{ni}$ | — | 570/$G_{MIN}$ | — | $\mu V_{P-P}$ | 1 to 10 | f = 0.1 Hz to 10 Hz |
| | | — | 18 | — | $\mu V_{P-P}$ | 100 | |
| Input Noise Voltage Density | $e_{ni}$ | — | 950/$G_{MIN}$ | — | nV/√Hz | 1 to 10 | f = 100 kHz |
| | | — | 35 | — | nV/√Hz | 100 | |
| Input Current Noise Density | $i_{ni}$ | — | 1 | — | fA/√Hz | all | f = 1 kHz |


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**TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = 25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

| Parameters | Sym | Min | Typ | Max | Units | $G_{MIN}$ | Conditions |
|---|---|---|---|---|---|---|---|
| **EN/$\overline{CAL}$ Low Specifications** | | | | | | | |
| EN/$\overline{CAL}$ Logic Threshold, Low | $V_{IL}$ | $V_{SS}$ | — | 0.2 $V_{DD}$ | V | all | |
| EN/$\overline{CAL}$ Input Current, Low | $I_{ENL}$ | — | -0.1 | — | nA | | EN/$\overline{CAL}$ = 0V |
| GND Current | $I_{SS}$ | -7 | -2.5 | — | µA | | EN/$\overline{CAL}$ = 0V, $V_{DD}$ = 5.5V |
| Amplifier Output Leakage | $I_{O(LEAK)}$ | — | 10 | — | nA | | EN/$\overline{CAL}$ = 0V |
| **EN/$\overline{CAL}$ High Specifications** | | | | | | | |
| EN/$\overline{CAL}$ Logic Threshold, High | $V_{IH}$ | 0.8 $V_{DD}$ | | $V_{DD}$ | V | all | |
| EN/$\overline{CAL}$ Input Current, High | $I_{ENH}$ | — | -0.01 | — | nA | | EN/$\overline{CAL}$ = $V_{DD}$ |
| **EN/$\overline{CAL}$ Dynamic Specifications** | | | | | | | |
| EN/$\overline{CAL}$ Input Hysteresis | $V_{HYST}$ | — | 0.2 | — | V | all | |
| EN/$\overline{CAL}$ Low to Amplifier Output High-Z Turn-off Time | $t_{OFF}$ | — | 3 | 10 | µs | | EN/$\overline{CAL}$ = 0.2$V_{DD}$ to $V_{OUT}$ = 0.1($V_{DD}$/2), $V_{DM}G_{DM}$ = 1 V, $V_L$ = 0V |
| EN/$\overline{CAL}$ High to Amplifier Output On Time | $t_{ON}$ | 12 | 20 | 28 | ms | | EN/$\overline{CAL}$ = 0.8$V_{DD}$ to $V_{OUT}$ = 0.9($V_{DD}$/2), $V_{DM}G_{DM}$ = 1 V, $V_L$ = 0V |
| EN/$\overline{CAL}$ Low to EN/$\overline{CAL}$ High low time | $t_{ENLH}$ | 100 | — | — | µs | | Minimum time before externally releasing EN/$\overline{CAL}$ (**Note 1**) |
| Amplifier On to EN/$\overline{CAL}$ Low Setup Time | $t_{ENOL}$ | — | 100 | — | µs | | |
| **POR Dynamic Specifications** | | | | | | | |
| $V_{DD}$ ↓ to Output Off | $t_{PHL}$ | — | 10 | — | µs | all | $V_L$ = 0V, $V_{DD}$ = 1.8V to $V_{PRL}$ – 0.1V step, 90% of $V_{OUT}$ change |
| $V_{DD}$ ↑ to Output On | $t_{PLH}$ | 140 | 250 | 360 | ms | | $V_L$ = 0V, $V_{DD}$ = 0V to $V_{PRH}$ + 0.1V step, 90% of $V_{OUT}$ change |

**Note 1:** For design guidance only; not tested.

**TABLE 1-4: TEMPERATURE SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **(Note 1)** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 150 | — | °C/W | |
| Thermal Resistance, 8L-TDFN (2×3) | $\theta_{JA}$ | — | 53 | — | °C/W | |

**Note 1:** Operation must not cause $T_J$ to exceed the Absolute Maximum Junction Temperature specification (+150°C).

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## 1.3 Timing Diagrams

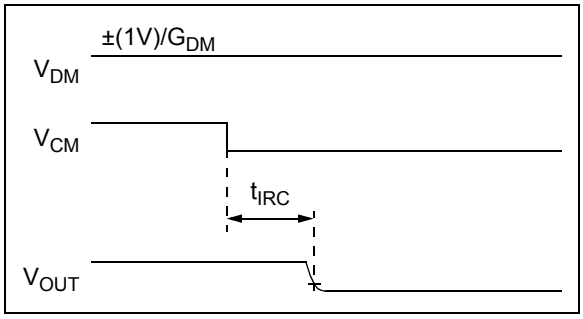



***FIGURE 1-1:*** *Common Mode Input Overdrive Recovery Timing Diagram.*

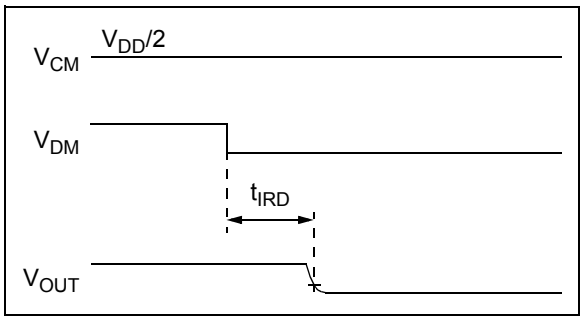



***FIGURE 1-2:*** *Differential Mode Input Overdrive Recovery Timing Diagram.*

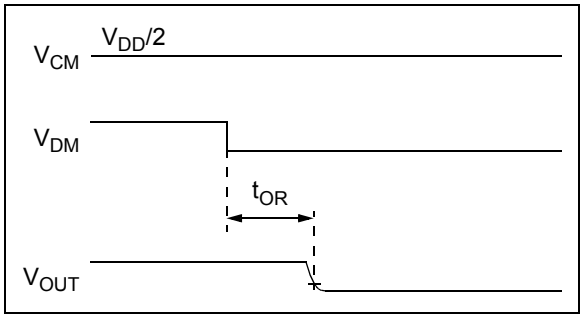



***FIGURE 1-3:*** *Output Overdrive Recovery Timing Diagram.*

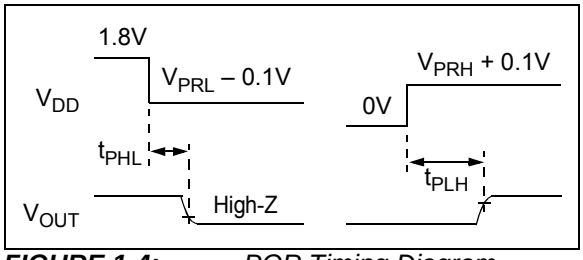



***FIGURE 1-4:*** *POR Timing Diagram.*

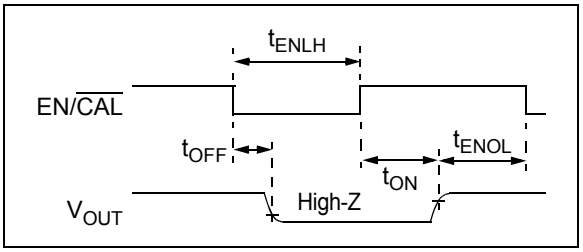



***FIGURE 1-5:*** *EN/$\overline{CAL}$ Timing Diagram.*


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## 1.4 DC Test Circuits

### 1.4.1 INPUT OFFSET TEST CIRCUIT

Figure 1-6 is used for testing the INA's input offset errors and input voltage range ($V_E$, $V_{IVL}$ and $V_{IVH}$; see **Section 1.5.1 "Input Offset Related Errors"** and **Section 1.5.2 "Input Offset Common Mode Non-linearity"**). $U_2$ is part of a control loop that forces $V_{OUT}$ to equal $V_{CNT}$; $U_1$ can be set to any bias point.

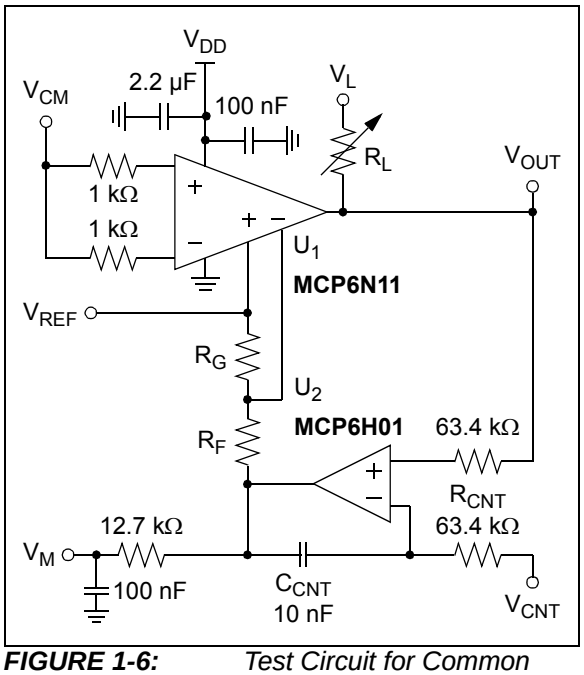



***FIGURE 1-6:*** *Test Circuit for Common Mode (Input Offset).*

When MCP6N11 is in its normal range of operation, the DC output voltages are (where $V_E$ is the sum of input offset errors and $g_E$ is the gain error):

**EQUATION 1-1:**

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{CNT} \\ V_M &= V_{REF} + G_{DM}(1 + g_E)V_E \end{aligned}$$

Table 1-5 gives the recommended $R_F$ and $R_G$ values for different $G_{MIN}$ options.

**TABLE 1-5: SELECTING $R_F$ AND $R_G$**

| $G_{MIN}$ (V/V) Nom. | $R_F$ (Ω) Nom. | $R_G$ (Ω) Nom. | $G_{DM}$ (V/V) Nom. | $G_{DM}V_{OS}$ (±V) Max. | BW (kHz) Nom. |
|---|---|---|---|---|---|
| 1 | 100k | 499 | 201.4 | 0.60 | 2.5 |
| 2 | | | | 0.40 | 5.0 |
| 5 | 100k | 100 | 1001 | 0.85 | 2.5 |
| 10 | | | | 0.50 | 5.0 |
| 100 | | | | 0.35 | 35 |

### 1.4.2 DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-7 is used for testing the INA's differential gain error, non-linearity and input voltage range ($g_E$, $INL_{DM}$, $V_{DML}$ and $V_{DMH}$; see **Section 1.5.3 "Differential Gain Error and Non-linearity"**). $R_F$ and $R_G$ are 0.01% for accurate gain error measurements.

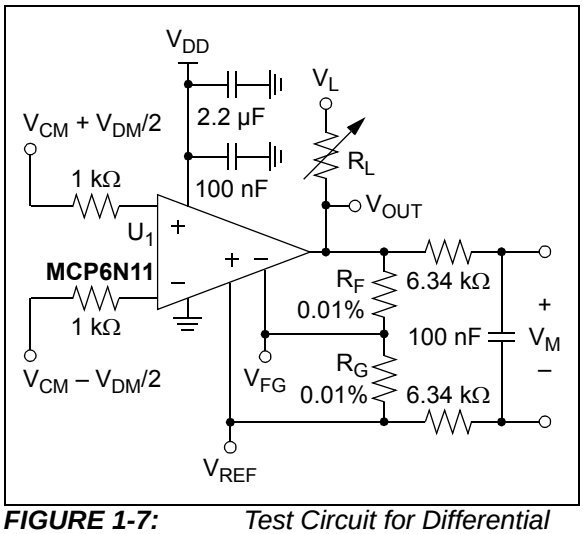



***FIGURE 1-7:*** *Test Circuit for Differential Mode.*

The output voltages are (where $V_E$ is the sum of input offset errors and $g_E$ is the gain error):

**EQUATION 1-2:**

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E) \\ V_M &= V_{OUT} - V_{REF} \\ &= G_{DM}(1 + g_E)(V_{DM} + V_E) \end{aligned}$$

To keep $V_{REF}$, $V_{FG}$ and $V_{OUT}$ within their ranges, set:

**EQUATION 1-3:**

$$V_{REF} = (V_{DD} - G_{DM}V_{DM})/2$$

Table 1-6 shows the recommended $R_F$ and $R_G$. They produce a 10 kΩ load; $V_L$ can usually be left open.

**TABLE 1-6: SELECTING $R_F$ AND $R_G$**

| $G_{MIN}$ (V/V) Nom. | $R_F$ (Ω) Nom. | $R_G$ (Ω) Nom. | $G_{DM}$ (V/V) Nom. |
|---|---|---|---|
| 1 | 0 | Open | 1.000 |
| 2 | 4.99k | 4.99k | 2.000 |
| 5 | 8.06k | 2.00k | 5.030 |
| 10 | 9.09k | 1.00k | 10.09 |
| 100 | 10.0k | 100 | 101.0 |

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## 1.5 Explanation of DC Error Specs

### 1.5.1 INPUT OFFSET RELATED ERRORS

The input offset error ($V_E$) is extracted from input offset measurements (see **Section 1.4.1 "Input Offset Test Circuit"**), based on Equation 1-1:

**EQUATION 1-4:**

$$V_E = \frac{V_M - V_{REF}}{G_{DM}(1 + g_E)}$$

$V_E$ has several terms, which assume a linear response to changes in $V_{DD}$, $V_{SS}$, $V_{CM}$, $V_{OUT}$ and $T_A$ (all of which are in their specified ranges):

**EQUATION 1-5:**

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR} + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot \frac{\Delta V_{OS}}{\Delta T_A}$$

Where:

*PSRR*, *CMRR* and $A_{OL}$ are in units of V/V

$\Delta T_A$ is in units of °C

$V_{DM}$ = 0

Equation 1-2 shows how $V_E$ affects $V_{OUT}$.

### 1.5.2 INPUT OFFSET COMMON MODE NON-LINEARITY

The input offset error ($V_E$) changes non-linearly with $V_{CM}$. Figure 1-8 shows $V_E$ vs. $V_{CM}$, as well as a linear fit line ($V_{E_LIN}$) based on $V_{OS}$ and CMRR. The op amp is in standard conditions ($\Delta V_{OUT}$ = 0, $V_{DM}$ = 0, etc.). $V_{CM}$ is swept from $V_{IVL}$ to $V_{IVH}$. The test circuit is in **Section 1.4.1 "Input Offset Test Circuit"** and $V_E$ is calculated using Equation 1-4.

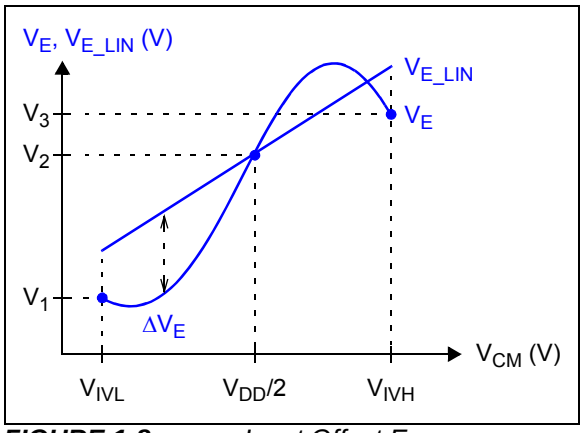



***FIGURE 1-8:*** *Input Offset Error vs. Common Mode Input Voltage.*

Based on the measured $V_E$ data, we obtain the following linear fit:

**EQUATION 1-6:**

$$V_{E_LIN} = V_{OS} + \frac{V_{CM} - V_{DD}/2}{CMRR}$$

Where:

$$V_{OS} = V_2$$

$$\frac{1}{CMRR} = \frac{V_3 - V_1}{V_{IVH} - V_{IVL}}$$

The remaining error ($\Delta V_E$) is described by the Common Mode Non-Linearity spec:

**EQUATION 1-7:**

$$INL_{CM} = \frac{max|\Delta V_E|}{V_{IVH} - V_{IVL}}$$

Where:

$$\Delta V_E = V_E - V_{E_LIN}$$

The same common mode behavior applies to $V_E$ when $V_{REF}$ is swept, instead of $V_{CM}$, since both input stages are designed the same:

**EQUATION 1-8:**

$$V_{E_LIN} = V_{OS} + \frac{V_{REF} - V_{DD}/2}{CMRR}$$

$$INL_{CM} = \frac{max|\Delta V_E|}{V_{IVH} - V_{IVL}}$$

### 1.5.3 DIFFERENTIAL GAIN ERROR AND NON-LINEARITY

The differential errors are extracted from differential gain measurements (see **Section 1.4.2 "Differential Gain Test Circuit"**), based on Equation 1-2. These errors are the differential gain error ($g_E$) and the input offset error ($V_E$, which changes non-linearly with $V_{DM}$):

**EQUATION 1-9:**

$$G_{DM} = 1 + R_F/R_G$$

$$V_M = G_{DM}(1 + g_E)(V_{DM} + V_E)$$

These errors are adjusted for the expected output, then referred back to the input, giving the differential input error ($V_{ED}$) as a function of $V_{DM}$:

**EQUATION 1-10:**

$$V_{ED} = \frac{V_M}{G_{DM}} - V_{DM}$$


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Figure 1-9 shows $V_{ED}$ vs. $V_{DM}$, as well as a linear fit line ($V_{ED_LIN}$) based on $V_E$ and $g_E$. The op amp is in standard conditions ($\Delta V_{OUT}$ = 0, etc.). $V_{DM}$ is swept from $V_{DML}$ to $V_{DMH}$.

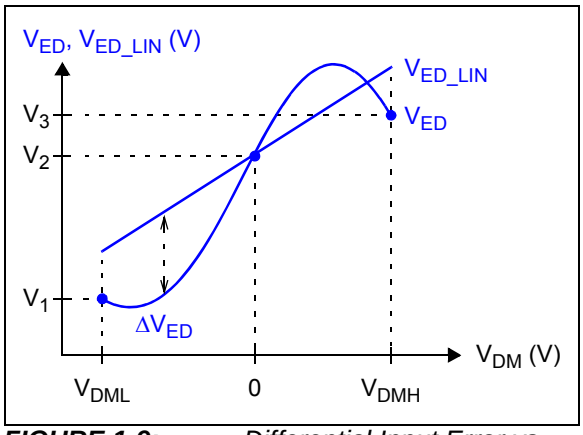



***FIGURE 1-9:*** *Differential Input Error vs. Differential Input Voltage.*

Based on the measured $V_{ED}$ data, we obtain the following linear fit:

**EQUATION 1-11:**

$$V_{ED_LIN} = (1 + g_E)V_E + g_E V_{DM}$$

Where:

$$g_E = \frac{V_3 - V_1}{V_{DMH} - V_{DML}} - 1$$

$$V_E = \frac{V_2}{1 + g_E}$$

Note that the $V_E$ value measured here is not as accurate as the one obtained in **Section 1.5.1 "Input Offset Related Errors"**.

The remaining error ($\Delta V_{ED}$) is described by the Differential Mode Non-Linearity spec:

**EQUATION 1-12:**

$$INL_{DM} = \frac{max|\Delta V_{ED}|}{V_{DMH} - V_{DML}}$$

Where:

$$\Delta V_{ED} = V_{ED} - V_{ED_LIN}$$

**NOTES:**


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## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

### 2.1 DC Voltages and Currents

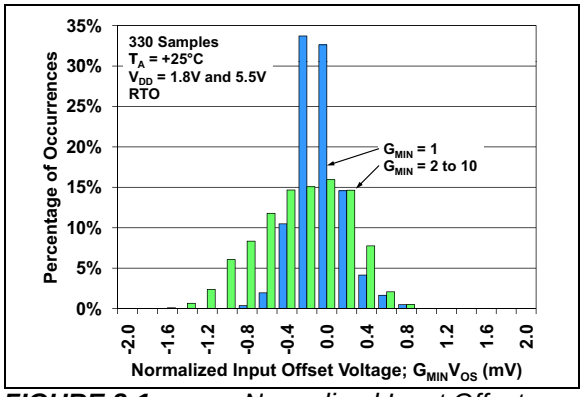



***FIGURE 2-1:*** *Normalized Input Offset Voltage, with $G_{MIN}$ = 1 to 10.*

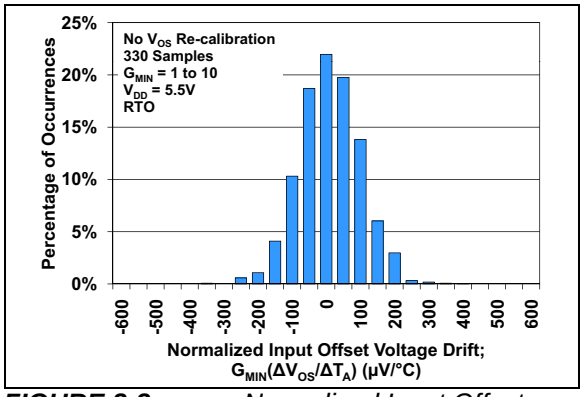



***FIGURE 2-3:*** *Normalized Input Offset Voltage Drift, with $G_{MIN}$ = 1 to 10.*

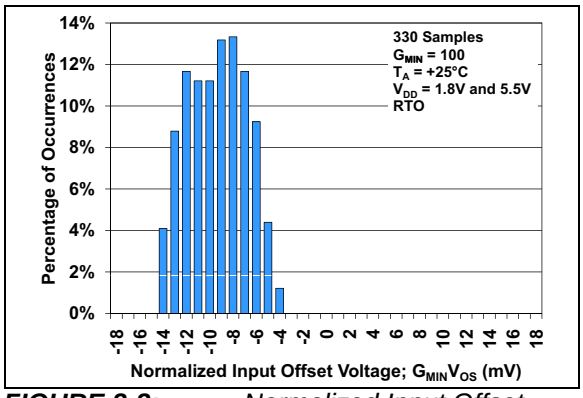



***FIGURE 2-2:*** *Normalized Input Offset Voltage, with $G_{MIN}$ = 100.*

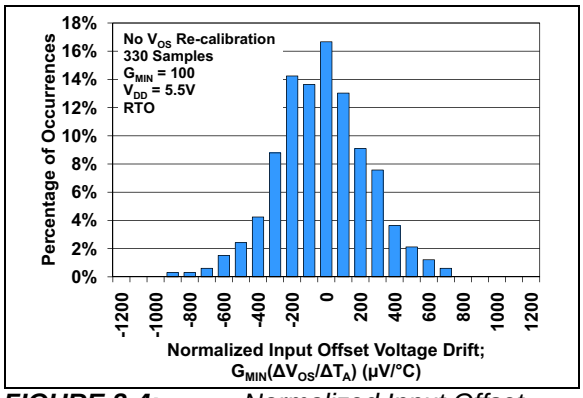



***FIGURE 2-4:*** *Normalized Input Offset Voltage Drift, with $G_{MIN}$ = 100.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}/2$, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

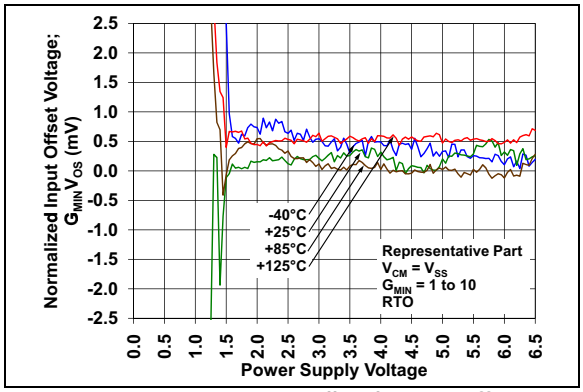



***FIGURE 2-5:*** *Normalized Input Offset Voltage vs. Power Supply Voltage, with $V_{CM}$ = 0V and $G_{MIN}$ = 1 to 10.*

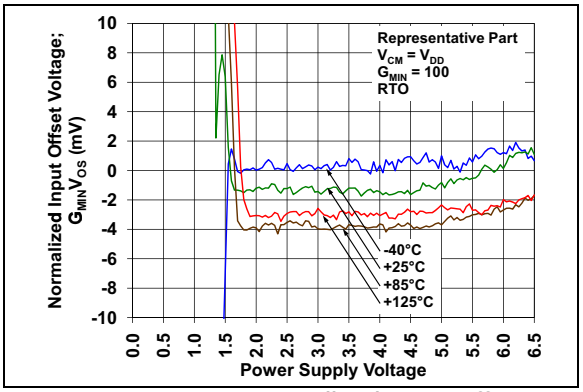



***FIGURE 2-8:*** *Normalized Input Offset Voltage vs. Power Supply Voltage, with $V_{CM}$ = $V_{DD}$ and $G_{MIN}$ = 100.*

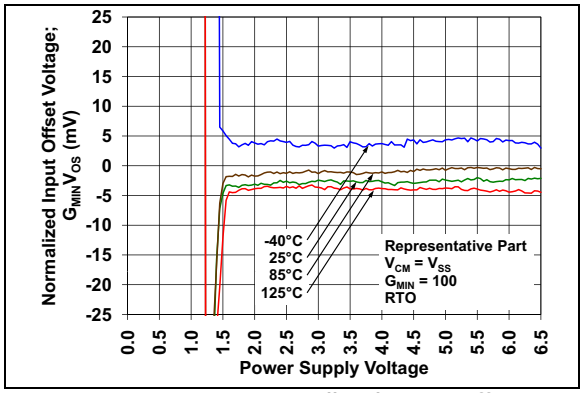



***FIGURE 2-6:*** *Normalized Input Offset Voltage vs. Power Supply Voltage, with $V_{CM}$ = 0V and $G_{MIN}$ = 100.*

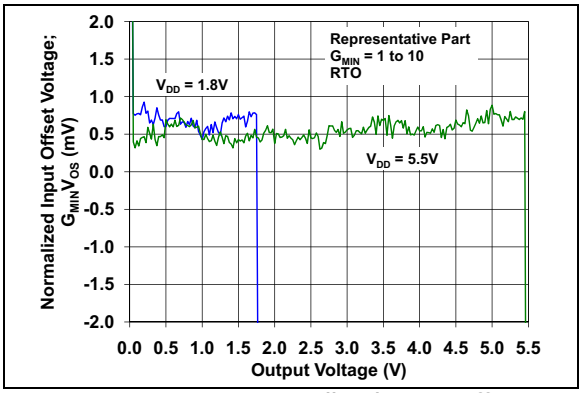



***FIGURE 2-9:*** *Normalized Input Offset Voltage vs. Output Voltage, with $G_{MIN}$ = 1 to 10.*

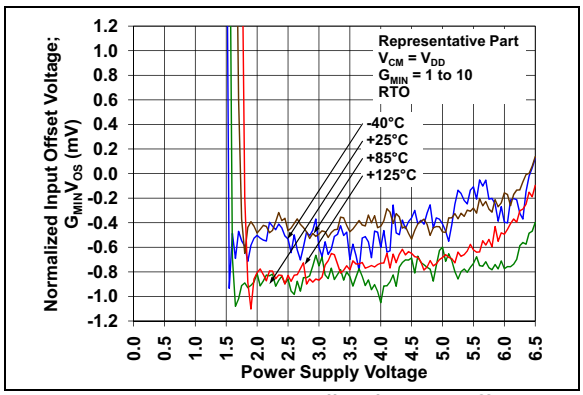



***FIGURE 2-7:*** *Normalized Input Offset Voltage vs. Power Supply Voltage, with $V_{CM}$ = $V_{DD}$ and $G_{MIN}$ = 1 to 10.*

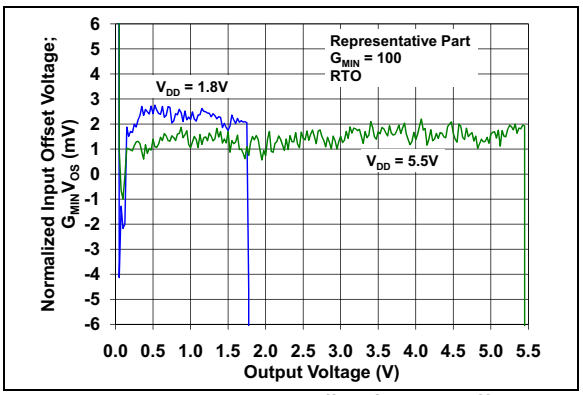



***FIGURE 2-10:*** *Normalized Input Offset Voltage vs. Output Voltage, with $G_{MIN}$ = 100.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

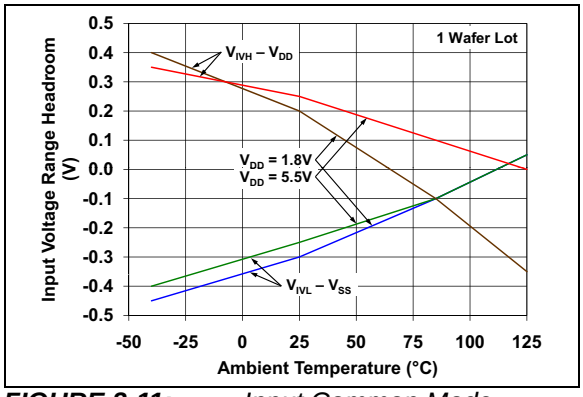



***FIGURE 2-11:*** *Input Common Mode Voltage Headroom vs. Ambient Temperature.*

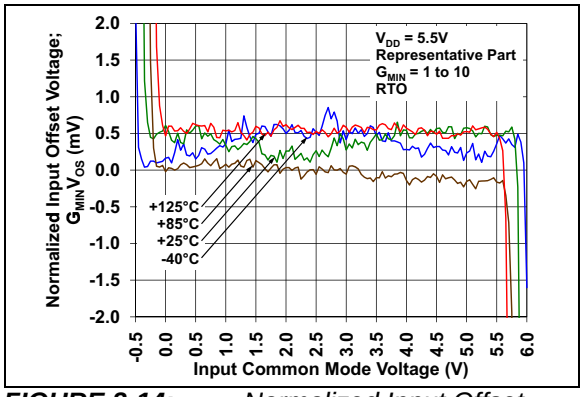



***FIGURE 2-14:*** *Normalized Input Offset Voltage vs. Common Mode Voltage, with $V_{DD}$ = 5.5V and $G_{MIN}$ = 1 to 10.*

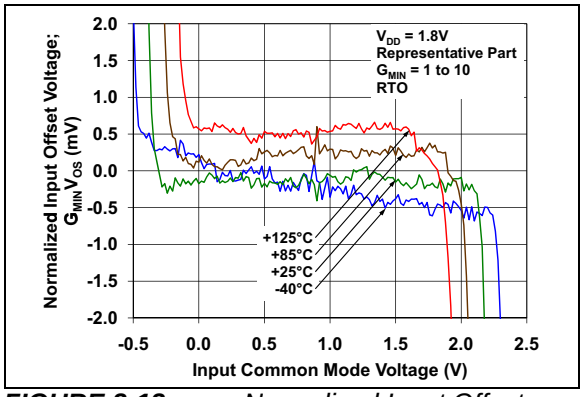



***FIGURE 2-12:*** *Normalized Input Offset Voltage vs. Common Mode Voltage, with $V_{DD}$ = 1.8V and $G_{MIN}$ = 1 to 10.*

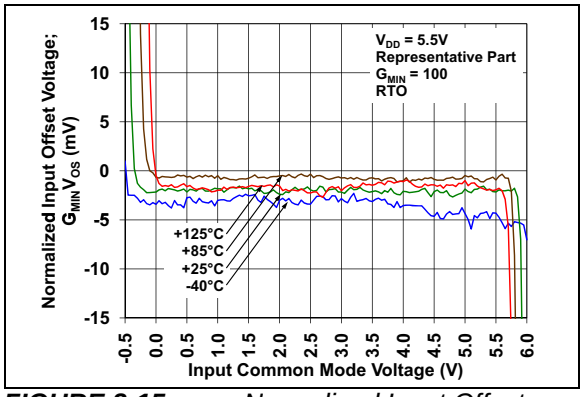



***FIGURE 2-15:*** *Normalized Input Offset Voltage vs. Common Mode Voltage, with $V_{DD}$ = 5.5V and $G_{MIN}$ = 100.*

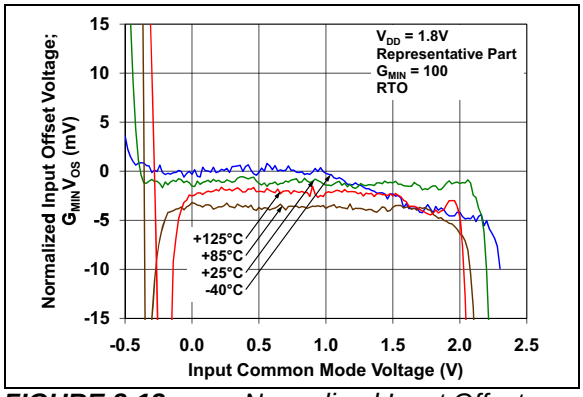



***FIGURE 2-13:*** *Normalized Input Offset Voltage vs. Common Mode Voltage, with $V_{DD}$ = 1.8V and $G_{MIN}$ = 100.*

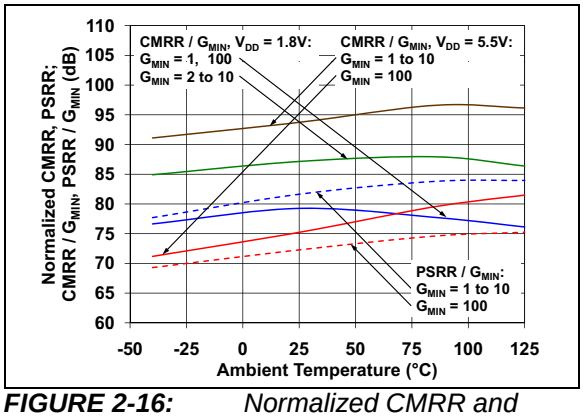



***FIGURE 2-16:*** *Normalized CMRR and PSRR vs. Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

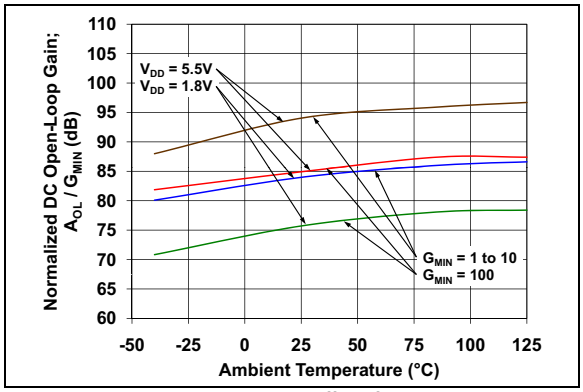



***FIGURE 2-17:*** *Normalized DC Open-Loop Gain vs. Ambient Temperature.*

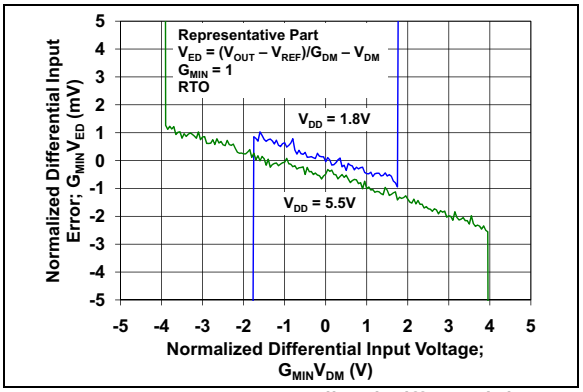



***FIGURE 2-20:*** *Normalized Differential Input Error vs. Differential Voltage, with $G_{MIN}$ = 1.*

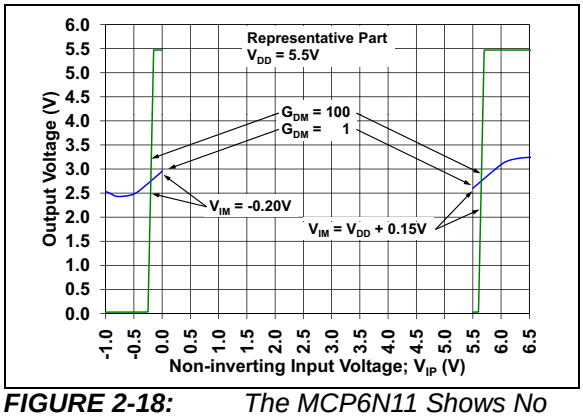



***FIGURE 2-18:*** *The MCP6N11 Shows No Phase Reversal vs. Common Mode Voltage.*

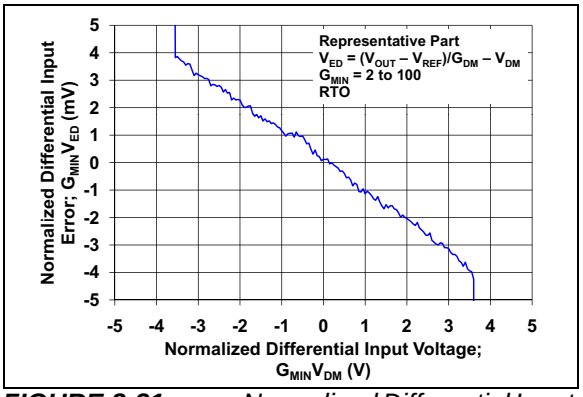



***FIGURE 2-21:*** *Normalized Differential Input Error vs. Differential Voltage, with $G_{MIN}$ = 2 to 100.*

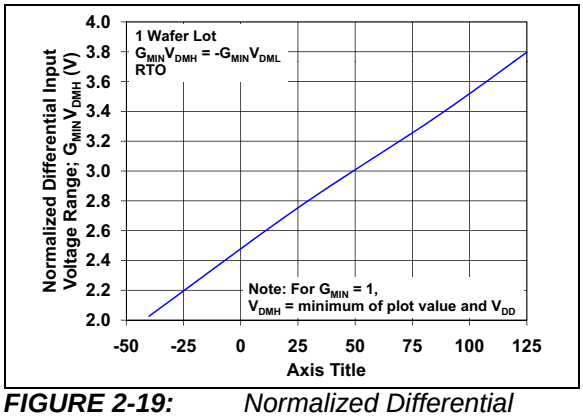



***FIGURE 2-19:*** *Normalized Differential Mode Voltage Range vs. Ambient Temperature.*

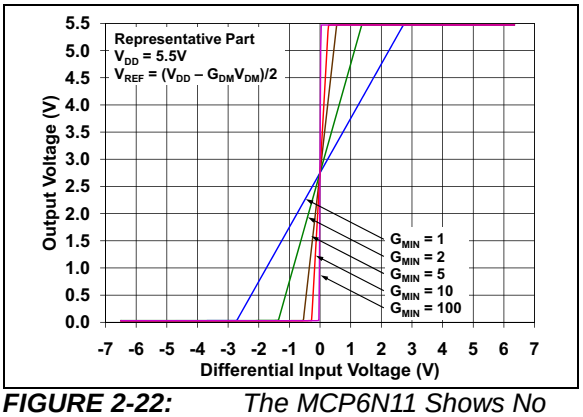



***FIGURE 2-22:*** *The MCP6N11 Shows No Phase Reversal vs. Differential Voltage, with $V_{DD}$ = 5.5V.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

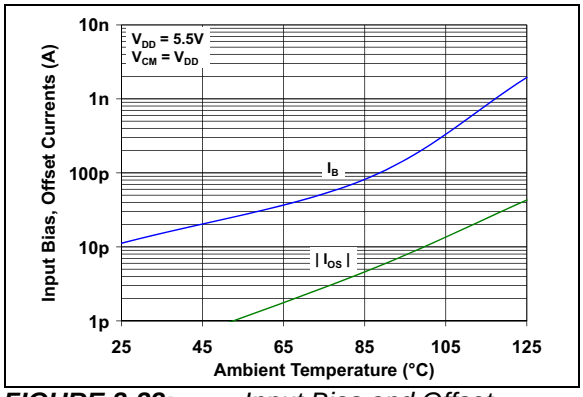



***FIGURE 2-23:*** *Input Bias and Offset Currents vs. Ambient Temperature, with $V_{DD}$ = +5.5V.*

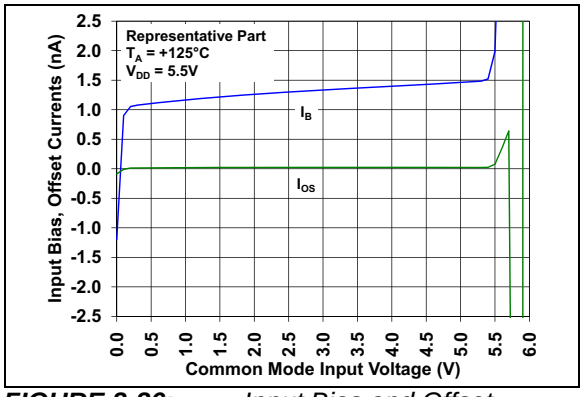



***FIGURE 2-26:*** *Input Bias and Offset Currents vs. Common Mode Input Voltage, with $T_A$ = +125°C.*

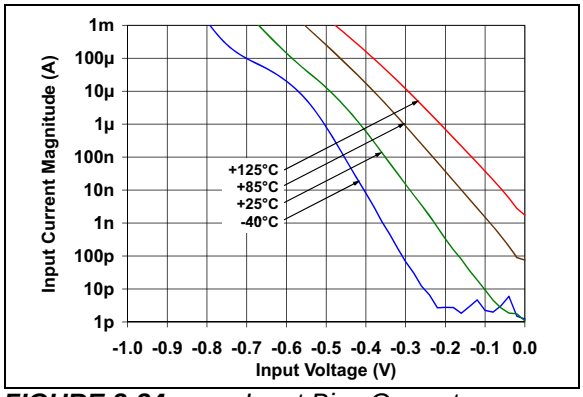



***FIGURE 2-24:*** *Input Bias Current vs. Input Voltage (below $V_{SS}$).*

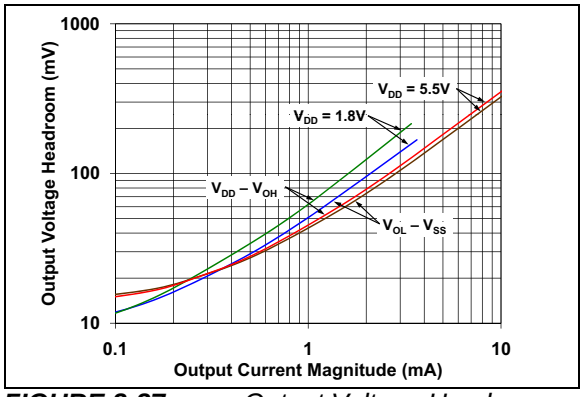



***FIGURE 2-27:*** *Output Voltage Headroom vs. Output Current.*

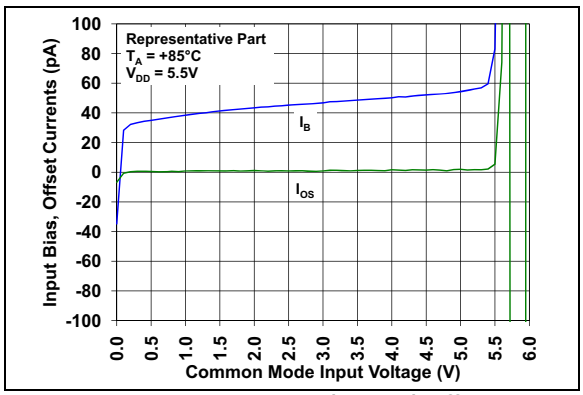



***FIGURE 2-25:*** *Input Bias and Offset Currents vs. Common Mode Input Voltage, with $T_A$ = +85°C.*

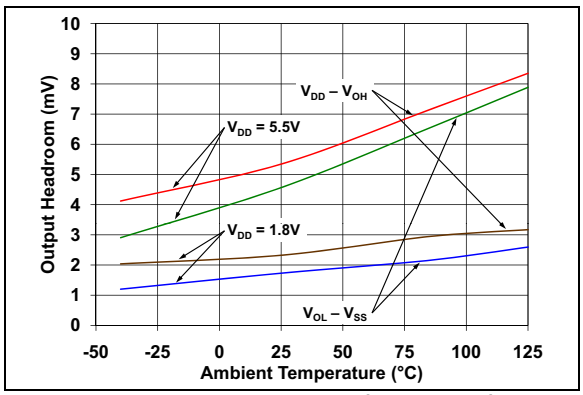



***FIGURE 2-28:*** *Output Voltage Headroom vs. Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

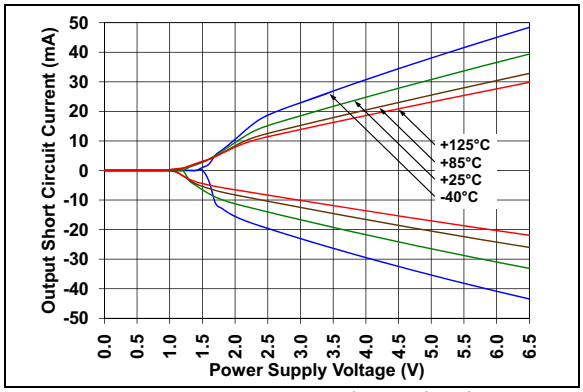



***FIGURE 2-29:*** *Output Short Circuit Current vs. Power Supply Voltage.*

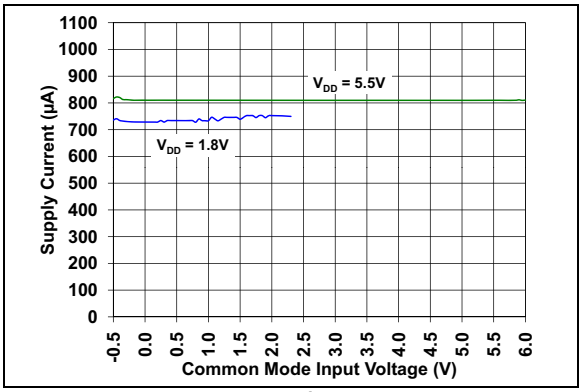



***FIGURE 2-31:*** *Supply Current vs. Common Mode Input Voltage.*

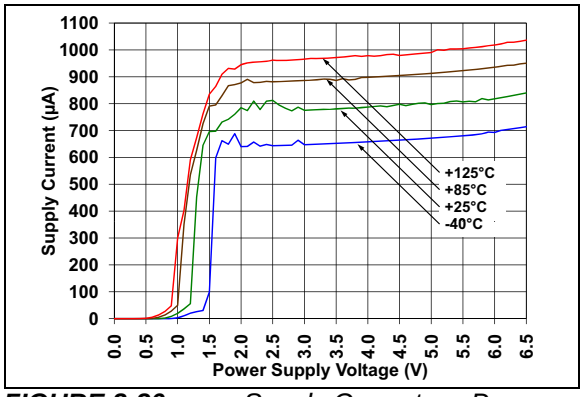



***FIGURE 2-30:*** *Supply Current vs. Power Supply Voltage.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

## 2.2 Frequency Response

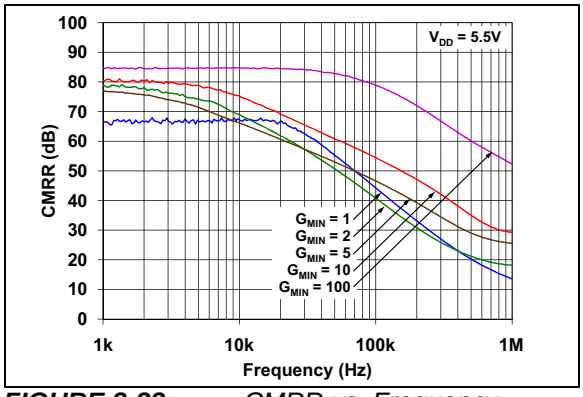



***FIGURE 2-32:*** *CMRR vs. Frequency.*

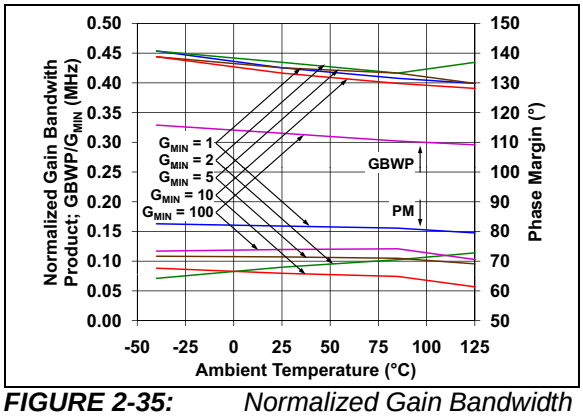



***FIGURE 2-35:*** *Normalized Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.*

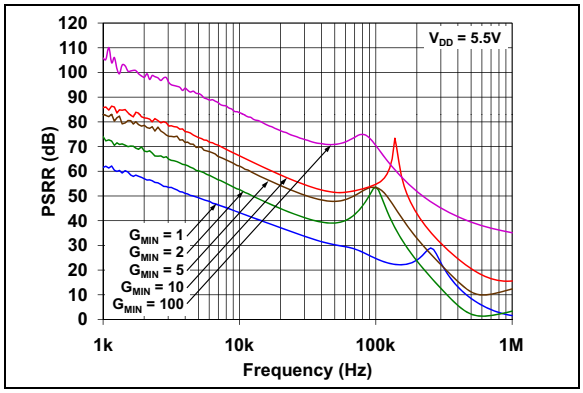



***FIGURE 2-33:*** *PSRR vs. Frequency.*

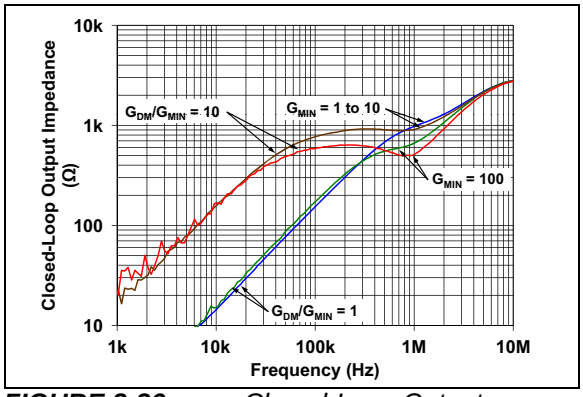



***FIGURE 2-36:*** *Closed-Loop Output Impedance vs. Frequency.*

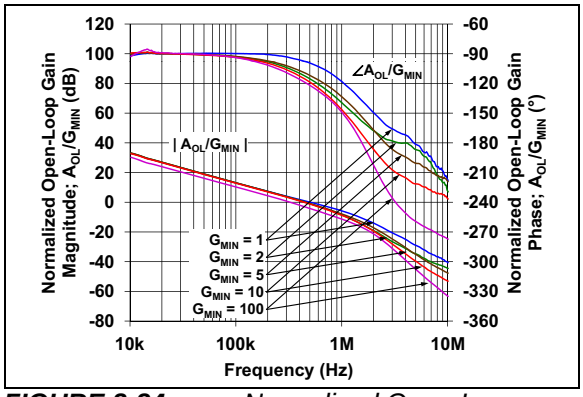



***FIGURE 2-34:*** *Normalized Open-Loop Gain vs. Frequency.*

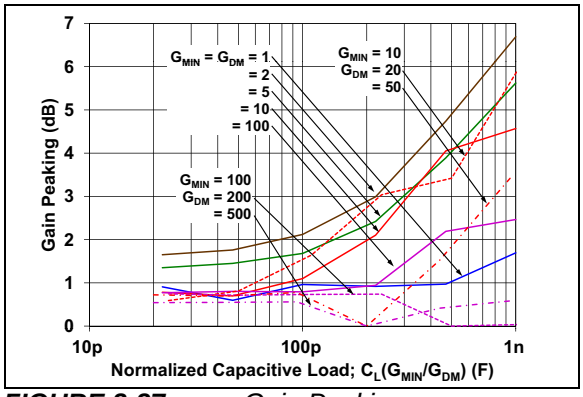



***FIGURE 2-37:*** *Gain Peaking vs. Normalized Capacitive Load.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}/2$, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

## 2.3 Noise

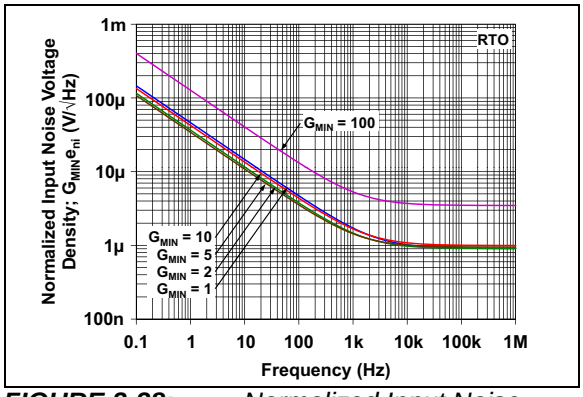



***FIGURE 2-38:*** *Normalized Input Noise Voltage Density vs. Frequency.*

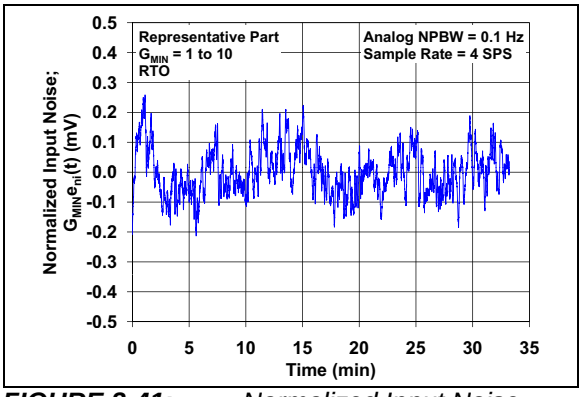



***FIGURE 2-41:*** *Normalized Input Noise Voltage vs. Time, with $G_{MIN}$ = 1 to 10.*

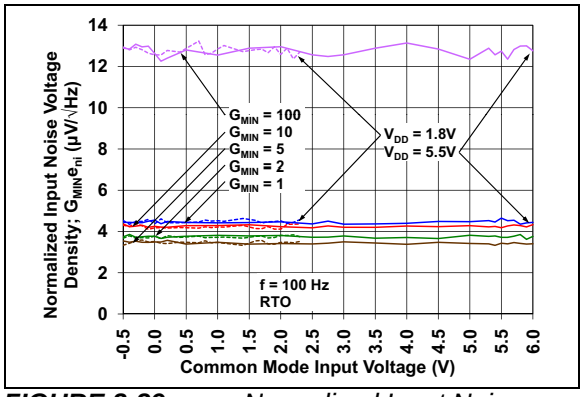



***FIGURE 2-39:*** *Normalized Input Noise Voltage Density vs. Input Common Mode Voltage, with f = 100 Hz.*

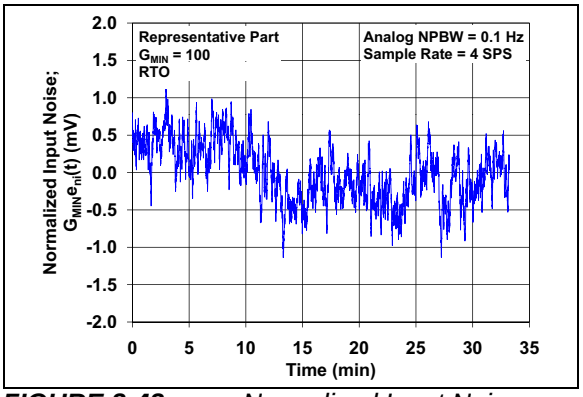



***FIGURE 2-42:*** *Normalized Input Noise Voltage vs. Time, with $G_{MIN}$ = 100.*

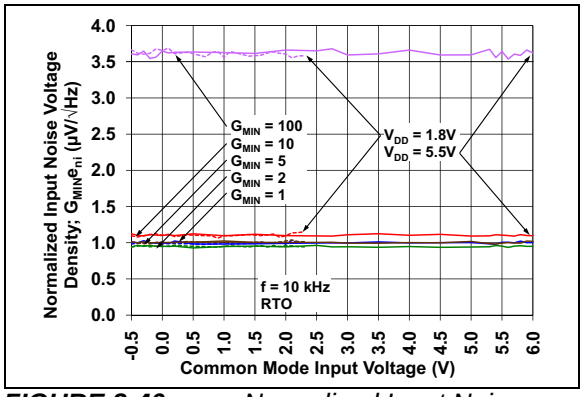



***FIGURE 2-40:*** *Normalized Input Noise Voltage Density vs. Input Common Mode Voltage, with f = 10 kHz.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

## 2.4 Time Response

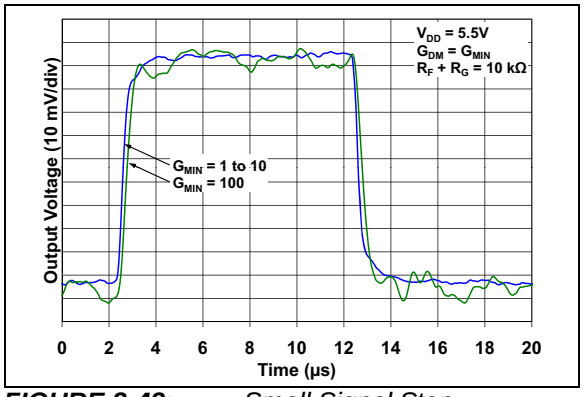



***FIGURE 2-43:*** *Small Signal Step Response.*

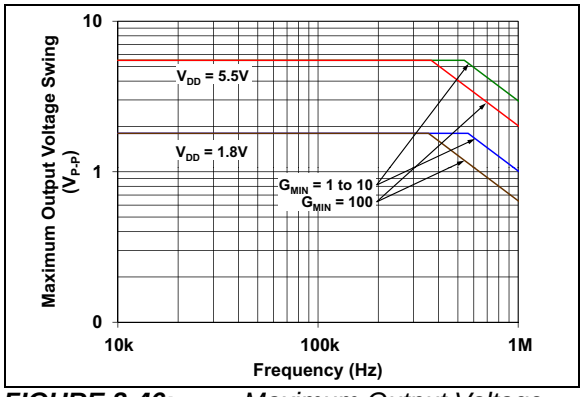



***FIGURE 2-46:*** *Maximum Output Voltage Swing vs. Frequency.*

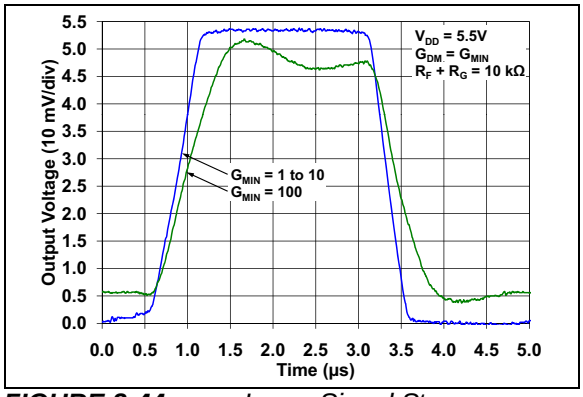



***FIGURE 2-44:*** *Large Signal Step Response.*

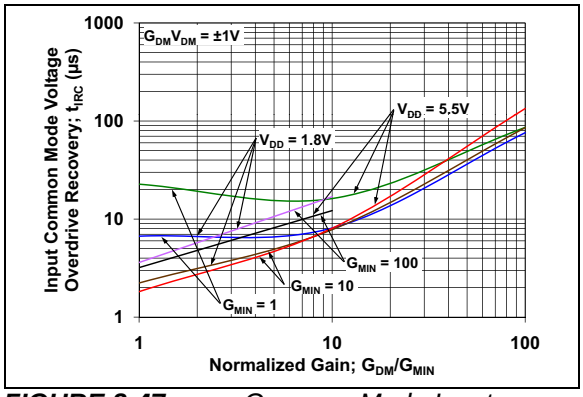



***FIGURE 2-47:*** *Common Mode Input Overdrive Recovery Time vs. Normalized Gain.*

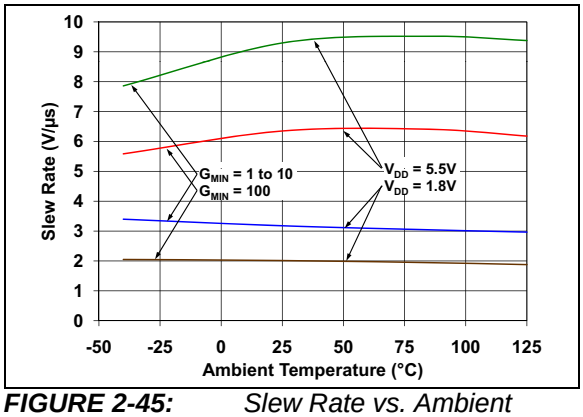



***FIGURE 2-45:*** *Slew Rate vs. Ambient Temperature.*

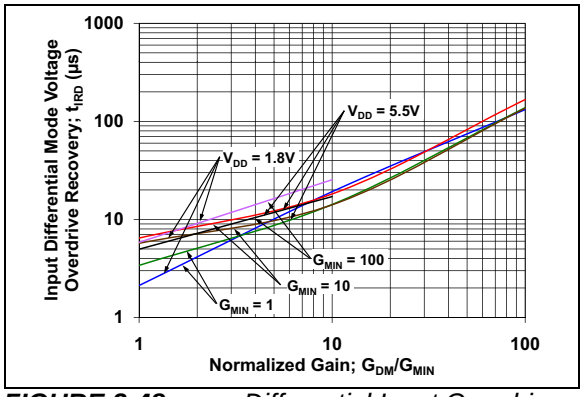



***FIGURE 2-48:*** *Differential Input Overdrive Recovery Time vs. Normalized Gain.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

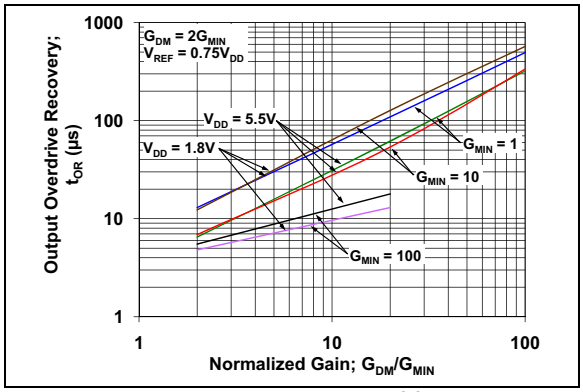



***FIGURE 2-49:*** *Output Overdrive Recovery Time vs. Normalized Gain.*

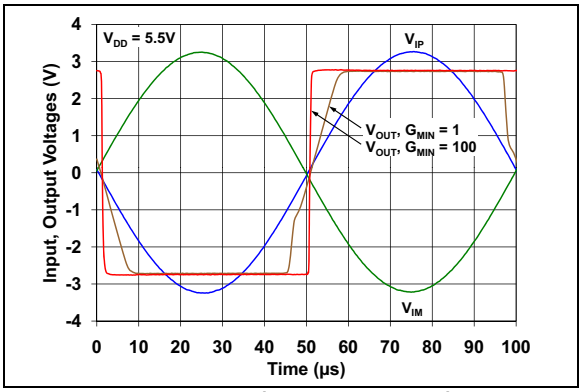



***FIGURE 2-51:*** *The MCP6N11 Shows No Phase Reversal vs. Differential Input Overdrive, with $V_{DD}$ = 5.5V.*

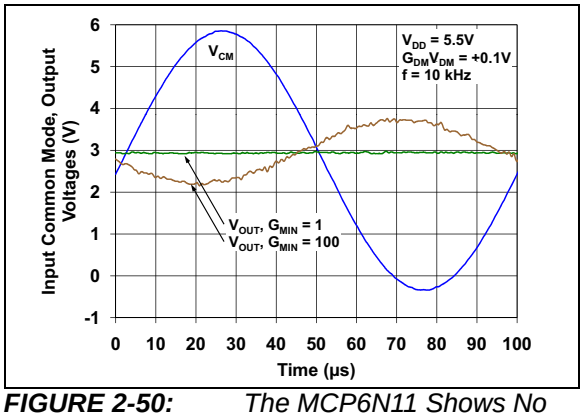



***FIGURE 2-50:*** *The MCP6N11 Shows No Phase Reversal vs. Common Mode Input Overdrive, with $V_{DD}$ = 5.5V.*


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**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

## 2.5 Enable/Calibration and POR Responses

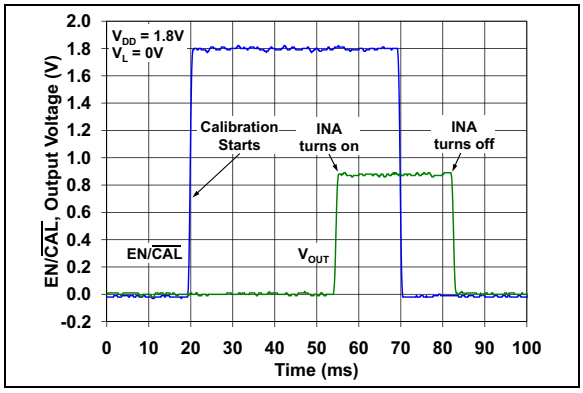



***FIGURE 2-52:*** *EN/$\overline{CAL}$ and Output Voltage vs. Time, with $V_{DD}$ = 1.8V.*

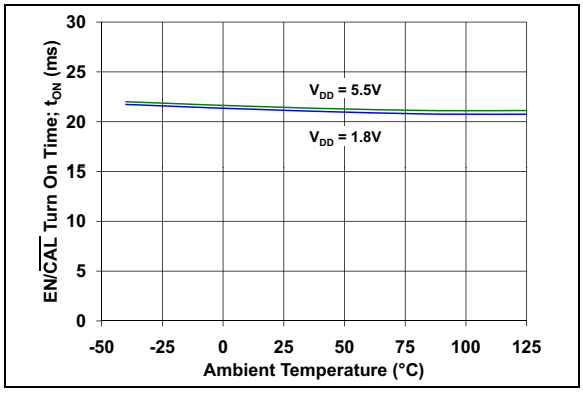



***FIGURE 2-55:*** *EN/$\overline{CAL}$ Turn On Time vs. Ambient Temperature.*

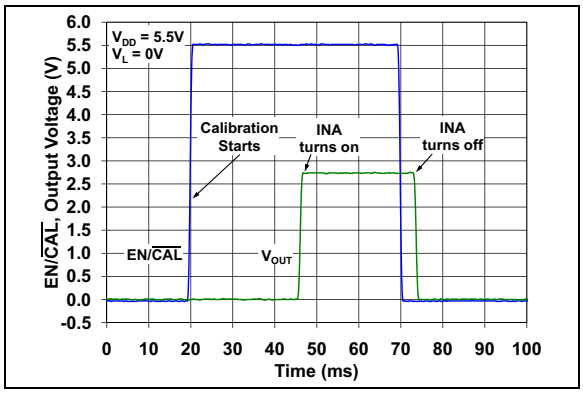



***FIGURE 2-53:*** *EN/$\overline{CAL}$ and Output Voltage vs. Time, with $V_{DD}$ = 5.5V*

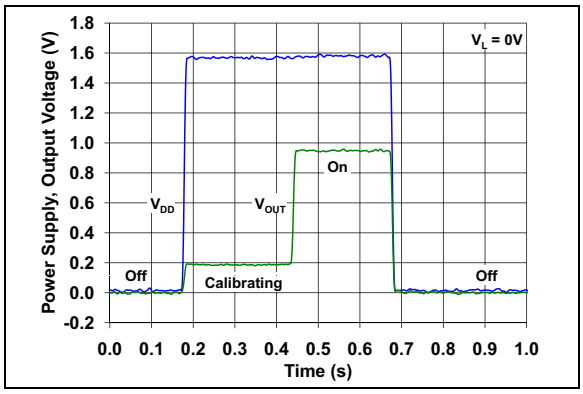



***FIGURE 2-56:*** *Power Supply On and Off and Output Voltage vs. Time.*

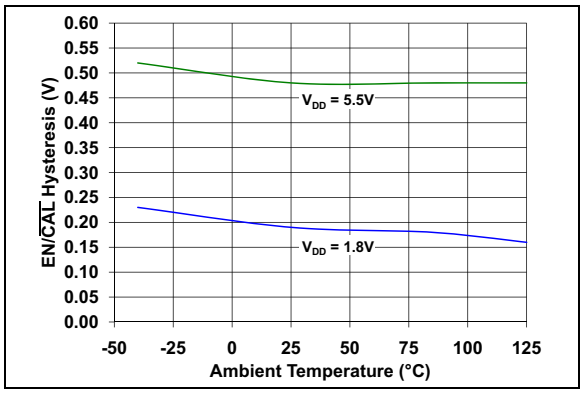



***FIGURE 2-54:*** *EN/$\overline{CAL}$ Hysteresis vs. Ambient Temperature.*

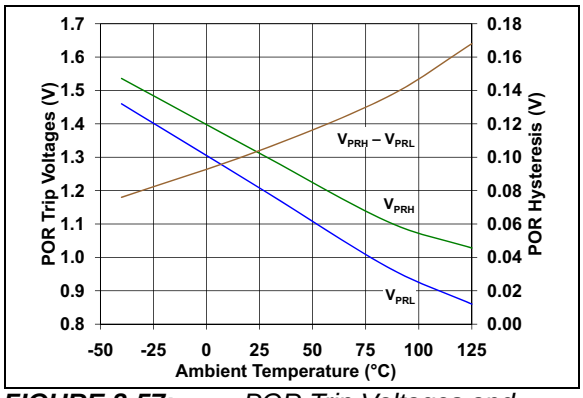



***FIGURE 2-57:*** *POR Trip Voltages and Hysteresis vs. Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = 1.8V to 5.5V, $V_{SS}$ = GND, EN/$\overline{CAL}$ = $V_{DD}$, $V_{CM}$ = $V_{DD}$/2, $V_{DM}$ = 0V, $V_{REF}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$, $C_L$ = 60 pF and $G_{DM}$ = $G_{MIN}$; see Figure 1-6 and Figure 1-7.

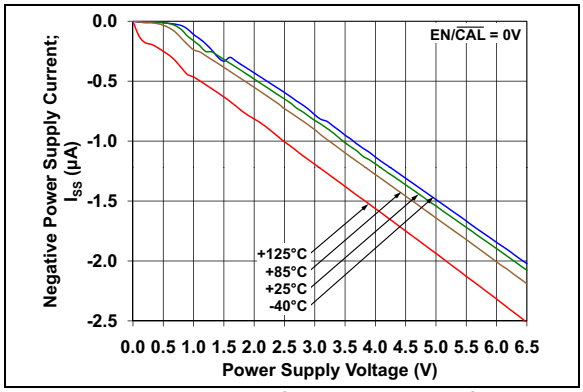



***FIGURE 2-58:*** *Quiescent Current in Shutdown vs. Power Supply Voltage.*

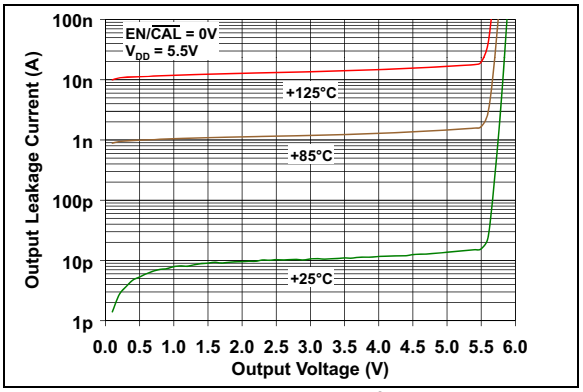



***FIGURE 2-59:*** *Output Leakage Current vs. Output Voltage.*


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## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| MCP6N11 | | Symbol | Description |
|---|---|---|---|
| SOIC | TDFN | | |
| 1 | 1 | $V_{FG}$ | Feedback Input |
| 2 | 2 | $V_{IM}$ | Inverting Input |
| 3 | 3 | $V_{IP}$ | Non-inverting Input |
| 4 | 4 | $V_{SS}$ | Negative Power Supply |
| 5 | 5 | $V_{REF}$ | Reference Input |
| 6 | 6 | $V_{OUT}$ | Output |
| 7 | 7 | $V_{DD}$ | Positive Power Supply |
| 8 | 8 | EN/$\overline{CAL}$ | Enable/$V_{OS}$ Calibrate Digital Input |
| — | 9 | EP | Exposed Thermal Pad (EP); must be connected to $V_{SS}$ |

### 3.1 Analog Signal Inputs

The non-inverting and inverting inputs ($V_{IP}$, and $V_{IM}$) are high-impedance CMOS inputs with low bias currents.

### 3.2 Analog Feedback Input

The analog feedback input ($V_{FG}$) is the inverting input of the second input stage. The external feedback components ($R_F$ and $R_G$) are connected to this pin. It is a high-impedance CMOS input with low bias current.

### 3.3 Analog Reference Input

The analog reference input ($V_{REF}$) is the non-inverting input of the second input stage; it shifts $V_{OUT}$ to its desired range. The external gain resistor ($R_G$) is connected to this pin. It is a high-impedance CMOS input with low bias current.

### 3.4 Analog Output

The analog output ($V_{OUT}$) is a low-impedance voltage output. It represents the differential input voltage ($V_{DM} = V_{IP} – V_{IM}$), with gain $G_{DM}$ and is shifted by $V_{REF}$. The external feedback resistor ($R_F$) is connected to this pin.

### 3.5 Power Supply Pins

The positive power supply ($V_{DD}$) is 1.8V to 5.5V higher than the negative power supply ($V_{SS}$). For normal operation, the other pins are between $V_{SS}$ and $V_{DD}$.

Typically, these parts are used in a single (positive) supply configuration. In this case, $V_{SS}$ is connected to ground and $V_{DD}$ is connected to the supply; $V_{DD}$ will need bypass capacitors.

### 3.6 Digital Enable and $V_{OS}$ Calibration Input

This input (EN/$\overline{CAL}$) is a CMOS, Schmitt-triggered input that controls the active, low power and $V_{OS}$ calibration modes of operation. When this pin goes low, the part is placed into a low power mode and the output is high-Z. When this pin goes high, the amplifier's input offset voltage is corrected by the calibration circuitry, then the output is re-connected to the $V_{OUT}$ pin, which becomes low impedance, and the part resumes normal operation.

### 3.7 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the $V_{SS}$ pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance ($\theta_{JA}$).

**NOTES:**


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## 4.0 APPLICATIONS

The MCP6N11 instrumentation amplifier (INA) is manufactured using Microchip's state of the art CMOS process. It is low cost, low power and high speed, making it ideal for battery-powered applications.

### 4.1 Basic Performance

#### 4.1.1 STANDARD CIRCUIT

Figure 4-1 shows the standard circuit configuration for these INAs. When the inputs and output are in their specified ranges, the output voltage is approximately:

**EQUATION 4-1:**

$$V_{OUT} \approx V_{REF} + G_{DM}V_{DM}$$

Where:

$$G_{DM} = 1 + R_F / R_G$$

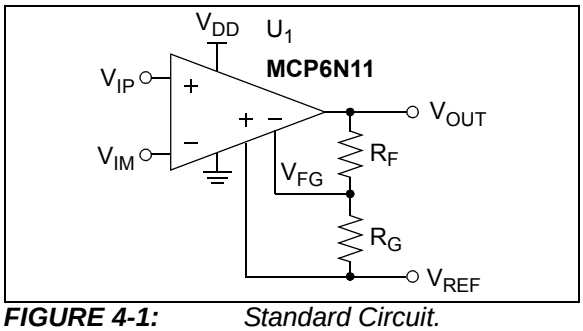



***FIGURE 4-1:*** *Standard Circuit.*

For normal operation, keep:

- $V_{IP}$, $V_{IM}$, $V_{REF}$ and $V_{FG}$ between $V_{IVL}$ and $V_{IVH}$
- $V_{IP} – V_{IM}$ (i.e., $V_{DM}$) between $V_{DML}$ and $V_{DMH}$
- $V_{OUT}$ between $V_{OL}$ and $V_{OH}$

#### 4.1.2 ARCHITECTURE

Figure 4-2 shows the block diagram for these INAs.

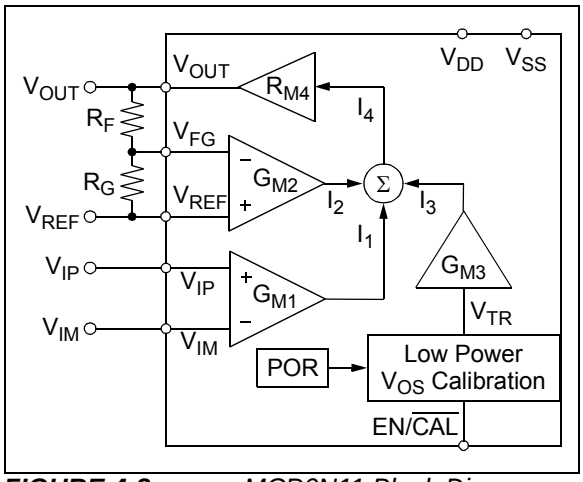



***FIGURE 4-2:*** *MCP6N11 Block Diagram.*

The input offset voltage ($V_{OS}$) is corrected by the voltage $V_{TR}$. Each time a $V_{OS}$ Calibration event occurs, $V_{TR}$ is updated to the best value (at that moment). These events are triggered by either powering up (monitored by the POR) or by toggling the EN/$\overline{CAL}$ pin high. The current out of $G_{M3}$ ($I_3$) is constant and very small (assumed to be zero in the following discussion).

The input signal is applied to $G_{M1}$. Equation 4-2 shows the relationships between the input voltages ($V_{IP}$ and $V_{IM}$) and the common mode and differential voltages ($V_{CM}$ and $V_{DM}$).

**EQUATION 4-2:**

$$\begin{aligned} V_{IP} &= V_{CM} + V_{DM}/2 \\ V_{IM} &= V_{CM} - V_{DM}/2 \\ V_{CM} &= (V_{IP} + V_{IM})/2 \\ V_{DM} &= V_{IP} - V_{IM} \end{aligned}$$

The negative feedback loop includes $G_{M2}$, $R_{M4}$, $R_F$ and $R_G$. These blocks set the DC open-loop gain ($A_{OL}$) and the nominal differential gain ($G_{DM}$):

**EQUATION 4-3:**

$$\begin{aligned} A_{OL} &= G_{M2}R_{M4} \\ G_{DM} &= 1 + R_F/R_G \end{aligned}$$

$A_{OL}$ is very high, so $I_4$ is very small and $I_1 + I_2 \approx 0$. This makes the differential inputs to $G_{M1}$ and $G_{M2}$ equal in magnitude and opposite in polarity. Ideally, this gives:

**EQUATION 4-4:**

$$\begin{aligned} (V_{FG} - V_{REF}) &= V_{DM} \\ V_{OUT} &= V_{DM}G_{DM} + V_{REF} \end{aligned}$$

For an ideal part, changing $V_{CM}$, $V_{SS}$ or $V_{DD}$ produces no change in $V_{OUT}$. $V_{REF}$ shifts $V_{OUT}$ as needed.

The different $G_{MIN}$ options change $G_{M1}$, $G_{M2}$ and the internal compensation capacitor. This results in the performance trade-offs shown in Table 1.

### 4.1.3 DC ERRORS

**Section 1.5 "Explanation of DC Error Specs"** defines some of the DC error specifications. These errors are internal to the INA, and can be summarized as follows:

**EQUATION 4-5:**

$$V_{OUT} = V_{REF} + G_{DM}(1 + g_E)(V_{DM} + \Delta V_{ED}) + G_{DM}(1 + g_E)(V_E + \Delta V_E)$$

Where:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR} + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot \frac{\Delta V_{OS}}{\Delta T_A}$$

$$\Delta V_{ED} \le INL_{DM}(V_{DMH} - V_{DML})$$

$$\Delta V_E \le INL_{CM}(V_{IVH} - V_{IVL})$$

Where:

*PSRR*, *CMRR* and $A_{OL}$ are in units of V/V

$\Delta T_A$ is in units of °C

The non-linearity specs ($INL_{CM}$ and $INL_{DM}$) describe errors that are non-linear functions of $V_{CM}$ and $V_{DM}$, respectively. They give the maximum excursion from linear response over the entire common mode and differential ranges.

The input bias current and offset current specs ($I_B$ and $I_{OS}$), together with a circuit's external input resistances, give an additional DC error. Figure 4-3 shows the resistors that set the DC bias point.

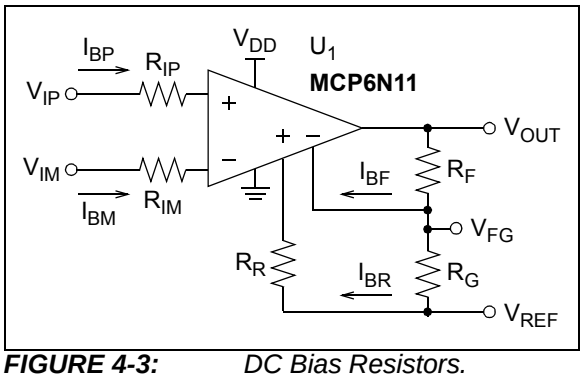



***FIGURE 4-3:*** *DC Bias Resistors.*

The resistors at the main input ($R_{IP}$ and $R_{IM}$) and its input bias currents ($I_{BP}$ and $I_{BM}$) give the following changes in the INA's bias voltages:

**EQUATION 4-6:**

$$\Delta V_{IP} = -I_{BP}R_{IP} = \left(-I_B - \frac{I_{OS}}{2}\right)R_{IP}$$

$$\Delta V_{IM} = -I_{BM}R_{IM} = \left(-I_B + \frac{I_{OS}}{2}\right)R_{IM}$$

$$\Delta V_{CM} = \frac{\Delta V_{IP} + \Delta V_{IM}}{2} = -I_B\left(\frac{R_{IP} + R_{IM}}{2}\right) + \frac{-I_{OS}}{2}\left(\frac{-R_{IP} + R_{IM}}{2}\right)$$

$$\Delta V_{DM} = \Delta V_{IP} - \Delta V_{IM} = I_B(-R_{IP} + R_{IM}) - \frac{I_{OS}}{2}(R_{IP} + R_{IM})$$

$$\Delta V_{OUT} = G_{DM}\left(\Delta V_{DM} + \frac{\Delta V_{CM}}{CMRR}\right)$$

Where:

CMRR is in units of V/V

The best design results when $R_{IP}$ and $R_{IM}$ are equal and small:

**EQUATION 4-7:**

$$\Delta V_{OUT} \approx G_{DM}\Delta V_{DM} \approx G_{DM}(\pm 2 I_B \varepsilon_{RTOL} - I_{OS})R_{IP}$$

Where:

$R_{IP} = R_{IM}$

$\varepsilon_{RTOL}$ = tolerance of $R_{IP}$ and $R_{IM}$

The resistors at the feedback input ($R_R$, $R_F$ and $R_G$) and its input bias currents ($I_{BR}$ and $I_{BF}$) give the following changes in the INA's bias voltages:

**EQUATION 4-8:**

$$\Delta V_{REF} = -I_{BR}R_R = \left(-I_{B2} - \frac{I_{OS2}}{2}\right)R_R$$

$\Delta V_{FG} \approx \Delta V_{REF}$, due to high $A_{OL}$

$$\Delta V_{OUT} \approx I_{B2}(R_F - G_{DM}R_R) + \frac{I_{OS2}}{2}(R_F + G_{DM}R_R)$$

Where:

$I_{B2}$ meets the $I_B$ spec, but is not equal to $I_B$

$I_{OS2}$ meets the $I_{OS}$ spec, but is not equal to $I_{OS}$

The best design results when $G_{DM}R_R$ and $R_F$ are equal and small:

**EQUATION 4-9:**

$$\Delta V_{OUT} \approx (\pm(2 I_{B2} \varepsilon_{RTOL} + I_{OS2}))R_F$$

Where:

$G_{DM}R_R = R_F$

$\varepsilon_{RTOL}$ = tolerance of $R_R$, $R_F$ and $R_G$


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### 4.1.4 AC PERFORMANCE

The bandwidth of these amplifiers depends on $G_{DM}$ and $G_{MIN}$:

**EQUATION 4-10:**

$$f_{BW} \approx \frac{f_{GBWP}}{G_{DM}}$$
$$\approx (0.50\ MHz)(G_{MIN} / G_{DM}), \quad G_{MIN} = 1, \ldots, 10$$
$$\approx (0.35\ MHz)(G_{MIN} / G_{DM}), \quad G_{MIN} = 100$$

Where:

$f_{BW}$ = -3 dB bandwidth

$f_{GBWP}$ = Gain bandwidth product

The bandwidth at the maximum output swing is called the Full Power Bandwidth ($f_{FPBW}$). It is limited by the Slew Rate (SR) for many amplifiers, but is close to $f_{BW}$ for these parts:

**EQUATION 4-11:**

$$f_{FPBW} \approx \frac{SR}{\pi V_O}$$
$$\approx f_{BW}, \quad \text{for these parts}$$

Where:

$V_O$ = Maximum output voltage swing

$\approx V_{OH} - V_{OL}$

CMRR is constant from DC to about 1 kHz.

### 4.1.5 NOISE PERFORMANCE

As shown in Figures 2-41 and 2-42, the 1/f noise causes an apparent wander in the DC output voltage. Changing the measurement time or bandwidth has little effect on this noise.

We recommend re-calibrating $V_{OS}$ periodically, to reduce 1/f noise wander. For example, $V_{OS}$ could be re-calibrated at least once every 15 minutes; more often when temperature or $V_{DD}$ change significantly.

## 4.2 Functional Blocks

### 4.2.1 RAIL-TO-RAIL INPUTS

Each input stage uses one PMOS differential pair at the input. The output of each differential pair is processed using current mode circuitry. The inputs show no crossover distortion vs. common mode voltage.

With this topology, the inputs ($V_{IP}$ and $V_{IM}$) operate normally down to $V_{SS}$ – 0.2V and up to $V_{DD}$ + 0.15V at room temperature (see Figure 2-11). The input offset voltage ($V_{OS}$) is measured at $V_{CM} = V_{SS}$ – 0.2V and $V_{DD}$ + 0.15V (at +25°C), to ensure proper operation.

#### 4.2.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figures 2-18 and 2-50 show an input voltage exceeding both supplies with no phase inversion.

The input devices also do not exhibit phase inversion when the differential input voltage exceeds its limits; see Figures 2-22 and 2-51.

#### 4.2.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). This requirement is independent of the current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-4. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize input bias current ($I_B$).

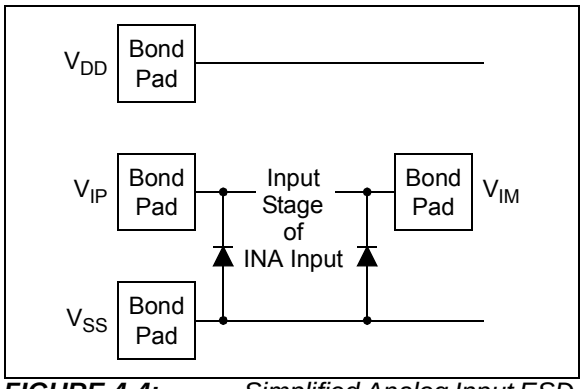



***FIGURE 4-4:*** *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below $V_{SS}$. They also clamp any voltages that go too far above $V_{DD}$; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow overvoltage (beyond $V_{DD}$) events. Very fast ESD events (that meet the spec) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs. Figure 4-5 shows one approach to protecting these inputs. $D_1$ and $D_2$ may be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode-connected FETs for low leakage.

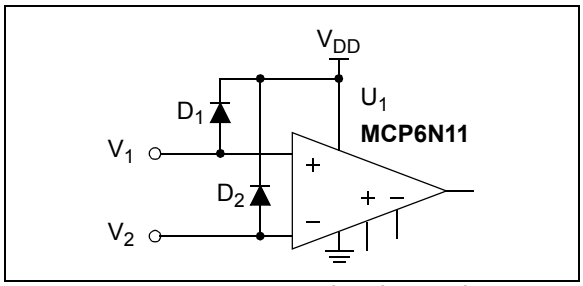



***FIGURE 4-5:*** *Protecting the Analog Inputs Against High Voltages.*

### 4.2.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). This requirement is independent of the voltage limits previously discussed.

Figure 4-6 shows one approach to protecting these inputs. The resistors $R_1$ and $R_2$ limit the possible current in or out of the input pins (and into $D_1$ and $D_2$). The diode currents will dump onto $V_{DD}$.

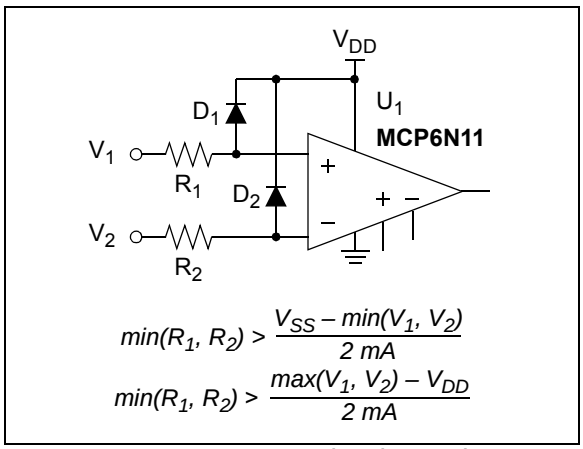



***FIGURE 4-6:*** *Protecting the Analog Inputs Against High Currents.*

It is also possible to connect the diodes to the left of the resistor $R_1$ and $R_2$. In this case, the currents through the diodes $D_1$ and $D_2$ need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IP}$ and $V_{IM}$) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage ($V_{CM}$) is below ground ($V_{SS}$); see Figure 2-25.

### 4.2.1.4 Input Voltage Ranges

Figure 4-7 shows possible input voltage values ($V_{SS}$ = 0V). Lines with a slope of +1 have constant $V_{DM}$ (e.g., the $V_{DM}$ = 0 line). Lines with a slope of -1 have constant $V_{CM}$ (e.g., the $V_{CM} = V_{DD}/2$ line).

For normal operation, $V_{IP}$ and $V_{IM}$ must be kept within the region surrounded by the thick blue lines. The horizontal and vertical blue lines show the limits on the individual inputs. The blue lines with a slope of +1 show the limits on $V_{DM}$; the larger $G_{MIN}$ is, the closer they are to the $V_{DM}$ = 0 line.

The input voltage range specs ($V_{IVL}$ and $V_{IVH}$) change with the supply voltages ($V_{SS}$ and $V_{DD}$, respectively). The differential input range specs ($V_{DML}$ and $V_{DMH}$) change with minimum gain ($G_{MIN}$). Temperature also affects these specs.

To take full advantage of $V_{DML}$ and $V_{DMH}$, set $V_{REF}$ (see Figure 1-6 and Figure 1-7) so that the output ($V_{OUT}$) is centered between the supplies ($V_{SS}$ and $V_{DD}$).

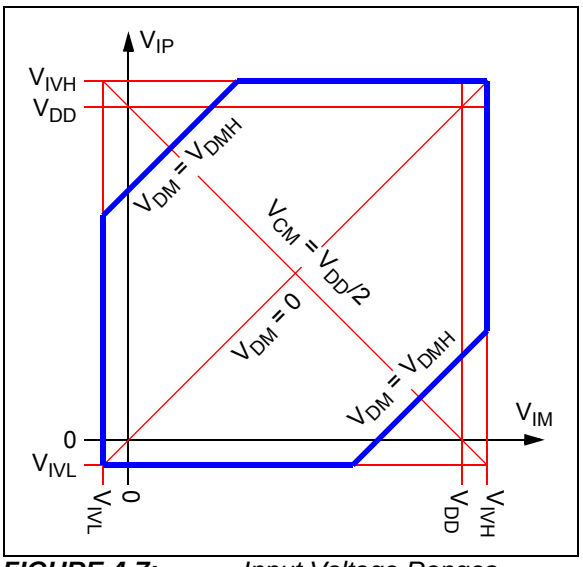



***FIGURE 4-7:*** *Input Voltage Ranges.*


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#### 4.2.2 ENABLE/$V_{OS}$ CALIBRATION (EN/$\overline{CAL}$)

These parts have a Normal mode, a Low Power mode and a $V_{OS}$ Calibration mode.

When the EN/$\overline{CAL}$ pin is high and the internal POR (with delay) indicates that power is good, the part operates in its Normal mode.

When the EN/$\overline{CAL}$ pin is low, the part operates in its Low Power mode. The quiescent current (at $V_{SS}$) drops to -2.5 µA (typical), the amplifier output is put into a high-impedance state. Signals at the input pins can feed through to the output pin.

When the EN/$\overline{CAL}$ pin goes high and the internal POR (with delay) indicates that power is good, the amplifier internally corrects its input offset voltage ($V_{OS}$) with the internal common mode voltage at mid-supply ($V_{DD}/2$) and the output tri-stated (after $t_{OFF}$). Once $V_{OS}$ Calibration is completed, the amplifier is enabled and normal operation resumes.

The EN/$\overline{CAL}$ pin does not operate normally when left floating. Either drive it with a logic output, or tie it high so that the part is always on.

#### 4.2.3 POR WITH DELAY

The internal POR makes sure that the input offset voltage ($V_{OS}$) is calibrated whenever the supply voltage goes from low voltage (< $V_{PRL}$) to high voltage (> $V_{PRH}$). This prevents corruption of the $V_{OS}$ trim registers after a low-power event.

After the POR goes high, the internal circuitry adds a fixed delay ($t_{PLH}$), before telling the $V_{OS}$ Calibration circuitry (see Figure 4-2) to start. If the EN/$\overline{CAL}$ pin is toggled during this time, the fixed delay is restarted (takes an additional time $t_{PLH}$).

#### 4.2.4 PARITY DETECTOR

A parity error detector monitors the memory contents for any corruption. In the rare event that a parity error is detected (e.g., corruption from an alpha particle), a POR event is automatically triggered. This will cause the input offset voltage to be re-corrected, and the op amp will not return to normal operation for a period of time (the POR turn on time, $t_{PLH}$).

#### 4.2.5 RAIL-TO-RAIL OUTPUT

The Minimum Output Voltage ($V_{OL}$) and Maximum Output Voltage ($V_{OH}$) specs describe the widest output swing that can be achieved under the specified load conditions.

The output can also be limited when $V_{IP}$ or $V_{IM}$ exceeds $V_{IVL}$ or $V_{IVH}$, or when $V_{DM}$ exceeds $V_{DML}$ or $V_{DMH}$.

### 4.3 Applications Tips

#### 4.3.1 MINIMUM STABLE GAIN

There are different options for different Minimum Stable Gains (1, 2, 5, 10 and 100 V/V; see Table 1-1). The differential gain ($G_{DM}$) needs to be greater than or equal to $G_{MIN}$ in order to maintain stability.

Picking a part with higher $G_{MIN}$ has the advantages of lower Input Noise Voltage Density ($e_{ni}$), lower Input Offset Voltage ($V_{OS}$) and increased Gain Bandwidth Product (GBWP); see Table 1. The Differential Input Voltage Range ($V_{DMR}$) is lower for higher $G_{MIN}$, but the output voltage range would limit $V_{DMR}$ anyway, when $G_{DM} \geq 2$.

#### 4.3.2 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. Lower gains ($G_{DM}$) exhibit greater sensitivity to capacitive loads.

When driving large capacitive loads with these instrumentation amps (e.g., > 100 pF), a small series resistor at the output ($R_{ISO}$ in Figure 4-8) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

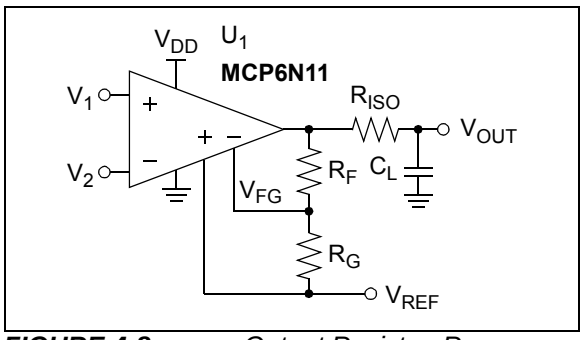



***FIGURE 4-8:*** *Output Resistor, $R_{ISO}$ stabilizes large capacitive loads.*

Figure 4-9 gives recommended $R_{ISO}$ values for different capacitive loads and gains. The x-axis is the normalized load capacitance ($C_L$ $G_{MIN}/G_{DM}$), where $G_{DM}$ is the circuit's differential gain ($1 + R_F / R_G$) and $G_{MIN}$ is the minimum stable gain.

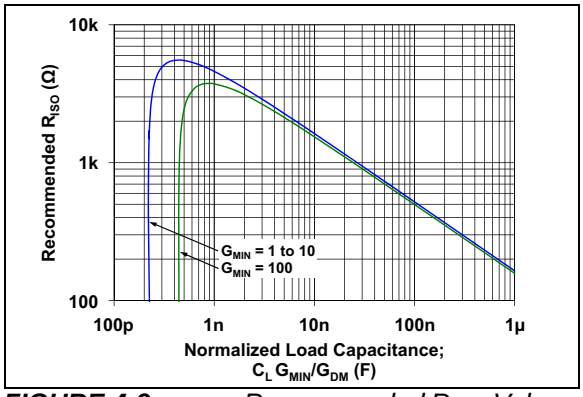



***FIGURE 4-9:*** *Recommended $R_{ISO}$ Values for Capacitive Loads.*

After selecting $R_{ISO}$ for your circuit, double check the resulting frequency response peaking and step response overshoot on the bench. Modify $R_{ISO}$'s value until the response is reasonable.

### 4.3.3 GAIN RESISTORS

Figure 4-10 shows a simple gain circuit with the INA's input capacitances at the feedback inputs ($V_{REF}$ and $V_{FG}$). These capacitances interact with $R_G$ and $R_F$ to modify the gain at high frequencies. The equivalent capacitance acting in parallel to $R_G$ is $C_G = C_{DM} + C_{CM}$ plus any board capacitance in parallel to $R_G$. $C_G$ will cause an increase in $G_{DM}$ at high frequencies, which reduces the phase margin of the feedback loop (i.e., reduce the feedback loop's stability).

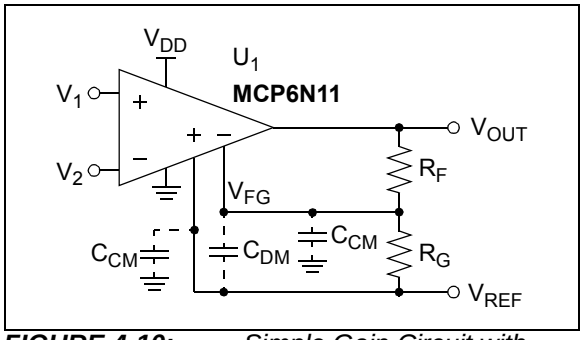



***FIGURE 4-10:*** *Simple Gain Circuit with Parasitic Capacitances.*

In this data sheet, $R_F + R_G = 10\ k\Omega$ for most gains (0Ω for $G_{DM} = 1$); see Table 1-6. This choice gives good Phase Margin. In general, $R_F$ (Figure 4-10) needs to meet the following limits to maintain stability:

**EQUATION 4-12:**

For $G_{DM}$ = 1:

$$R_F = 0$$

For $G_{DM}$ > 1:

$$R_F < \frac{\alpha G_{DM}^2}{2\pi f_{GBWP} C_G}$$

Where:

$\alpha \leq 0.25$

$G_{DM} \geq G_{MIN}$

$f_{GBWP}$ = Gain Bandwidth Product

$C_G = C_{DM} + C_{CM}$ + (PCB stray capacitance)

### 4.3.4 SUPPLY BYPASS

With these INAs, the power supply pin ($V_{DD}$ for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. Surface mount, multilayer ceramic capacitors, or their equivalent, should be used.

These INAs require a bulk capacitor (i.e., 1.0 µF or larger) within 100 mm, to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts as long as crosstalk through the supplies does not prove to be a problem.


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## 4.4 Typical Applications

### 4.4.1 HIGH INPUT IMPEDANCE DIFFERENCE AMPLIFIER

Figure 4-11 shows the MCP6N11 used as a difference amplifier. The inputs are high impedance and give good CMRR performance.

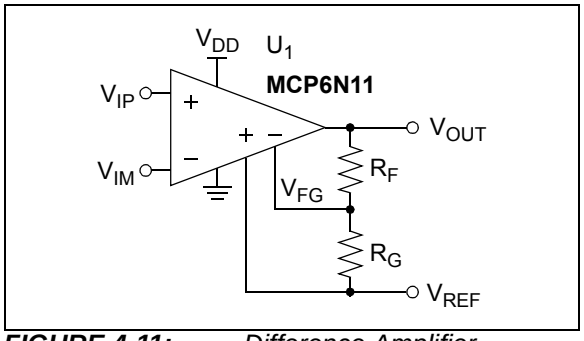



***FIGURE 4-11:*** *Difference Amplifier.*

### 4.4.2 DIFFERENCE AMPLIFIER FOR VERY LARGE COMMON MODE SIGNALS

Figure 4-12 shows the MCP6N11 INA used as a difference amplifier for signals with a very large common mode component. The input resistor dividers ($R_1$ and $R_2$) ensure that the voltages at the INA's inputs are within their range of normal operation. The capacitors $C_1$, with the parasitic capacitances $C_2$ (the resistors' parasitic capacitance plus the INA's input common mode capacitance, $C_{CM}$), set the same division ratio, so that high-frequency signals (e.g., a step in voltage) have the same gain. Select the INA gain to compensate for $R_1$ and $R_2$'s attenuation. Select $R_1$ and $R_2$'s tolerances for good CMRR.

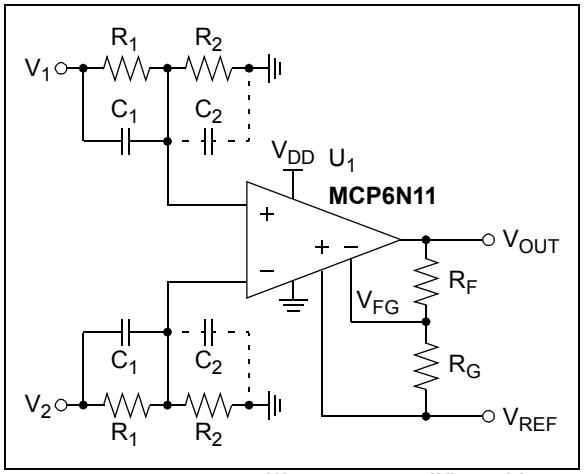
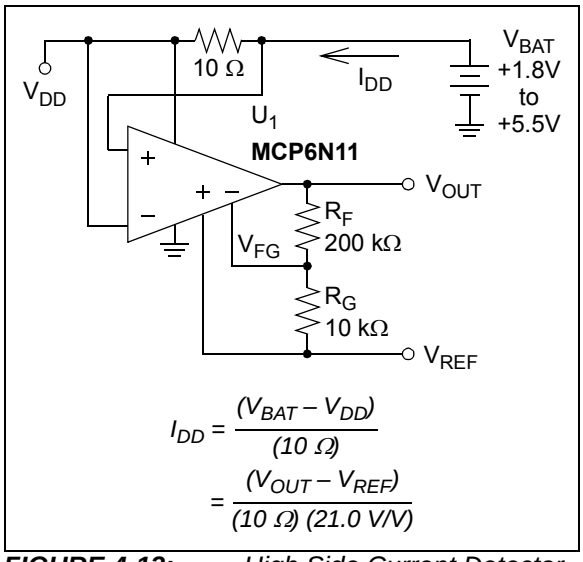



***FIGURE 4-12:*** *Difference Amplifier with Very Large Common Mode Component.*

### 4.4.3 HIGH SIDE CURRENT DETECTOR

Figure 4-13 shows the MCP6N11 INA used as to detect and amplify the high side current in a battery powered design. The INA gain is set at 21 V/V, so $V_{OUT}$ changes 210 mV for every 1 mA of $I_{DD}$ current. The best $G_{MIN}$ option to pick would be a gain of 10 (MCP6N11-010).




$$I_{DD} = \frac{(V_{BAT} - V_{DD})}{(10\ \Omega)} = \frac{(V_{OUT} - V_{REF})}{(10\ \Omega)\ (21.0\ V/V)}$$

***FIGURE 4-13:*** *High Side Current Detector.*

### 4.4.4 WHEATSTONE BRIDGE

Figure 4-14 shows the MCP6N11 single instrumentation amp used to condition the signal from a Wheatstone bridge (e.g., strain gage). The overall INA gain is set at 201 V/V. The best $G_{MIN}$ option to pick, for this gain, is 100 V/V (MCP6N11-100).

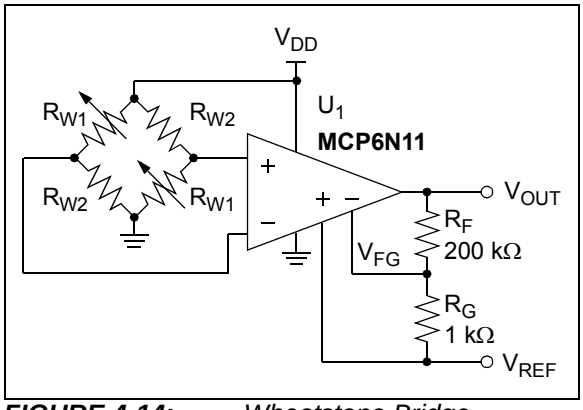



***FIGURE 4-14:*** *Wheatstone Bridge Amplifier.*

**NOTES:**


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## 5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6N11 instrumentation amplifiers.

### 5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase and Sampling of Microchip parts.

### 5.2 Analog Demonstration Board

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

### 5.3 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **AN884:** *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1228:** *"Op Amp Precision Design: Random Noise"*, DS01228

Some of these application notes, and others, are listed in the design guide:

- *"Signal Chain Design Guide"*, DS21825

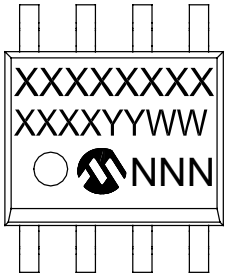
**NOTES:**


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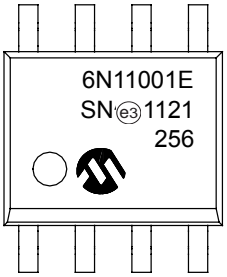
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

8-Lead SOIC (150 mil) **(MCP6N11)**




Example




**Note:** The example is for a MCP6N11-001 part.

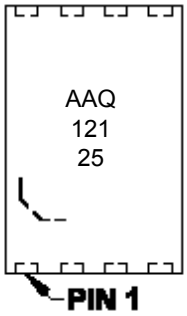
8-Lead TDFN (2×3) **(MCP6N11)**




| Device | Code |
|---|---|
| MCP6N11-001 | AAQ |
| MCP6N11-002 | AAR |
| MCP6N11-005 | AAS |
| MCP6N11-010 | AAT |
| MCP6N11-100 | AAU |

**Note:** Applies to 8-Lead 2x3 TDFN

Example

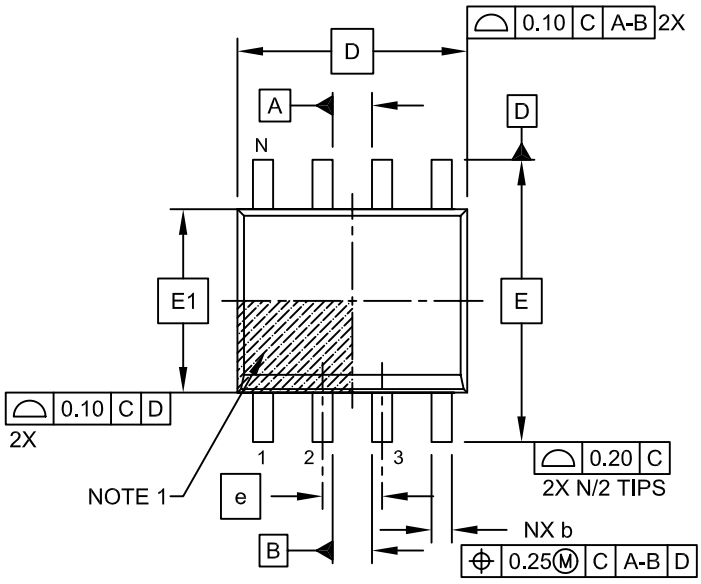



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

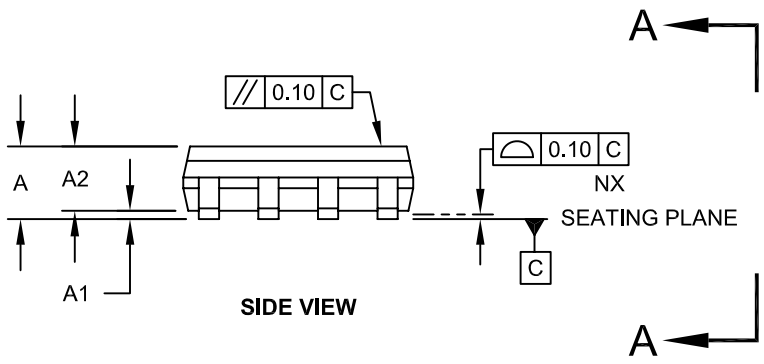
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

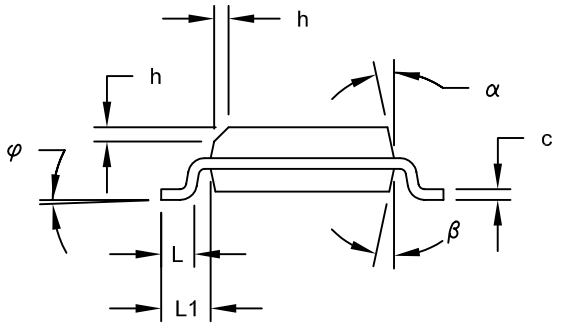
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**



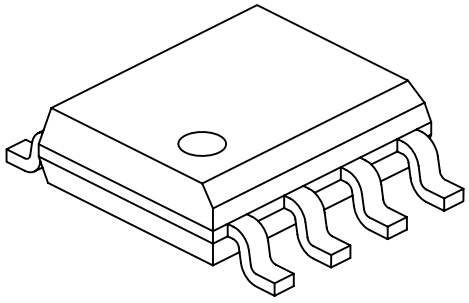

**VIEW A-A**

Microchip Technology Drawing No. C04-057C Sheet 1 of 2


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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | $\varphi$ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | $\alpha$ | 5° | - | 15° |
| Mold Draft Angle Bottom | $\beta$ | 5° | - | 15° |

**Notes:**

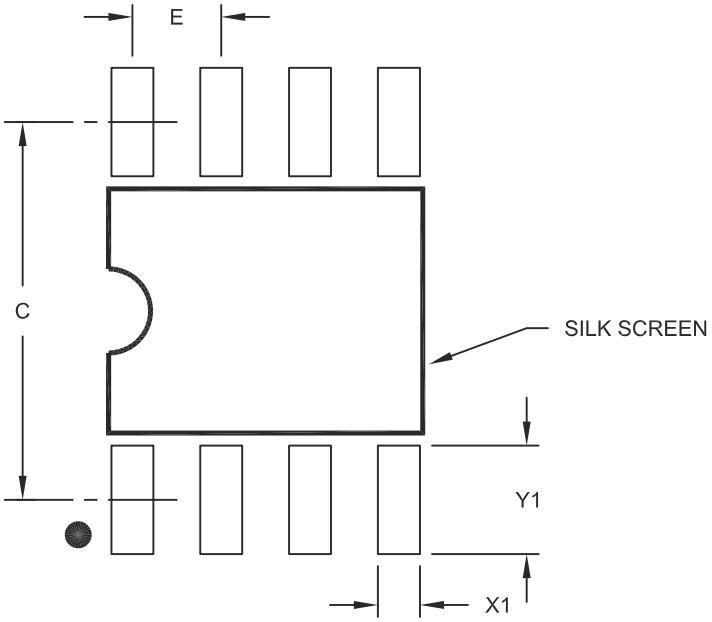
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

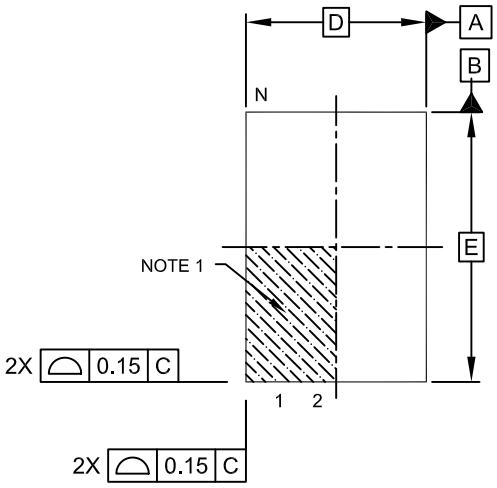
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

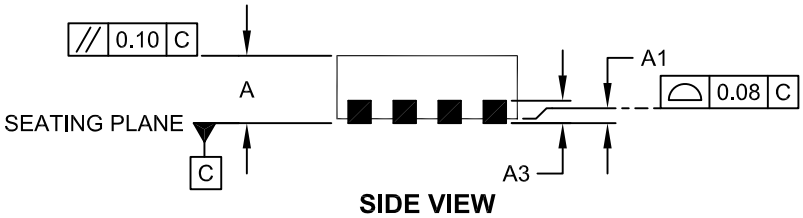

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## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

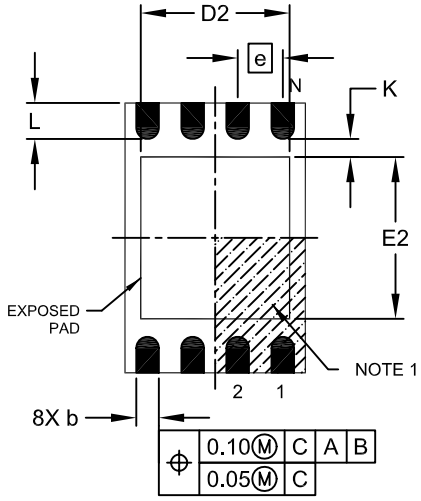
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**

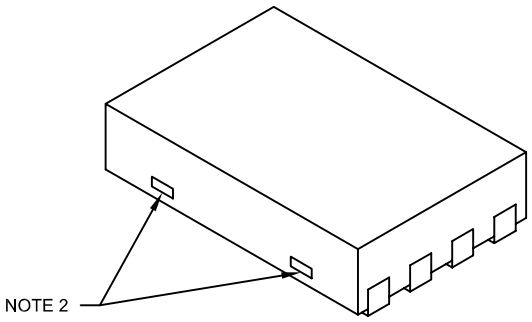



**BOTTOM VIEW**

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.20 | - | 1.60 |
| Exposed Pad Width | E2 | 1.20 | - | 1.60 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

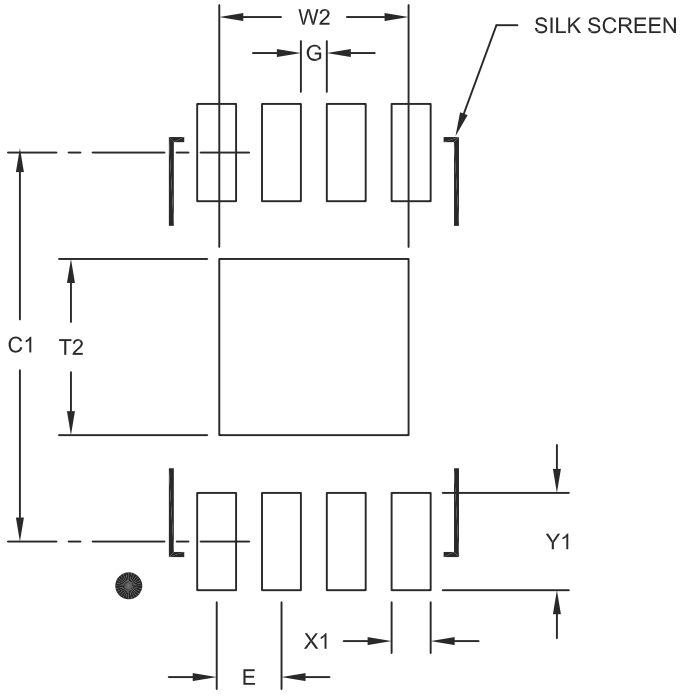
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2


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## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 1.46 |
| Optional Center Pad Length | T2 | | | 1.36 |
| Contact Pad Spacing | C1 | | 3.00 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

**NOTES:**


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# APPENDIX A: REVISION HISTORY

## Revision A (October 2011)

- Original Release of this Document.

**NOTES:**


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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | –X | X | /XX |
|---|---|---|---|
| Device | Gain Option | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP6N11 | Single Instrumentation Amplifier |
| | MCP6N11T | Single Instrumentation Amplifier (Tape and Reel) |
| Gain Option: | 001 = | Minimum gain of 1 V/V |
| | 002 = | Minimum gain of 2 V/V |
| | 005 = | Minimum gain of 5 V/V |
| | 010 = | Minimum gain of 10 V/V |
| | 100 = | Minimum gain of 100 V/V |
| Temperature Range: | E = | -40°C to +125°C |
| Package: | MNY = | 2×3 TDFN, 8-lead * |
| | SN = | Plastic SOIC (150mil Body), 8-lead |

* Y = nickel palladium gold manufacturing designator. Only available on the TDFN package.

**Examples:**

a) MCP6N11T-001E/MNY: Tape and Reel, Minimum gain = 1, Extended temperature, 8LD 2×3 TDFN.

b) MCP6N11-002E/SN: Minimum gain = 2, Extended temperature, 8LD SOIC.

**NOTES:**


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