

MCP651 Input Offset Evaluation Board User's Guide

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MCP651 INPUT OFFSET EVALUATION BOARD USER'S GUIDE

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MCP651 INPUT OFFSET EVALUATION BOARD USER'S GUIDE

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the MCP651 Input Offset Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- The Microchip Web Site
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the MCP651 Input Offset Evaluation Board. The manual layout is as follows:

- **Chapter 1. "Product Overview"** - Important information about the MCP651 Input Offset Evaluation Board.
- **Chapter 2. "Installation and Operation"** – Covers the initial set-up of the MCP651 Input Offset Evaluation Board. It lists the required tools, shows how to set up the board and how to connect lab equipment. It then demonstrates how to use this board.
- **Chapter 3. "Possible Modifications"** – Shows how to modify the board for other single Microchip op amps in SOIC-8, PDIP-8 and other packages.
- **Appendix A. "Schematics and Layouts"** – Shows the schematic and board layouts for the MCP651 Input Offset Evaluation Board.
- **Appendix B. "Bill Of Materials (BOM)"** – Lists the parts used to populate the MCP651 Input Offset Evaluation Board. Also lists loose parts shipped with the board in an ESD bag, alternate components and components not populated.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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RECOMMENDED READING

This user's guide describes how to use MCP651 Input Offset Evaluation Board. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources.

MCP6V01/2/3 Data Sheet, "*300 µA, Auto-Zeroed Op Amps*", DS22058

Gives detailed information on the op amp family that is used for signal processing and output voltage control on the MCP651 Input Offset Evaluation Board.

MCP651 Data Sheet, "*5 mA Op Amps with mCal*", DS22146

Gives detailed information on the op amp family that is used as the DUT on the MCP651 Input Offset Evaluation Board.

AN1177 Application Note, "*Op Amp Precision Design: DC Errors*", DS01177

Discusses how to achieve high DC accuracy in op amp circuits. Also discusses the relationship between an op amp's input offset voltage (V_{OS}), CMRR, PSRR, Open-Loop Gain and V_{OS} Drift over Temperature.

AN1258 Application Note, "*Op Amp Precision Design: PCB Layout Techniques*", DS01258

Discusses how to lay out PCBs for high DC accuracy in op amp circuits. Also discusses other PCB related accuracy issues.

8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board User's Guide, DS51544

Covers the usage of the SOIC8EV Evaluation Board.

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
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- Technical Support
- Development Systems Information Line

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Technical support is available through the web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (May 2009)

- Initial Release of this Document.

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Chapter 1. Product Overview

1.1 INTRODUCTION

The MCP651 Input Offset Evaluation Board is described by the following:

- Assembly # : 102-00258-R2
- Order # : MCP651EV-VOS
- Name: MCP651 Input Offset Evaluation Board

Items discussed in this chapter include:

- Kit Contents
- Intended Use
- Description

1.2 KIT CONTENTS

- One MCP651 Input Offset Evaluation Board, 102-00258-R2
- Important Information "Read First"



FIGURE 1-1: *MCP651 Input Offset Evaluation Board Kit Contents.*

1.3 INTENDED USE

The MCP651 Input Offset Evaluation Board is intended to provide a simple means to measure the MCP651 Input Offset Evaluation Board op amp's input offset voltage under a variety of operating conditions. The measured input offset voltage (V_{OST}) includes the input offset voltage specified in the data sheet (V_{OS}) plus changes due to: power supply voltage (PSRR), common mode voltage (CMRR), output voltage (A_{OL}), input offset voltage drift over temperature ($\Delta V_{OS}/\Delta T_A$) and 1/f noise.

The MCP651 Input Offset Evaluation Board works most effectively at room temperature (near 25°C). Measurements at other temperatures should be done in an oven where the air velocity is minimal.

1.4 DESCRIPTION

This section starts with the conversion of DUT bias voltages described in the MCP651 data sheet to the voltages on this board. Then there is a discussion of the circuitry that controls the DUT's output voltage (V_{OUTX}) and amplifies its total input offset voltage (V_{OST}). Finally, other portions of the circuit, and their purpose, are discussed. Complete details of this board are given in **Appendix A. "Schematics and Layouts"** and **Appendix B. "Bill Of Materials (BOM)"**.

1.4.1 Conversion of Bias Voltages

The MCP651 data sheet describes all of its bias voltages relative to V_{SS}, which is assumed to be at ground (0V). On the other hand, the MCP651 Input Offset Evaluation Board sets the DUT's input common mode voltage to 0V. The user needs to convert from the first set of voltages to the second set (by subtracting V_{CM}):

TABLE 1-1: CONVERSION OF BIAS VOLTAGES

Data Sheet Bias Voltage (V)	Conversion Equations	Evaluation Board Bias Voltage (V)
V_{CM}	$V_{CM} - V_{CM}$	$V_{CMX} = 0V$
V_{DD}	$V_{DD} - V_{CM}$	V_{DDI}
V_{SS}	$V_{SS} - V_{CM}$	V_{SSI}
V_{OUT}	$V_{OUT} - V_{CM}$	V_{OUTX}
V_L	$V_L - V_{CM}$	V_{LX}
V_{CAL}	$V_{CAL} - V_{CM}$	V_{CALX}

The supply voltages V_{DDX} and V_{SSX} can be estimated using the MCP651's typical quiescent current (I_Q = 6 mA):

EQUATION 1-1:

$$V_{DDX} = V_{DDI} + I_Q(10\Omega) \approx V_{DDI} + 60\ mV$$
$$V_{SSX} = V_{SSI} - I_Q(10\Omega) \approx V_{SSI} - 60\ mV$$

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1.4.2 Simplified Circuit and Operation

Figure 1-2 is a simplified diagram of the circuitry that biases the DUT and produces an amplified version of the DUT's input offset voltage (V_{OST}). It includes gain at the input, a Proportional plus Integral (PI) controller loop, a high gain amplifier and a filter.

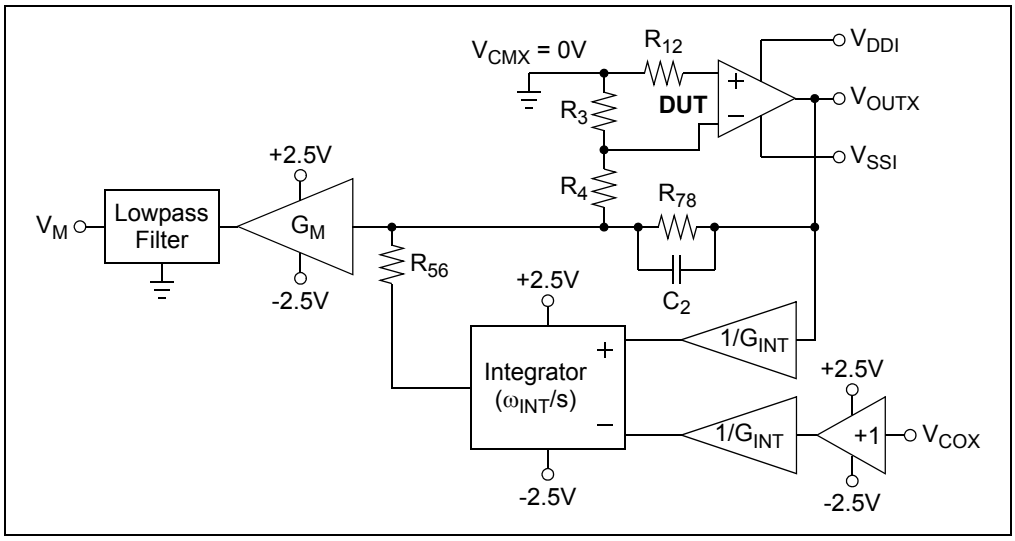


FIGURE 1-2: *Simplified Circuit.*

The elements of Figure 1-2 correspond to the components in the complete schematic (**A.3 "Board – Schematic"**) as follows.

TABLE 1-2: CONVERSION OF SCHEMATIC COMPONENTS

Complete Schematic Components	Simplified Schematic Component	Conversion Equations	Typical Values (Note 1)
R1, R2	R_{12}	= R1 || R2	≈ 196.1Ω
R3	R_3	= R3	≈ 200.0Ω
R4	R_4	= R4	≈ 10.00 kΩ
R5, R6	R_{56}	= R5 + R6	≈ 8.04 kΩ
R7, R8	R_{78}	= R7 + R8	≈ 40.0 kΩ
C2	C_2	= C2	≈ 22 nF
U1	"DUT"	—	—
U2	"+1 Buffer"	—	—
R11, R12	"$1/G_{INT}$"	= R11 / (R11 + R12)	≈ 1 / (3.213 V/V)
R13, R14		= R13 / (R13 + R14)	≈ 1 / (3.213 V/V)
U3, R11, R12, C6	"Integrator (ω_{INT}/s)"	ω_{INT} = 1 / ((R11 || R12)C6)	≈ 2π (10.3 Hz)
U3, R17, C7		ω_{INT}= 1 / (R17 · C7)	≈ 2π (10.4 Hz)
U4, R23, R24, R25, R26, S2	"G_M"	= 1 + R24 / R23	≈ 3.941 V/V, S2 closed
		= 1 + (R24 + R25 + R26) / R23	≈ 39.18 V/V, S2 open
R28, C12	"Lowpass Filter (ω_{BW})"	ω_{BW} = 1 / (R28 · C12)	≈ 2π (1.59 Hz)

Note 1: Switch S2's top position is closed when to the right (LOW GAIN), and is open when to the left (HI GAIN).

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Analysis of this simplified circuit gives the following nominal circuit outputs:

EQUATION 1-2:

$$V_{OUTX} \approx V_{COX}$$
$$V_M \approx G_A G_M V_{OST}$$

Where:

G_A = 1 + R4/R3 ≈ 51.00 V/V

$G_A G_M$ ≈ 201.0 V/V, S2 (position 1) closed

≈ 1998 V/V, S2 (position 1) open

R_1 and R_2 (R_{12}) balance the circuit at the DUT's input. These resistors are small, and are oriented on the Printed Circuit Board (PCB) to cancel their thermoelectric voltages. The parallel resistances $R_1||R_2$ and $R_3||R_4$ are equal to minimize the contribution of the DUT's input bias currents to the measured V_{OST} (contributions by R_5 through R_8 do not affect V_M); the typical value of I_{OS} at +125°C is ±100 pA, which produces a change in V_{OST} of ±0.02 µV.

The unity gain buffer (+1 gain on the bottom right) isolates the V_{COX} input filters from the following attenuator and integrator. Although it's not shown here, the resistor R14 at the input to the "+1 Buffer" ensures its output voltage is 0V when the V_{COX} connector is left open.

The attenuators ($1/G_{INT}$) scale V_{COX} and V_{OUTX} so that they do not overdrive op amps U2 and U3 ("+1 Buffer" and ("Integrator"). For instance, when V_{OUTX} = 5.6V (given V_{SSI} =0.3V and V_{DDI} = 5.8V), the voltages at the outputs of the attenuators ($1/G_{INT}$) is 1.80V.

The differential integrator accumulates the scaled difference between V_{COX} and V_{OUTX}, which slowly forces this difference to zero (the I part of the PI controller). Resistor R_{56} injects the integrator's output at the DUT's input through resistors R_4 and R_3; it minimizes the error at V_{OUTX}.

A proportional term (the P part of the PI controller) is also injected at the DUT's input through resistor R_{78}; it stabilizes the control loop (the integrator term becomes negligible above 16 Hz). It also sets a low frequency DUT noise gain of about 505 V/V. This proportional term is rolled off by C_2 starting at 0.18 kHz; this is high enough to not interact with the integrator term, and low enough to keep the DUT stable. Thus, C_2 minimizes noise gain at higher frequencies, which reduces the chance of unwanted feedback effects.

With the overall gain $G_A G_M$ of either 201 V/V or 1998 V/V, this circuit can measure V_{OST} values up to either ±12.4 mV or ±1.25 mV. A voltmeter with 1 mV resolution can distinguish steps of either 5 µV or 0.5 µV, respectively.

The DUT's noise seen at the input to G_M has a noise power bandwidth (NPBW) set by R_{78} and C_2 (0.28 kHz). This implies that this noise is dominated by the 1/f noise. The Lowpass Filter (f_{BW} ≈ 1.6 Hz) reduces this 1/f noise a little more before it is seen at V_M. The measured noise, over a 140 second period of time with a typical part, was about 19 μV_{P-P} referred to input (RTI). This compares favorably with the MCP651's calibrated V_{OS} specification (±200 µV, maximum at +25°C).

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1.4.3 DUT Bias Voltage Inputs

Figure 1-3 shows the basic DUT biasing circuitry, except the input pins which have already been discussed (V_{CMX} = 0V).

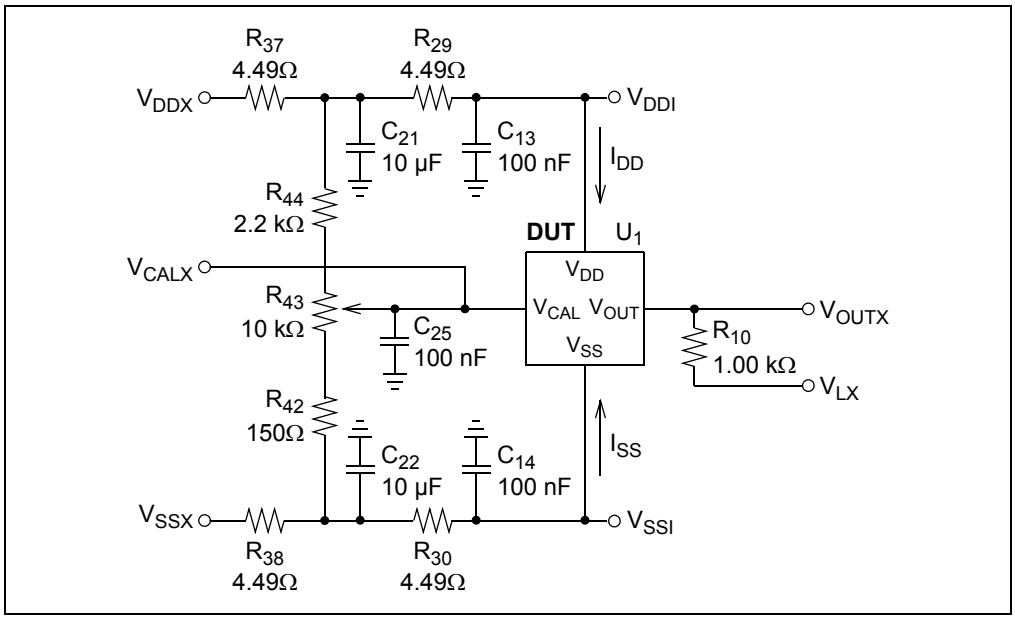


FIGURE 1-3: *DUT Bias Circuitry.*

Lab power supplies are connected to V_{DDX} and V_{SSX}. The resistors R_{29}, R_{30}, R_{37} and R_{38}, along with the capacitors C_{13}, C_{14}, C_{21} and C_{22}, minimize crosstalk from the other op amps on the board. Since the MCP651's quiescent current is between 3 mA and 9 mA, the actual power supply voltages (V_{DDI} and V_{SSI}) are different by 30 mV to 90 mV. I_{DD} and I_{SS} can be calculated as (I_{SS} is negative):

EQUATION 1-3:

$$I_{DD} = \frac{V_{DDX} - V_{DDI}}{10\Omega}$$

$$I_{SS} = \frac{V_{SSX} - V_{SSI}}{10\Omega}$$

The DUT's V_{CAL} pin sets its internal common mode voltage (V_{CMX} of the MCP651) when it is in calibration mode. Thus, the DUT's offset (V_{OS}) is small when V_{CMX} (0V on this board) is equal to V_{CALX}.

The RCAL potentiometer (POT or R43), with the resistors R_{42} and R_{43}, sets V_{CALX}. The values chosen allow the POT to cover the specified V_{CALX} range, and a little more. Connecting a voltmeter to V_{CALX} makes it possible to set the POT accurately. Notice that it is also possible to drive V_{CALX} with an external voltage source (the wiper should be, but doesn't have to be, at mid-range).

V_{OUTX} is set, as previously explained, to be equal to V_{COX} by the integrator in the PI control loop. If V_{COX} is at or beyond V_{SSI} or V_{DDI}, then the loop forces V_{OUTX} to be railed at the corresponding supply voltage.

The load resistor (R_L or R_{10}) is biased to the externally supplied voltage V_{LX}. V_{LX} is usually set to mid-supply. The V_{LX} connection can be left open, which minimizes the loading on V_{OUTX} (about 40 kΩ).

1.4.4 CAL Input

The DUT's CAL/$\overline{CS}$ input pin is normally held at V_{SSX} by resistors R_{20} and R_{21}; this keeps the MCP651 in its normal mode of operation. When S_1 is closed by the user, R_{20} pulls CAL/$\overline{CS}$ up to V_{DDX} (after a time set by R_{20} and C_9), so that the MCP651 enters its low power mode of operation. Releasing S_1 then brings CAL/$\overline{CS}$ back to V_{SSX} (after a time set by R_{20}, R_{21} and C_9); the time constant $(R_{20} + R_{21})C_9$ is 0.11s, which is slow enough to de-glitch S_1. Note that the supply voltages need to be constant while the DUT is being put into calibration mode, and during calibration mode (up to 4 ms of time after CAL/$\overline{CS}$ goes low).

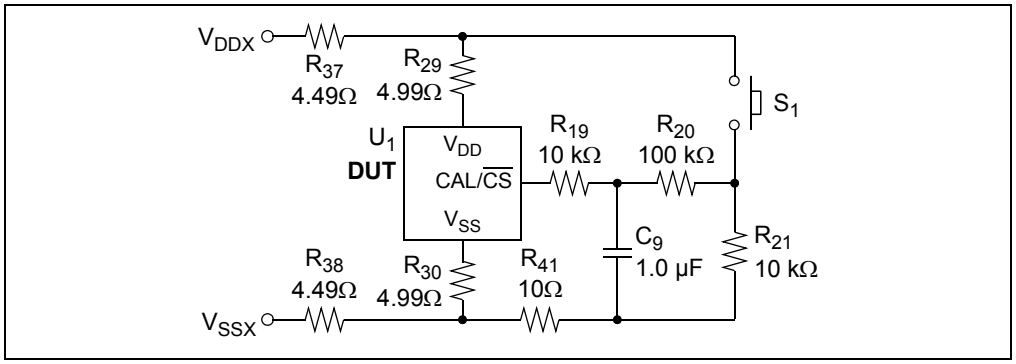


FIGURE 1-4: *CAL Switch and De-glitching Circuitry.*

1.4.5 Bias Inputs for Other Op Amps

The other op amps (U_2, U_3 and U_4) are run on dual power supplies centered on ground. The design assumes that these supplies are ±2.5V, for the best performance. These supplies can be set as low as ±0.9V, which will keep the MCP6V01's working, but will reduce the range of possible V_{COX} and V_M values.

1.4.6 Outputs

The connector V_{CALX} outputs the voltage set by the POT RCAL. V_{DDI} and V_{SSI} are used to measure the actual DUT supply voltages, and to estimate its supply currents I_{DD} and I_{SS}. V_{OUTX} is the DUT's output voltage; it is used only to verify that the circuit is operating correctly. V_M is the most important output; it is V_{OST} multiplied by either 201 V/V or 1998 V/V.

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Chapter 2. Installation and Operation

2.1 INTRODUCTION

This chapter shows how to set up and operate the MCP651 Input Offset Evaluation Board. Items discussed in this chapter include:

- Required Tools
- Configuring the Lab Equipment and PCB
- Operating Conditions
- Calculating DUT Parameters
- Settling Time, Noise, and Sampling Rate

2.2 REQUIRED TOOLS

- (1 or 2) Lab Power Supplies with (two) tracking outputs
  - One for +2.5V, GND -2.5V
  - The other for V_{DDX}, GND, V_{SSX} (adjustable up to ±7.0V; optional if V_{DDX} = 2.5V and V_{SSX} = -2.5V)
- (0 to 3) independent Lab Power Supplies
  - Drive V_{CALX}, V_{LX} and V_{COX} (any or all of these can be not used, as described in the next section)
  - Adjustable up to ±7.0V
- (1 or 2) Voltmeters
  - Measure V_M, V_{OUTX} (the latter is for troubleshooting only)
  - 1 mV resolution
  - -6V to +6V minimum range
  - Differential measurement (e.g., hand held meter)

2.3 CONFIGURING THE LAB EQUIPMENT AND PCB

Lab equipment is connected to this board as shown in Figure 2-1. The (surface mount) test points allow lab equipment to be connected to these boards.

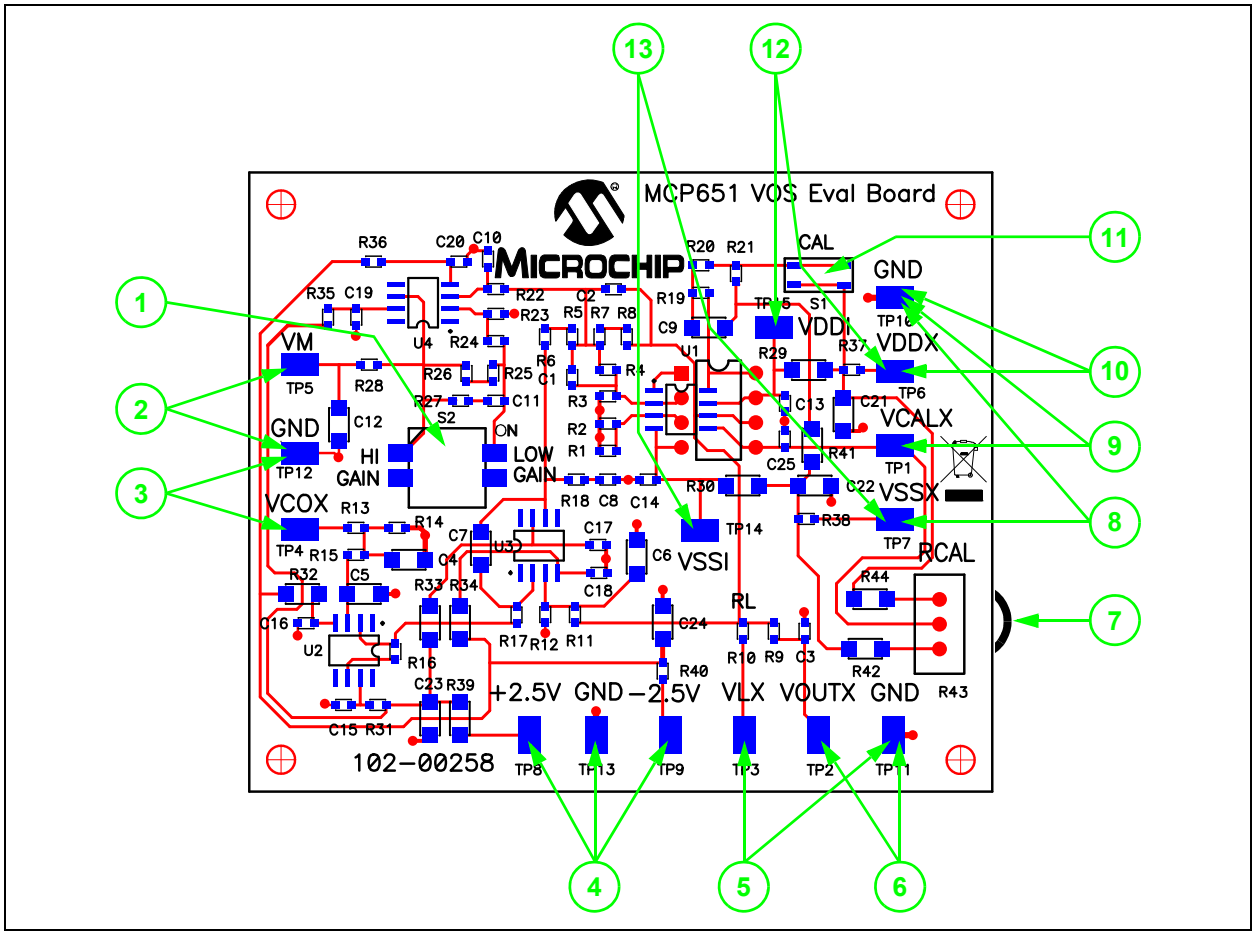


FIGURE 2-1: *Lab Equipment Connections and Configuration Switches for the MCP651 Input Offset Evaluation Board.*

The arrows and numbers in Figure 2-1 signify the following:

1. Gain Setting Switch – top position (# 1)
   a) To the right (ON) for low gain (G_M = 201 V/V).
   b) To the left for high gain (G_M = 1998 V/V).
2. Voltmeter to measure VM
   a) Gives amplified offset ($G_A G_M V_{OST}$).
3. Power Supply for VCOX
   a) Can be left open (forces VOUTX = 0V).
   b) Set between VSSI and VDDI.
4. ±2.5V Power Supplies with GND
   a) Set at +2.5V and -2.5V (for best performance).
5. Power Supply for VLX (Load Resistor's bias point)
   a) Can be left open (fewer lab power supplies; R_L = 40 kΩ).
   b) Can be shorted to GND with a jumper wire (VLX = 0V and R_L = 1 kΩ).
   c) Can connect to an external lab power supply (R_L = 1 kΩ).

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6. Voltmeter to measure VOUTX
   a) Typically not used (mainly used for validating DUT and board).
7. POT (RCAL) Thumb-wheel (to adjust VCALX)
   a) Rotate clockwise (CW) to increase VCALX.
   b) Rotate counter-clockwise (CCW) to decrease VCALX.
   c) Usually set at mid-turn.
   d) Can override with an external power supply at VCALX or a jumper wire (see # 9 below)
8. Power Supply for VSSX
   a) Minimum of about VDDX – (DUT's maximum operating supply voltage) – (0.12V for the resistors in the supply line).
   b) Maximum of +0.3V (for V_{CMX} at 0.3V below negative rail).
   c) When VSSX = -2.5V and VDDX = +2.5V, you can connect to the -2.5V supply with a jumper wire (fewer lab power supplies).
9. Power Supply for VCALX
   a) Usually not connected (RCAL sets V_{CALX}; fewer lab power supplies).
   b) Can be shorted to GND with a jumper wire (fewer lab power supplies; $V_{CALX} = V_{CMX} = 0V$).
   c) Can connect to an external lab power supply (it is best, but not necessary, to set RCAL to mid-supply).
10. Power Supply for VDDX
    a) Minimum of -0.3V (for V_{CMX} at 0.3V above positive rail).
    b) Maximum of about VSSX + (DUT's maximum operating supply voltage) + (0.12V for the resistors in the supply line).
    c) When VSSX = -2.5V and VDDX = +2.5V, you can connect to the +2.5V supply with a jumper wire (fewer lab power supplies).
11. CAL Switch
    a) Press to initiate calibration sequence (corrects DUT's V_{OST}, with internal common mode voltage set to VCALX).
    b) There is a delay of about 4 ms for the calibration to complete, plus several tenths of a second for the circuit to settle.
12. Voltmeter at VDDI and VDDX (to measure I_{DD})
    a) Measure $\Delta V = V_{DDX} - V_{DDI}$.
    b) Calculate $I_{DD} = \Delta V / (10\Omega)$
13. Voltmeter at VSSI and VSSX (to measure I_{SS})
    a) Measure $\Delta V = V_{SSX} - V_{SSI}$.
    b) Calculate $I_{SS} = \Delta V / (10\Omega)$; (this is a negative value)

Note: For the best accuracy and ease of use, short VCALX to GND, set the other voltages for the desired bias during calibration, then initiate a calibration event in the DUT (push S1). Change the bias point afterwards to see how V_{OST} is changed.

2.4 OPERATING CONDITIONS

The MCP651 Input Offset Evaluation Board works most effectively at room temperature (near 25°C). Measurements at other temperatures should be done in an oven where the air velocity is minimal. Table 2-1 shows the various DUT voltages (as described in the data sheet), their nominal values and ranges, and how to convert to the voltages needed on the MCP651 Input Offset Evaluation Board.

TABLE 2-1: CONVERTING VOLTAGES FOR THE BOARD

Single Supply Voltages (V)			Conversion Equations (V)
Data Sheet Symbol	Nominal	Range	
V_{DD}	2.5 or 5.5	2.5 to 5.5	$V_{DDX} \leftarrow V_{DD} - V_{CM}$
V_{SS}	0	0	$V_{SSX} \leftarrow V_{SS} - V_{CM}$
V_{CM}	$V_{DD}/3$	V_{SS} – 0.3 to V_{DD} – 1.3 **(Note 1)**	$0 \leftarrow V_{CM} - V_{CM}$
V_{OUT} **(Note 2)**	$V_{DD}/2$	V_{SS} + 0.2 to V_{DD} – 0.2	$V_{OUTX} \leftarrow V_{OUT} - V_{CM}$
V_L	$V_{DD}/2$	V_{SS} to V_{DD}	$V_{LX} \leftarrow V_L - V_{CM}$
V_{CAL}	$V_{DD}/3$ **(Note 3)**	V_{SS} + 0.1 to V_{DD} – 1.4	$V_{CALX} \leftarrow V_{CAL} - V_{CM}$
CAL/$\overline{CS}$	V_{SS}	V_{SS} to V_{DD}	**(Note 4)**

Note 1: At T_A = +25°C. See the data sheet for changes in V_{CM} range vs. T_A.

2: Set the desired V_{OUT} voltage at the V_{COX} input; the integrator then forces V_{OUT} to be the same voltage.

3: When the V_{CAL} pin left open. However, this board always has the POT (R43) connected, so V_{CALX} is never truly open.

4: The circuit forces CAL/$\overline{CS}$ to stay within its range (as long as the supply voltages are constant when the CAL switch is activated). Normally, the part is on.

5: These numbers are for the MCP651 op amp.

Once the MCP651 Input Offset Evaluation Board is powered up, the switches can be set for the desired operation. S1 (a normally off push-button switch) starts a calibration event (CAL), internal to the DUT, when pushed. S2 (top position) sets the gain of the amplifier (G_M) either high or low. See Table 2-2 for details.

TABLE 2-2: SWITCH OPERATION

Switch	Input	Result
S1	No Input	Normal Operation
	Pushed	Calibration event started in DUT
S2	Top Switch to the left	High Gain (1998 V/V)
	Top Switch to the right	Low Gain (201 V/V)
	(Bottom Switch)	(Don't Care)

The gain is usually set low. It can be set high just after a calibration event, before changing the DUT's bias point, to obtain more accurate results for the calibrated offset voltage.

The POT (R_{CAL} or R_{43}) adjusts V_{CALX}. This voltage is where the DUT's common mode input voltage set during a calibration event (initiated by pushing S1). Adjusting this POT does not have an effect on the circuit's behavior until the CAL switch (S1) is pushed.

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2.5 CONVERTING TO OTHER PARAMETERS

2.5.1 Calculating DUT Parameters

The DUT's total input offset voltage (V_{OST}) can be calculated from a measurement as shown in Equation 2-1.

EQUATION 2-1:

$$V_{OST} = V_M / (G_A G_M)$$

Changing the DUT's bias voltages or ambient temperature changes V_{OST}. Microchip's application note AN1177 discusses in detail how these changes in V_{OST} are related to specifications found in our data sheets. The following list summarizes the results:

- Specified Input Offset Voltage:
  - V_{OS} = Input offset at the specified bias point
- DC Common Mode Rejection Ratio:
  - CMRR = $\Delta V_{CM}/\Delta V_{OS}$
- DC Power Supply Rejection Ratio:
  - PSRR = $(\Delta V_{DD} - \Delta V_{SS})/\Delta V_{OS}$
- DC Open-loop Gain:
  - $A_{OL} = \Delta V_{OUT}/\Delta V_{OS}$
- Input Offset Drift over Temperature:
  - $\Delta V_{OS}/\Delta T_A$

Note: The data sheet Input Offset Voltage (V_{OS}) specification applies to one bias point and temperature only. The total input offset voltage (V_{OST}) includes V_{OS} and changes in input offset as bias voltages and temperature change.

Example 2-1 gives an example of how V_{OST} changes with the common mode input voltage (V_{CM}).

EXAMPLE 2-1: COMMON MODE CHANGE EXAMPLE

Given:

V_{OST} = 0.5 mV, V_{CM} = 0V
V_{OST} = 1.0 mV, V_{CM} = 5V

Then:

ΔV_{OST} = 0.5 mV
ΔV_{CM} = 5.0V
CMRR = 5.0V / 0.5 mV
= 10 V/mV
= 80 dB

2.5.2 Application

Table 2-3 shows one possible measurement matrix that will allow the user to estimate key parameters for the DUT. Obviously, other values of V_{DD} and V_{CAL} could be selected.

TABLE 2-3: MEASUREMENT MATRIX

Operating Inputs						Measurement (Note 1)
T_A (°C)	V_{DD} (V)	V_{OUT} (V)	V_{CM} (V)	G_M (V/V)	Symbol	Comments
+25	5.5	2.75	1.83	40	V_{M1}	V_{OS} and PSRR
			-0.30	4	V_{M2}	CMRR
			4.20		V_{M3}	CMRR
		0.20	1.83		V_{M4}	A_{OL}
		5.30			V_{M5}	A_{OL}
	2.5	1.25	0.83		V_{M6}	V_{OS} and PSRR
			-0.30		V_{M7}	CMRR
			1.20		V_{M8}	CMRR
		0.20	0.83		V_{M9}	A_{OL}
		2.30			V_{M10}	A_{OL}
-40	5.5	2.75	1.83		V_{M11}	V_{OS} at temperature and $\Delta V_{OS}/\Delta T_A$
+85					V_{M12}	
+125					V_{M13}	

Note 1: Before making these measurements, set up the DUT to the bias point described for V_{M1}. Short V_{CALX} to GND. Then start a calibration (CAL) event using S1. Measure V_{M1}, then alter the operating conditions for each succeeding measurement; do not initiate another calibration event until all measurements are done.

Based on these measurements, we can make the following estimates, where the V_{OST_k} values are calculated from the measured V_{Mk} values (see Equation 2-1):

TABLE 2-4: ESTIMATES

Operating Inputs		Estimates	
V_{DD} (V)	T_A (°C)	Equations	Units
1.8 and 5.5	+25	$1/PSRR = (V_{OST_1} - V_{OST_6}) / (3.0V)$	µV/V
5.5	-40	$V_{OS} = V_{OST_11}$	µV
	+25	$V_{OS} = V_{OST_1}$	µV
	+85	$V_{OS} = V_{OST_12}$	µV
	+125	$V_{OS} = V_{OST_13}$	µV
	-40 to +125	$\Delta V_{OS}/\Delta T_A = (V_{OST_13} - V_{OST_11}) / (165°C)$	µV/°C
	+25	$1/CMRR = (V_{OST_3} - V_{OST_2}) / (4.5V)$	µV/V
		$1/A_{OL} = (V_{OST_5} - V_{OST_4}) / (5.1V)$	µV/V
1.8	+25	$V_{OS} = V_{OST_6}$	µV
		$1/CMRR = (V_{OST_8} - V_{OST_7}) / (1.5V)$	µV/V
		$1/A_{OL} = (V_{OST_10} - V_{OST_9}) / (2.1V)$	µV/V

Obviously, other values of T_A, V_{DD}, … can be used instead, with the proper adjustments to these equations.

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2.6 SETTLING TIME, NOISE AND SAMPLING RATE

The bandwidth seen by the signal (DUT's V_{OST} and noise voltage), between the DUT's input and VM, is set mainly by the lowpass filter at the VM test point (TP5); this bandwidth is about 1.6 Hz. This bandwidth sets the settling time seen at VM (after the DUT's bias point has been changed) to about 0.6 seconds.

The noise seen in the measurements is a result of DUT's input noise voltage passed through the same 1.6 Hz lowpass filter. The MCP651's 1/f noise dominates at such low frequencies, so V_{OST} will appear to wander over time. The standard deviation of this 1/f wander can be estimated to be roughly:

- 5 μV_{P-P} for a time period of 1 second
- 34 μV_{P-P} for a time period of 10 years

Averaging several measurements together will help reduce the noise over a short period of time. It must be understood, however, that the 1/f noise will make V_{OST} appear to change over long periods of time.

There is a practical limit on increasing the sample rate; the noise does not improve significantly after a certain point. The analog lowpass pole at 1.6 Hz causes closely spaced samples to be correlated. To avoid the overhead caused by sampling too fast, keep the sampling period near or above the pole's time constant (0.10s); this gives a minimum sample rate of 10 samples per second.

Note: Sampling much faster than 10 SPS will not improve the averaged noise significantly.

NOTES:

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Chapter 3. Possible Modifications

3.1 INTRODUCTION

This chapter shows how to modify the MCP651 Input Offset Evaluation Board to measure other single op amps from Microchip Technology Inc. Items discussed in this chapter include:

- Range of Parts Supported by the MCP651 Input Offset Evaluation Board
- Changes to Accommodate Other DUTs

3.2 RANGE OF PARTS SUPPORTED BY MCP651 INPUT OFFSET EVALUATION BOARD

Only op amps that fall within a certain performance range are supported by the MCP651 Input Offset Evaluation Board.

3.2.1 Input Offset Voltage

In order to keep op amps U3 and U4 operating normally, the DUT's V_{OS} must be:

EQUATION 3-1:

$$V_{OS} < \pm 12.4\ mV, \quad Low\ Gain$$
$$V_{OS} < \pm 1.25\ mV, \quad High\ Gain$$

Where:

Low Gain = 201 V/V
High Gain = 1998 V/V

More accurate op amps need higher gain for good resolution. Table 3-1 shows what V_{OS} specs can be supported for different voltmeter resolutions and amplifier gains.

TABLE 3-1: LOWER LIMIT ON V_{OS} RANGE (NOTE 1)

Voltmeter Resolution (mV)	$G_A G_M$ (V/V)	$max(V_{OS}) \geq$ (±µV)
1 mV	201 (low gain)	500
	1998 (high gain)	50
0.1 mV	201 (low gain)	50
	1998 (high gain)	5 **(Note 2)**

Note 1: These results assume a minimum measurement resolution of 1% of the V_{OS} range.

2: The DUT needs to be soldered to the PCB when the maximum V_{OST} is less than ±50 µV, or so. Inserting a PDIP-8 part into a 8-pin socket creates a contact potential (error) of the order of ±1 µV. Also, 1/f noise needs to be low.

3.2.2 Output Headroom

The DUT's output headroom needs to be close enough to 0V to not overdrive U2 or U3. The maximum DUT V_{OH} and V_{OL} values supported (relative to V_{CM}) are:

EQUATION 3-2:

$$V_{OH} - V_{CM} \leq 7.5V$$
$$V_{CM} - V_{OL} \leq 7.5V$$

Rail-to-rail output op amps, on a single supply voltage, must be less than 7.5V.

3.2.3 Gain Bandwidth Product

There is a minimum Gain Bandwidth Product (GBWP) to keep the feedback loop stable, and a maximum GBWP to avoid crosstalk and other issues.

EQUATION 3-3:

$$500\ kHz \leq GBWP \leq 100\ MHz$$

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3.3 CHANGES TO ACCOMMODATE OTHER DUTS

This section focuses on methods to connect to other DUTs; the circuit's design is not changed. Parts information can be found in **Appendix B. "Bill Of Materials (BOM)"**.

3.3.1 Pinout

Figure 3-1 shows the MCP651 op amp's pinout. This is the standard 8-lead pinout, except for pins 5 and 8 (V_{CAL} and CAL/$\overline{CS}$). The MCP651 Input Offset Evaluation Board is designed to take advantage of these input pins, but they are not necessary to this board's operation.

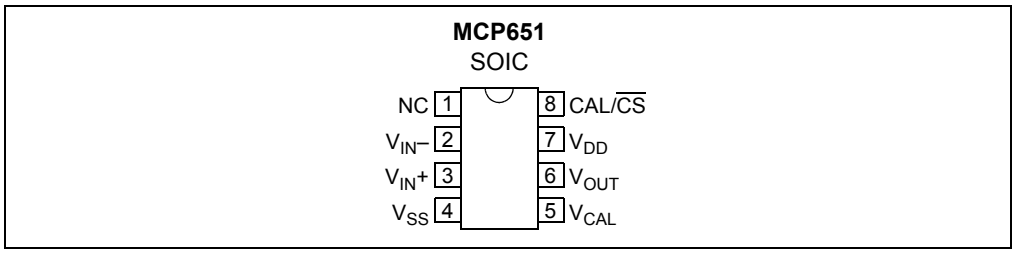


FIGURE 3-1: *MCP651 Pinout.*

Op Amps with No Connection (NC) at pins 1, 5 and 8 will operate properly on the MCP651 Input Offset Evaluation Board. Other op amps may need to use an adaptor board; see **Section 3.3.5 "Other Single Op Amps"**.

3.3.2 Removing the DUT

Since these boards come with the DUT (in SOIC-8) soldered on, it is necessary to de-solder them. Figure 3-2 shows the location of the DUT for either a SOIC-8 or a PDIP-8 package. A good de-soldering station makes this work much easier to do.

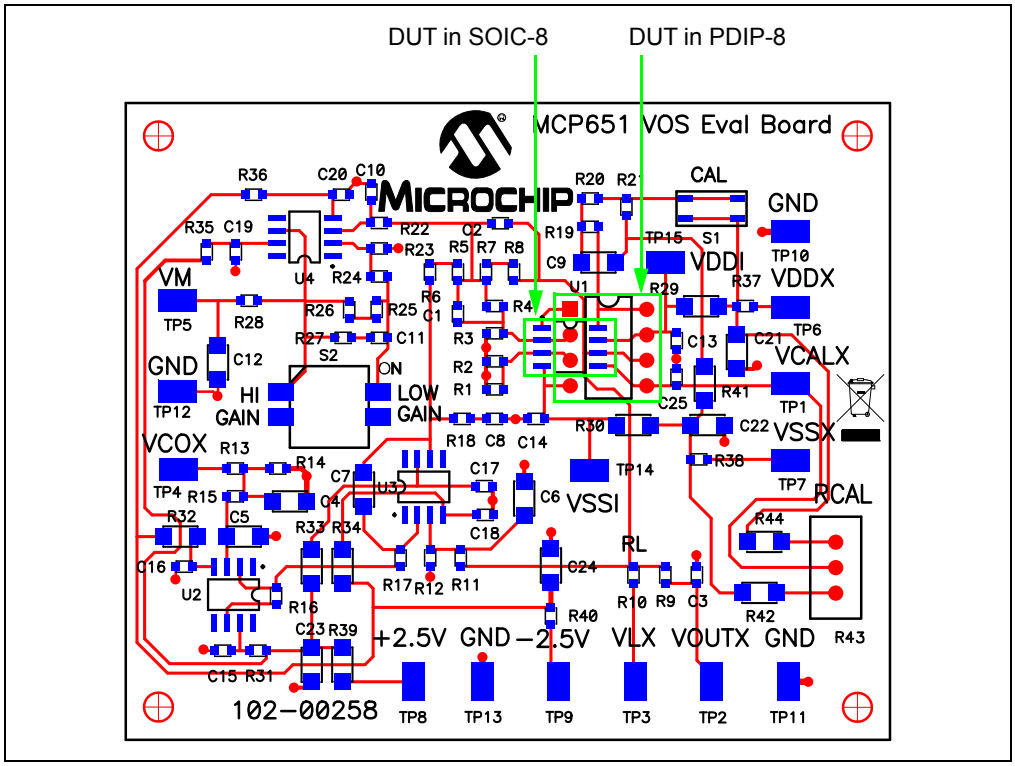


FIGURE 3-2: *DUT's Location on the PCB.*

3.3.3 Single Op Amps in SOIC-8 Package

Solder onto the SOIC-8 pad shown in Figure 3-2. Pin 1 is on the top left (next to the U1 label). To avoid soldering and de-soldering many times, for slower parts, it may be better to use the option discussed in **Section 3.3.5 "Other Single Op Amps"**.

3.3.4 Single Op Amps in PDIP-8 Package

Remove the original SOIC-8 packaged part. Solder a DIP-8 IC Socket in the PDIP-8 location shown on Figure 3-2; this makes it easy to change PDIP-8 parts. It also is helpful for parts for other package and pinout options; see **Section 3.3.5 "Other Single Op Amps"**. Figure 3-3 shows this board after the DIP-8 IC socket has been installed.

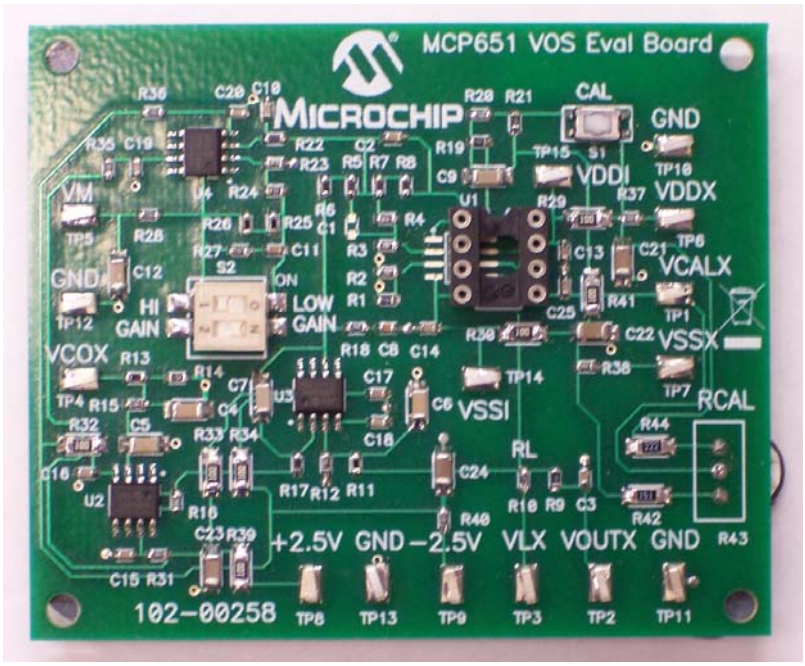


FIGURE 3-3: *PCB with SOIC-8 Part Removed and DIP-8 IC Socket Installed.*

The socket may not work well in two cases (solder directly to the PCB instead):

- Very fast op amps (i.e., GBWP > 100 MHz)
- Very accurate op amps (i.e., V_{OST} < ±50 µV)

3.3.5 Other Single Op Amps

With a DIP-8 IC Socket on the evaluation board (see **Section 3.3.4 "Single Op Amps in PDIP-8 Package"**), it is relatively easy to adapt the MCP651 Input Offset Evaluation Board to many other op amps. An adaptor board is stacked on top using headers that solder to the adaptor board, using PDIP-8 through holes, and are inserted into the DIP-8 socket on the evaluation board. The adaptor board can accommodate:

- Different packages
- Different pinout options (can be dealt with on the adaptor board)
- Parts with multiple op amps

The adaptor boards approach may not work well in two cases:

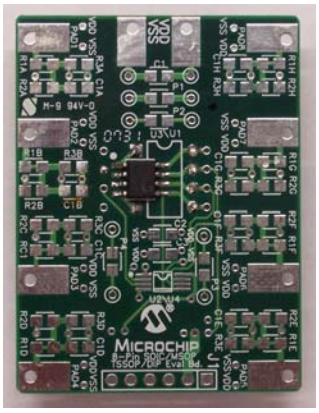
- Fast op amps (i.e., GBWP > 10 MHz); adding bypass capacitors to the adaptor board may help
- Accurate op amps (i.e., V_{OST} < ±50 µV)

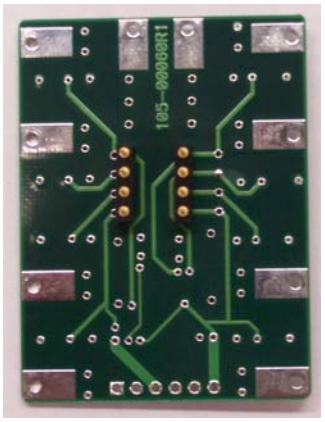
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Figure 3-4 shows a SOIC-8 op amp soldered onto the 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board available from Microchip Technology Inc. The two interconnect strips on the bottom are soldered into the through holes for the DIP-8 socket. Figure 3-5 shows this board plugged into the MCP651 Input Offset Evaluation Board.

Note 1:	Build the adaptor board in the following sequence. Insert the interconnect headers into the DIP-8 socket on the MCP651 Input Offset Evaluation Board. Place the SOIC8EV board on the top of the interconnect headers, while maintaining the correct pin orientation. Solder the headers to the top board. Clip the pins flush with the top surface of the SOIC8EV board, then solder the (SOIC-8) op amp on the top.
2:	See Table B-4 for part numbers of this board and its components.

Front View





Back View

FIGURE 3-4: *Op Amp in SOIC-8 Package and Connector Headers Soldered to Adaptor PCB.*

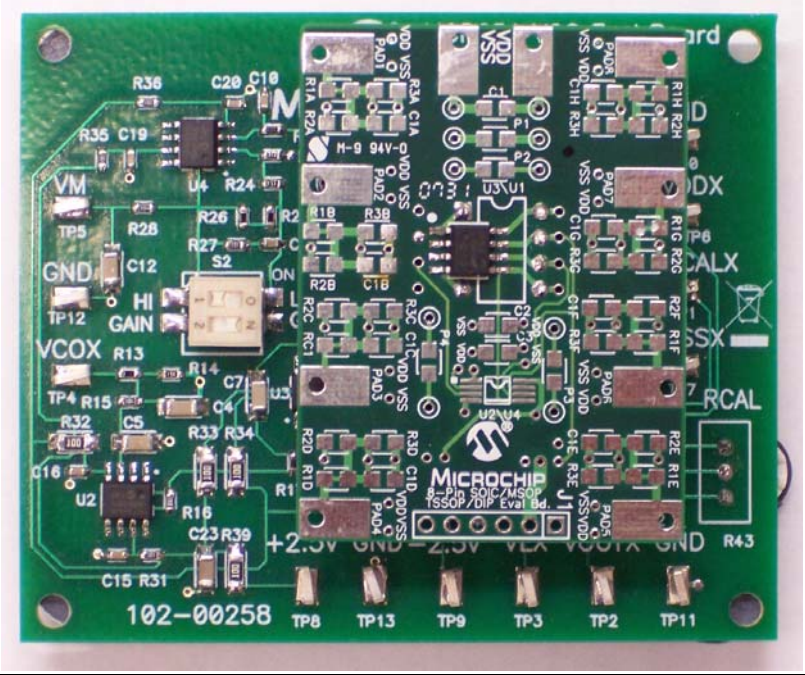


FIGURE 3-5: *Adaptor Board Connected to the MCP651 Input Offset Evaluation Board.*

NOTES:

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Appendix A. Schematics and Layouts

A.1 INTRODUCTION

This appendix contains the schematics and layouts for the MCP651 Input Offset Evaluation Board.

A.2 SCHEMATIC AND LAYOUTS

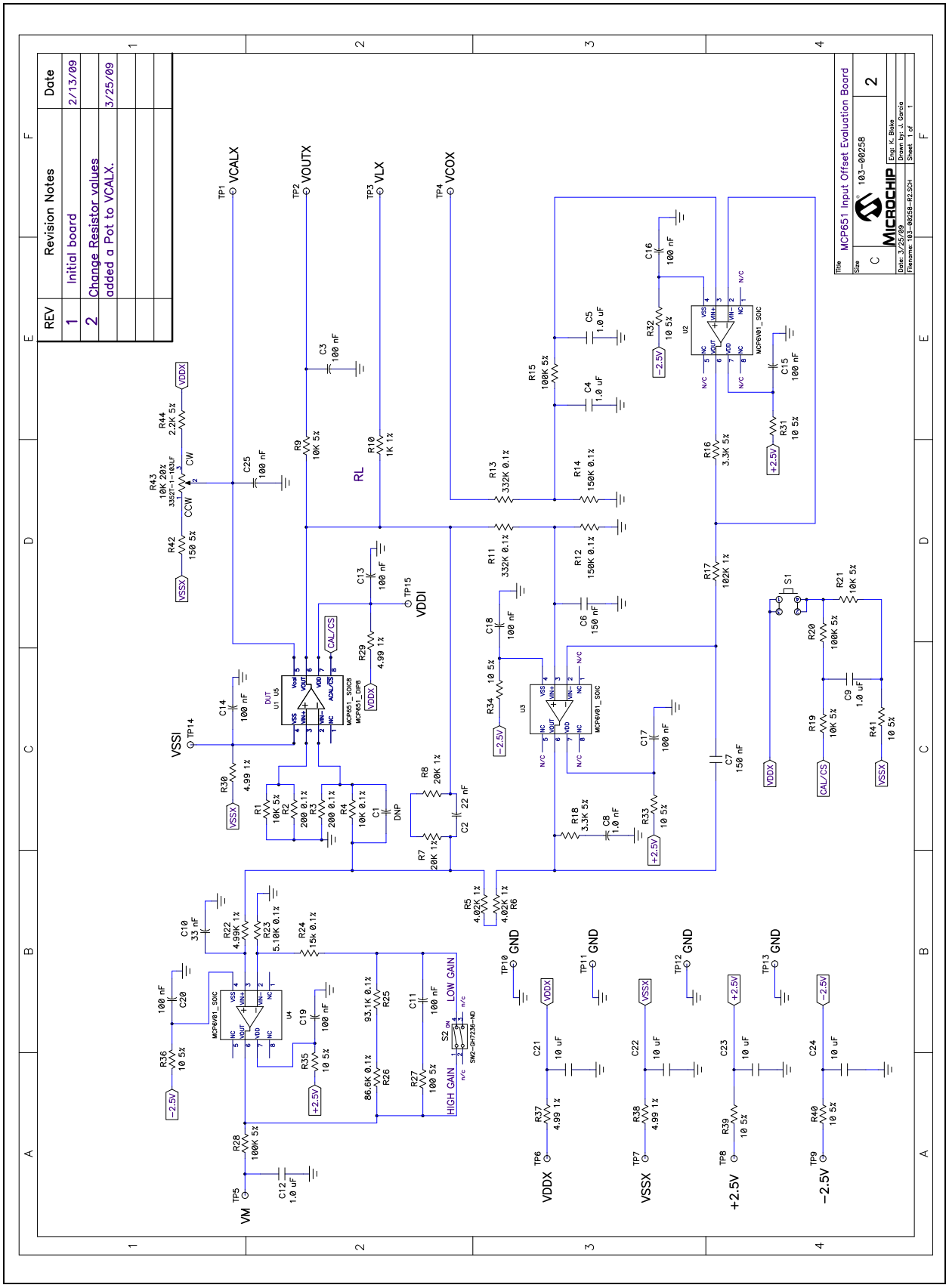
See **A.3 "Board – Schematic"** for the circuit diagram. U1 is the DUT (MCP651). U2 buffers the attenuated and filtered control voltage VCOX. U3 is the differential integrator. U4 is the amplifier that gives the final gain to the DUT's input offset voltage (V_{OST}). Switch S1 gives the user a means of starting an auto-calibration cycle in the DUT. Switch S2 makes it so the amplifier (U4) can have two different gains, providing a tradeoff between accuracy and range.

A.4 "Board – Combination of the Top Silk-Screen, Top Solder Mask and Top Metal Layers" through **A.7 "Board – Bottom Metal Layer"** show the PCB layout plots. This PCB has two metal layers: signal and power traces on top and ground plane on bottom. Groups of critical resistors have been arranged so that their thermoelectric voltages cancel (assuming constant temperature gradient); these groups are:

- R_1 through R_4
- R_5 and R_6
- R_7 and R_8
- R_{21} through R_{23}
- R_{24} and R_{25}

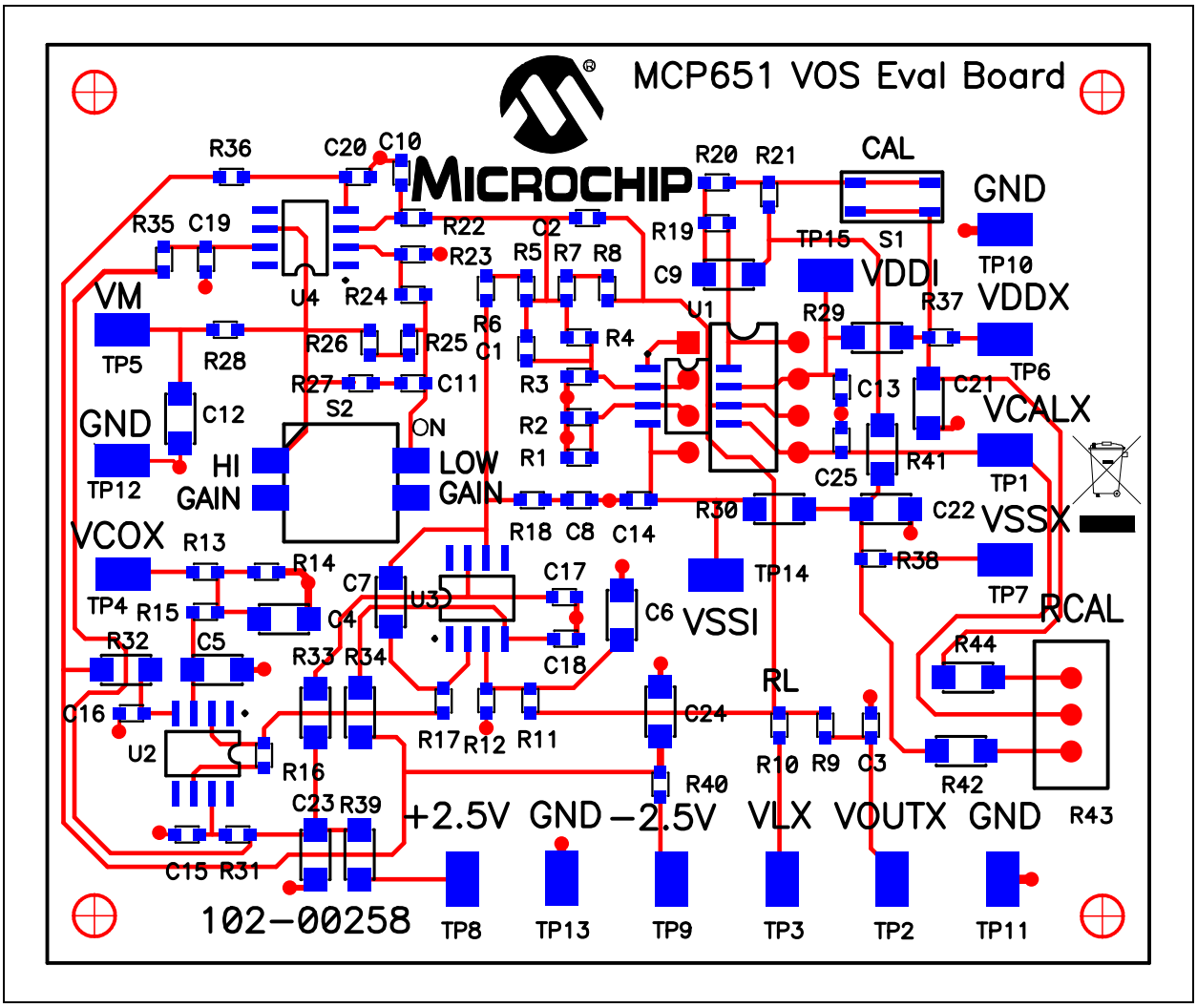
The Gerber files for this board are available on the Microchip website (www.microchip.com) and are contained in the zip file "`00258R2_Gerbers.zip`".

A.3 BOARD – SCHEMATIC

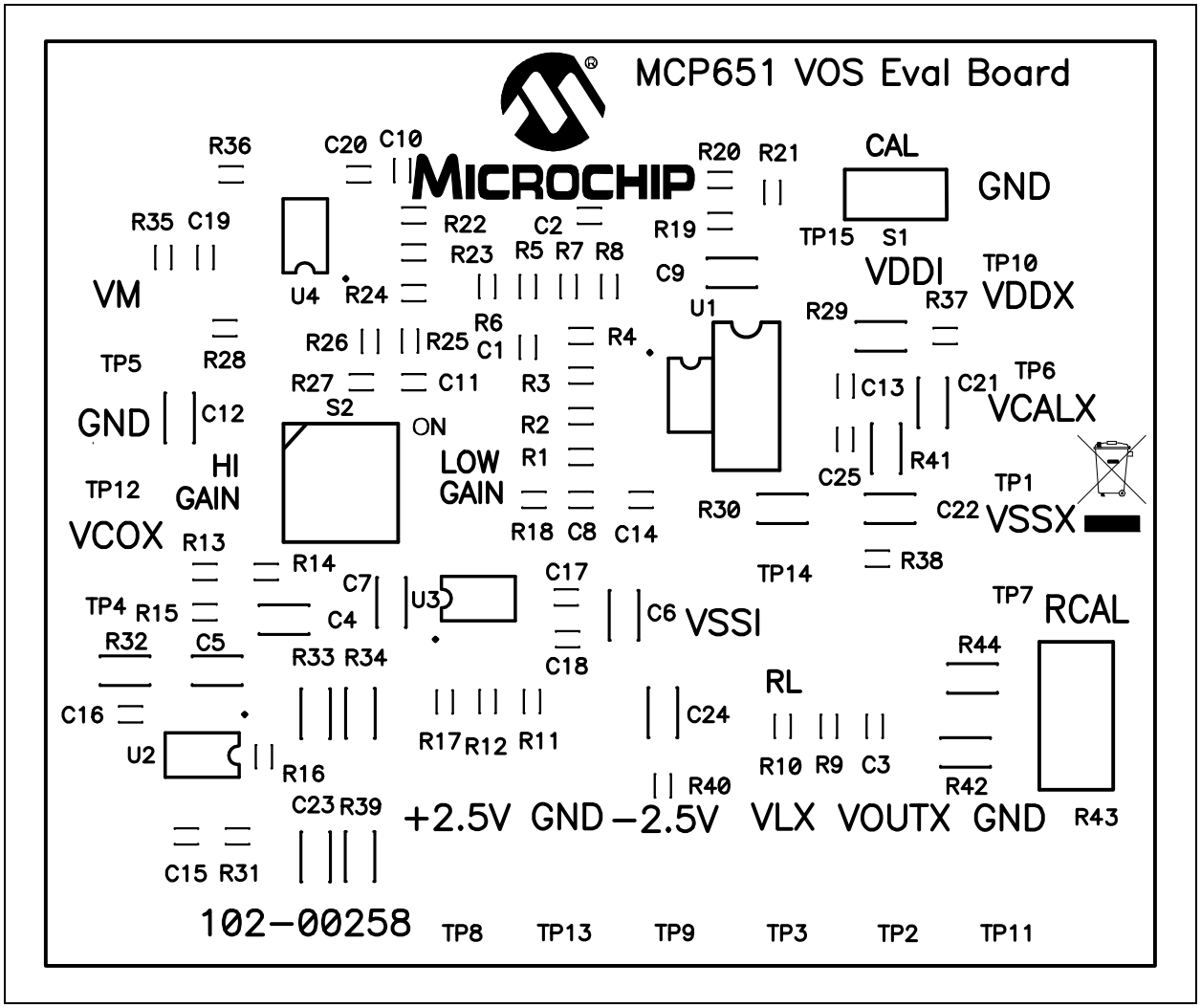


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A.4 BOARD – COMBINATION OF THE TOP SILK-SCREEN, TOP SOLDER MASK AND TOP METAL LAYERS

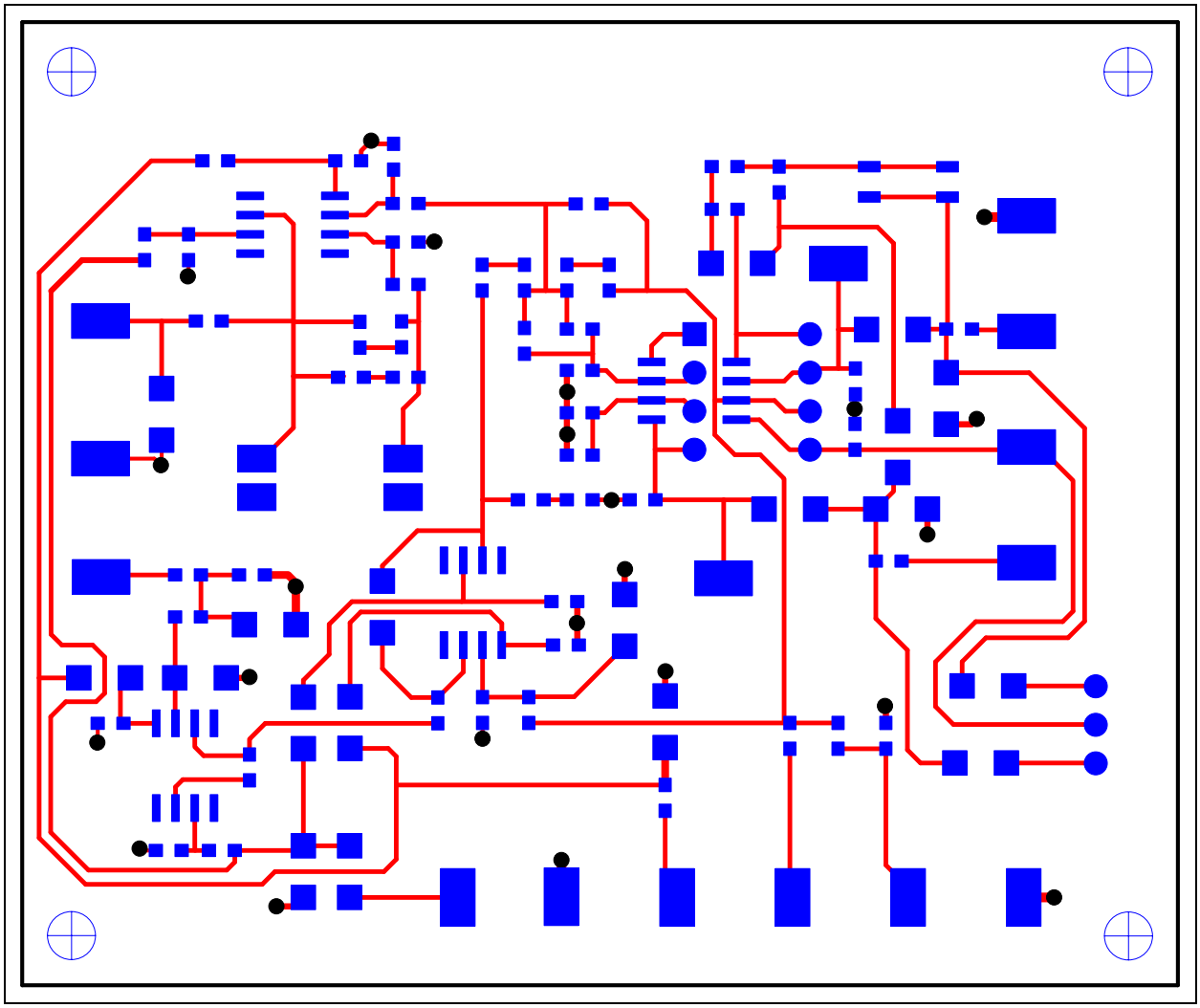


A.5 BOARD – TOP SILK-SCREEN

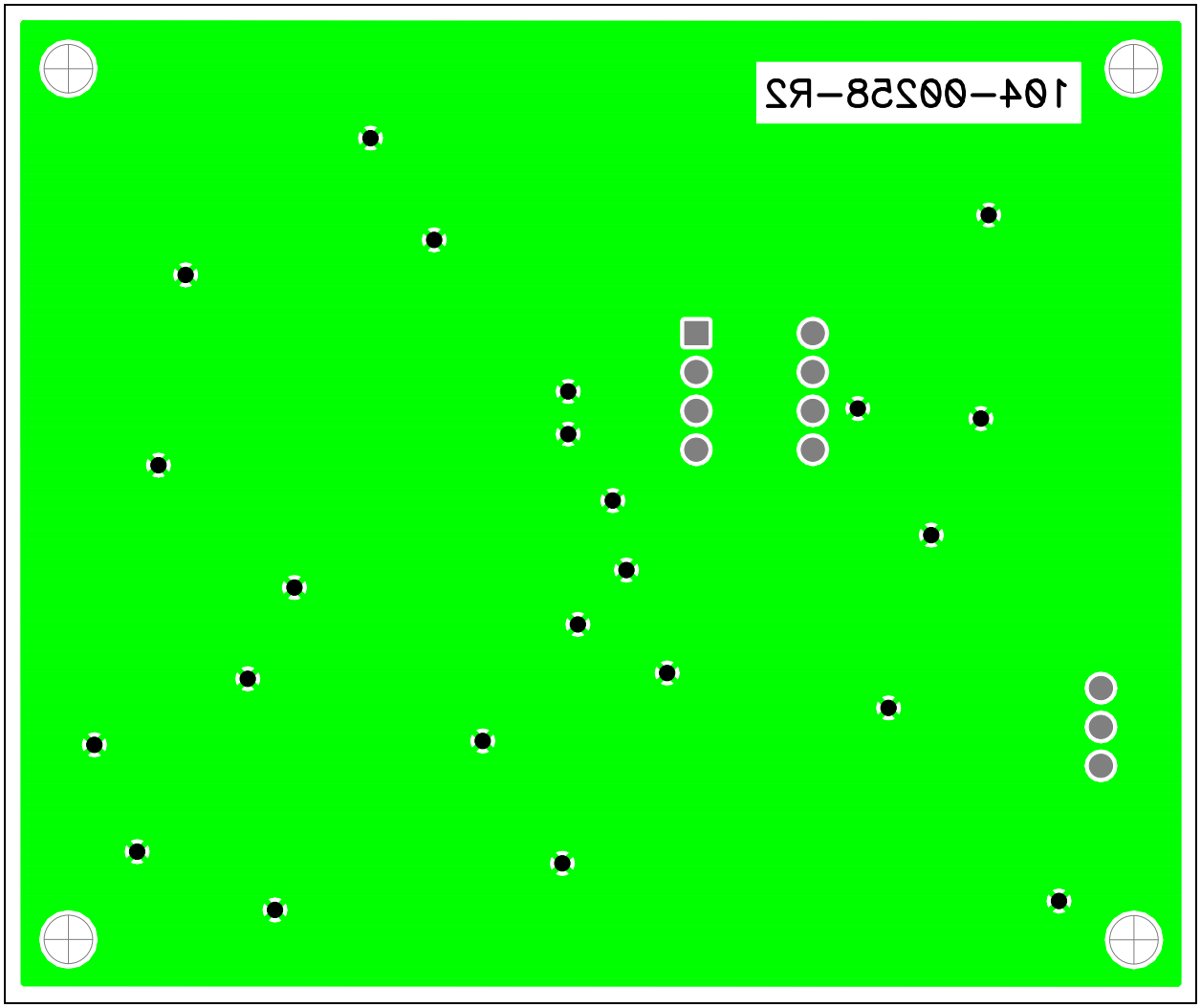


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A.6 BOARD – TOP SOLDER MASK AND TOP METAL LAYER



A.7 BOARD – BOTTOM METAL LAYER



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Appendix B. Bill Of Materials (BOM)

B.1 MCP651 INPUT OFFSET EVALUATION BOARD BOM

The BOM in Table B-1 shows all of the components assembled on the PCB. Table B-2 shows alternate components that can be placed on this PCB (after modification). Table B-3 shows components that are not populated.

TABLE B-1: BILL OF MATERIALS FOR ASSEMBLED PCB

Qty	Reference Designator	Description	Manufacturer	Part Number
1	C8	1.0 nF, 0603 SMD, X7R, 16V, 10%	Panasonic®-ECG	ECJ-1VB1H102K
1	C2	22 nF, 0603 SMD, X7R, 16V, 10%	Panasonic-ECG	ECJ-1VB1C223K
1	C10	33 nF, 0603 SMD, X7R, 16V, 10%	Panasonic-ECG	ECJ-1VB1C333K
11	C3, C11, C13 – C20, C25	100 nF, 0603 SMD, X7R, 16V, 10%	Panasonic-ECG	ECJ-1VB1C104K
2	C6, C7	150 nF, 1206 SMD, X7R, 50V, 10%	Panasonic-ECG	ECJ-3VB1C154K
4	C4, C5, C9, C12	1.0 µF, 1206 SMD, X7R, 16V, 10%	Panasonic-ECG	ECJ-3YB1C105K
4	C21 – C24	10 µF, 1206 SMD, X7R, 16V, 10%	Panasonic-ECG	ECJ-3YX1C106K
1	PCB	MCP651 Input Offset Evaluation Board, 2-layer PCB (3.00 in × 2.50 in)	Microchip Technology Inc.	102-00258
2	R2, R3	200Ω, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-201-B-T5
1	R23	5.10 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-512-B-T5
1	R4	10.0 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-103-B-T5
1	R24	15.0 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-153-B-T5
1	R26	86.6 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-8662-B-T5
1	R25	93.1 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-9312-B-T5
2	R12, R14	150 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-154-B-T5
2	R11, R13	332 kΩ, 0603 SMD, 0.1%, 25 ppm/°C, 1/10W	Susumu Co. Ltd.	RG1608P-3323-B-T5
2	R37, R38	4.99Ω, 0603 SMD, 1%, 1/10W	Yageo	RC0603FR-074R99L
1	R10	1.00 kΩ, 0603 SMD, 1%, 1/10W	Panasonic-ECG	ERJ-3EKF1001V
2	R5, R6	4.02 kΩ, 0603 SMD, 1%, 1/10W	Panasonic-ECG	ERJ-3EKF4021V
1	R22	4.99 kΩ, 0603 SMD, 1%, 1/10W	Panasonic-ECG	ERJ-3EKF4991V
2	R7, R8	20.0 kΩ, 0603 SMD, 1%, 1/10W	Panasonic-ECG	ERJ-3EKF2002V
1	R17	102 kΩ, 0603 SMD, 1%, 1/10W	Panasonic-ECG	ERJ-3EKF1023V
4	R31, R35, R36, R40	10Ω, 0603 SMD, 5%, 1/10W	Panasonic-ECG	ERJ-3GEYJ100V
1	R27	100Ω, 0603 SMD, 5%, 1/10W	Panasonic-ECG	ERJ-3GEYJ101V
2	R16, R18	3.3 kΩ, 0603 SMD, 5%, 1/10W	Panasonic-ECG	ERJ-3GEYJ332V
4	R1, R9, R19, R21	10 kΩ, 0603 SMD, 5%, 1/10W	Panasonic-ECG	ERJ-3GEYJ103V
3	R15, R20, R28	100 kΩ, 0603 SMD, 5%, 1/10W	Panasonic-ECG	ERJ-3GEYJ104V
2	R29, R30	4.99Ω, 1206 SMD, 1%, 1/4W	Yageo	RC1206FR-074R99L

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Qty	Reference Designator	Description	Manufacturer	Part Number
5	R32 – R34, R39, R41	10Ω, 1206 SMD, 5%, 1/4W	Panasonic-ECG	ERJ-8GEYJ100V
1	R42	150Ω, 1206 SMD, 5%, 1/4W	Panasonic-ECG	ERJ-8GEYJ151V
1	R44	2.2 kΩ, 1206 SMD, 5%, 1/4W	Panasonic-ECG	ERJ-8GEYJ222V
1	R43	10 kΩ POT, SMD, 20%, 1 Turn Thumbwheel	Bournes Inc.	3352T-1-103LF
1	S1	SPST-NO, SMD, Switch, Push Button, 1 Pos.	Panasonic-ECG	EVQ-P2R02M
1	S2	SMD, Switch, DIP, 2 Pos.	Grayhill Inc.	90HBW02PT
15	TP1 – TP15	SMD, Test Point	Keystone Electronics®	5016
1	U1	SOIC-8, Single Op Amp	Microchip Technology Inc.	MCP651-E/SN
3	U2 – U4	MCP6V01, SOIC-8, Single Op Amp		MCP6V01-E/SN
4	(for PCB mounting)	Hemispherical Bumpon Standoff, 0.44 in × 0.20 in	3M	SJ-5003 (BLACK)

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

TABLE B-2: BILL OF MATERIALS FOR ALTERNATE COMPONENTS

Qty	Reference Designator	Description	Manufacturer	Part Number
0	U1	PDIP-8, Single Op Amp	Microchip Technology Inc.	MCP6XXX **(Note 1)**
0	U1	DIP-8 IC Socket	Tyco Electronics	2-641260-1
0	(for PCB mounting)	Stand-off, Hex, 0.500", 4 × 40 Thread, Nylon, 0.285" max. O.D.	Keystone Electronics	1902C
0	(for PCB mounting)	Machine Screw, Phillips, 4 × 40 Thread, 1/4" long, Nylon	Building Fasteners	NY PMS 440 0025 PH

Note 1: The MCP6XXX represents any Microchip single op amp, with standard pinout, that fits the given design.

2: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

TABLE B-3: BILL OF MATERIALS FOR NOT POPULATED COMPONENTS

Qty	Reference Designator	Description	Manufacturer	Part Number
0	C1	Unknown Value, 0603 SMD, X7R, 16V, 10%	Panasonic®-ECG	—

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

B.2 ADAPTOR BOARD BOM

The BOM in Table B-4 shows the components needed to build the adaptor board for alternate DUT's (see Figure 3-4).

TABLE B-4: BILL OF MATERIALS FOR ADAPTOR BOARD

Qty	Reference Designator	Description	Manufacturer	Part Number
1	—	8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board	Microchip Technology Inc.	SOIC8EV
2	—	Board-to-Board Connector, Low Profile Header, 4 Positions, 0.100 in, Gold Plated	Samtec Inc.	BBL-104-G-F
2	—	100 nF, 0603 SMD, X7R, 16V, 10%	Panasonic®-ECG	ECJ-1VB1C104K
1	—	Single Op Amp in Standard 8-pin pinout	Microchip Technology Inc.	MCP6XXX

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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