MCP629x 10-MHz, Rail-to-Rail Operational Amplifier

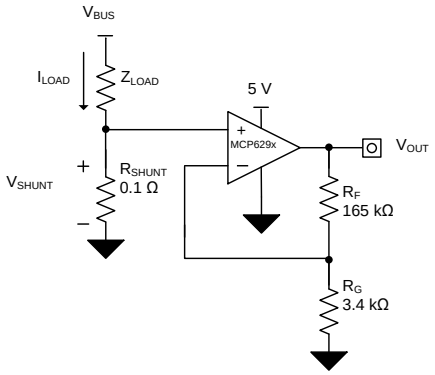
1 Features

- Gain Bandwidth Product: 10 MHz Typical
- Operating Supply Voltage: 2.4 V to 5.5 V
- Rail-to-Rail Input/Output
- Low Input Bias Current: 1 pA
- Low Quiescent Current: 0.6 mA
- Input Voltage Noise: 8.7 nV/√Hz at f = 10 kHz
- Internal RF and EMI Filter
- Extended Temperature Range: –40°C to +125°C
- Unity-Gain Stable
- Easier to Stabilize With Higher Capacitive Load Due to Resistive Open-Loop Output Impedance

2 Applications

- Power Modules
- Smoke Detectors
- HVAC: Heating, Ventilating, and Air Conditioning
- Battery-Powered Applications
- Sensor Signal Conditioning
- Photodiode Amplifier
- Analog Filters
- Medical Instrumentation
- Notebooks and PDAs
- Barcode Scanners
- Audio Receiver
- Automotive Infotainment

Low-Side Motor Control



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3 Description

The MCP6291 (single), MCP6292 (dual), and MCP6294 (quad) devices comprise a family of general-purpose, low-power operational amplifiers. Features such as rail-to-rail input and output swings, low quiescent current (600 µA/ch typical) combined with a wide bandwidth of 10 MHz, and low noise (8.7 nV/√Hz at 10 kHz) make this family attractive for a variety of applications that require a balance between cost and performance. The low input bias current enables the family to be used in applications with high-source impedances.

The robust design of the MCP629x provides ease-of-use to the circuit designer: a unity-gain stable, integrated RFI and EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

The MCP629x family operates over the extended temperature range of –40°C to +125°C. The family has a power supply range of 2.4 V to 5.5 V.

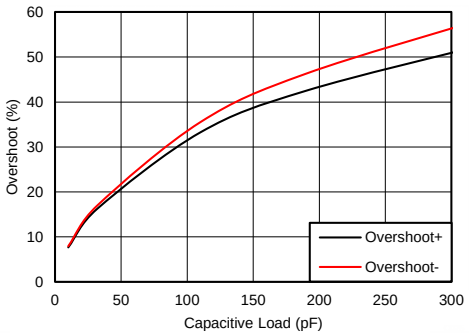
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCP6291	SOT-23 (5) (2)	1.60 mm × 2.90 mm
MCP6292	SOIC (8)	3.91 mm × 4.90 mm
	VSSOP (8) (2)	3.00 mm × 3.00 mm
MCP6294	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14) (2)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Package is preview only.

Small-Signal Overshoot vs Load Capacitance



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (July 2017) to Revision A **Page**

- Deleted MCP6291 SC70, SOT-553, and SOIC packages from *Device Information* table ... 1
- Deleted MCP6292 WSON and VSSOP (10) packages from *Device Information* table ... 1
- Changed MCP6294 14-pin SOIC package from preview to production data in *Device Information* table ... 1
- Deleted DCK, DRL, DSG, RTE and 8-pin D packages from *Device Comparison* table ... 3
- Deleted DRL (SOT-533) package from MCP6291 pinout image and table in *Pin Configuration and Functions* section ... 4
- Deleted MCP6291 DCK (SC70) and D (SOIC) package pinout drawings and pin information from *Pin Configuration and Functions* section ... 4
- Deleted MCP6292 DSG (WSON) and DGS (VSSOP) package pinout drawings and pin table information in *Pin Configuration and Functions* section ... 5
- Deleted package preview note from MCP6294 pinout drawing in *Pin Configuration and Functions* section ... 6
- Added MCP6294 *Thermal Information* table ... 8

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5 Device Comparison Table

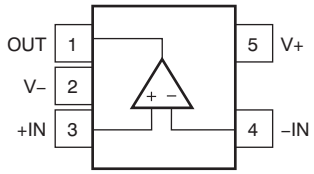
DEVICE	NO. OF CHANNELS	PACKAGE LEADS			
		DBV(1)	D	DGK(1)	PW(1)
MCP6291 (2)	1	5	—	—	—
MCP6292	2	—	8	8	—
MCP6294	4	—	14	—	14

(1) Package preview
(2) Device preview

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6 Pin Configuration and Functions

MCP6291 DBV Package (1)
5-Pin SOT-23
Top View



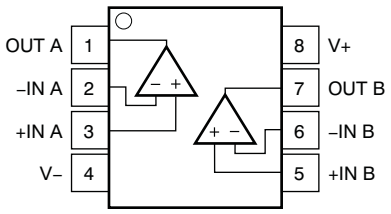
(1) Package preview

Pin Functions: MCP6921

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	—	Positive (highest) supply

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MCP6292 D, DGK Packages (1)
8-Pin SOIC, VSSOP
Top View



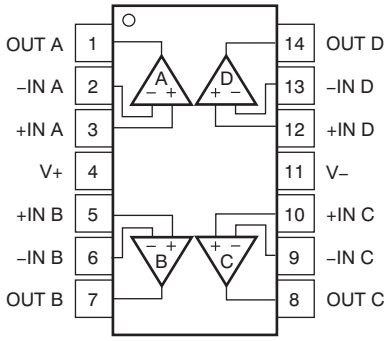
(1) DGK (VSSOP) package is preview only.

Pin Functions: MCP6292

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

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MCP6294 D, PW Packages (1)
14-Pin SOIC, TSSOP
Top View



(1) PW (TSSOP) package is preview only

Pin Functions: MCP6294

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage				6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		mA
Specified, T_A			–40	125	°C
Junction, T_J				150	
Storage, T_{stg}			–65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	2.4	5.5	V
	Specified temperature	–40	125	°C

7.4 Thermal Information: MCP6292

THERMAL METRIC(1)		MCP6292 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	104.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	55.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Thermal Information: MCP6294

THERMAL METRIC		MCP6294 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	64	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.7	°C/W

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7.6 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 2.4 V to 5.5 V

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±3	mV
		V_S = 5 V, T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±1.1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.4 V – 5.5 V, V_{CM} = (V–)		±7		µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 2.4 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C	57	87		
		V_S = 2.4 V (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		88		
		V_S = 2.4 V V_{CM} = –0.1 V to 1.9 V T_A = –40°C to 125°C		81		
INPUT BIAS CURRENT						
I_B	Input bias current			±1		pA
I_{OS}	Input offset current			±0.05		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz, R_L = 10 kΩ		8.7		$nV/\sqrt{Hz}$
		V_S = 5 V, f = 1 kHz, R_L = 10 kΩ		16		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		10		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 2.4 V (V–) + 0.04 V < V_O < (V+) – 0.04 V R_L = 10 kΩ		100		dB
		V_S = 5.5 V (V–) + 0.05 V < V_O < (V+) – 0.05 V R_L = 10 kΩ	104	130		
		V_S = 2.4 V (V–) + 0.06 V < V_O < (V+) – 0.06 V R_L = 2 kΩ		100		
		V_S = 5.5 V (V–) + 0.15 V < V_O < (V+) – 0.15 V R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = 1		10		MHz
φ_m	Phase margin	V_S = 5 V, G = 1		55		Degrees
SR	Slew rate	V_S = 5 V, G = 1		6.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		0.5		µs
		To 0.01%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V V_{IN} × gain > V_S		0.2		µs

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Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 2.4 V to 5.5 V (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion + noise(1)	V_S = 5 V V_O = 1 V_{RMS} G = 1, f = 1 kHz		0.0008%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			15	mV
		V_S = 5.5 V, R_L = 2 kΩ			50	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		600	1300	µA

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

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7.7 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

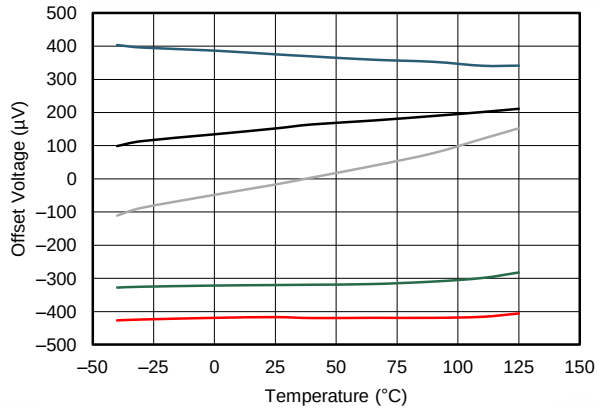


Figure 1. Offset Voltage vs Temperature

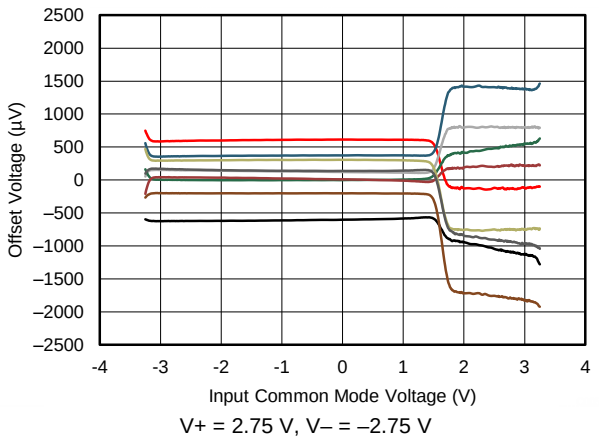


Figure 2. Offset Voltage vs Common-Mode Voltage

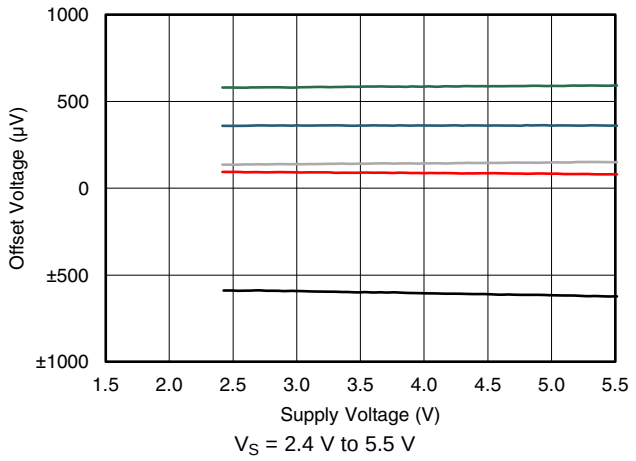


Figure 3. Offset Voltage vs Power Supply

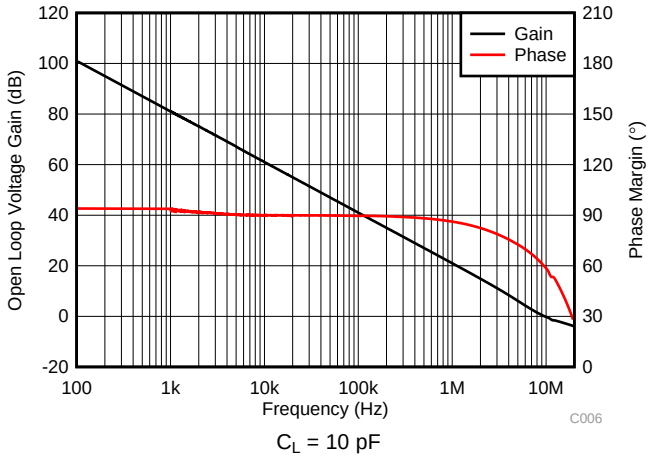


Figure 4. Open-Loop Gain and Phase vs Frequency

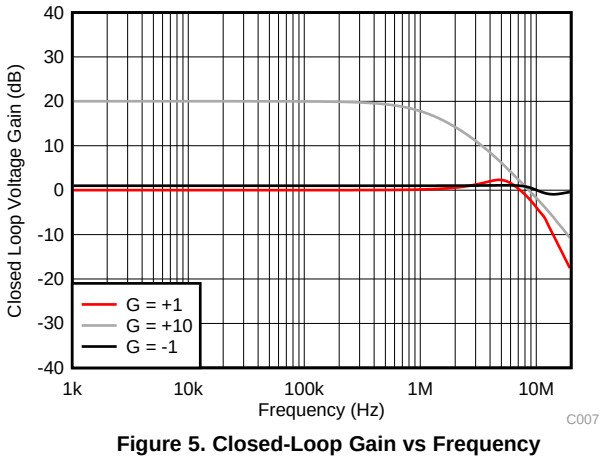


Figure 5. Closed-Loop Gain vs Frequency

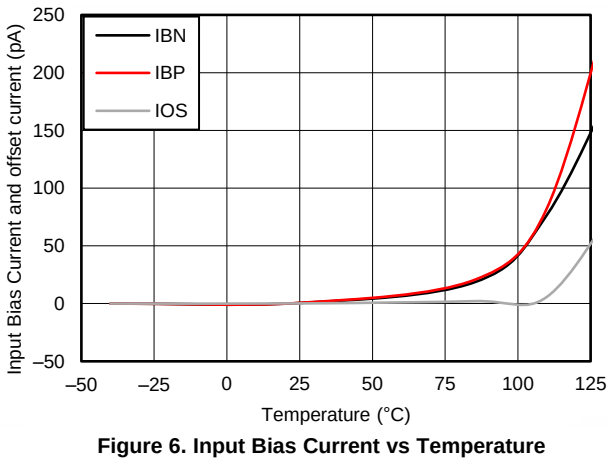


Figure 6. Input Bias Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

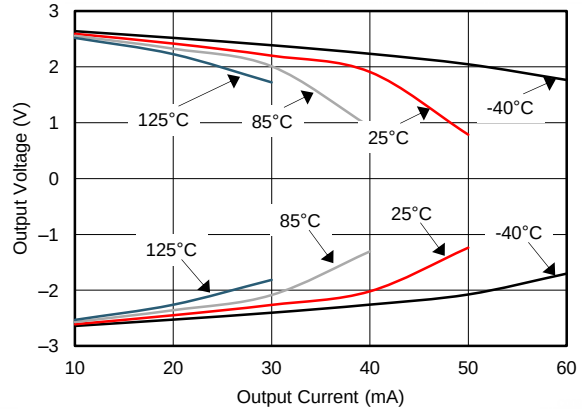


Figure 7. Output Voltage Swing vs Output Current

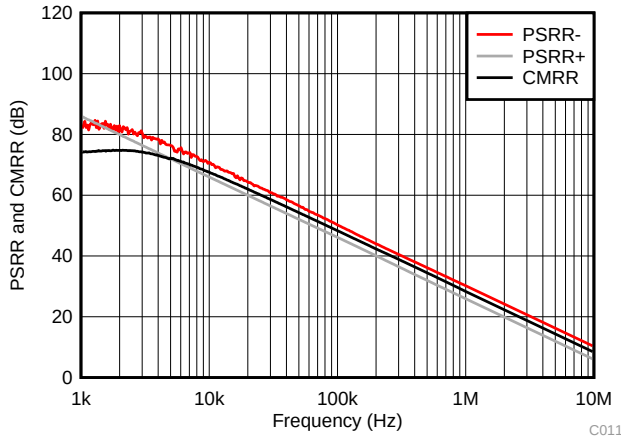


Figure 8. CMRR and PSRR vs Frequency (Referred to Input)

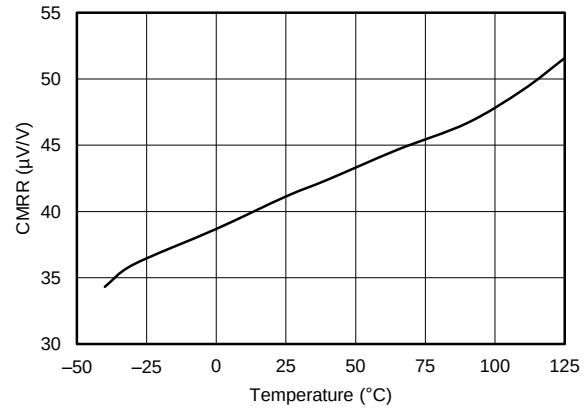


Figure 9. CMRR vs Temperature

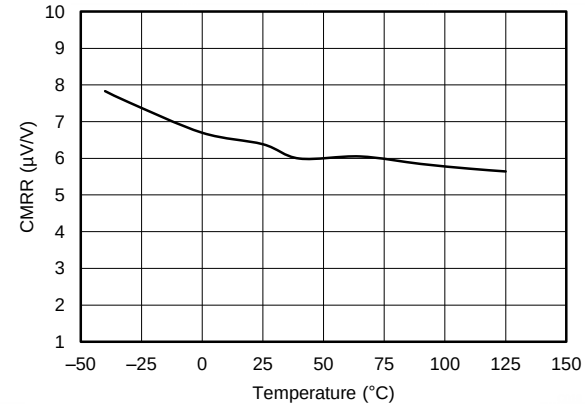


Figure 10. CMRR vs Temperature

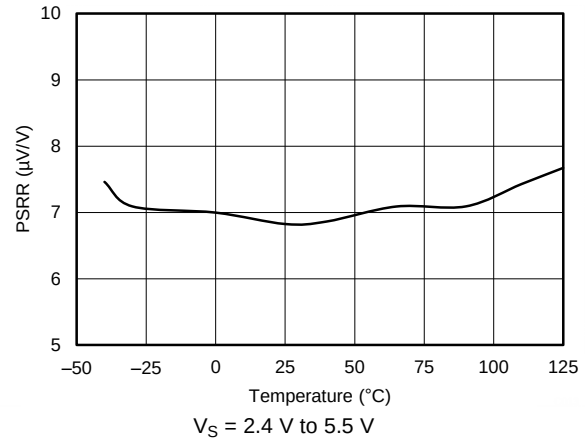


Figure 11. PSRR vs Temperature

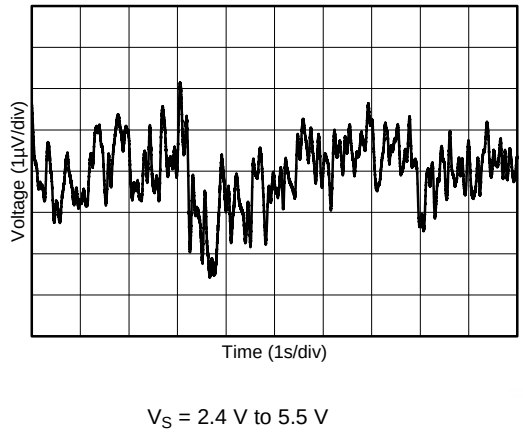


Figure 12. 0.1-Hz to 10-Hz Input Voltage Noise

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

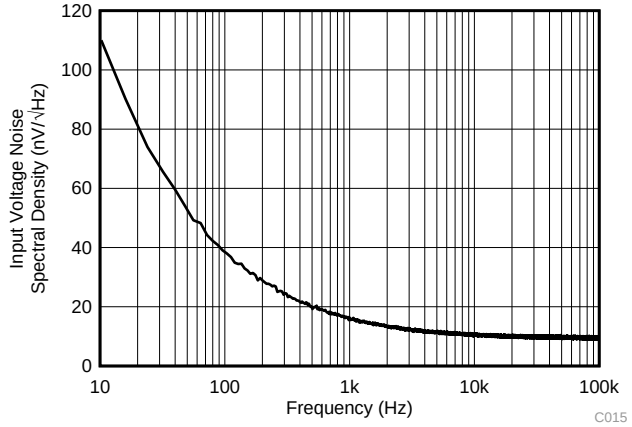
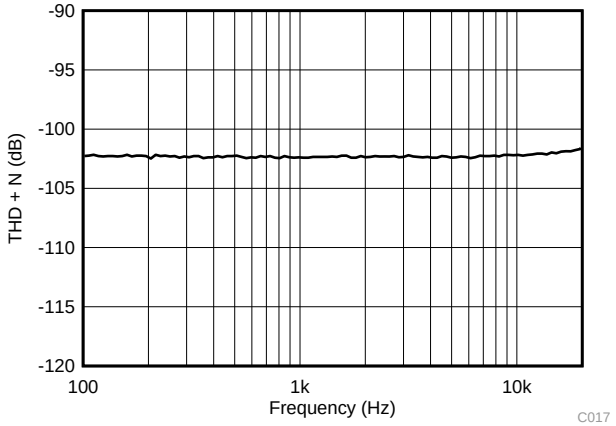
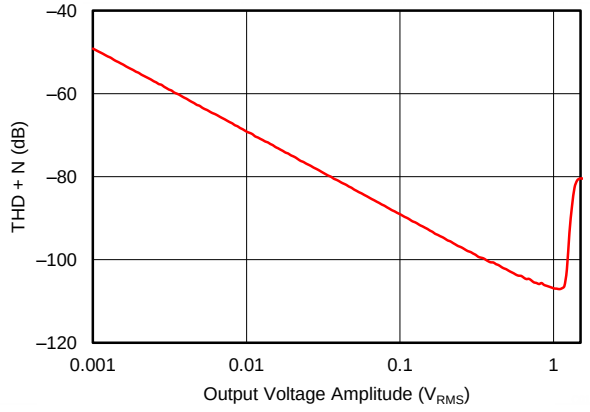


Figure 13. Input Voltage Noise Spectral Density vs Frequency



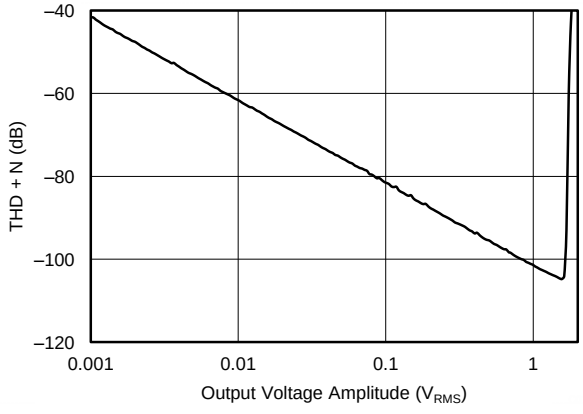
V_S = 5.5 V | V_{CM} = 2.5 V | R_L = 2 kΩ
V_{OUT} = 0.5 V_{RMS} | G = 1 | BW = 80 kHz

Figure 14. THD + N vs Frequency



V_S = 5.5 V | V_{CM} = 2.5 V | R_L = 2 kΩ
G = 1 | BW = 80 kHz | f = 1 kHz

Figure 15. THD + N vs Amplitude



V_S = 5.5 V | V_{CM} = 2.5 V | R_L = 2 kΩ
G = –1 | BW = 80 kHz | f = 1 kHz

Figure 16. THD + N vs Amplitude

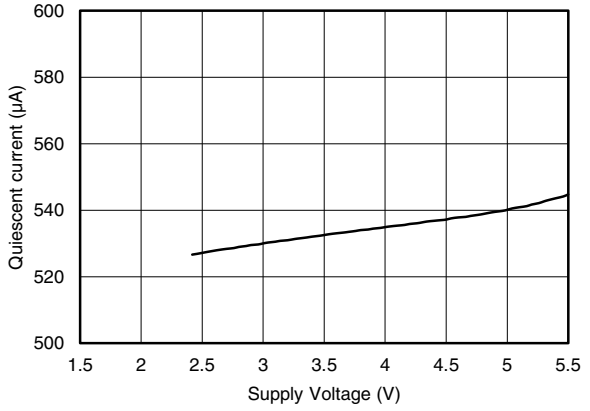


Figure 17. Quiescent Current vs Supply Voltage

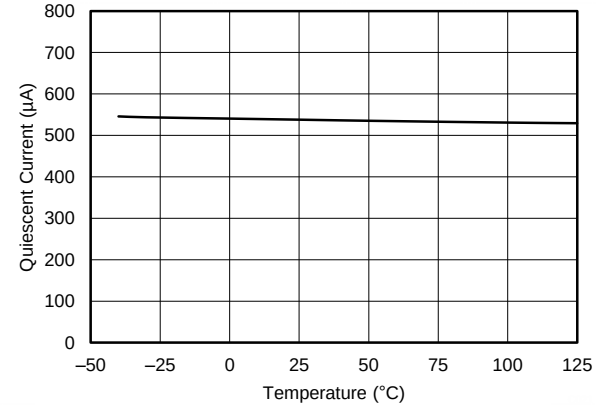


Figure 18. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

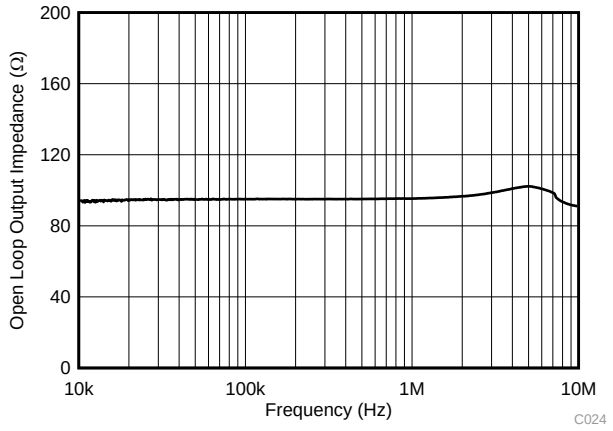
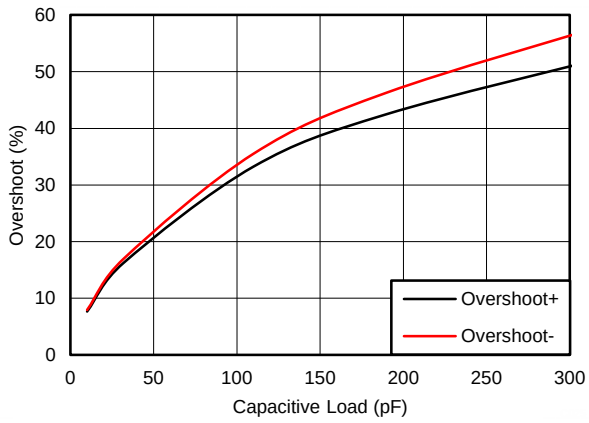
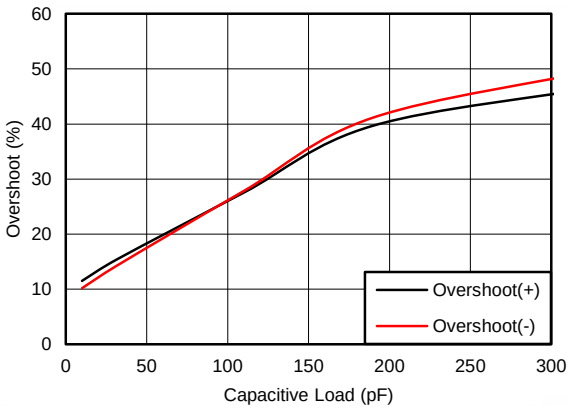


Figure 19. Open-Loop Output Impedance vs Frequency



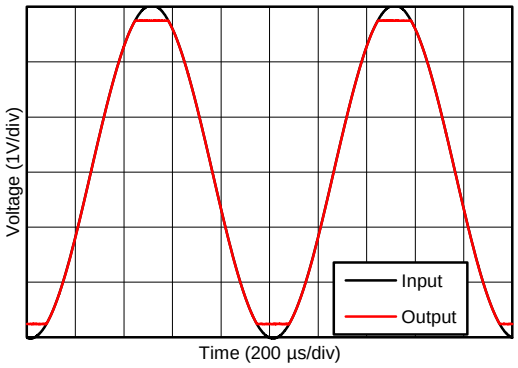
V+ = 2.75 V V– = –2.75 V G = 1 V/V
R_L = 10 kΩ V_{OUT} step = 100 mV_{p-p}

Figure 20. Small-Signal Overshoot vs Load Capacitance



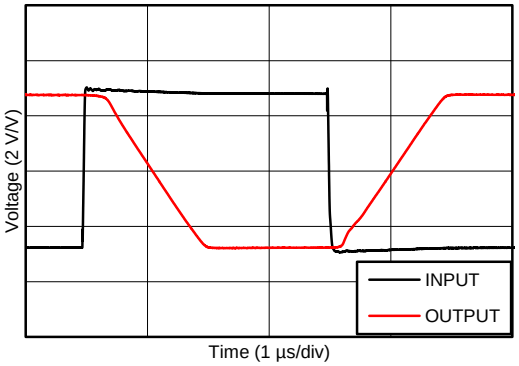
V+ = 2.75 V V– = –2.75 V G = –1 V/V
R_L = 10 kΩ V_{OUT} step = 100 mV_{p-p}

Figure 21. Small-Signal Overshoot vs Load Capacitance



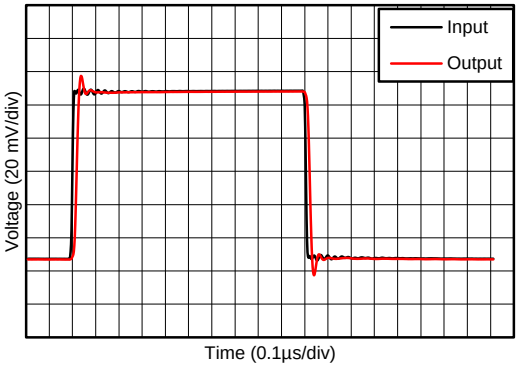
V+ = 2.75 V, V– = –2.75 V

Figure 22. No Phase Reversal



V+ = 2.75 V V– = –2.75 V G = –10 V/V

Figure 23. Overload Recovery



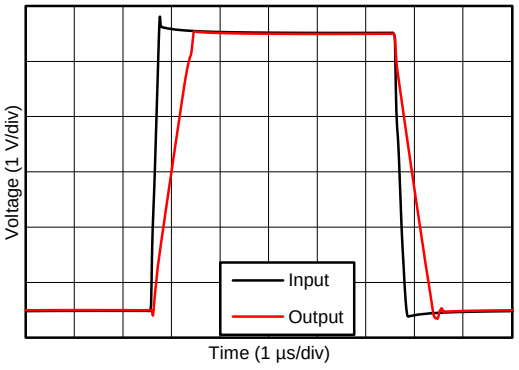
V+ = 2.75 V V– = –2.75 V G = 1 V/V

Figure 24. Small-Signal Step Response

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V+ = 2.75 V V– = –2.75 V C_L = 100 pF
G = 1 V/V

Figure 25. Large-Signal Step Response

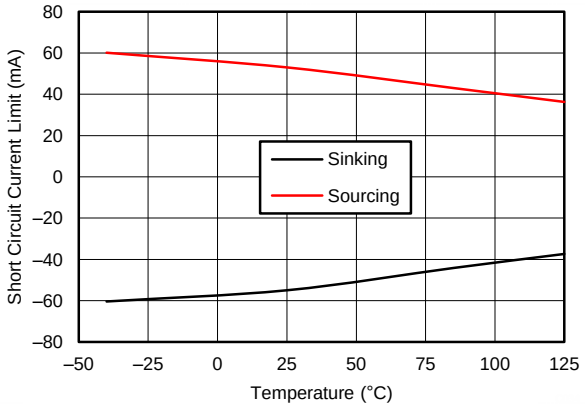
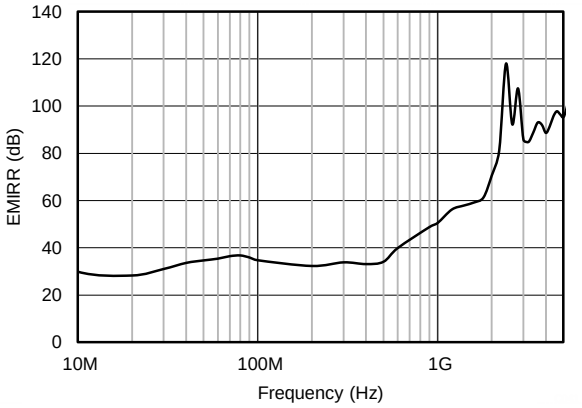
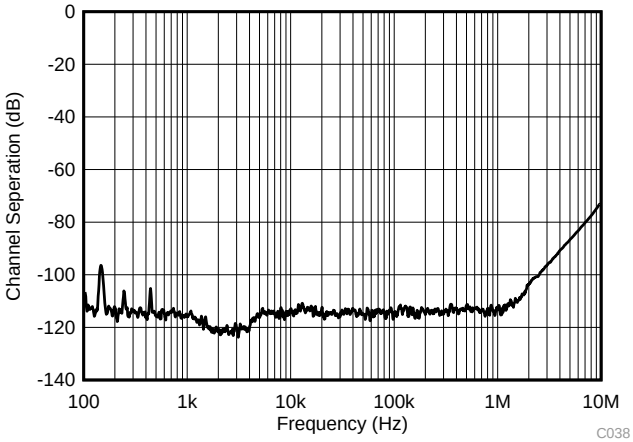


Figure 26. Short-Circuit Current vs Temperature



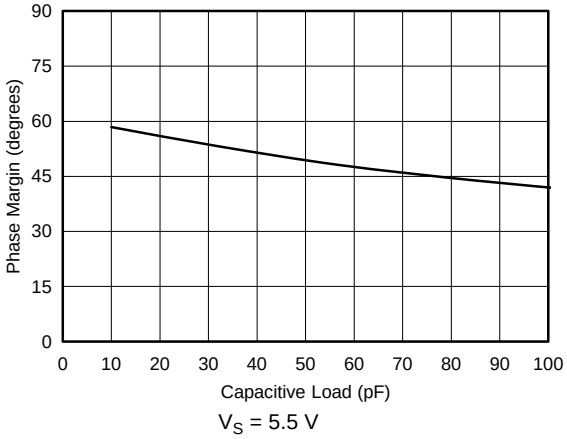
P_{RF} = –10 dBm

Figure 27. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



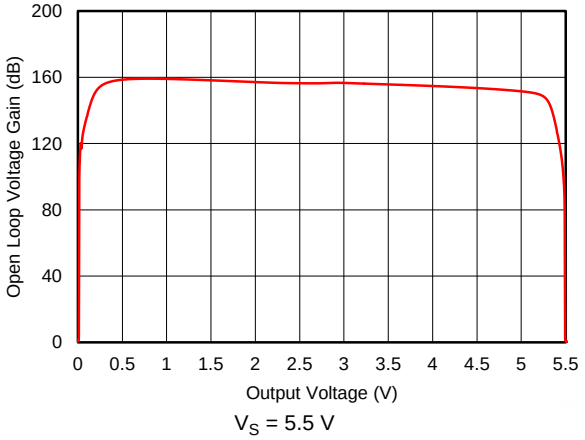
V+ = 2.75 V, V– = –2.75 V

Figure 28. Channel Separation vs Frequency



V_S = 5.5 V

Figure 29. Phase Margin vs Capacitive Load



V_S = 5.5 V

Figure 30. Open Loop Voltage Gain vs Output Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

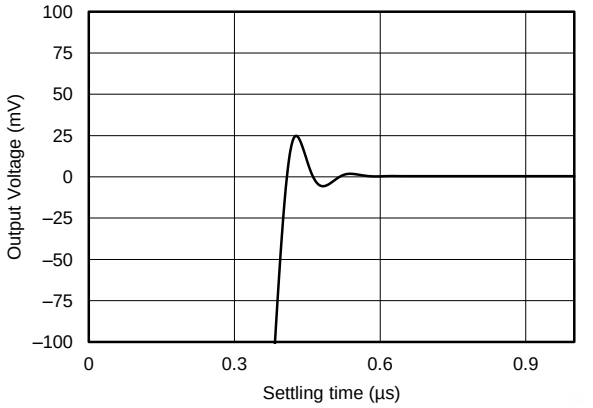


Figure 31. Large Signal Settling Time (Positive)

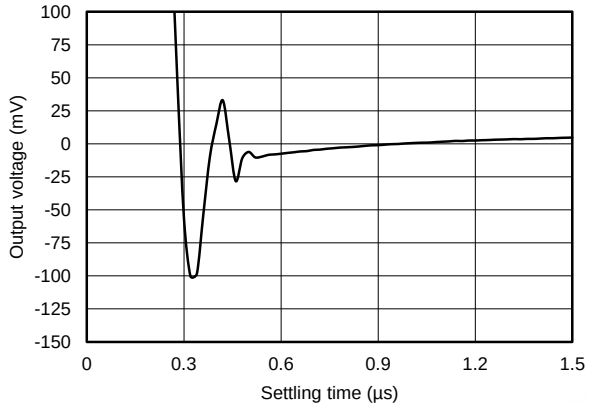


Figure 32. Large Signal Settling Time (Negative)

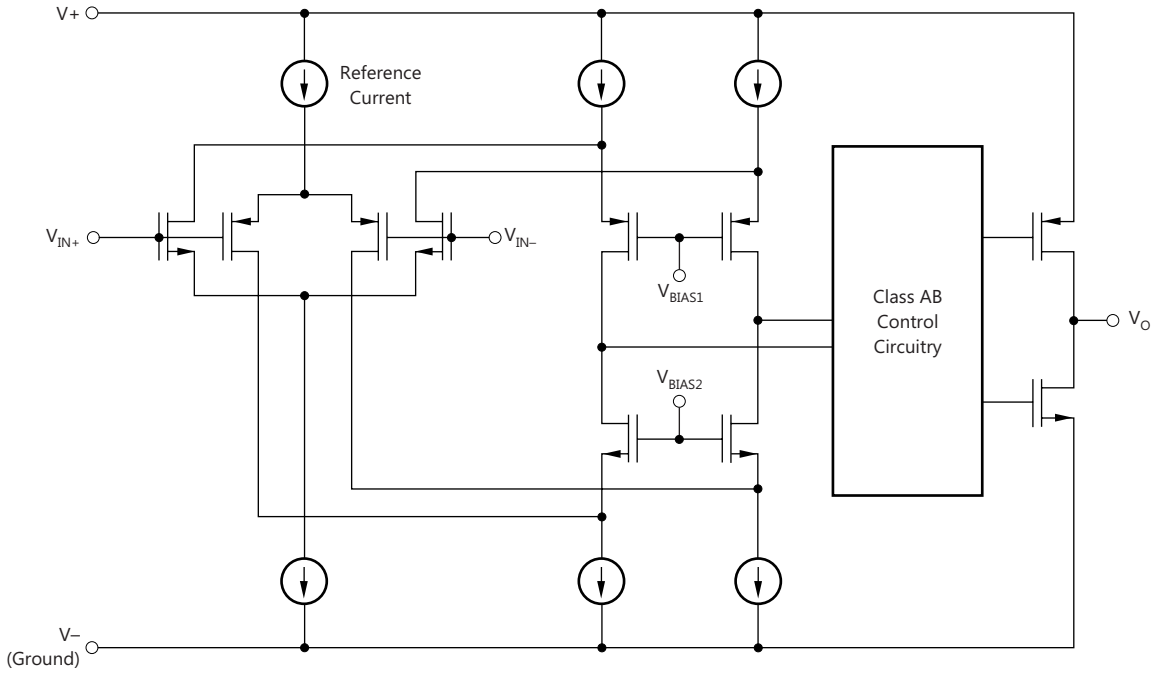
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8 Detailed Description

8.1 Overview

The MCP629x series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.4 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the MCP629x series to be used in any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the MCP629x family extends 100 mV beyond the supply rails for the full supply voltage range of 2.4 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as the *Functional Block Diagram* shows. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the MCP629x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the MCP629x series is approximately 200 ns.

8.4 Device Functional Modes

The MCP629x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.4 V (±1.2 V) and 5.5 V (±2.75 V).

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9 Application and Implementation

NOTE

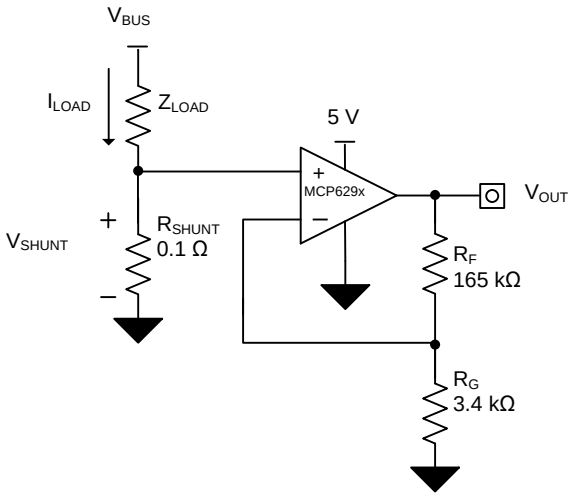
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MCP629x series features 10-MHz bandwidth and 6.5-V/µs slew rate with only 600-µA of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 8.7 nV / $\sqrt{\text{Hz}}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

9.2 Typical Application

Figure 33 shows the MCP629x configured in a low-side, motor-control application.



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Figure 33. MCP629x in a Low-Side, Motor-Control Application

9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

Typical Application (continued)

9.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 33 is shown in Equation 1

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the MCP629x to produce an output voltage of roughly 0 V to 4.95 V. The gain needed by the MCP629x to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{\left(V_{OUT_MAX} - V_{OUT_MIN}\right)}{\left(V_{IN_MAX} - V_{IN_MIN}\right)} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49.5 V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the MCP629x to 49.5 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \quad (4)$$

Choosing R_F as 165 kΩ and R_G as 3.4 kΩ provides a combination that equals roughly 49.5 V/V. Figure 34 shows the measured transfer function of the circuit shown in Figure 33.

9.2.3 Application Curve

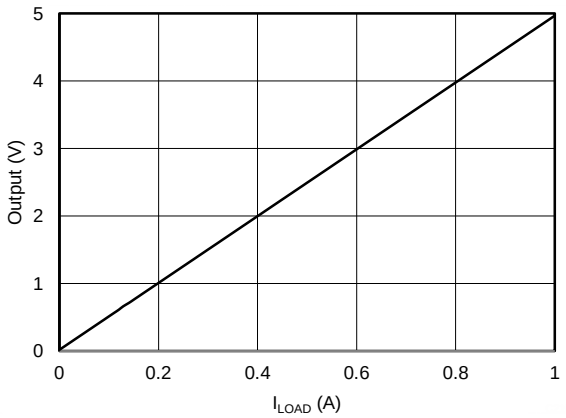


Figure 34. Low-Side, Current-Sense Transfer Function

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10 Power Supply Recommendations

The MCP629x series is specified for operation from 2.4 V to 5.5 V (±1.2 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the section.

10.1 Input and ESD Protection

The MCP629x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the *Absolute Maximum Ratings* table. Figure 35 shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

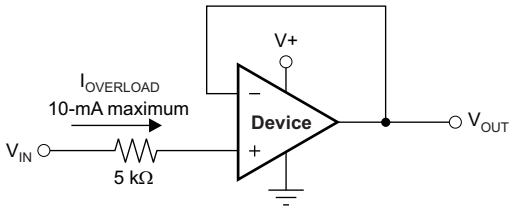


Figure 35. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 37, keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

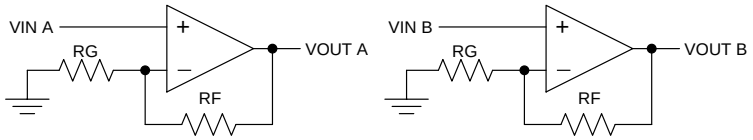


Figure 36. Schematic Representation for Figure 37

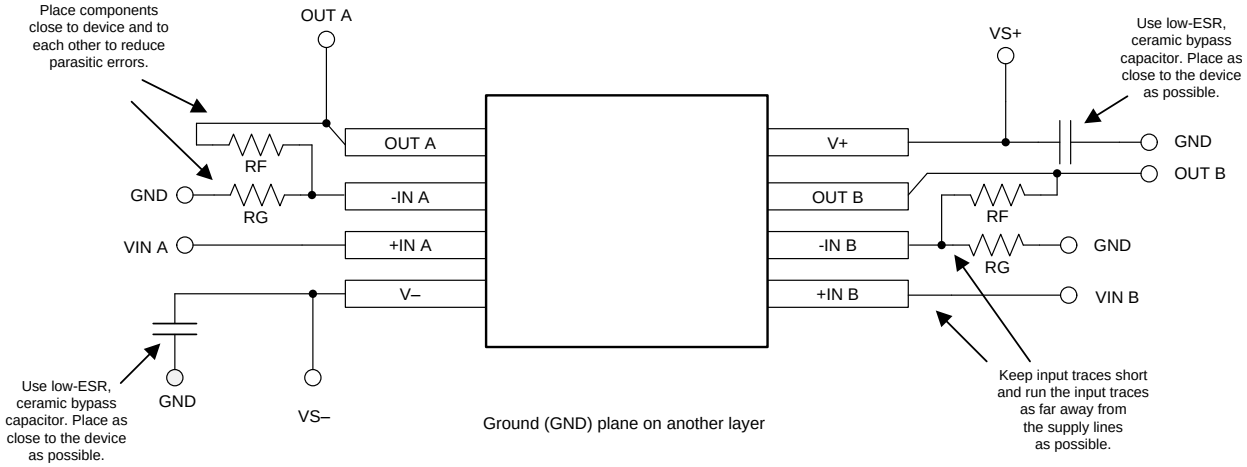


Figure 37. Layout Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Circuit Board Layout Techniques

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MCP6291	Click here	Click here	Click here	Click here	Click here
MCP6292	Click here	Click here	Click here	Click here	Click here
MCP6294	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MCP6292IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	MC6292	Samples
MCP6294IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPD	Level-2-260C-1 YEAR	-40 to 125	MCP6294D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

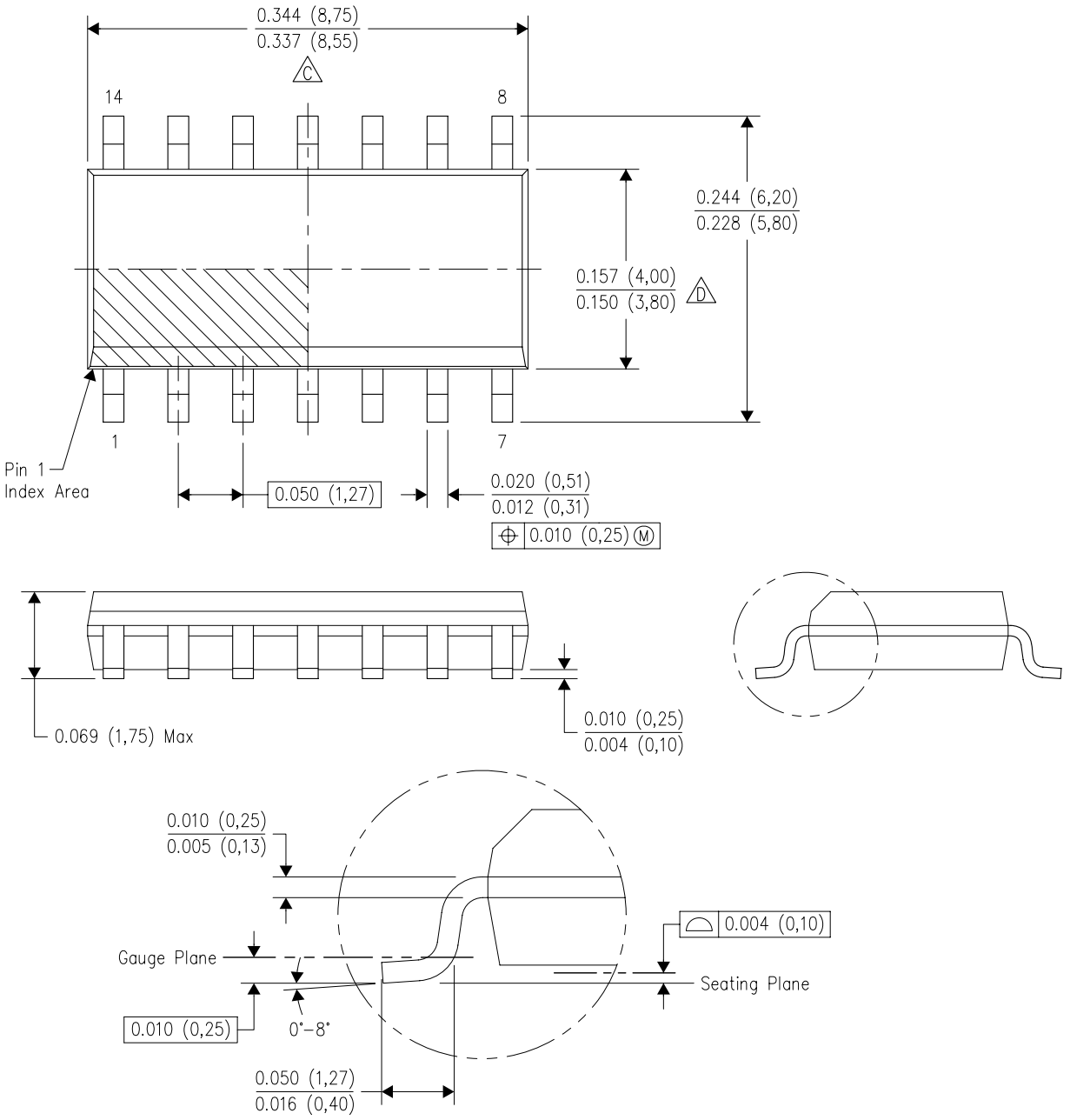
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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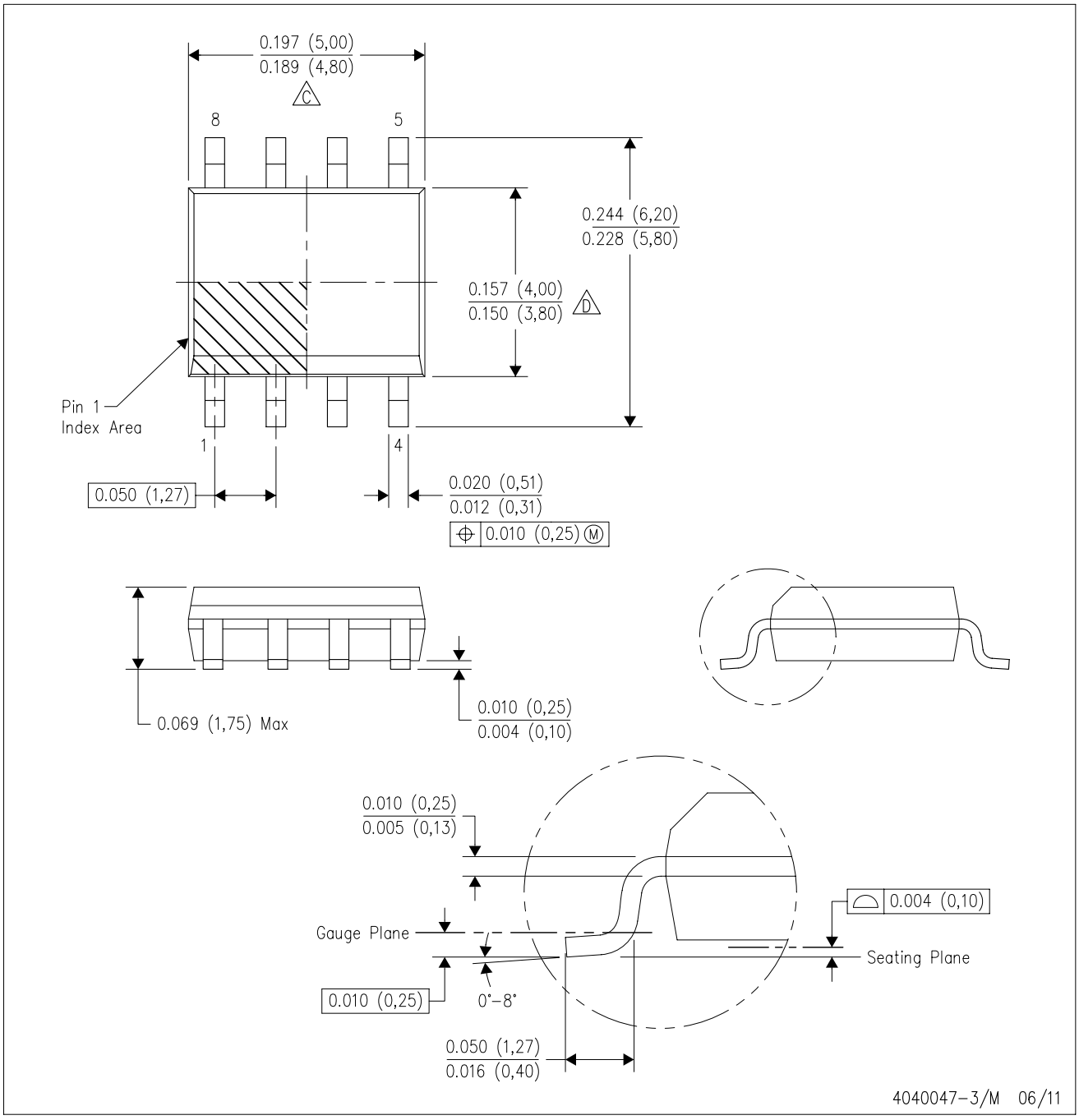
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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