MCP47A1

6-Bit Volatile DAC with Command Code

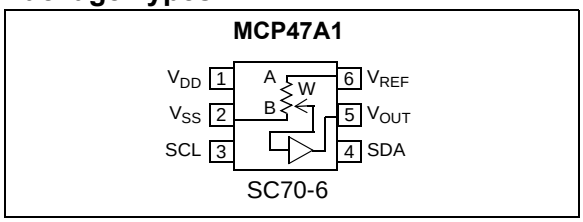
Features:

- 6-Bit DAC
  - 65 Taps: 64 Resistors with Taps to Full-Scale and Zero-Scale (Wiper Code 00h to 40h)
- V_{REF} Pull-down Resistance: 20 kΩ (typical)
- V_{OUT} Voltage Range
  - V_{SS} to V_{REF}
- $I^2C^{™}$ Protocol
  - Supports SMBus 2.0 Write Byte/Word Protocol Formats
  - Supports SMBus 2.0 Read Byte/Word Protocol Formats
  - Slave Addresses: 5Ch and 7Ch
- Brown-out Reset Protection (1.5V typical)
- Power-on Default Wiper Setting (Mid-scale)
- Low-Power Operation: 90 µA Static Current (typical)
- Wide Operating Voltage Range:
  - 1.8V to 5.5V
- Low Tempco: 15 ppm (typical)
- 100 kHz (typical) Bandwidth (-3 dB) Operation
- Extended Temperature Range (-40°C to +125°C)
- Small Packages, SC70-6
- Lead Free (Pb-free) Package

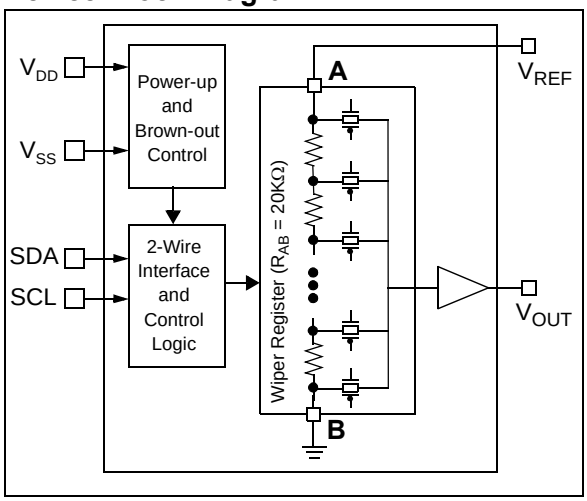
Applications

- Set point or offset trimming
- Cost-sensitive mechanical trim pot replacement

Package Types



Device Block Diagram



Description

The MCP47A1 devices are volatile, 6-Bit digital potentiometers with a buffered output. The wiper setting is controlled through an I^2C serial interface. The I^2C slave addresses of "010 1110" and "011 1110" are supported.

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Device Features

Device	Interface	# of Taps	# of Resistors	V_{REF} Resistance (kΩ)	Data Value Range	POR/BOR Value	I^2C Slave Address	V_{DD} Operating Range	V_{OUT} Range	Package(s)
MCP47A1	I^2C	65	64	20	00h - 40h	20h	5Ch, 7Ch	1.8V (1) to 5.5V	V_{SS} to V_{REF}	SC70-6
MCP47DA1(2)	I^2C	65	64	30	00h - 7Fh	40h	5Ch, 7Ch	1.8V (1) to 5.5V	1/3 V_{REF} to 2/3 V_{REF}	SC70-6, SOT-23-6
MCP4706	I^2C	256	256	210	00h - FFh	7Fh	Cxh (3)	2.7V to 5.5V	V_{SS} to V_{DD} or V_{SS} to V_{REF} (5)	SOT-23-6, DFN-6 (2x2)
MCP4716	I^2C	1024	1024	210	000h - 3FFh	1FFh	Cxh (3)	2.7V to 5.5V	V_{SS} to V_{DD} or V_{SS} to V_{REF} (5)	SOT-23-6, DFN-6 (2x2)
MCP4726	I^2C	4096	4096	210	000h - FFFh	3FFh	Cxh (3)	2.7V to 5.5V	V_{SS} to V_{DD} or V_{SS} to V_{REF} (5)	SOT-23-6, DFN-6 (2x2)
MCP4725	I^2C	4096	4096	N.A.	000h - FFFh	3FFh	Cxh (4)	2.7V to 5.5V	V_{SS} to V_{DD}	SOT-23-6

Note 1: Analog characteristics only tested from 2.7V to 5.5V.

2: Refer to MCP47DA1 Data Sheet (DS25118).

3: The A2:A0 bits are determined by device ordered.

4: The A2 and A1 bits are determined by device ordered and A0 is determined by the state of the A0 pin.

5: User programmable.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} ..... 0.6V to +7.0V
Voltage on SCL, and SDA with respect to V_{SS} ..... -0.6V to V_{DD} + 0.3V
Voltage on all other pins (V_{OUT} and V_{REF}) with respect to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Maximum output current sunk by any Output pin ..... 25 mA
Maximum output current sourced by any Output pin ..... 25 mA
Maximum current out of V_{SS} pin ..... 100 mA
Maximum current into V_{DD} pin ..... 100 mA
Maximum current into V_{REF} pin ..... 250 uA
Maximum current sourced by V_{OUT} pin ..... 40 mA
Maximum current sunk by V_{REF} pin ..... 40 mA
Package power dissipation (T_A = +50°C, T_J = +150°C)
SC70-6 ..... 480 mW
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied ..... -40°C to +125°C
ESD protection on all pins ..... ≥ 6 kV (HBM)
..... ≥ 400V (MM)
..... ≥ 1.5 kV (CDM)
Latchup (JEDEC JESD78A) at +125°C ..... ±100 mA
Soldering temperature of leads (10 seconds) ..... +300°C
Maximum Junction Temperature (T_J) ..... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	Analog Characteristics specified
		1.8	—	5.5	V	Digital Characteristics specified
V_{DD} Start Voltage to ensure Wiper to default reset state	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	**Note 5**			V/ms	
Delay after device exits the reset state (V_{DD} > V_{BOR}) to Digital Interface Active	T_{BORD}	—	—	1	µS	
Delay after device exits the reset state (V_{DD} > V_{BOR}) to V_{OUT} valid	T_{OUTV}			20	µS	Within ± 0.5 LSb of V_{REF} / 2 (for default POR/BOR wiper value).
Supply Current (**Note 6**)	I_{DD}	—	130	220	µA	Serial Interface Active, Write all 0's to Volatile Wiper, No Load on V_{OUT} V_{DD} = 5.5V, V_{REF} = V_{DD}, F_{SCL} = 400 kHz
		—	90	130	µA	Serial Interface Inactive (Static), (Stop condition, SCL = SDA = V_{IH}), No Load on V_{OUT} Wiper = 0, V_{DD} = 5.5V, V_{REF} = V_{DD}
V_{REF} Input Range	V_{REF}	1	—	V_{DD}	V	**Note 7**

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	V_{SS}	—	V	Device Output minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{REF}	—	V	Device Output maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	5	15	24	mA	
Settling Time	$t_{SETTLING}$	—	15	—	µs	
External Reference (V_{REF}) (Note 3)						
Input Capacitance	C_{VREF}	—	7	—	pF	
Total Harmonic Distortion	THD	—	-73	—	dB	V_{REF} = 1.65V ± 0.1V, Frequency = 1 kHz
Dynamic Performance (Note 3)						
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (20h to 1Fh)
Digital Feedthrough		—	<10	—	nV-s	

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Resistance (± 20%)	R_{VREF}	16.0	20	24.0	kΩ	**Note 1,**
Resolution	N		65		Taps	No Missing Codes
Step Resistance	R_S	—	R_{VREF} / 64	—	Ω	**Note 3**
Nominal Resistance Tempco	$\Delta R_{VREF}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C
		—	100	—	ppm/°C	T_A = -40°C to +85°C
		—	150	—	ppm/°C	T_A = -40°C to +125°C
Ratiometeric Tempco	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (20h)
V_{OUT} Accuracy		0.72	0.75	0.78	V	V_{REF} = 1.5V, code = 20h
V_{OUT} Load	L_{VOUTR}	5	—	—	kΩ	Resistive Load
	L_{VOUTC}	—	—	1	nF	Capacitive Load
Maximum current through Terminal (V_{REF}) **Note 3**	I_{VREF}	—	—	345	µA	V_{REF} = 5.5V
Leakage current into V_{REF}	I_L	—	100	—	nA	V_{REF} = V_{SS}
Full-Scale Error (code = 40h)	V_{FSE}	-1	±0.35	+1	LSb	V_{REF} = V_{DD}
Zero-Scale Error (code = 00h)	V_{ZSE}	-0.75	±0.35	+0.75	LSb	V_{REF} = V_{DD}
V_{OUT} Integral Nonlinearity	INL	-1	±0.25	+1	LSb	**Note 2,** V_{REF} = V_{DD}
V_{OUT} Differential Nonlinearity	DNL	-0.5	±0.25	+0.5	LSb	**Note 2,** V_{REF} = V_{DD}
Bandwidth -3 dB	BW	—	100	—	kHz	V_{DD} = 5.0V, V_{REF} = 3.0V ± 2.0V, Code = 20h
Capacitance (V_{REF})	C_{REF}	—	75	—	pF	f =1 MHz, Code = Full-Scale

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to +5.5V. C_L = 1 nF, R_L = 5 kΩ . Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Digital Inputs/Outputs (SDA, SCK)								
Schmitt Trigger High Input Threshold	V_{IH}	0.7 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V		
Schmitt Trigger Low Input Threshold	V_{IL}	-0.5	—	0.3V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V		
Hysteresis of Schmitt Trigger Inputs **(Note 3)**	V_{HYS}	N.A.	—	—	V	SDA and SCL	100 kHz	V_{DD} < 2.0V
		N.A.	—	—	V			V_{DD} ≥ 2.0V
		0.1 V_{DD}	—	—	V		400 kHz	V_{DD} < 2.0V
		0.05 V_{DD}	—	—	V			V_{DD} ≥ 2.0V
Output Low Voltage (SDA)	V_{OL}	V_{SS}	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA		
		V_{SS}	—	0.2V_{DD}	V	V_{DD} < 2.0V, I_{OL} = 1 mA		
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{REF} = V_{DD} and V_{REF} = V_{SS}		
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 400 kHz		
RAM (Wiper) Value								
Value Range	N	0h	—	40h	hex			
Wiper POR/BOR Value	$N_{POR/BOR}$	20h			hex			
Power Requirements								
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%		V_{REF} = V_{DD}, Code = 20h	

Note 1: Resistance is defined as the resistance between the V_{REF} pin and the V_{SS} pin.

2: INL and DNL are measured at V_{OUT} from Code = 00h (Zero-Scale) through Code = 3Fh (Full-Scale - 1).

3: This specification by design.

4: Nonlinearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature.

5: POR/BOR is not rate dependent.

6: Supply current is independent of V_{REF} current.

7: See **Section 7.1.3**.

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1.1 I²C Mode Timing Waveforms and Requirements

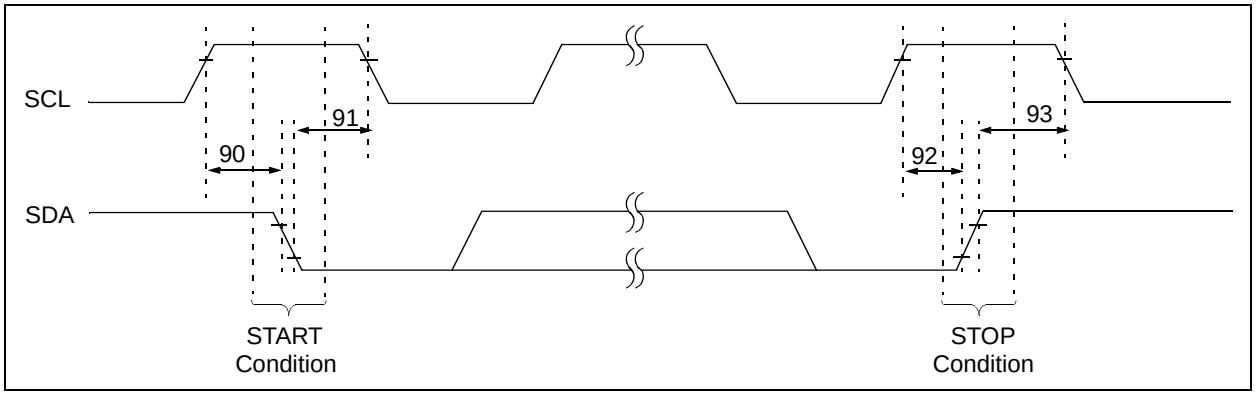
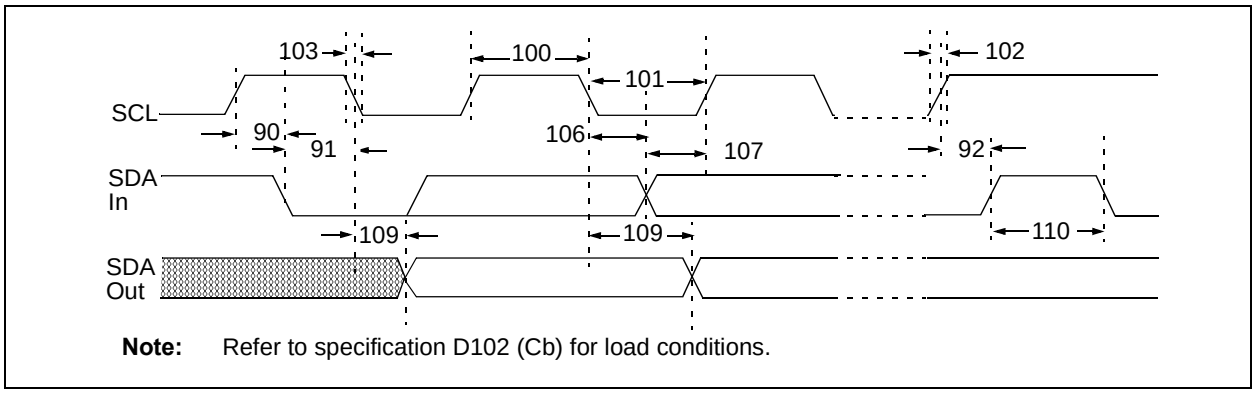


FIGURE 1-1: *I²C Bus Start/Stop Bits Timing Waveforms.*



Note: Refer to specification D102 (Cb) for load conditions.

FIGURE 1-2: *I²C Bus Data Timing.*

TABLE 1-1: I²C BUS START/STOP BITS REQUIREMENTS

I²C AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **Section 2.0 "Typical Performance Curves"**				
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
D102	Cb	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	ns	
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
92	TSU:STO	STOP condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	

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TABLE 1-2: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

I²C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage VDD range is described in **AC/DC characteristics**			
Parameter No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	T_{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
101	T_{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
102A(5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
102B(5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
103A (5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	40	ns	
103B (5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb(5)	300	ns	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V (**Note 6**)
			400 kHz mode	0	—	ns	2.7V-5.5V (**Note 6**)
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**Note 5**
			400 kHz mode	100	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	**Note 5**
			400 kHz mode	—	900	ns	
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	Philips Spec states N.A.
			400 kHz mode	—	50	ns	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement tsu; DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP47A1 device must provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to guarantee that the output data will meet the setup and hold specifications for the receiving device.

4: Use C_b in pF for the calculations.

5: Not tested.

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 6L-SC70	θ_{JA}	—	207	—	°C/W	**Note 1**

Note 1: Package Power Dissipation (P_{DIS}) is calculated as follows:
$P_{DIS} = (T_J - T_A) / \theta_{JA}$,
where: T_J = Junction Temperature, T_A = Ambient Temperature.

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2.0 TYPICAL PERFORMANCE CURVES

Note 1: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

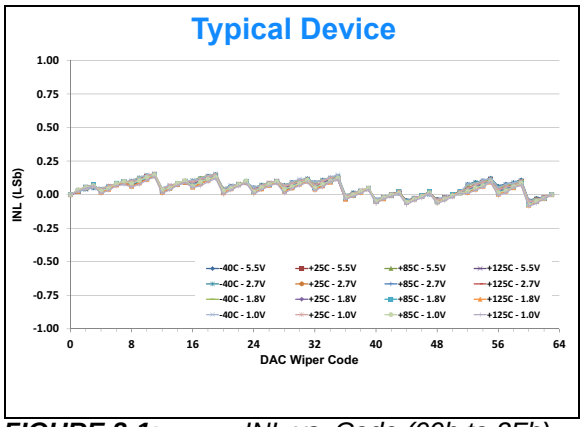


FIGURE 2-1: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

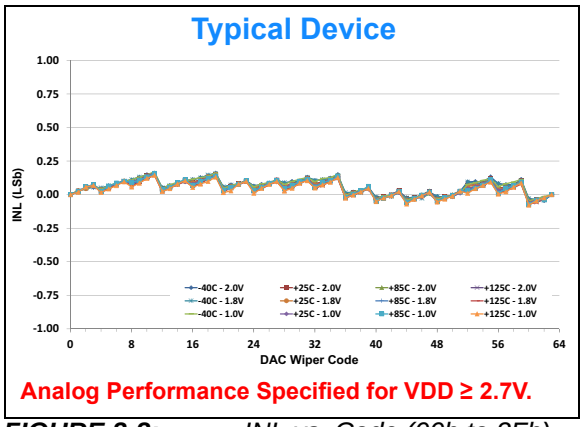


FIGURE 2-3: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

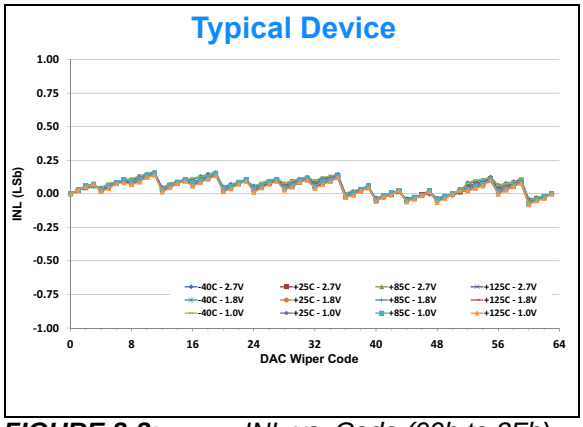


FIGURE 2-2: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

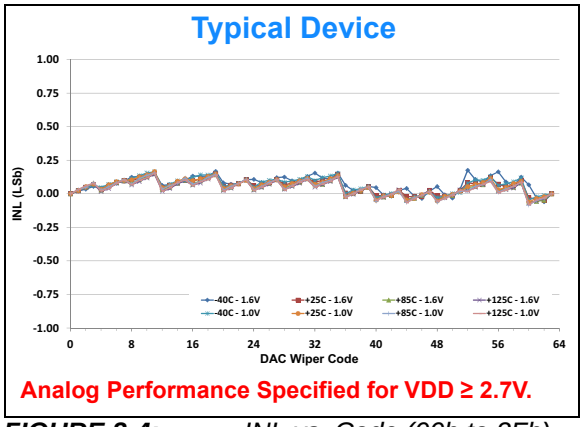


FIGURE 2-4: *INL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

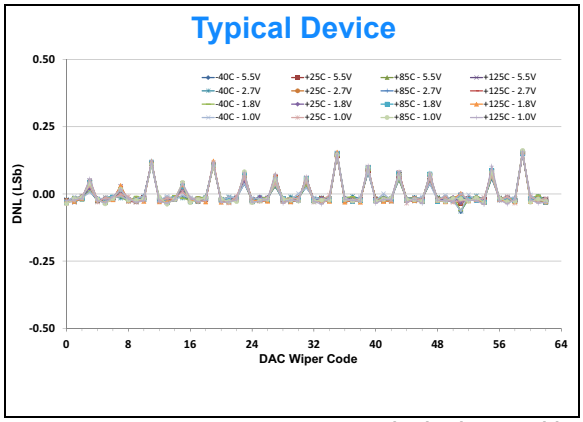


FIGURE 2-5: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

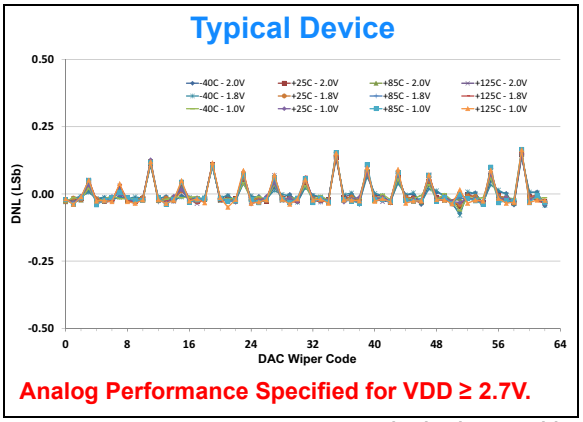


FIGURE 2-7: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

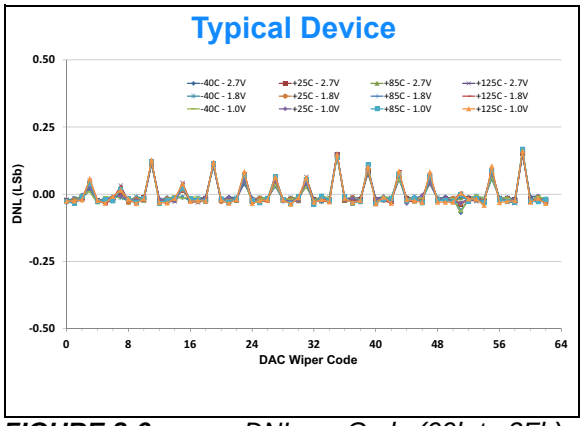


FIGURE 2-6: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

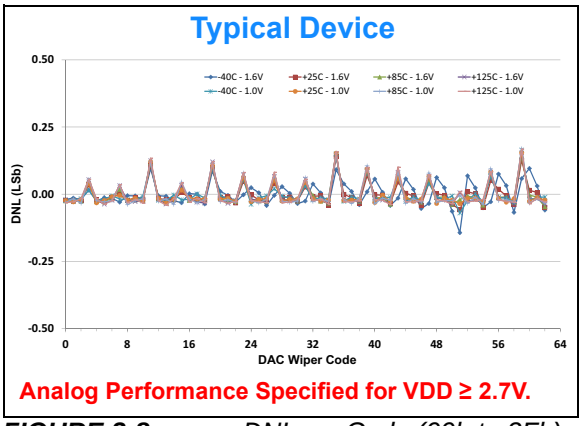


FIGURE 2-8: *DNL vs. Code (00h to 3Fh) and Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

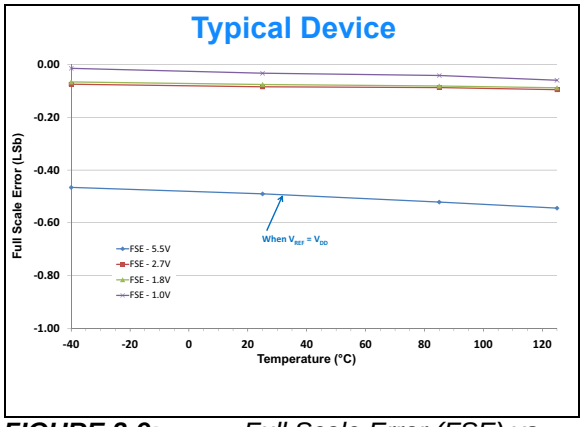


FIGURE 2-9: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

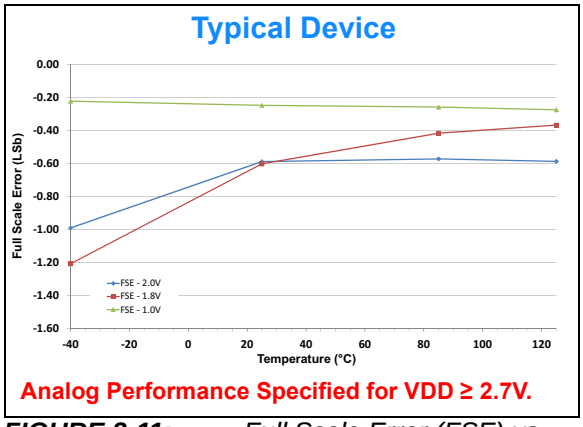


FIGURE 2-11: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

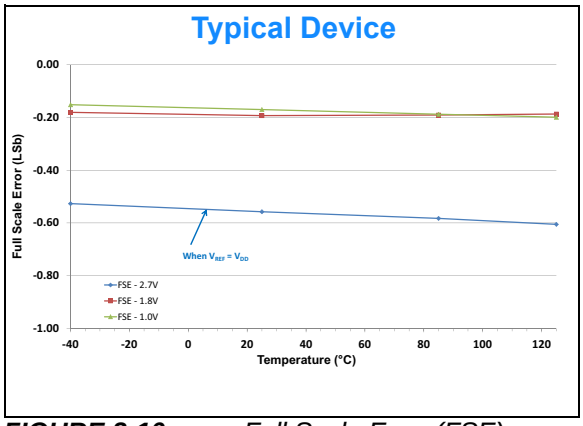


FIGURE 2-10: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

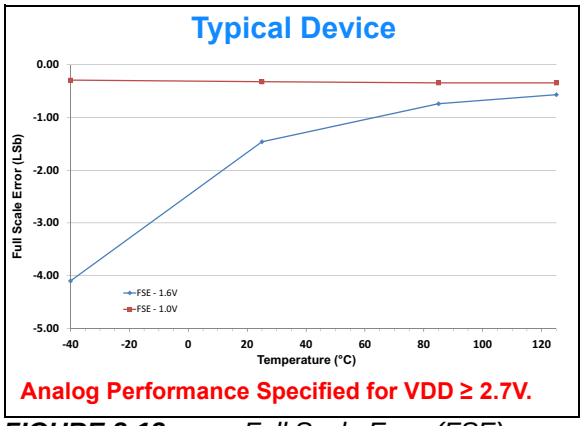


FIGURE 2-12: *Full Scale Error (FSE) vs. Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

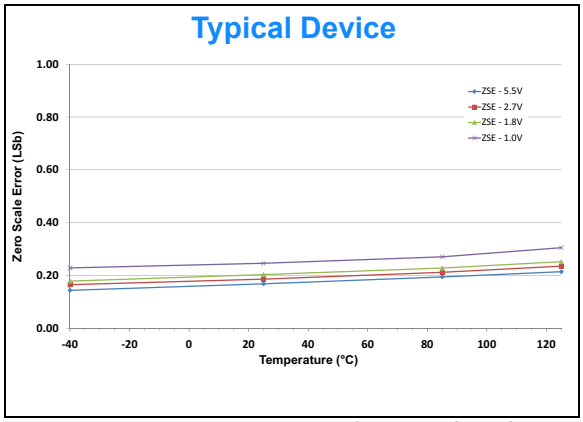


FIGURE 2-13: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.

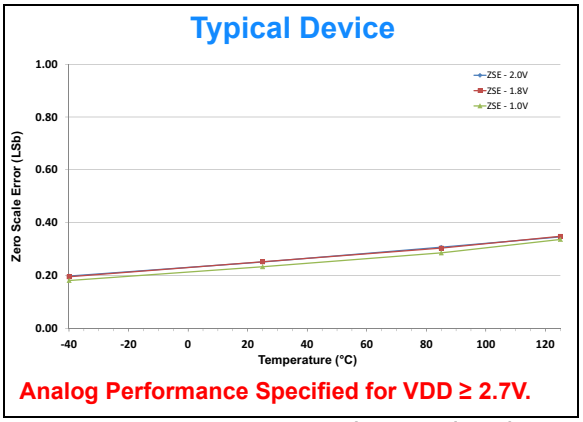


FIGURE 2-15: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.

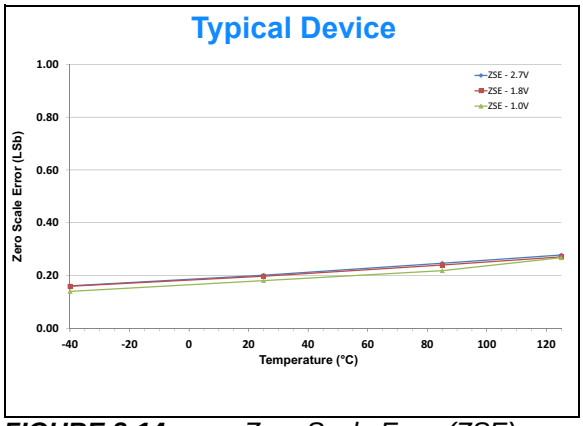


FIGURE 2-14: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.

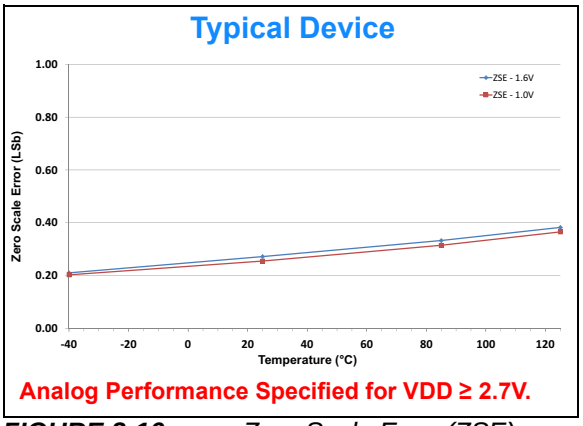


FIGURE 2-16: *Zero Scale Error (ZSE) vs. Temperature.*
V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

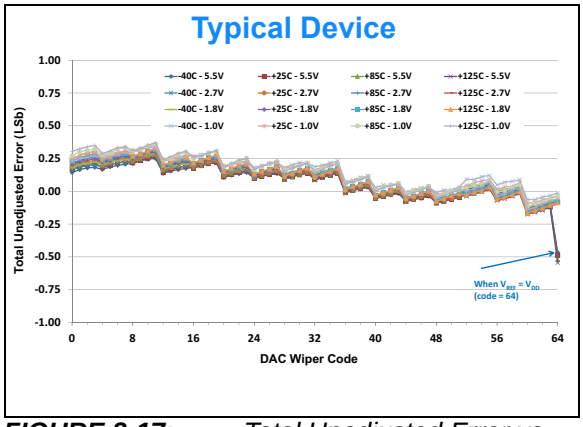


FIGURE 2-17: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.*

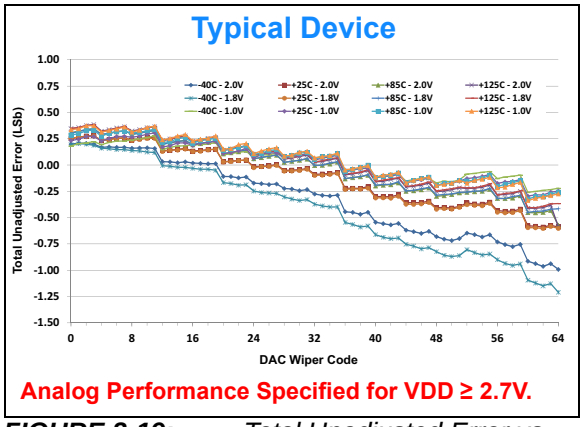


FIGURE 2-19: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.*

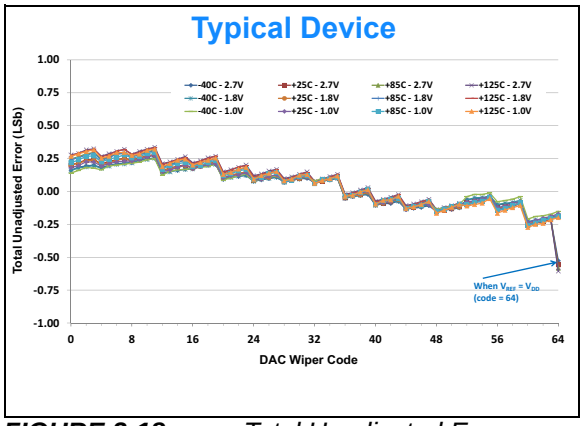


FIGURE 2-18: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.*

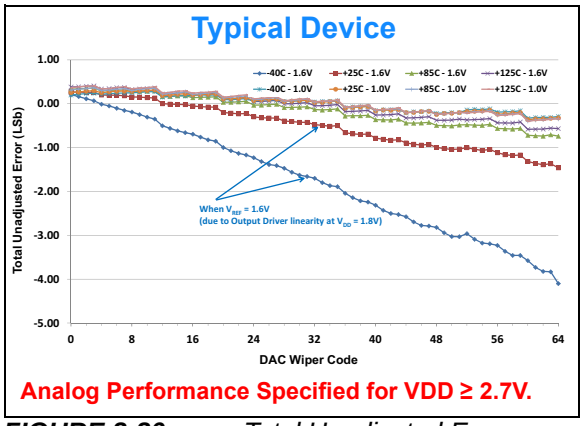


FIGURE 2-20: *Total Unadjusted Error vs. Code and Temperature. V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

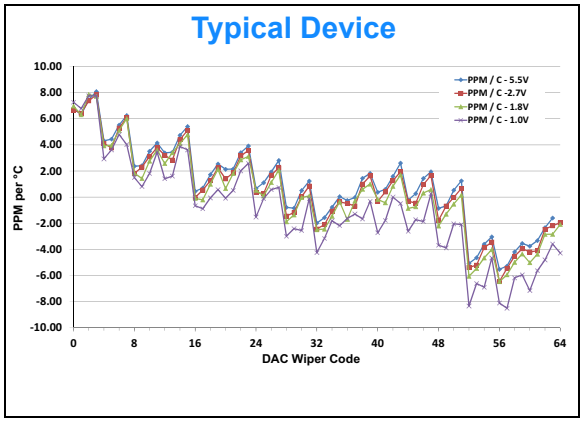


FIGURE 2-21: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000), V_{DD} = 5.5V, V_{REF} = 5.5V, 2.7V, 1.8V, and 1.0V.*

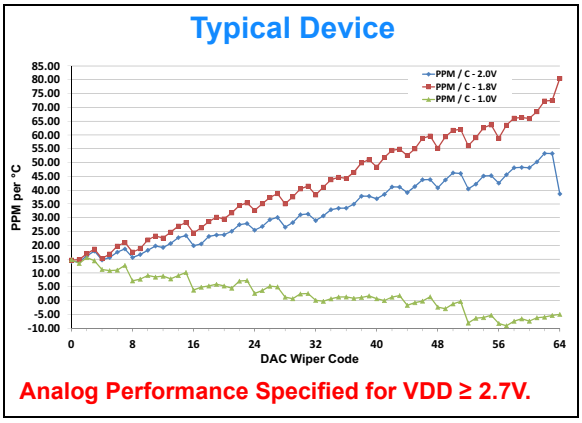


FIGURE 2-23: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000), V_{DD} = 2.0V, V_{REF} = 2.0V, 1.8V, and 1.0V.*

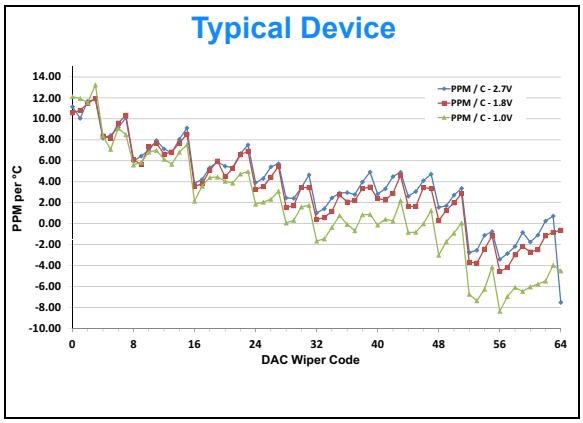


FIGURE 2-22: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000), V_{DD} = 2.7V, V_{REF} = 2.7V, 1.8V, and 1.0V.*

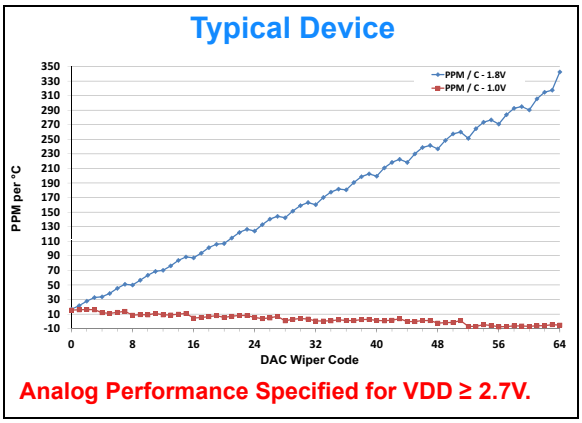


FIGURE 2-24: *V_{OUT} Tempco vs. Code (((($V_{OUT(+125C)}$ - $V_{OUT(-40C)}$) / $V_{OUT(+25C,Code=FS)}$) / 165) * 1,000,000), V_{DD} = 1.8V, V_{REF} = 1.6V, and 1.0V.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

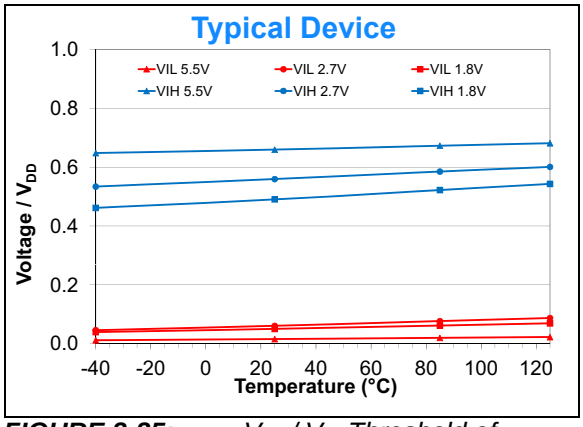


FIGURE 2-25: *V_{IH} / V_{IL} Threshold of SDA/SCL Inputs vs. Temperature and V_{DD}.*

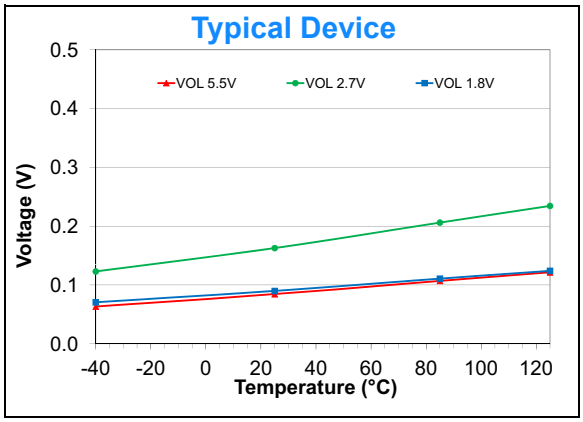


FIGURE 2-26: *V_{OL} (SDA) vs. V_{DD} and Temperature.*

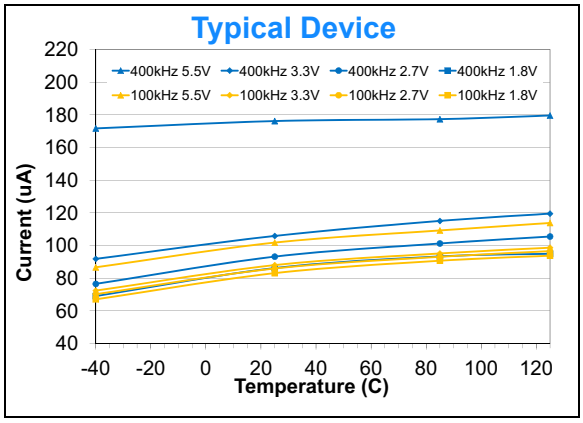


FIGURE 2-27: *Interface Active Current (I_{DD}) vs. SCL Frequency (f_{SCL}) and Temperature V_{DD} = 1.8V, 2.7V and 5.5V, V_{REF} = 1.0V and V_{DD}. (no load on V_{OUT}).*

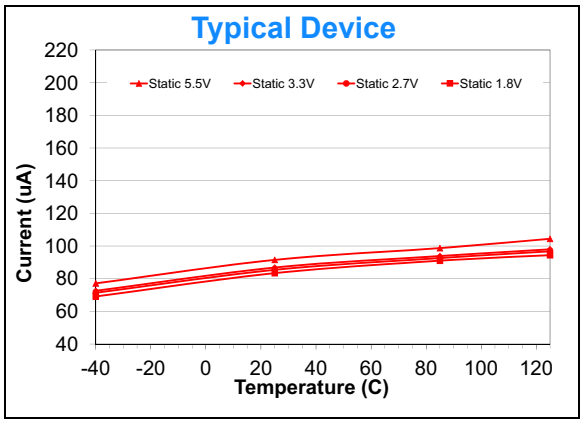


FIGURE 2-28: *Interface Inactive Current (STATIC) vs. Temperature and V_{DD}. V_{DD} = 1.8V, 2.7V and 5.5V, V_{REF} = 1.0V and V_{DD}. (no load on V_{OUT}, SCL = SDA = V_{DD}).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

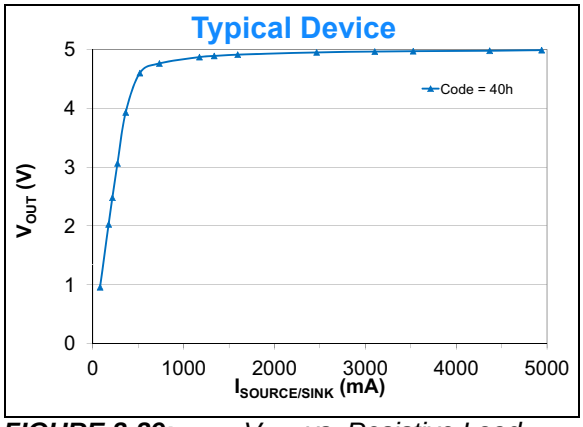


FIGURE 2-29: *V_{OUT} vs. Resistive Load. V_{DD} = 5.0V.*

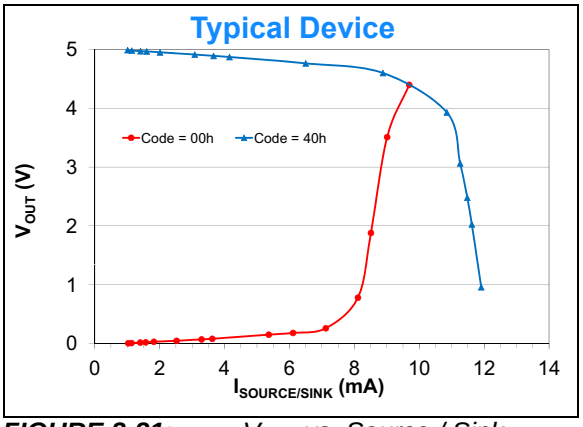


FIGURE 2-31: *V_{OUT} vs. Source / Sink Current. V_{DD} = 5.0V.*

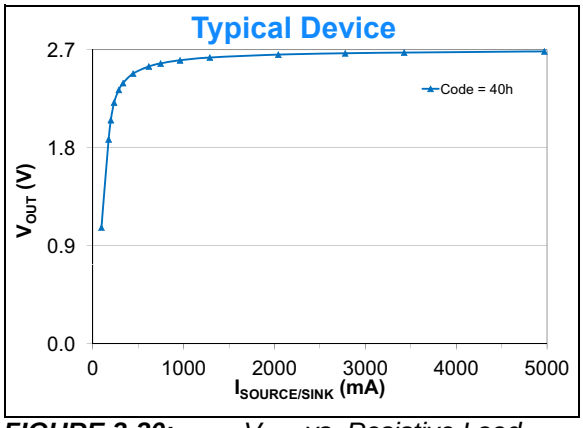


FIGURE 2-30: *V_{OUT} vs. Resistive Load. V_{DD} = 2.7V.*

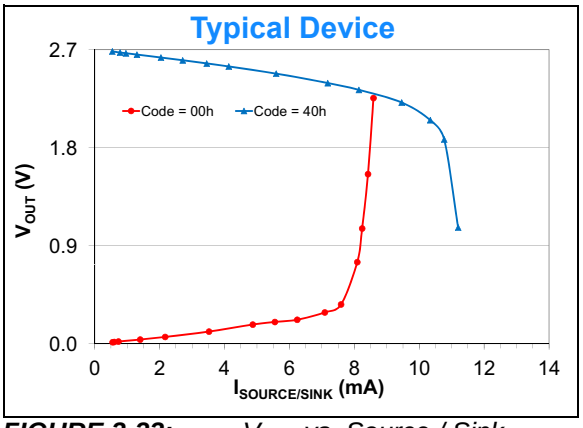


FIGURE 2-32: *V_{OUT} vs. Source / Sink Current. V_{DD} = 2.7V.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

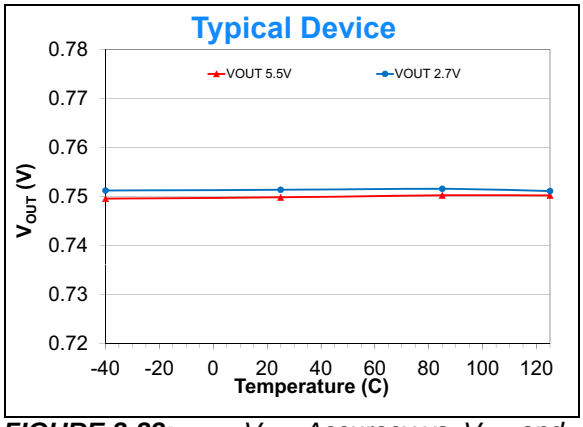


FIGURE 2-33: *V_{OUT} Accuracy vs. V_{DD} and Temperature.*

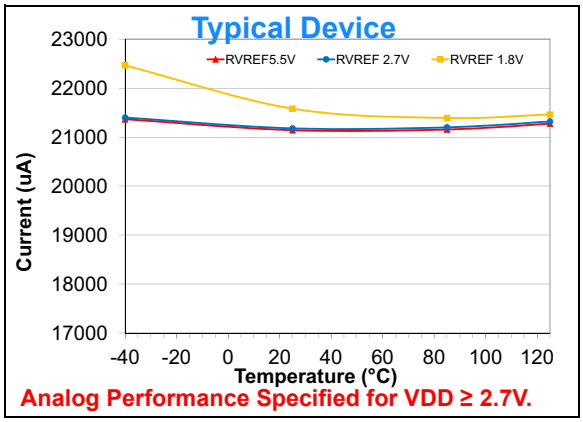


FIGURE 2-34: *R_{VREF} Resistances vs. V_{DD} and Temperature.*

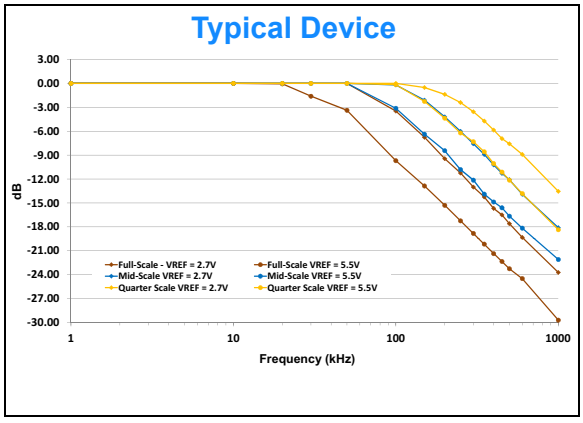


FIGURE 2-35: *-3dB Bandwidth vs Frequency, V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

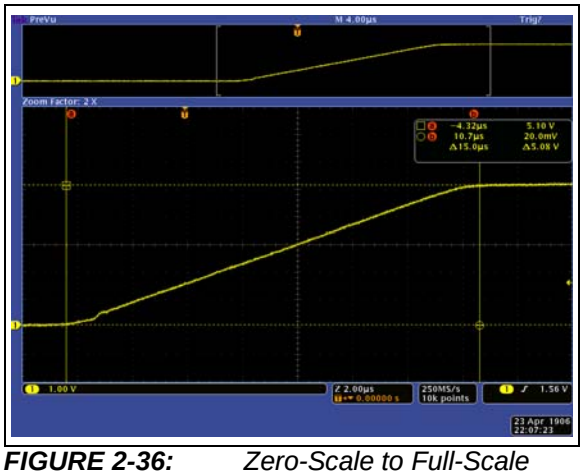


FIGURE 2-36: *Zero-Scale to Full-Scale Settling Time (00h to 40h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF (Time scale = 2 µs / div).*

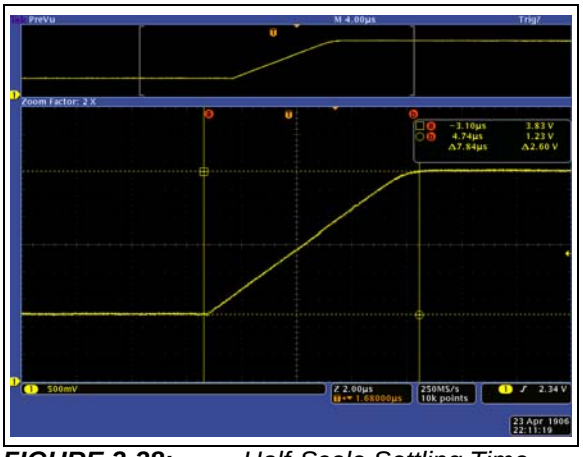


FIGURE 2-38: *Half-Scale Settling Time (10h to 30h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF. (Time scale = 2 µs / div)*

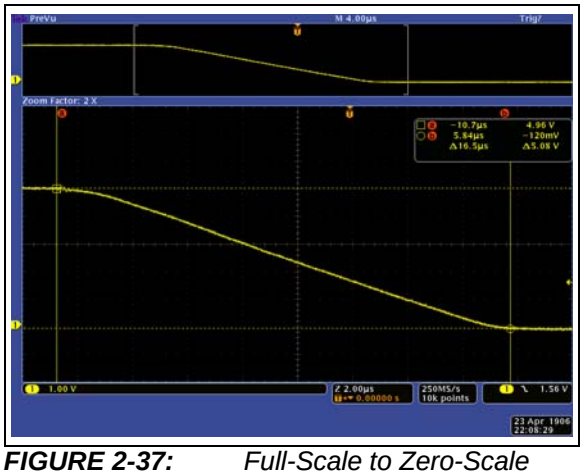


FIGURE 2-37: *Full-Scale to Zero-Scale Settling Time (40h to 00h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF (Time scale = 2 µs / div).*



FIGURE 2-39: *Half-Scale Settling Time (30h to 10h), V_{DD} = 5.0V, V_{REF} = 5.0V, R_L = 5kΩ, C_L = 200 pF (Time scale = 2 µs / div).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = V_{REF} = 5V, V_{SS} = 0V, R_L = 5 kΩ, C_L = 1 nF.

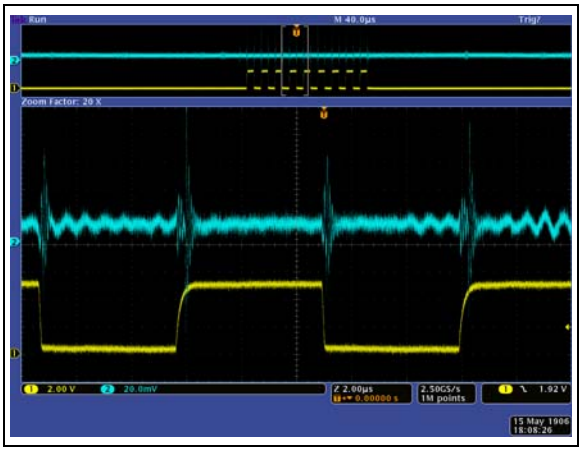


FIGURE 2-40: *Digital Feedthrough (SCL signal coupling to V_{OUT} pin); V_{DD} = 5.0V, V_{REF} = 5.0V, F_{SCL} = 100 kHz, V_{OUT} = 20h (V_{OUT} Voltage Scale = 20 mV/div, Time scale = 2 µs / div).*

2.1 Test Circuit

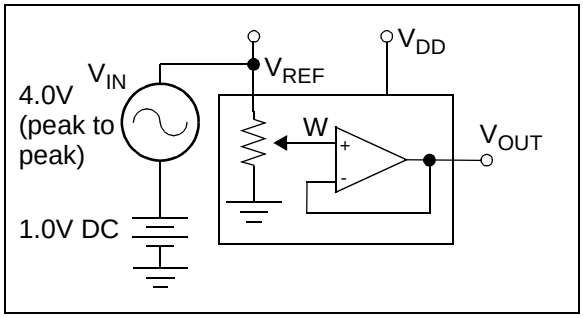


FIGURE 2-41: *-3 db Gain vs. Frequency Test.*

NOTES:

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1. Additional descriptions of the device pins follow.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP47A1

Pin Name	Package	Pin Type	Buffer Type	Function
	SC70-6			
V_{DD}	1	P	—	Positive Power Supply Input
V_{SS}	2	P	—	Ground
SCL	3	I/O	ST (OD)	I^2C Serial Clock pin
SDA	4	I/O	ST (OD)	I^2C Serial Data pin
V_{OUT}	5	I/O	A	Output voltage
V_{REF}	6	I/O	A	Reference Voltage for V_{OUT} output

Legend: A = Analog input, I = Input, ST (OD) = Schmitt Trigger with Open Drain, O = Output, I/O = Input/Output, P = Power

3.1 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device's positive power supply input. The input power supply is relative to V_{SS} and can range from 1.8V to 5.5V. A decoupling capacitor on V_{DD} (to V_{SS}) is recommended to achieve maximum performance. Analog specifications are tested from 2.7V.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.3 I^2C Serial Clock (SCL)

The SCL pin is the serial clock pin of the I^2C interface. The MCP47A1 acts only as a slave and the SCL pin accepts only external serial clocks. The SCL pin is an open-drain output. Refer to **Section 5.0 "Serial Interface - I^2C Module"** for more details of I^2C Serial Interface communication.

3.4 I^2C Serial Data (SDA)

The SDA pin is the serial data pin of the I^2C interface. The SDA pin has a Schmitt trigger input and an open-drain output. Refer to **Section 5.0 "Serial Interface - I^2C Module"** for more details of I^2C Serial Interface communication.

3.5 Analog Output Voltage Pin (V_{OUT})

V_{OUT} is the DAC analog output pin. The DAC output has an output amplifier.

V_{OUT} can swing from approximately V_{ZS} (= V_{SS}) to V_{FS} (= V_{REF}). In normal mode, the DC impedance of the output pin is about 1Ω . See **Section 7.0 "Output Buffer"** for more information.

3.6 Voltage Reference Pin (V_{REF})

This pin is the external voltage reference input. The V_{REF} pin signal is unbuffered so the reference voltage must have the current capability not to drop its voltage when connected to the internal resistor ladder circuit (20 kΩ typical). See **Section 6.0 "Resistor Network"** for more information.

NOTES:

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4.0 GENERAL OVERVIEW

The MCP47A1 device is a general purpose DAC intended to be used in applications where a programmable voltage output with moderate bandwidth is desired.

Applications generally suited for the MCP47A1 devices include:

- Set point or offset trimming
- Sensor calibration
- Cost-sensitive mechanical trim pot replacement

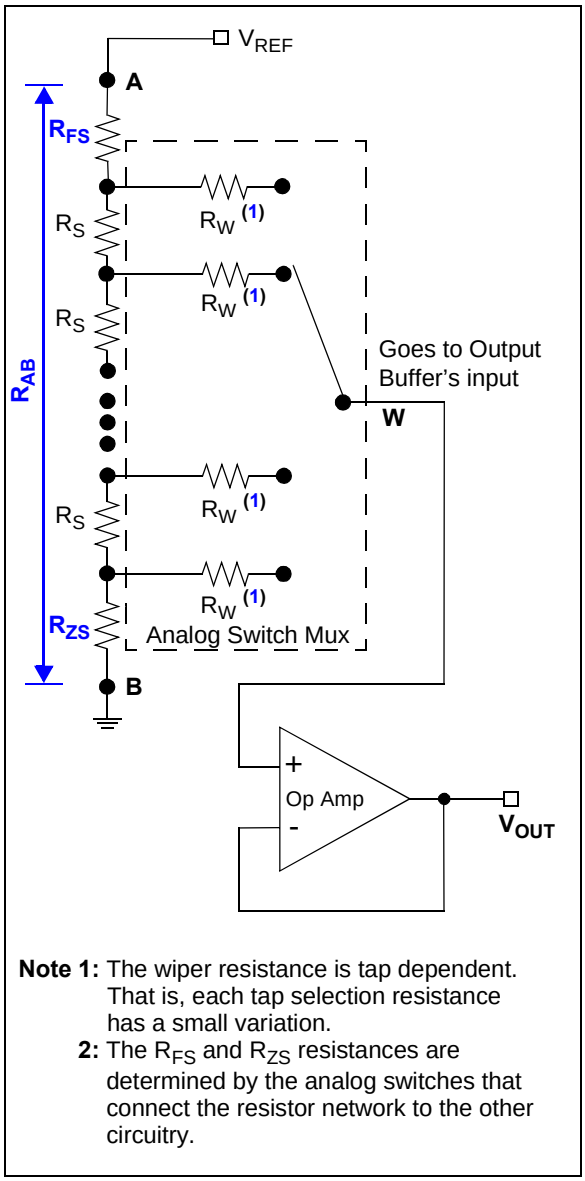
The MCP47A1 has four main functional blocks. These are:

- **POR/BOR Operation**
- **Serial Interface - I²C Module**
- **Resistor Network**
- **Output Buffer**

The POR/BOR operation is discussed in this section and the I²C and Resistor Network operation are described in their own sections. The commands are discussed in **Section 5.3, Serial Commands**.

Figure 4-1 shows a block diagram for the resistive network of the device. An external pin, called V_{REF}, is the DAC's reference voltage. The resistance from the V_{REF} pin to ground is typically 20 kΩ. The reference voltage connected to the V_{REF} pin needs to support this resistive load.

This resistor network functions as a windowed voltage divider. This means that the V_{OUT} pin's voltage range is from approximately V_{SS} to approximately V_{REF}.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation.

2: The R_{FS} and R_{ZS} resistances are determined by the analog switches that connect the resistor network to the other circuitry.

FIGURE 4-1: *Resistor Network and Output Buffer Block Diagram.*

4.1 POR/BOR Operation

The Power-on Reset is the case where the device has power applied to it from V_{SS}. The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). This ensures that when the device Power-on Reset occurs, the logic can retain default values that are loaded. The maximum V_{POR}/V_{BOR} voltage is less than 1.8V. When $V_{POR}/V_{BOR} < V_{DD} < 1.8V$, the DACs' electrical performance may not meet the data sheet specifications.

Table 4-2 shows the DAC's level of functionality across the entire V_{DD} range, while Figure 4-2 illustrates the Power-up and Brown-out functionality.

4.1.1 POWER-ON RESET

When the device powers up, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage. Once the V_{DD} voltage crosses the V_{POR}/V_{BOR} voltage, the following happens:

- Volatile Serial Shift Register / Wiper register is loaded with the default values (see Table 4-1)
- The device is capable of digital operation

Note:	At voltages below $V_{DD(MIN)}$, the electrical performance of the I^2C interface may not meet the data sheet specifications

TABLE 4-1: DEFAULT POR WIPER SETTING SELECTION

Default POR Wiper Setting	Serial Shift Register (SSR)	Wiper Register
Mid-scale	20h	20h

4.1.2 BROWN-OUT RESET

When the device powers down, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage ($V_{BOR} < 1.8V$). Once the V_{DD} voltage decreases below the V_{POR}/V_{BOR} voltage, the following happens:

- Serial Interface is disabled

If the V_{DD} voltage decreases below the V_{RAM} voltage, the following happens:

- Volatile Serial Shift Register (SSR) and Wiper register may become corrupted

As the voltage recovers above the V_{POR}/V_{BOR} voltage, see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a Brown-out condition may cause the memory location to become corrupted.

4.1.3 WIPER REGISTER (RAM)

The Wiper Register is 7-bit volatile memory that starts functioning at the RAM retention voltage (V_{RAM}). The Wiper Register will be loaded with the default wiper value when V_{DD} rises above the V_{POR}/V_{BOR} voltage.

4.1.4 DEVICE CURRENTS

The current of the device can be classified into two modes of the device operation. These are:

- Serial Interface Inactive (Static Operation)
- Serial Interface Active

Static Operation occurs when a Stop condition is received. Static Operation is exited when a Start condition is received.

TABLE 4-2: DEVICE FUNCTIONALITY AT EACH V_{DD} REGION (Note 1)

V_{DD} Level	Serial Interface	V_{OUT}	DAC Register Setting	Comment
$V_{DD} < V_{TH}$	Ignored	"Unknown"	Unknown	
$V_{TH} < V_{DD} < V_{BOR}$	Ignored	Pulled Low	Unknown	
$V_{BOR} \leq V_{DD} < 1.8V$	"Unknown"	Operational with reduced electrical specifications	DAC Register loaded with POR/BOR value	
$1.8V \leq V_{DD} \leq 5.5V$	Accepted	Operational	DAC Register determines Serial Value	Meets the data sheet specifications

Note 1: For system voltages below the minimum operating voltage, it is recommended to use a voltage supervisor to hold the system in reset. This will ensure that MCP47x1 commands are not attempted out of the operating range of the device.

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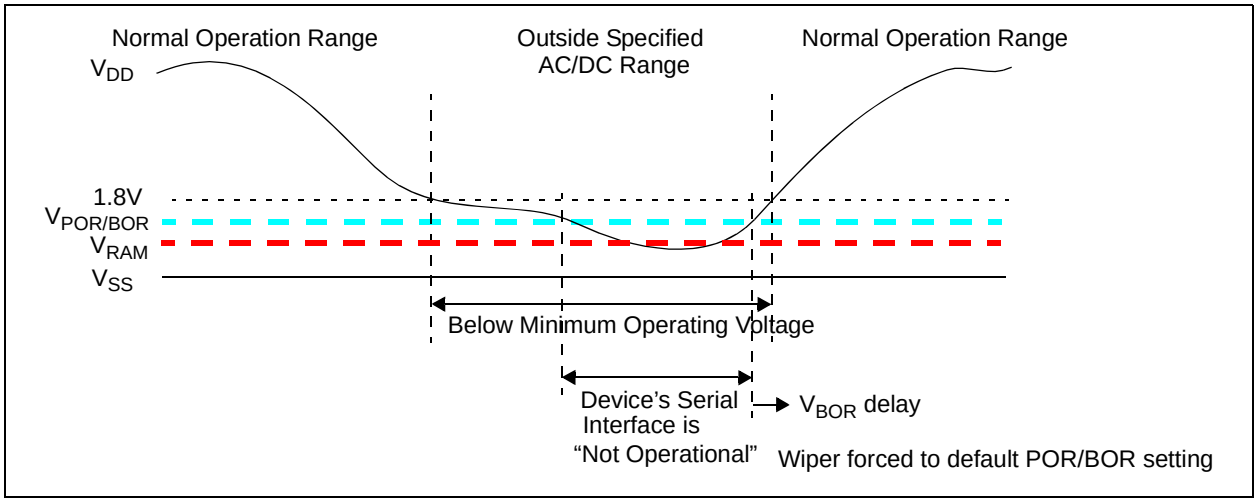


FIGURE 4-2: *Power-up and Brown-out.*

NOTES:

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5.0 SERIAL INTERFACE - I²C MODULE

A 2-wire I²C serial protocol is used to write or read the DAC's wiper register. The I²C protocol utilizes the SCL input pin and SDA input/output pin.

The I²C serial interface supports the following features:

- Slave mode of operation
- 7-bit addressing
- The following clock rate modes are supported:
  - Standard mode, bit rates up to 100 kb/s
  - Fast mode, bit rates up to 400 kb/s
- Support Multi-Master Applications

The serial clock is generated by the Master.

The I²C Module is compatible with the NXP I²C specification (# UM10204). Only the field types, field lengths, timings, etc. of a frame are defined. The frame *content* defines the behavior of the device. The frame content for the MCP47A1 device is defined in this section of the data sheet.

Figure 5-1 shows a typical I²C bus configuration.

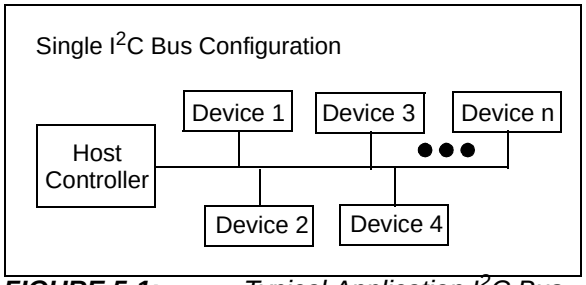


FIGURE 5-1: *Typical Application I²C Bus Configurations.*

Refer to **Section 2.0 "Typical Performance Curves"**, AC/DC Electrical Characteristics table for detailed input threshold and timing specifications.

5.1 I²C I/O Considerations

I²C specifications require active low, passive high functionality on devices interfacing to the bus. Since devices may be operating on separate power supply sources, ESD clamping diodes are not permitted. The specification recommends using open drain transistors tied to V_{SS} (common) with a pull-up resistor. The specification makes some general recommendations on the size of this pull-up, but does not specify the exact value since bus speeds and bus capacitance impacts the pull-up value for optimum system performance.

Common pull-up values range from 1 kΩ to a maximum of ~10 kΩ. Power sensitive applications tend to choose higher values to minimize current losses during communication but these applications also typically utilize lower V_{DD}.

The SDA and SCL float (are not driving) when the device is powered down.

A "glitch" filter is on the SCL and SDA pins when the pin is an input. When these pins are an output, there is a slew rate control of the pin that is independent of device frequency.

5.1.1 SLOPE CONTROL

The device implements slope control on the SDA output. The slope control is defined by the fast mode specifications.

For Fast (FS) mode, the device has spike suppression and Schmidt trigger inputs on the SDA and SCL pins.

5.2 I²C Bit Definitions

I²C bit definitions include:

- **Start Bit**
- **Data Bit**
- **Acknowledge (A) Bit**
- **Repeated Start Bit**
- **Stop Bit**
- **Clock Stretching**

Figure 5-8 shows the waveform for these states.

5.2.1 START BIT

The Start bit (see Figure 5-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is “High”.

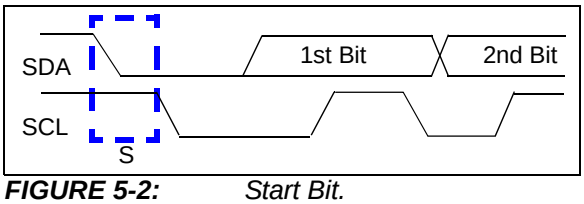


FIGURE 5-2: *Start Bit.*

5.2.2 DATA BIT

The SDA signal may change state while the SCL signal is Low. While the SCL signal is High, the SDA signal MUST be stable (see Figure 5-3).

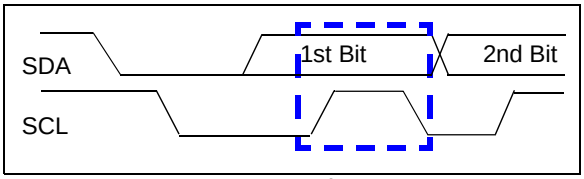


FIGURE 5-3: *Data Bit.*

5.2.3 ACKNOWLEDGE (A) BIT

The A bit (see Figure 5-4) is a response from the Slave device to the Master device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically the Slave device will supply an A response after the Start bit and 8 “data” bits have been received. The A bit will have the SDA signal low.

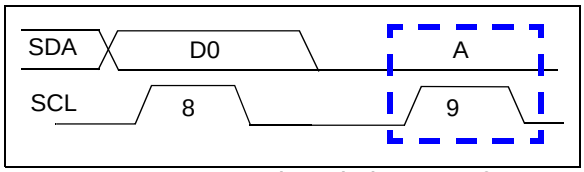


FIGURE 5-4: *Acknowledge Waveform.*

If the Slave Address is not valid, the Slave Device will issue a Not A ($\overline{A}$). The $\overline{A}$ bit will have the SDA signal high.

If an error condition occurs (such as an $\overline{A}$ instead of A) then a START bit must be issued to reset the command state machine.

TABLE 5-1: MCP47A1 A / $\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	$\overline{A}$	
Slave Address valid	A	
Slave Address not valid	$\overline{A}$	
Bus Collision	N.A.	I²C Module Resets, or a “Don’t Care” if the collision occurs on the Masters “Start bit”.

5.2.4 REPEATED START BIT

The Repeated Start bit (see Figure 5-5) indicates the current Master Device wishes to continue communicating with the current Slave Device without releasing the I²C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is “High”.

Note 1: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

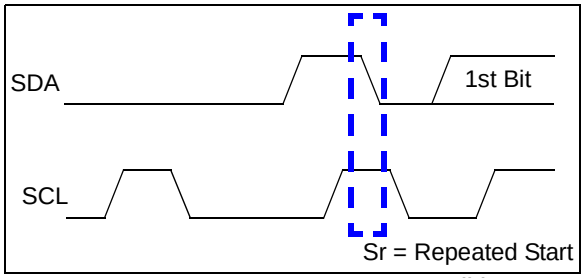


FIGURE 5-5: *Repeat Start Condition Waveform.*

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5.2.5 STOP BIT

The Stop bit (see Figure 5-6) indicates the end of the I^2C Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is “High”.

A Stop bit resets the I^2C interface of the other devices.

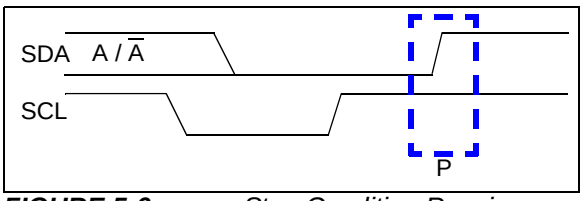


FIGURE 5-6: *Stop Condition Receive or Transmit Mode.*

5.2.6 CLOCK STRETCHING

“Clock Stretching” is something that the secondary device can do, to allow additional time to “respond” to the “data” that has been received.

The MCP47A1 will not stretch the clock signal (SCL) since memory read accesses occur fast enough.

5.2.7 ABORTING A TRANSMISSION

If any part of the I^2C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a START or STOP condition. This is done so that noisy transmissions (usually an extra START or STOP condition) are aborted before they corrupt the device.

5.2.8 IGNORING AN I^2C TRANSMISSION AND “FALLING OFF” THE BUS

The MCP47A1 expects to receive entire, valid I^2C commands and will assume any command not defined as a valid command is due to a bus corruption, and will enter a passive high condition on the SDA signal. All signals will be ignored until the next valid START condition and CONTROL BYTE are received.

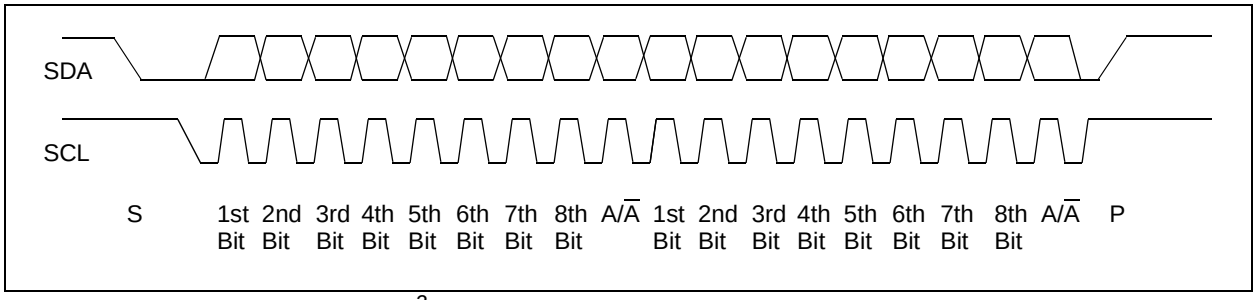


FIGURE 5-7: *Typical 16-bit I^2C Waveform Format.*

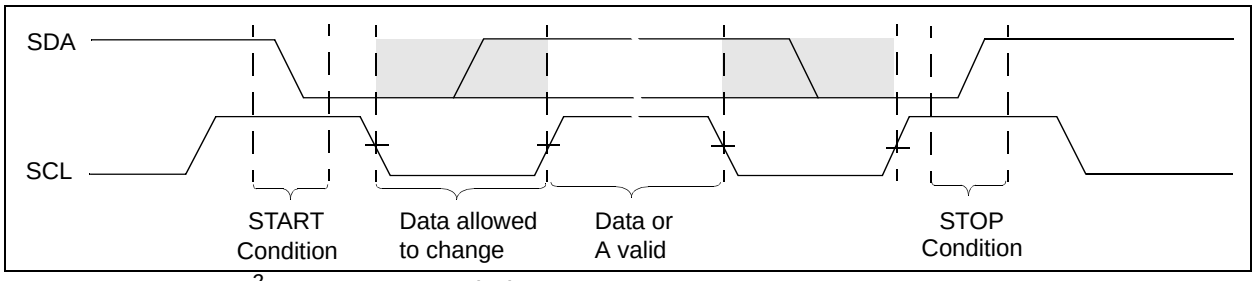


FIGURE 5-8: *I^2C Data States and Bit Sequence.*

5.2.9 I²C COMMAND PROTOCOL

The MCP47A1 is a slave I²C device which supports 7-bit slave addressing. The slave address contains seven fixed bits. Figure 5-9 shows the control byte format.

5.2.9.1 Control Byte (Slave Address)

The Control Byte is always preceded by a START condition. The Control Byte contains the slave address consisting of seven fixed bits and the R/$\overline{W}$ bit. Figure 5-9 shows the control byte format and Table 5-2 shows the I²C address for the devices.

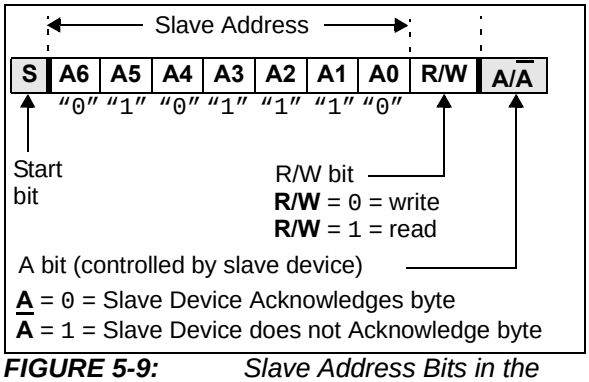


FIGURE 5-9: *Slave Address Bits in the I²C Control Byte.*

TABLE 5-2: DEVICE I²C ADDRESS

Device	I²C Address			
	Binary	Hex (1)	Code	Comment
MCP47A1	'0101110'	0x5C	A0	
	'0111110'	0x7C	A1	

Note 1: The LSb of the 8-bit hex code is the I²C Read/Write (R/W) bit. This hex value has a R/W bit = "0" (write). If the R/W bit reflected a read, these values would be 0x5D and 0x7D.

Note 1: The MCP47A1 device supports two different I²C address (A0 and A1). This allows two MCP47A1 devices on the same I²C bus.

5.2.9.2 Hardware Address Pins

The MCP47A1 does not support hardware address bits.

5.2.10 GENERAL CALL

The General Call is a method that the Master device can communicate with all other Slave devices.

The MCP47A1 devices do not respond to General Call address and commands, and therefore the communications are Not Acknowledged.

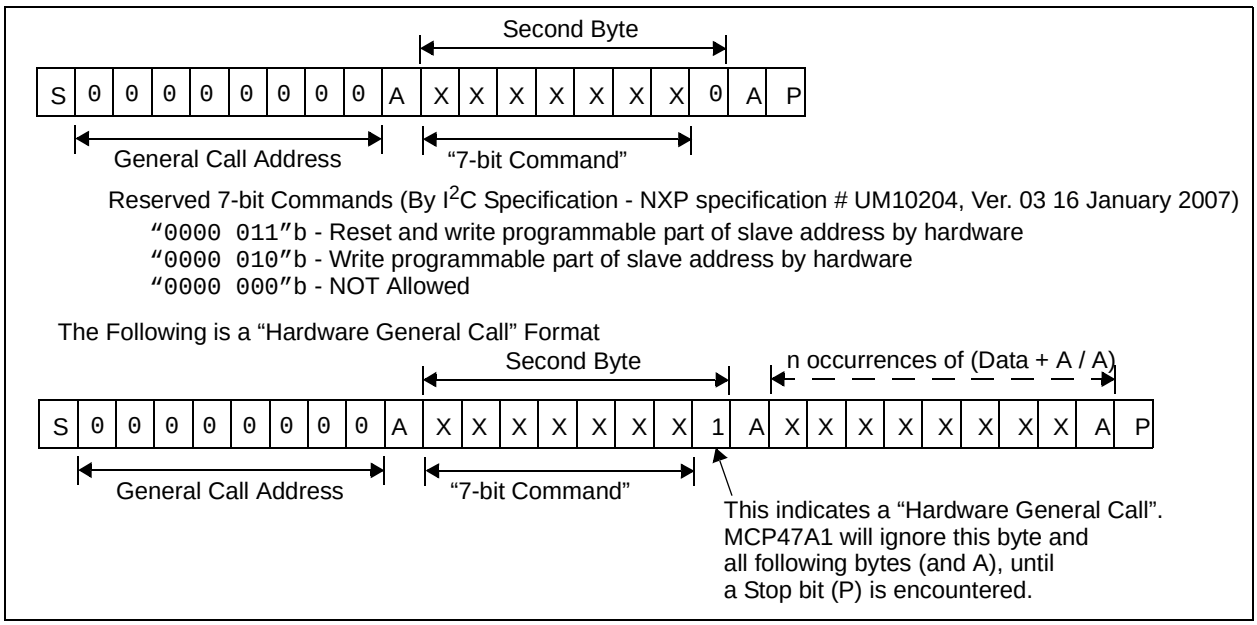


FIGURE 5-10: *General Call Formats.*

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5.3 Serial Commands

The MCP47A1 devices support two serial commands. These commands are:

- **Write Operation**
- **Read Operations**

The I^2C command formats have been defined to support the SMBus version 2.0 Write Byte/Word Protocol formats and Read Byte/Word Protocol formats. The SMBus specification that defines this operation is Section 5 of the Version 2.0 document (August 3, 2000).

This protocol format may be convenient for customers using library routines for the I^2C bus, where all they need to do is specify the command (read, write, ...) with the Device Address, the Register Address, and the Data.

5.3.1 WRITE OPERATION

The write operation requires the START condition, Control Byte, Acknowledge, Command Code, Acknowledge, Data Byte, Acknowledge and STOP (or RESTART) condition. The Control (Slave Address) Byte requires the R/$\overline{W}$ bit equal to a logic zero (R/$\overline{W}$ = "0") to generate a write sequence. The MCP47A1 is responsible for generating the Acknowledge (A) bits.

Data is written to the MCP47A1 after every byte transfer (during the A bit). If a STOP or RESTART condition is generated during a data transfer (before the A bit), the data will not be written to MCP47A1.

Data bytes may be written after each Acknowledge. The command is terminated once a Stop (P) condition occurs. Refer to Figure 5-11 for the single byte write sequence and Figure 5-12 for the generic (multi-byte) write sequence. For a single byte write, the master sends a STOP or RESTART condition after the 1st data byte is sent.

The MSb of each Data Byte is a don't care, since the wiper register is only 7-bits wide.

The command is terminated once a Stop (P) or Restart (S) condition occurs.

Figure 5-13 shows the I^2C write communication behavior of the Master Device and the MCP47A1 device and the resultant I^2C bus values.

Note:	A command code with a non-zero value will cause the data not to be written to the wiper register

5.3.2 READ OPERATIONS

The read operation requires the START condition, Control Byte, Acknowledge, Command Code, Acknowledge, Restart Condition, Control Byte, Acknowledge, Data Byte, the master generating the $\overline{A}$ and STOP (or RESTART) condition. The first Control Byte requires the R/$\overline{W}$ bit equal to a logic zero (R/$\overline{W}$ = "0") to write the Command Code, while the second Control Byte requires the R/$\overline{W}$ bit equal to a logic one (R/$\overline{W}$ = "1") to generate a read sequence. The MCP47A1 will A the Slave Address Byte and $\overline{A}$ all the Data Bytes. The I^2C Master will $\overline{A}$ the Slave Address Byte and the last Data Byte. If there are multiple Data Bytes, the I^2C Master will A all Data Bytes except the last Data Byte (which it will $\overline{A}$).

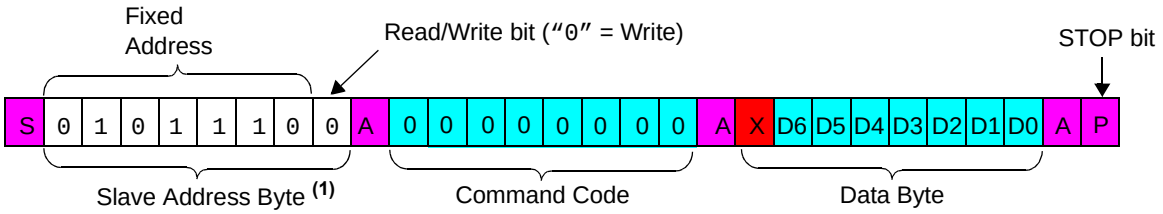
The MCP47A1 maintains control of the SDA signal until all data bits have been clocked out.

The command is terminated once a Stop (P) or Restart (S) condition occurs. Refer to Figure 5-14 for the read command sequence. For a single read, the master sends a STOP or RESTART condition after the 1st data byte (and A bit) is sent from the slave.

The MSb of each Data Byte is always a "0", since the wiper register is only 7-bits wide.

Figure 5-15 shows the I^2C read communication behavior of the Master Device and the MCP47A1 device and the resultant I^2C bus values.

Note:	A command code with a non-zero value will cause the data not to be read from the wiper register

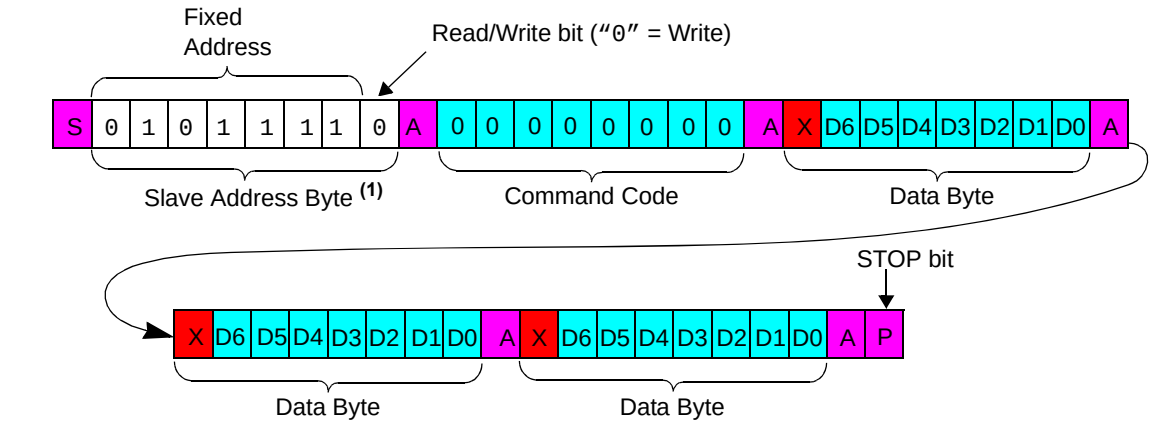


Legend

S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don’t Care
R/$\overline{W}$ = Read/$\overline{\text{Write}}$ bit
D6:D0 = Data bits

Note 1: Example using Slave Address Option A0 (5Ch).

FIGURE 5-11: *I^2C Single Byte Write Command Format.*



Legend

S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don’t Care
R/W = Read/Write bit
D6:D0 = Data bits

Note 1: Example using Slave Address Option A0 (5Ch).

FIGURE 5-12: *I^2C Write Command Format.*

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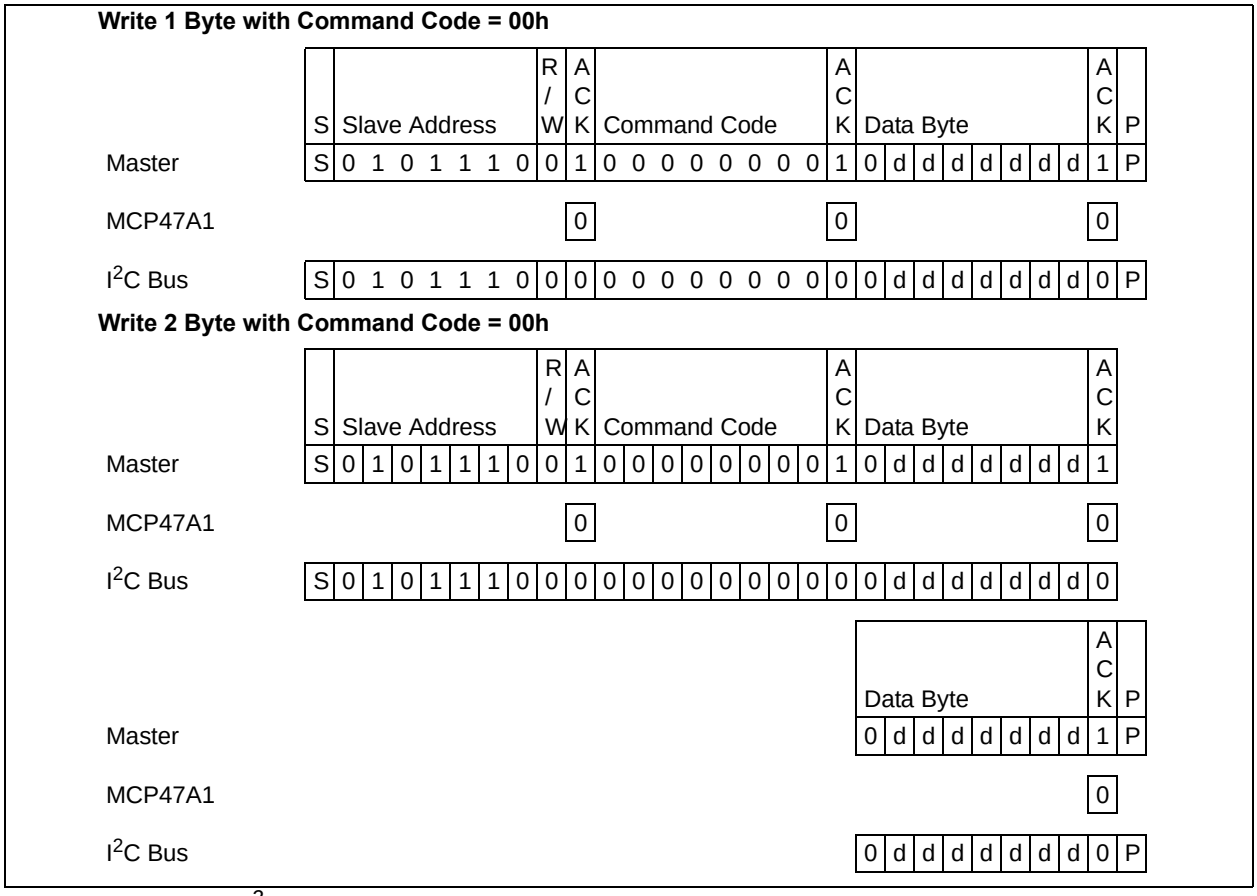
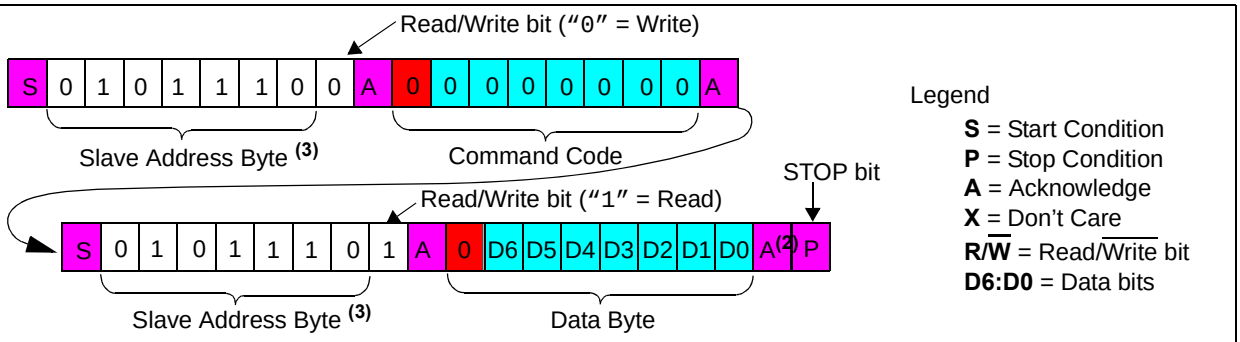


FIGURE 5-13: *I^2C Write Communication Behavior.*



Note 1: Master Device is responsible for ACK / NACK signal. If a NACK signal occurs, the MCP47A1 will abort this transfer and release the bus.

2: The Master Device will Not ACK, and the MCP47A1 will release the bus so the Master Device can generate a Stop or Repeated Start condition.

3: Example using Slave Address Option A0 (5Ch).

FIGURE 5-14: *I^2C Read Command Format.*

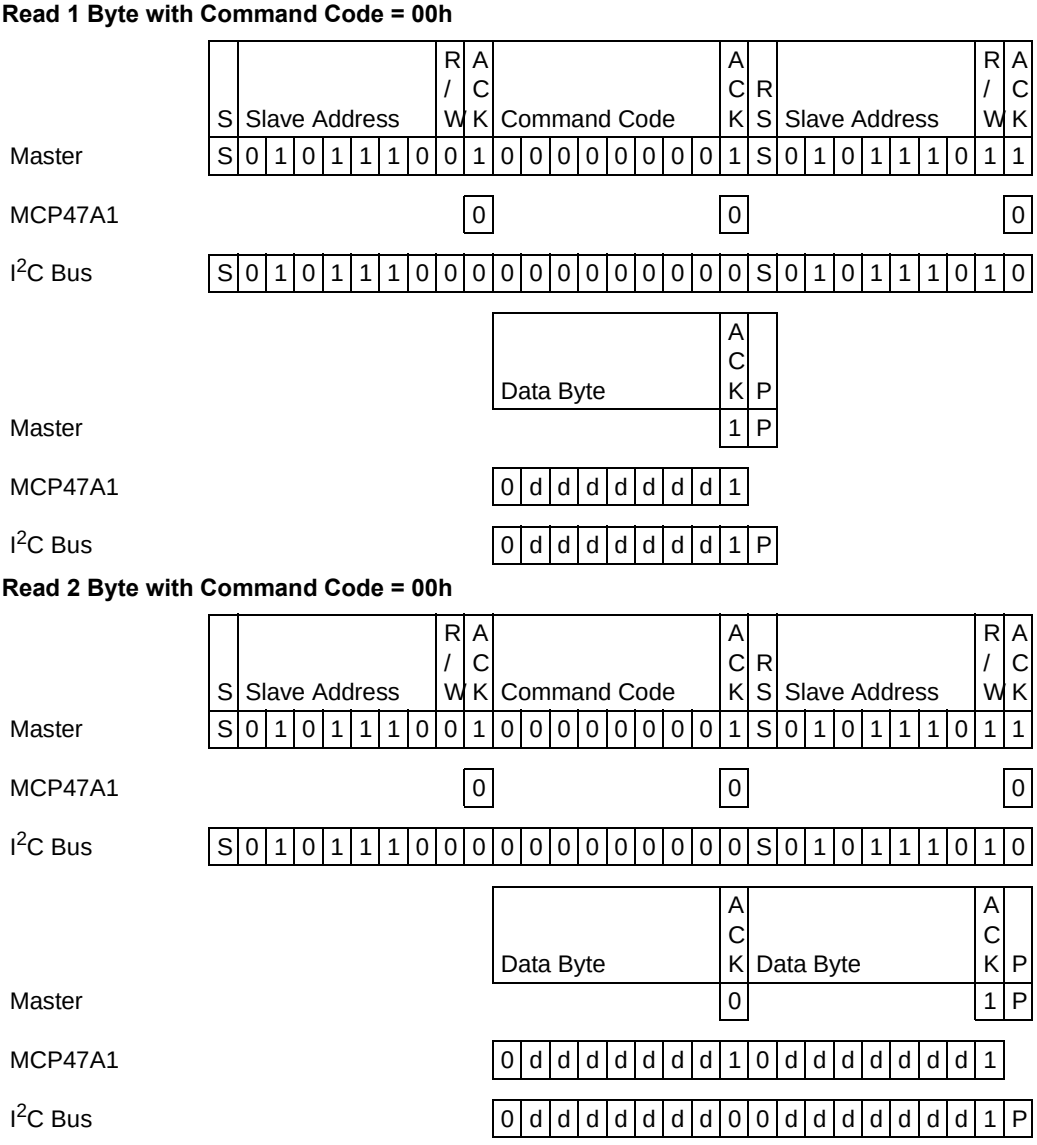


FIGURE 5-15: *I^2C Read Communication Behavior.*

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6.0 RESISTOR NETWORK

The Resistor Network is made up of an R_{AB} resistor ladder. The R_{AB} resistor has a typical resistance of 20 kΩ. Figure 6-1 shows a block diagram for the resistor network and output buffer. The resistance from the V_{REF} pin to ground is referred to as R_{VREF}.

The 7-bit I^2C Data Byte (00h - 7Fh) is decoded to the 6-bit wiper value (00h - 40h). **Section 6.3** describes the Serial Shift buffer to Wiper register decoding.

6.1 R_{VREF} Resistance

R_{VREF} resistance is the resistance from the V_{REF} pin to ground and is the R_{AB} resistances. Equation 6-1 shows how to calculate R_{VREF}.

6.1.1 V_{REF} PIN CURRENT (I_{VREF})

The current into the V_{REF} pin is dependent on the voltage on the V_{REF} pin (V_{REF}) and the R_{VREF} resistance. The V_{REF} pin's voltage source current capability should support a resistive load that is the minimum R_{VREF} resistance.

EQUATION 6-1: CALCULATING R_{VREF}

$$R_{VREF} = \frac{(V_{REF})}{(I_{VREF})}$$

V_{REF} is the voltage on the V_{REF} pin.
I_{VREF} is the current into the V_{REF} pin.

6.2 R_{AB} Resistor Ladder

The R_{AB} resistor ladder is a digital potentiometer in a voltage divider configuration. The R_{AB} resistor ladder has 64 R_S resistors in series. This resistor ladder has 65 wiper taps which allow wiper connectivity to the bottom (terminal B), Zero-Scale, and the top (terminal A), Full-Scale, of the resistor ladder (see Figure 6-1). With an even number of R_S resistors in the R_{AB} ladder, when the wiper is at the Mid-Scale value, V_{OUT} equals V_{REF} / 2. The R_{AB} resistance also includes the R_{FS} and R_{ZS} resistances (see **Section 6.2.2**). The R_{AB} (and R_S) resistance has small variations over voltage and temperature. The typical R_{AB} resistance is 10kΩ .

6.2.1 THE WIPER

The value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder. The Wiper register value is derived from the Serial Shift Register value (see **Section 6.3**).

Any variation of the wiper resistance does not effect the voltage at the W terminal, and therefore the input of the output buffer.

6.2.2 R_{FS} AND R_{ZS} RESISTORS

The R_{FS} and R_{ZS} resistances are artifacts of the R_{AB} resistor implementation. These resistors are included in the block diagram to help better model the actual device operation. Equation 6-2 shows how to estimate the R_S, R_{FS}, and R_{ZS} resistances, based on the measured voltages of V_{REF}, V_{FS}, and V_{ZS} and the measured current I_{VREF}.

EQUATION 6-2: ESTIMATING R_S, R_{FS}, AND R_{ZS}

$$R_{FS} = \frac{V_{REF}}{I_{VREF}}$$

$$R_{ZS} = \frac{V_{ZS}}{I_{VREF}}$$

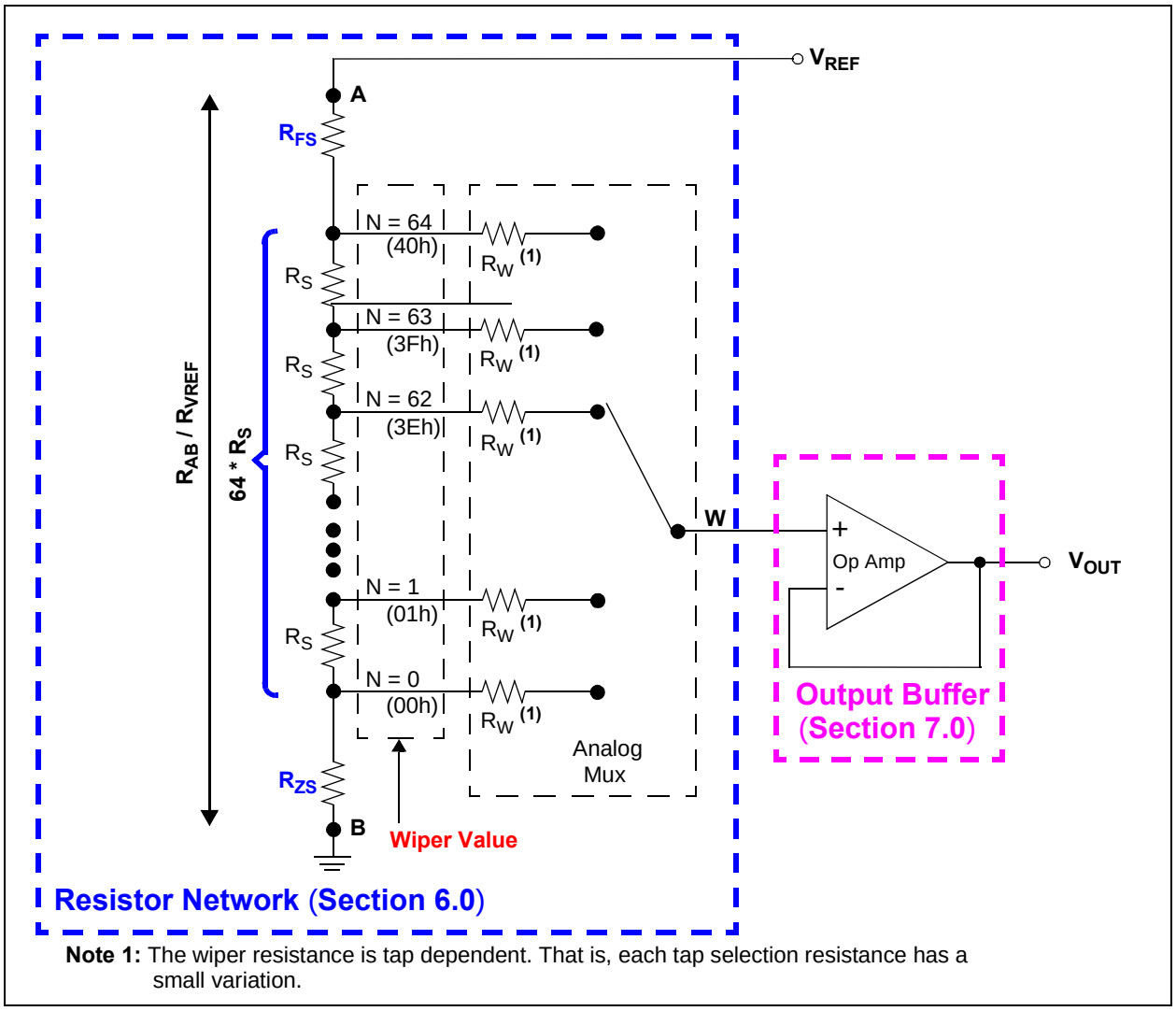
$$R_S = \frac{V_S}{I_{VREF}}$$

Where:

$$V_S = \frac{(V_{FS} - V_{ZS})}{64}$$

V_{FS} is the V_{OUT} voltage when the wiper code is at full-scale.

V_{ZS} is the V_{OUT} voltage when the wiper code is at zero-scale.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation.

FIGURE 6-1: *Resistor Network and Output Buffer Block Diagram.*

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6.3 Serial Buffer to Wiper Register Decode

The I^2C's Data Byte is 8-bits, where only the lower 7-bits are implemented. This register is called the Serial Shift Register (SSR). The Wiper register supports addressing of 65 taps (6-bit resolution). Table 6-1 shows the decoding of the Serial Shift Register to the Wiper Register value.

Note 1: The I^2C Write and Read commands access the value in the Serial Shift Register (SSR).

2: The MSb of the I^2C Data Byte is ignored and not loaded into the SSR. A write of C0h, will result in the same V_{OUT} voltage as a write of 40h (mid-scale). A subsequent read command (of the SSR) will result in a value of 40h.

3: The 7-bit SSR value is decoded to a 6-bit (65 taps) value that controls the wiper's position.

TABLE 6-1: SERIAL SHIFT REGISTER VALUE TO WIPER VALUE

I^2C Write Data	SSR(1)	Wiper Value(2)	Comment
00h	00h	00h	Wiper Register at Zero Scale, $V_{OUT} = V_{SS}$
01h or 81h	01h	01h	
02h or 82h	02h	02h	
	:	:	:
20h or A0h	20h	20h	Mid-Scale (POR value), $V_{OUT} = (1/2) * V_{REF}$
	:	:	:
3Eh or BEh	3Eh	3Eh	Wiper Register = SSR - 20h
3Fh or BFh	3Fh	3Fh	Wiper Register = SSR - 20h
40h - 7Fh or C0h - FFh	40h - 7Fh	40h	Wiper Register at Full Scale, $V_{OUT} = V_{REF}$

Note 1: The Serial Shift Register (SSR) is 7-bits wide and holds the value written from the I^2C Write command. An I^2C Read command will read the value in this register.

2: The Wiper value is the value that controls the resistor ladder's wiper position.

6.4 Resistor Variations (Voltage and Temperature)

The R_{AB} resistors are implemented to have minimal variations (by design). Any variations should occur uniformly on all the resistor elements, so the resistor's elements will track each other over temperature and process variations.

The variation of the resistive elements over the operating voltage range is also minimal. Therefore the V_{REF} resistance (R_{VREF}) of the device has minimal variation due to operating voltage.

Since the V_{OUT} pin's voltage is ratiometric, and the resistive elements change uniformly over temperature, process, and operating voltage variations. Minimal variation should be seen on the V_{OUT} pin's voltage.

6.5 POR Value

A POR/BOR event will load the volatile Serial Shift Register (and therefore Wiper register) with the default value. Table 6-2 shows the default values offered.

TABLE 6-2: POR/BOR SETTINGS

Device	Setting	Register Value (1)	
		SSR	Wiper
MCP47A1	Mid-scale	20h or A0h	20h

Note 1: Custom POR/BOR Wiper Setting options are available; contact the local Microchip Sales Office for additional information. Custom options have NRE and minimum volume requirements.

NOTES:

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7.0 OUTPUT BUFFER

As the device powers up, the V_{OUT} pin will float to an unknown value. When the device's V_{DD} is above the transistor threshold voltage of the device, the output will start being pulled low. After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper will be loaded with the POR value (20h, which is midscale). The output voltage of the buffer (V_{OUT}) may not be within specification until the device V_{DD} is at 2.7V. The outputs' slew rate and settling time must also be taken into account.

7.1 Output Buffer / V_{OUT} Operation

The DAC output is buffered with a low power and precision output amplifier (op amp). This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. Figure 7-1 shows a block diagram.

Note 1: The load resistance must stay higher than 5 kΩ for the stable and expected analog output (to meet electrical specifications). Refer to:

- **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.
- **Section 7.3 "Driving Resistive and Capacitive Loads"** for additional design information.

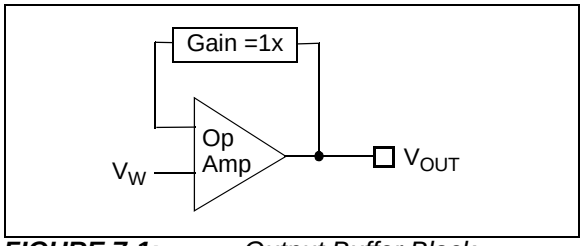


FIGURE 7-1: *Output Buffer Block Diagram.*

7.1.1 OUTPUT VOLTAGE

The volatile DAC Register's value controls the analog V_{OUT} voltage. The volatile Wiper Register's value is unsigned binary. The formula for the output voltage is given in Equation 7-1.

EQUATION 7-1: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = V_{ZS} + (N * V_S)$$

When $R_{FS} = R_{ZS} = 0\Omega$: $V_{ZS} = 0V$

$V_{FS} = V_{REF}$

V_{ZS} is the V_{OUT} voltage when the wiper code = 00h.

N = wiper code = 0 to 64;

The Serial Shift Register's value will be latched on the falling edge of the acknowledge pulse of the write command's last byte. Then the V_{OUT} voltage will start driving to the new value.

The following events update the analog voltage output (V_{OUT}):

- Power-On-Reset.
- Falling edge of the acknowledge pulse of the last write command byte.

7.1.2 STEP VOLTAGE (V_S)

The Step voltage is dependent on the device resolution (64 R_S) and the output voltage range (V_{ZS} to V_{FS}). Equation 7-2 shows the calculation for the step resistance.

EQUATION 7-2: V_S CALCULATION

$$V_S = \frac{(V_{FS} - V_{ZS})}{64}$$

V_{FS} is the V_{OUT} voltage when the wiper code is at full-scale.

V_{ZS} is the V_{OUT} voltage when the wiper code is at zero-scale.

Table 7-1 shows the calculated V_{OUT} voltages for the given volatile Wiper Register value. These calculations are based on different V_{REF} voltage values (1.5V, 3.3V, and 5.0V) with an assumption that $R_{FS} = R_{ZS} = 0\Omega$.

TABLE 7-1: THEORETICAL DAC OUTPUT VALUES

Wiper Value		V_{OUT} (1)			
		Ratio	V_{REF}		
Hex	Dec		1.5	3.3	5.0
00h	0	0.0000	0.0000	0.0000	0.0000
01h	1	0.0156	0.0234	0.0516	0.0781
02h	2	0.0313	0.0469	0.1031	0.1563
03h	3	0.0469	0.0703	0.1547	0.2344
04h	4	0.0625	0.0938	0.2063	0.3125
05h	5	0.0781	0.1172	0.2578	0.3906
06h	6	0.0938	0.1406	0.3094	0.4688
07h	7	0.1094	0.1641	0.3609	0.5469
08h	8	0.1250	0.1875	0.4125	0.6250
09h	9	0.1406	0.2109	0.4641	0.7031
0Ah	10	0.1563	0.2344	0.5156	0.7813
0Bh	11	0.1719	0.2578	0.5672	0.8594
0Ch	12	0.1875	0.2813	0.6188	0.9375
0Dh	13	0.2031	0.3047	0.6703	1.0156
0Eh	14	0.2188	0.3281	0.7219	1.0938
0Fh	15	0.2344	0.3516	0.7734	1.1719
10h	16	0.2500	0.3575	0.8250	1.2500
11h	17	0.2656	0.3984	0.8766	1.3281
12h	18	0.2813	0.4219	0.9281	1.4063
13h	19	0.2969	0.4453	0.9797	1.4844
14h	20	0.3125	0.4688	1.0313	1.5625
15h	21	0.3281	0.4922	1.0828	1.6406
16h	22	0.3438	0.5156	1.1344	1.7188
17h	23	0.3594	0.5391	1.1859	1.7969
18h	24	0.3750	0.5625	1.2375	1.8750
19h	25	0.3906	0.5859	1.2891	1.9531
1Ah	26	0.4063	0.6094	1.3406	2.0313
1Bh	27	0.4219	0.6328	1.3922	2.1094
1Ch	28	0.4375	0.6563	1.4438	2.1875
1Dh	29	0.4531	0.6797	1.4953	2.2656
1Eh	30	0.4688	0.7031	1.5469	2.3438
1Fh	31	0.4844	0.7266	1.5984	2.4219
20h	32	0.5000	0.7500	1.6500	2.5000
21h	33	0.5156	0.7734	1.7016	2.5781
22h	34	0.5313	0.7969	1.7531	2.6563
23h	35	0.5469	0.8203	1.8047	2.7344
24h	36	0.5625	0.8438	1.8563	2.8125
25h	37	0.5781	0.8672	1.9078	2.8906
26h	38	0.5938	0.8906	1.9594	2.9688
27h	39	0.6094	0.9141	2.0109	3.0469
28h	40	0.6250	0.9375	2.0625	3.1250
29h	41	0.6406	0.9609	2.1141	3.2031
2Ah	42	0.6563	0.9844	2.1656	3.2813
2Bh	43	0.6719	1.0078	2.2172	3.3594
2Ch	44	0.6875	1.0313	2.2688	3.4375
2Dh	45	0.7031	1.0547	2.3203	3.5156
2Eh	46	0.7188	1.0781	2.3719	3.5938
2Fh	47	0.7344	1.1016	2.4234	3.6719
30h	48	0.7500	1.1250	2.4750	3.7500
31h	49	0.7656	1.1484	2.5266	3.8281
32h	50	0.7813	1.1719	2.5781	3.9063
33h	51	0.7969	1.1953	2.6297	3.9844
34h	52	0.8125	1.2188	2.6813	4.0625
35h	53	0.8281	1.2422	2.7328	4.1406
36h	54	0.8438	1.2656	2.7844	4.2188
37h	55	0.8594	1.2891	2.8359	4.2969
38h	56	0.8750	1.3125	2.8875	4.3750
39h	57	0.8906	1.3359	2.9391	4.4531
3Ah	58	0.9063	1.3594	2.9906	4.5313
3Bh	59	0.9219	1.3828	3.0422	4.6094
3Ch	60	0.9375	1.4063	3.0938	4.6875
3Dh	61	0.9531	1.4297	3.1453	4.7656
3Eh	62	0.9688	1.4531	3.1969	4.8438
3Fh	63	0.9844	1.4766	3.2484	4.9219
40h	64	1.0000	1.5000	3.3000	5.0000

Note 1: V_{OUT} voltages based on R_{FS} and $R_{ZS} = 0\Omega$.

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7.1.3 AMPLIFIER INPUT VOLTAGE (V_W)

To ensure that the amplifier is operating in its linear range, the voltage (V_W) into the output amplifier's input has requirements that must be met.

For device V_{DD} voltages ≥ 2.7V, the amplifier is in the linear region for all V_{REF} voltages (≥ 1.0V) and DAC register codes.

For device V_{DD} voltages < 2.7V, there will be a voltage where the amplifier output is no longer linear with the amplifier input voltage (V_W). This is shown in Figure 2-20, where V_{DD} = 1.8V and the V_{REF} = 1.6V. Higher DAC register codes are the first to encounter the nonlinearity of the output buffer. The nonlinearity is also influenced by the temperature of operation.

Figure 7-2 shows the trend of the amplifier linearity based on the device V_{DD} / V_{REF} voltages and the input voltage to the amplifier. The trend will also be affected by device temperature. V_{NL} is the voltage where the amplifier's output becomes nonlinear. While the V_W voltage is less than the V_{NL} voltage, the amplifier's output is linear. Once the device V_{DD} has been lowered to where the amplifier's nonlinear range increases, the two methods to keep $V_W < V_{NL}$ are:

1. Lower the V_{REF} voltage
2. Decrease the DAC Register code

Both methods reduce the maximum usable output voltage.

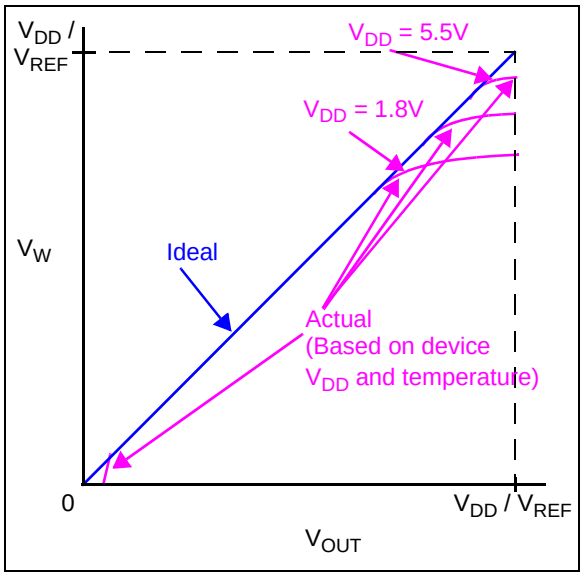


FIGURE 7-2: *Amplifier Input (V_W) to Amplifier Output (V_{OUT}) General Characteristics ($V_{REF} = V_{DD}$).*

Figure 7-3 shows the equations for solving for V_{OUT} voltage, the V_{REF} voltage, or the maximum DAC Register code, based on knowing the requirements for two of these variables. For V_{DD} voltages below the specified analog performance voltage (2.7V), the calibration of the device could be done to ensure V_{OUT} voltage is not driven into the output amplifier nonlinear region via the DAC Register value / V_{REF} voltage. Using the measured V_{NL} voltage as the V_{OUT} voltage will allow you to balance your selection of the V_{REF} voltage and maximum DAC Code. The DAC Register code of 64 is the full-scale code.

$$V_{OUT} = V_{REF} * \frac{\text{DAC Code}}{64}$$

$$V_{REF} = \frac{64 * V_{OUT}}{\text{DAC Code}}$$

$$\text{DAC Code} = \frac{64 * V_{OUT}}{V_{REF}}$$

FIGURE 7-3: *Solving for V_{OUT}, V_{REF}, or DAC Register Code.*

7.2 Output Slew Rate

Figure 7-4 shows an example of the slew rate of the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

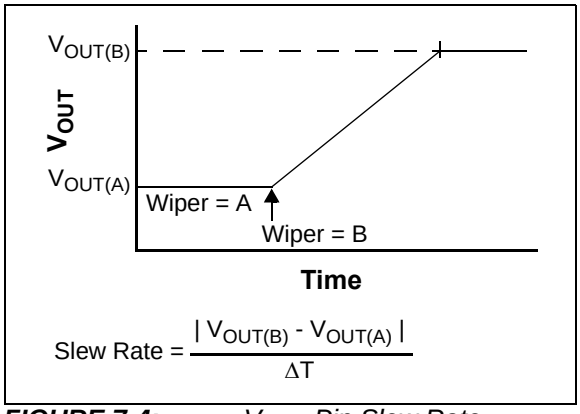


FIGURE 7-4: *V_{OUT} Pin Slew Rate.*

7.2.1 SMALL CAPACITIVE LOAD

With a small capacitive load, the output buffer's current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin's voltage is not a step transition from one output value (wiper code value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the buffer slew rate (SR_{BUF}).

7.2.2 LARGE CAPACITIVE LOAD

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

So the V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

7.3 Driving Resistive and Capacitive Loads

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). Figure 2-29 shows the V_{OUT} vs. Resistive Load.

V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ . It is recommended to use a load with R_L greater than 5 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

So, when driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see Figure 7-5) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

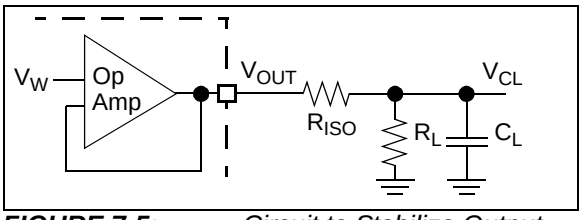


FIGURE 7-5: *Circuit to Stabilize Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value should be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note:	Additional insight into circuit design for driving capacitive loads can be found in AN884 "Driving Capacitive Loads With Op Amps" (DS00884).

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7.4 Output Errors

The output error is caused by two factors. These are:

- Characteristics of the Resistor Network
- Characteristics of the Output Buffer

Figure 7-6 shows the components of the error on the output voltage. The first part of the error is from the resistor ladder and the R_{FS} and R_{ZS} resistances. The second part is due to the output buffer's input offset characteristics.

The R_{FS} and R_{ZS} resistances affect the voltage between V_{ZS} and V_{FS}. The larger that $R_{FS} + R_{ZS}$ is, the smaller that the step voltage (V_S) will be (from the theoretical step voltage). The increase in the R_{FS} and R_{ZS} resistances also effects the Full Scale Error (FSE), Zero Scale Error (ZSE), and gain error.

Table 7-2 compares theoretical resistor network voltages for full scale and zero scale, where $R_{FS} = R_{ZS} = 0\Omega$, to an example where R_{FS} and R_{ZS} and non-zero. The voltage calculations show cases of V_{REF} = 5.0V and V_{REF} = 1.5V. Figure 2-34 shows R_{VREF}, R_{FS}, and R_{ZS} resistances V_{DD}.

So, as the voltage reference (V_{REF}) decreases, the Step voltages (V_S) decrease. At a low V_{REF} voltage, the step voltage approaches the magnitude of the output buffer's input offset voltage (design target of ± 4.5 mV). So, for low V_{REF} voltages, the output buffer errors have greater influence on the V_{OUT} voltage.

TABLE 7-2: CALCULATION COMPARISON

	Example	Theoretical	Delta
R_{VREF}	20,180Ω		—
R_{FS}	100Ω	0Ω	100Ω
R_{ZS}	80Ω	0Ω	80Ω
$R_1 + 64*R_S + R_2$	30,000Ω	30,180Ω	- 180Ω
R_1, R_{AB}, R_2	10,000Ω	10,060Ω	- 60Ω
V_{REF}	5.00 V		—
V_{FS}	3.3267 V	3.3333 V	- 6.6 mV
V_{ZS}	1.6700 V	1.6667 V	+ 3.3 mV
V_S	25.88 mV	26.04 mV	- 0.16 mV
V_{REF}	1.5V		—
V_{FS}	0.9980 V	1.0000 V	- 2.0 mV
V_{ZS}	0.5010 V	0.5000 V	+ 1.0 mV
V_S	7.766 mV	7.813 mV	-0.047mV

Note 1: $R_{VREF} = R_1 + R_{AB} + R_2$,
$R_{AB} = R_{FS} + 64*R_S + R_{ZS}$.
$V_S = (V_{FS} - V_{ZS}) / 64$

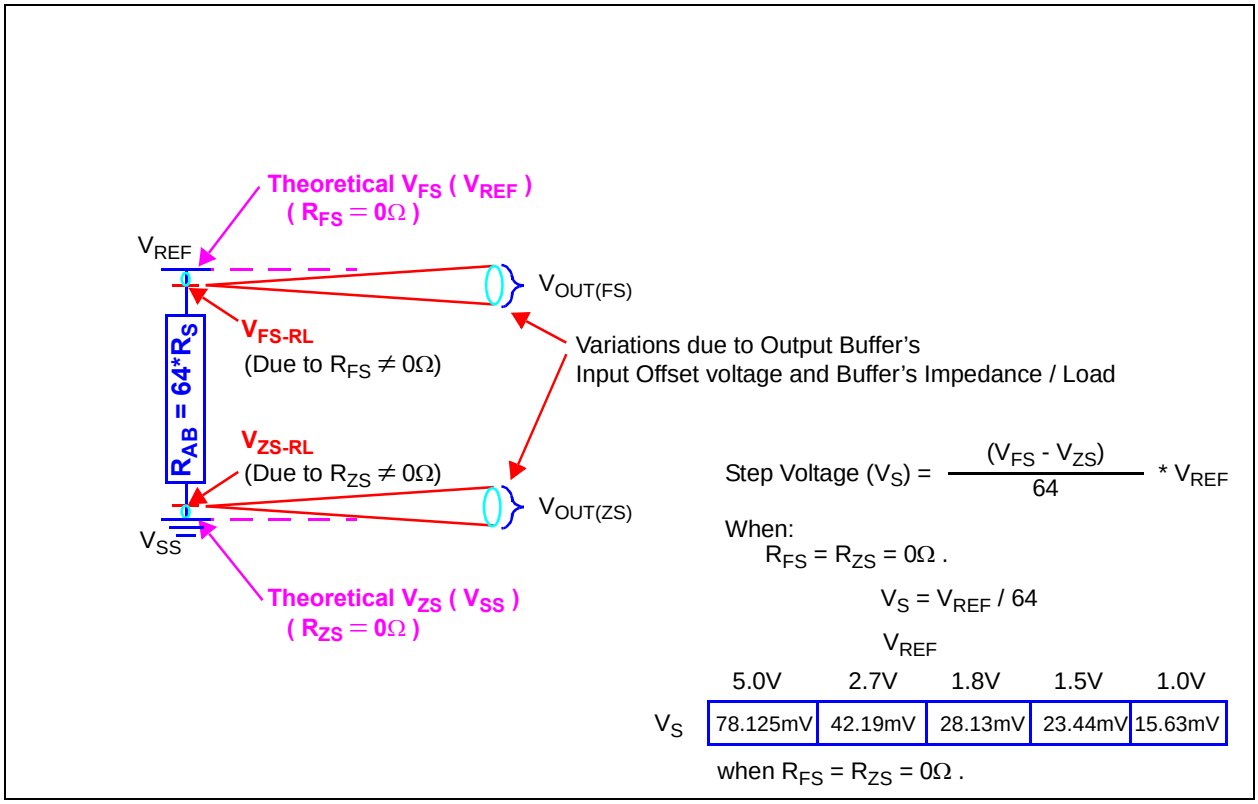


FIGURE 7-6: *Output Voltage (V_{OUT}) Error.*

NOTES:

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8.0 APPLICATIONS EXAMPLES

The MCP47A1 family of devices are general purpose, single-channel voltage output DACs for various applications where a precision operation with low power is needed.

The MCP47A1 devices are rail-to-rail output DACs designed to operate with a V_{DD} range of 1.8V to 5.5V. The internal output op amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of external buffers for most applications.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery Powered)
- Motor Control

Application examples include:

- **DC Set Point or Calibration**
- **Decreasing Output Step Size**
- **Building a "Window" DAC**
- **Selectable Gain and Offset Bipolar Voltage Output**
- **Building Programmable Current Source**
- **Serial Interface Communication Times**
- **Software I2C Interface Reset Sequence**

In the design of a system with the MCP47A1 devices, the following considerations should be taken into account:

- **Power Supply Considerations (Noise)**
- **PCB Area Requirements**
- **Connecting to I2C BUS using Pull-Up Resistors**

8.1 DC Set Point or Calibration

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP47A1 provides 64 output steps over the voltage reference range. If voltage reference is 1.65V, the LSb size is 1.65V / 64, or ~ 25.78 mV.

Applications that need accurate detection of an input threshold event often need several sources of error eliminated. Use of comparators and operational amplifiers (op amps) with low offset and gain error can help achieve the desired accuracy, but in many applications, the input source variation is beyond the designer's control. If the entire system can be calibrated after assembly in a controlled environment (like factory test), these sources of error are minimized, if not entirely eliminated. Figure 8-1 illustrates this example circuit. Equation 8-1 shows a quick estimation of the wiper value given the desired voltage trip (V_{TRIP}) point.

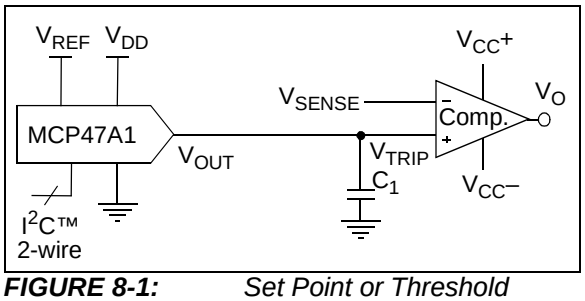


FIGURE 8-1: *Set Point or Threshold Calibration.*

EQUATION 8-1: ESTIMATING THE WIPER VALUE (N) FROM THE DESIRED V_{TRIP}

$$V_{TRIP} = V_{OUT} = (N * V_S)$$

$$N = \frac{(V_{TRIP} - V_{REF})}{V_S}$$

Where: $V_S = V_{REF} / 64$

Note: Calculation does not take into account R_{FS} and R_{ZS} resistors of the DAC's resistor ladder (see **Section 7.1** for additional information).

8.1.1 DECREASING OUTPUT STEP SIZE

Due to the step voltage and output range of the MCP47A1, it may be desirable to reduce the step voltage while also modifying the range of the output. A common method to achieve this smaller step size is a voltage divider on the DAC's output. Figure 8-2 illustrates this concept. Equation 8-2 shows a quick estimation of the wiper value given the desired voltage trip (V_{TRIP}) point.

For example, if $R_1 = R_2$, then the V_{TRIP} voltage range is from V_{SS} to 1/2 * V_{REF}. Also at the V_{TRIP} node, the step voltage is 1/2 the step voltage at the V_{OUT} node.

A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

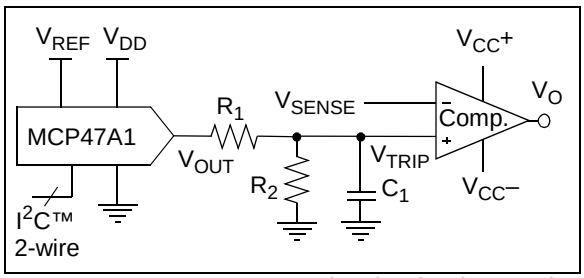


FIGURE 8-2: *Example Circuit Of Set Point or Threshold Calibration.*

EQUATION 8-2: V_{OUT} AND V_{TRIP} ESTIMATIONS

$$V_{OUT} = N * V_S$$

$$V_S = V_{REF} / 64$$

$$V_{TRIP} = V_{OUT} * \frac{R_2}{R_1 + R_2}$$

Note: The V_{OUT} voltage can also be scaled by a resistor from the V_{REF} pin to the system reference voltage. Care should be taken with this implementation due to the ± 20% variation to the 20kΩ typical resistance from the V_{REF} pin to ground (R_{VREF}). This variation in resistance directly effects the actual V_{OUT} voltage.

8.1.2 BUILDING A "WINDOW" DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application's accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF}, 2 • V_{REF}, or V_{SS} then creating a "window" around the threshold has several advantages. One simple method to create this "window" is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-3 and Figure 8-4 illustrate this concept.

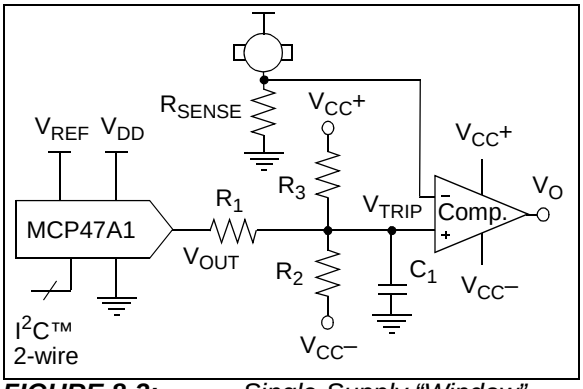


FIGURE 8-3: *Single-Supply "Window" DAC.*

EQUATION 8-3: V_{OUT} AND V_{TRIP} ESTIMATIONS

$$V_{OUT} = N * V_S$$

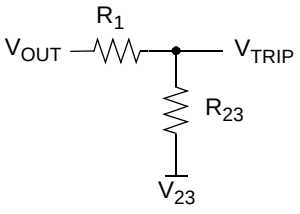
$$V_S = V_{REF} / 64$$

$$V_{TRIP} = \frac{V_{OUT} * R_{23} + V_{23} * R_1}{R_1 + R_{23}}$$

Thevenin Equivalent:

$$R_{23} = \frac{R_2 * R_3}{R_2 + R_3}$$

$$V_{23} = \frac{(V_{CC+} * R_2) * (V_{CC-} * R_3)}{R_2 + R_3}$$



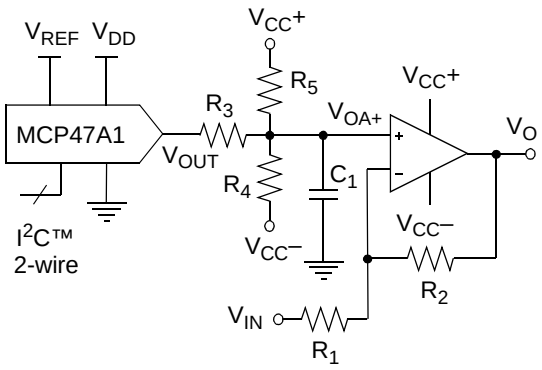
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8.2 Selectable Gain and Offset Bipolar Voltage Output

In some applications, control of the output range is desirable. Figure 8-4 shows a circuit using a DAC device to achieve a bipolar or single-supply application. This circuit is typically used for linearizing a sensor whose slope and offset varies. Depending on the output range desired, resistor R_4 or resistor R_5 may not be required. Equation 8-4 shows the calculation of the Gain, while Equation 8-5 shows the calculation of the V_O voltage.

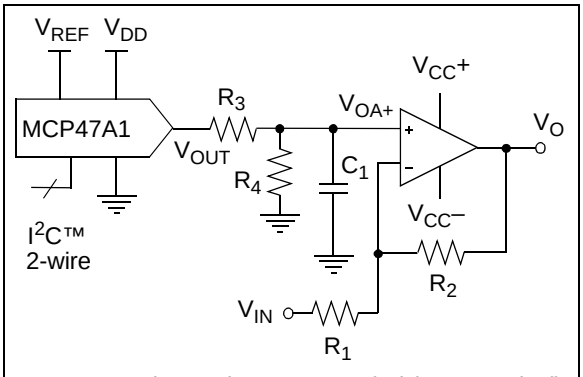
This circuit can be simplified if the window range is limited (by removing either the R_4 or R_5 resistor). Figure 8-5 shows a circuit for the case where the R_5 resistor is removed. Resistors R_1 and R_2 control the gain, while resistors R_3 and R_4 shift the DAC's output to a selected offset. Equation 8-6 shows the calculation of the V_O voltage.

Note: R4 can be tied to V_{DD}, instead of V_{SS}, if a higher offset is desired.



Note: Capacitor C_1 is recommended (0.1uF typical)

FIGURE 8-4: *Bipolar Voltage Source with Selectable Gain and Offset Circuit.*



Note: Capacitor C_1 is recommended (0.1uF typical)

FIGURE 8-5: *Simplified Bipolar Voltage Source with Selectable Gain and Offset Circuit.*

EQUATION 8-4: GAIN CALCULATION

$$\text{Gain} = \frac{R_2}{R_1}$$

If desired Gain = 0.5, and R_1 is selected as 20 kΩ then R_2 would need to be 10 kΩ .

EQUATION 8-5: BIPOLAR "WINDOW" DAC CALCULATIONS

$$V_O = \underbrace{V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{IN} \bullet \left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

$$V_{OA+} = \frac{(V_{OUT} \bullet R_{45}) + (V_{45} \bullet R_3)}{R_3 + R_{45}}$$

$$V_{45} = \frac{(V_{CC+} \bullet R_4) + (V_{CC-} \bullet R_5)}{R_4 + R_5}$$

$$R_{45} = \frac{R_4 \bullet R_5}{R_4 + R_5}$$

$$V_{OUT} = N * V_S \quad (1)$$

$$V_S = \frac{V_{REF}}{192}$$

Note 1: V_{OUT} calculation does not take into account R_{FS} and R_{ZS} resistors of the DAC's resistor ladder (see **Section 7.1** for additional information).

EQUATION 8-6: SIMPLIFIED BIPOLAR "WINDOW" DAC CALCULATIONS

$$V_O = V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \bullet \left(\frac{R_2}{R_1}\right)$$

$$V_{OA+} = V_{OUT} \bullet \left(\frac{R_4}{R_3 + R_4}\right)$$

$$V_{OUT} = N * V_S$$

Note 1: V_{OUT} calculation does not take into account R_{FS} and R_{ZS} resistors of the DAC's resistor ladder (see **Section 7.1** for additional information).

8.3 Building Programmable Current Source

Figure 8-6 shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller R_{SENSE} is, the less power is dissipated across it. However, this also reduces the resolution that the current can be controlled.

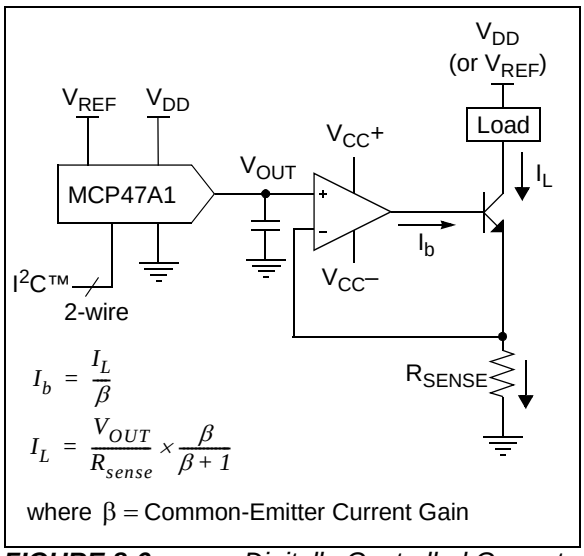


FIGURE 8-6: *Digitally-Controlled Current Source.*

8.4 Serial Interface Communication Times

Table 8-1 shows time for each I^2C serial interface command as well as the effective data update rate that can be supported by the digital interface (based on the two I^2C serial interface frequencies). The continuous write command allows a higher data update frequency since for the fixed overhead more bytes are transferred. The Serial Interface performance, along with the V_{OUT} output performance (such as slew rate), would be used to determine the application's volatile DAC register update rate.

TABLE 8-1: SERIAL INTERFACE TIMES / FREQUENCIES

Command	# of Serial Interface bits(1)	Example		Command Time (µs)		Effective Data Update Frequency (kHz) (2)	
		# Bytes Transferred	# of Serial Interface bits	100kHz	400kHz	100kHz	400kHz
Write Single Byte	29	1	29	290.0	72.5	3.4	13.8
Write Continuous Bytes	20 + N * 9	5	65	650.0	162.5	7.7	30.8
Read Byte	39	1	39	390.0	97.5	2.6	10.3

Note 1: Includes the Start or Stop bits.

2: This is the command frequency multiplied by the number of bytes transferred.

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8.5 Software I²C Interface Reset Sequence

Note:	This technique should be supported by any I²C compliant device. The 24XXXX I²C Serial EEPROM devices support this technique, which is documented in AN1028.

At times, it may become necessary to perform a Software Reset Sequence to ensure the MCP47A1 device is in a correct and known I²C Interface state. This technique only resets the I²C state machine.

This is useful if the MCP47A1 device powers up in an incorrect state (due to excessive bus noise, etc), or if the Master Device is reset during communication. Figure 8-7 shows the communication sequence to software reset the device.

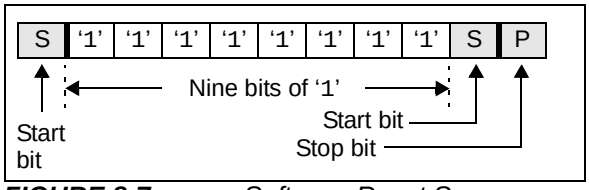


FIGURE 8-7: *Software Reset Sequence Format.*

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the Master Device. In this mode, the device is monitoring the data bus in Receive mode and can detect if the Start bit forces an internal Reset.

The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP47A1 is driving an A bit on the I²C bus, or is in output mode (from a Read command) and is driving a data bit of '0' onto the I²C bus. In both of these cases, the previous Start bit could not be generated due to the MCP47A1 holding the bus low. By sending out nine '1' bits, it is ensured that the device will see an $\overline{A}$ bit (the Master Device does not drive the I²C bus low to acknowledge the data sent by the MCP47A1), which also forces the MCP47A1 to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the Master Device was reset while sending a Write command to the MCP47A1, AND then as the Master Device returns to normal operation and issues a Start condition, while the MCP47A1 is issuing an Acknowledge. In this case, if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP47A1 could initiate a write cycle.

Note:	The potential for this erroneous write ONLY occurs if the Master Device is reset while sending a Write command to the MCP47A1.

The Stop bit terminates the current I²C bus activity. The MCP47A1 waits to detect the next Start condition.

This sequence does not effect any other I²C devices which may be on the bus, as they should disregard this as an invalid command.

8.6 Design Considerations

8.6.1 POWER SUPPLY CONSIDERATIONS (NOISE)

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47A1's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are suggested. Particularly harsh environments may require shielding of critical signals.

The device's power sources (V_{DD} and V_{REF}) should be as clean as possible. Any noise induced on the V_{DD} and V_{REF} signals can affect the DAC performance. Separate digital and analog ground planes are recommended.

Typical applications require a bypass capacitor in order to filter high-frequency noise on the V_{DD} and V_{REF} signals. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-8 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close to the device power pin (V_{DD}) as possible (within 4 mm).

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors should be terminated to the analog ground plane and V_{DD} and V_{SS} should reside on the analog plane.

Figure 8-9 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device should reside on the analog plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

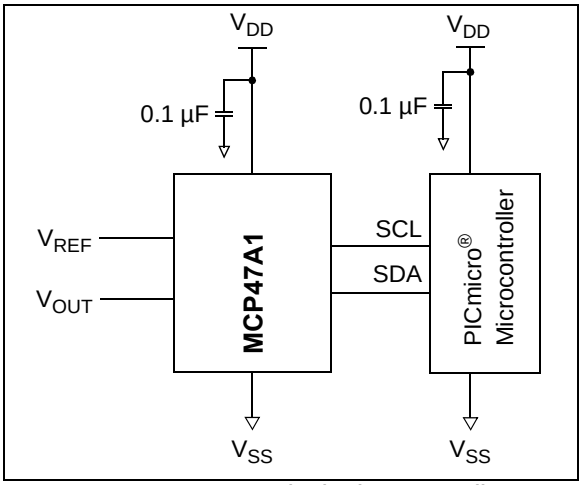
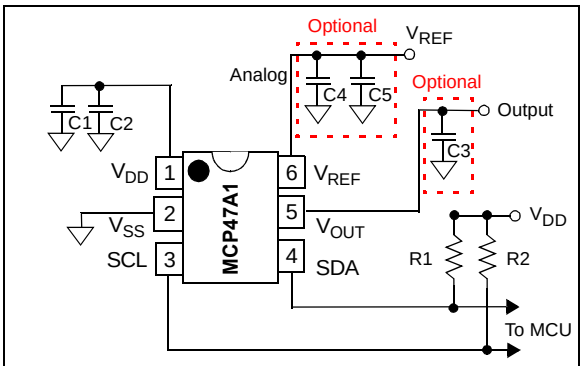


FIGURE 8-8: *Typical Microcontroller Connections.*



R1 and R2 are I^2C pull-up resistors:

R1 and R2:

5 kΩ - 10 kΩ for f_{SCL}	=	100 kHz to 400 kHz	
C1:	0.1 µF capacitor	Ceramic	
C2:	10 µF capacitor	Tantalum	
C3:	~ 0.1 µF	Optional to reduce noise in V_{OUT} pin.	
C4:	0.1 µF capacitor	Ceramic	
C5:	10 µF capacitor	Tantalum	

FIGURE 8-9: *Example MCP47A1 Circuit.*

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8.6.2 PCB AREA REQUIREMENTS

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the typical package dimensions and area for the different package options.

TABLE 8-2: PACKAGE FOOTPRINT (1)

Package			Package Footprint		
			Dimensions (mm)		
Pins	Type	Code	Length	Width	Area (mm^2)
6	SC70	LT	3.10	3.20	9.92

Note 1: Does not include recommended Land Pattern dimensions. Dimensions are Max values.

8.6.3 PINOUT/FOOTPRINT COMPATIBILITY

The MCP47A1 has a pinout and footprint compatibility to the MCP40D18 and MCP4018 devices.

The MCP40D18/MCP4018's W pin is analogous to the MCP47A1's V_{OUT} pin, while the MCP40D18/MCP4018's A pin is analogous to the MCP47A1's V_{REF} pin. The MCP40D18 and MCP47A1 share the same I^2C command protocol structure.

8.6.4 CONNECTING TO I^2C BUS USING PULL-UP RESISTORS

The SCL and SDA pins of the MCP47A1 devices are open-drain configurations. These pins require a pull-up resistor as shown in Figure 8-9.

The pull-up resistor values (R1 and R2) for SCL and SDA pins depend on the operating speed (standard, fast, and high speed) and loading capacitance of the I^2C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for standard and fast modes.

8.6.4.1 Device Connection Test

The user can test the presence of the device on the I^2C bus line using a simple I^2C command. This test can be achieved by checking an acknowledge response from the device after sending a read or write command. Figure 8-10 shows an example with a read command. The steps are:

a) Set the R/$\overline{W}$ bit "High" in the device's address byte.

b) Check the ACK bit of the address byte.
If the device acknowledges (ACK = 0) the command, then the device is connected, otherwise it is not connected.

c) Send Stop bit.

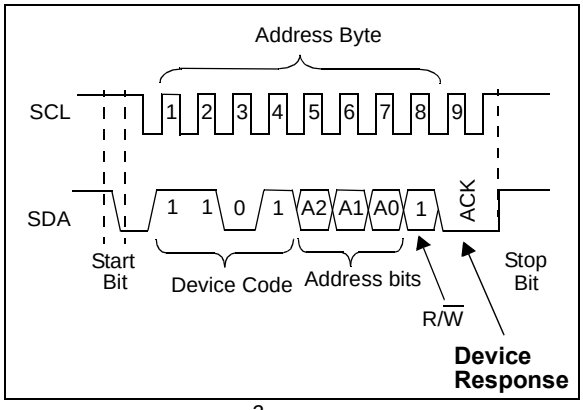


FIGURE 8-10: *I^2C Bus Connection Test.*

NOTES:

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9.0 DEVELOPMENT SUPPORT

9.1 Evaluation/Demonstration Boards

The MCP47A1 devices do not have a dedicated evaluation or demonstration board. Figure 9-1 shows the component connections to make an evaluation board using the SC70EV Bond Out PCB (order # SC70EV). This will allow the MCP47A1's capabilities to be evaluated with the PICkit™ Serial Analyzer (order # DV164122).

Note: Since the SC70EV is a generic board, the noise immunity of the board will not be optimal. If noise immunity is a requirement, then a you will need to develop a custom PCB for the MCP47A1. This PCB would need to use good layout techniques to reduce noise coupling.

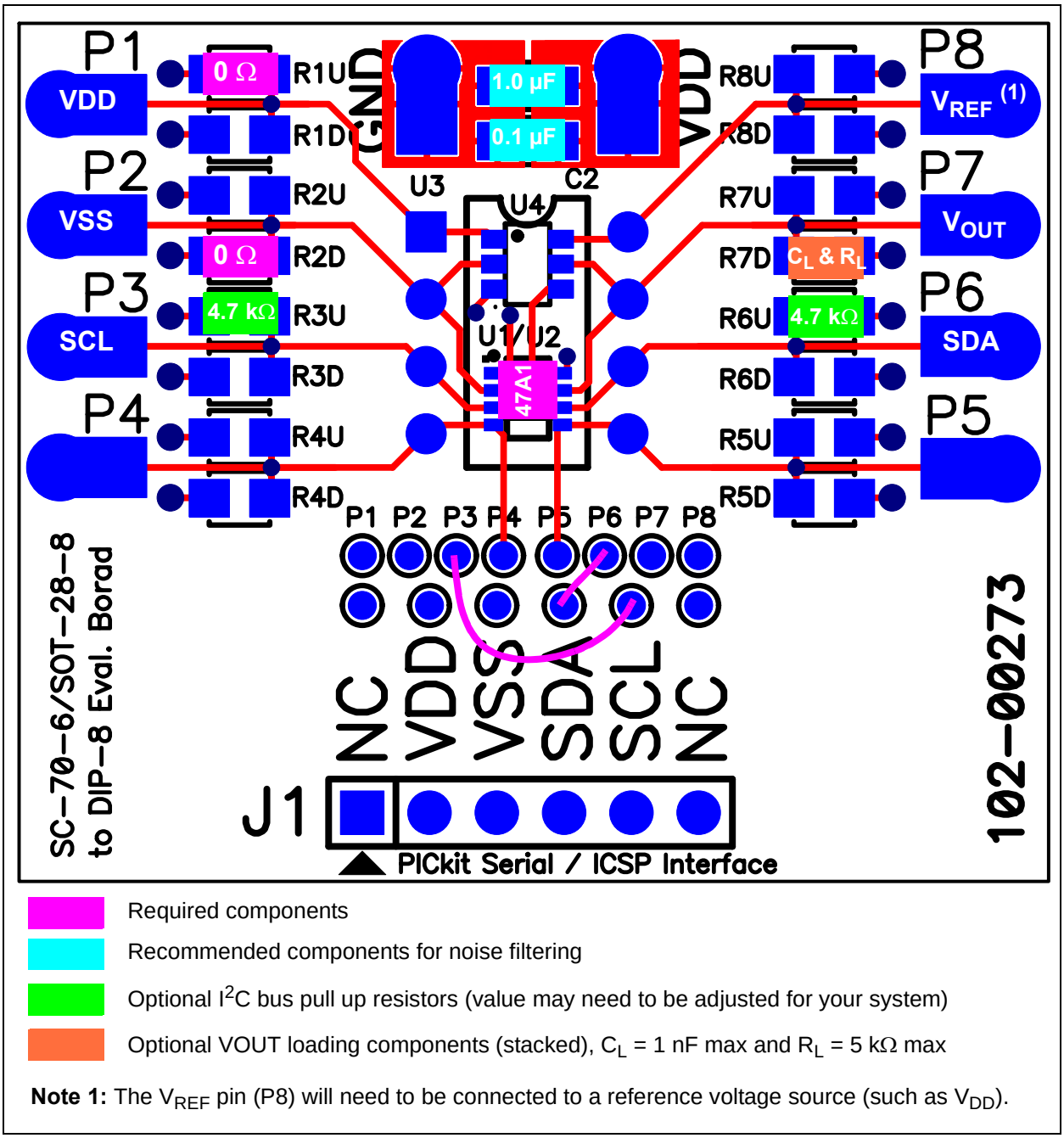


FIGURE 9-1: *SC70EV Bond Out PCB – Top Layer and Silk-Screen.*

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-1 shows some of these documents.

TABLE 9-1: TECHNICAL DOCUMENTATION

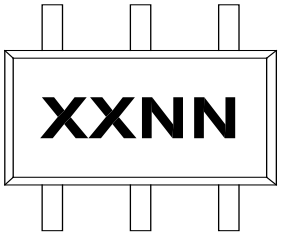
Application Note Number	Title	Literature #
AN1326	Using DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

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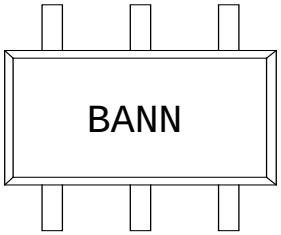
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

6-Lead SC-70



Example



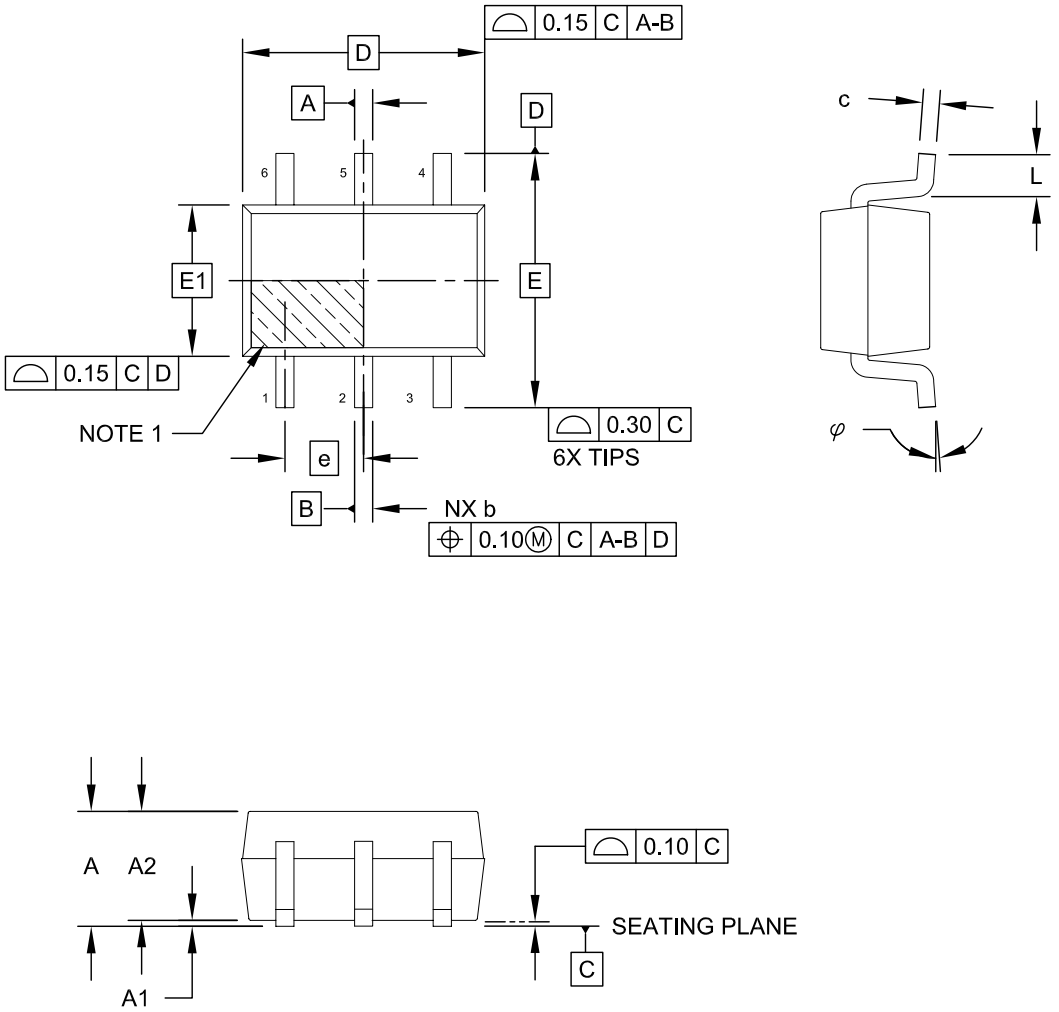
Part Number	Code	Part Number	Code
MCP47A1T-A0E/LT	BANN	MCP47A1T-A1E/LT	BCNN

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

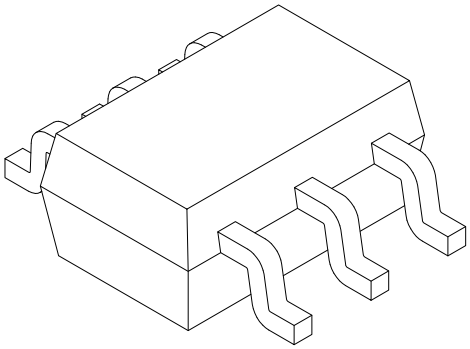


Microchip Technology Drawing No. C04-151A Sheet 1 of 2

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6-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Molded Package Thickness	A2	0.70	0.90	1.00
Standoff	A1	0.00	-	0.10
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Overall Length	D		2.00 BSC	
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.22
Lead Width	b	0.15	-	0.30

Notes:

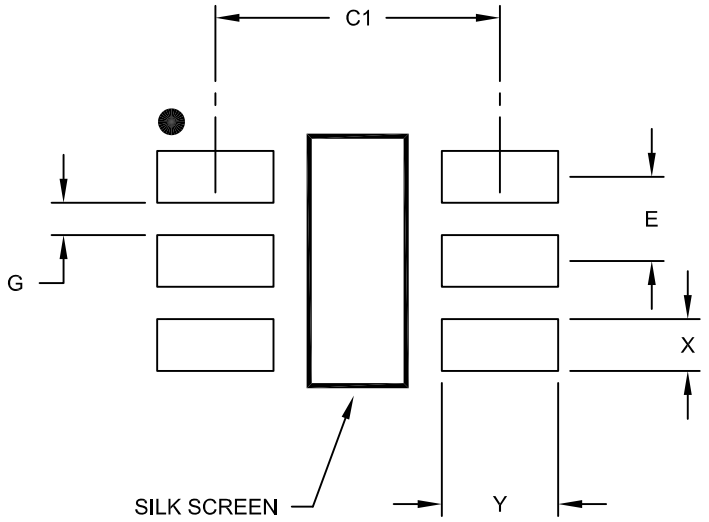
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-151A Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width (X6)	X			0.40
Contact Pad Length (X6)	Y			0.90
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2151A

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APPENDIX A: REVISION HISTORY

Revision A (August 2012)

- Original Release of this Document.

APPENDIX B: TERMINOLOGY

B.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 6-bit DAC, the resolution is 2^6, meaning the DAC code ranges from 0 to 64.

B.2 Least Significant Bit (LSb)

Normally, this is thought of as the ideal voltage difference between two successive codes. This bit has the smallest value or weight of all bits in the register.

For a given output voltage range, which is typically the voltage between the Full-Scale voltage and the Zero-Scale voltage ($V_{OUT(FS)}$ - $V_{OUT(ZS)}$), it is divided by the resolution of the device (Equation B-1).

EQUATION B-1: LSb VOLTAGE CALCULATION

$$V_{LSb} = \frac{V_{OUT(FS)} - V_{OUT(ZS)}}{2^N}$$

2^N = 64 (MCP47A1)

B.3 Monotonic Operation

Monotonic operation means that the device's output voltage (V_{OUT}) increases with every one code step (LSb) change (from terminal B to terminal A). The V_{OUT} voltage (V_W voltage) is the sum of all the Step voltages plus the voltage at Zero-Scale (V_{ZS}). The Zero-Scale voltage is dependent on the resistance between the tap 0 point and the B Terminal.

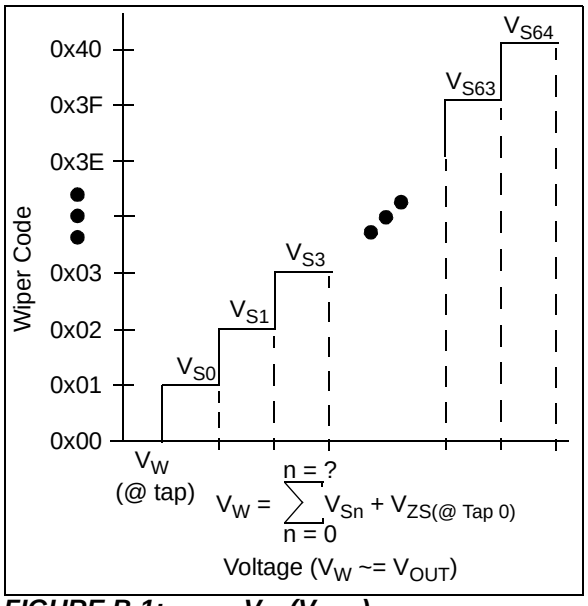


FIGURE B-1: V_W (V_{OUT}).

B.4 Full-Scale Error (FSE)

The Full-Scale Error (FSE) is the difference between the ideal and measured DAC output voltage with the Wiper's position set to its maximum (Wiper code = 40h); see Figure B-3. Full-scale error may also be thought of as the sum of the offset error plus gain error.

See Figure 2-9 through Figure 2-12 for FSE characterization graphs.

EQUATION B-2: FULL SCALE ERROR

$$FSE = \frac{V_{IDEAL(@FS)} - V_{OUT(@FS)}}{V_{LSb}}$$

Where:

FSE is expressed in LSb

$V_{OUT(@FS)}$ is the V_{OUT} voltage when the DAC register code is at Full-scale.

$V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at Full-scale.

V_{LSb} is the delta voltage of one DAC register code step (such as code 20h to code 21h).

B.5 Zero-Scale Error (ZSE)

The Zero-Scale Error (ZSE) is the difference between the ideal and measured V_{OUT} voltage with the Wiper position set to its minimum (Wiper code = 00h); see Figure B-3. The Zero-Scale Error is the same as the Offset Error for this case (Wiper code = 00h). Equation B-3 shows how to calculate the zero scale error.

See Figure 2-13 through Figure 2-16 for ZSE characterization graphs.

EQUATION B-3: ZERO SCALE ERROR

$$ZSE = \frac{V_{OUT(@ZS)}}{V_{LSb}}$$

Where:

FSE is expressed in LSb

$V_{OUT(@ZS)}$ is the V_{OUT} voltage when the DAC register code is at Zero-scale.

V_{LSb} is the delta voltage of one DAC register code step (such as code 20h to code 21h).

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B.6 Total Unadjusted Error

The Total Unadjusted Error is the difference between the ideal and measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve system performance.

Total Unadjusted Error can be calculated, see Equation B-4.

EQUATION B-4: TOTAL UNADJUSTED ERROR (LSb)

$$V_{IDEAL} = \frac{V_{REF}}{64} * DAC\ Code$$

$$V_{LSb} = \frac{V_{REF}}{64}$$

$$Error_{LSb} = \frac{V_{IDEAL} - V_{MEASURED}}{V_{LSb}}$$

Where:

V_{REF} is the voltage on the V_{REF} pin.

$V_{MEASURED}$ is the V_{OUT} voltage for the same DAC register code as V_{IDEAL} is calculated.

See Figure 2-17 through Figure 2-20 for Total Unadjusted Error characterization graphs.

B.7 Offset Error

The Offset error (see Figure B-2) is the deviation from zero voltage output when the volatile DAC Register value = 00h (zero scale voltage). This error affects all codes by the same amount. The offset error can be calibrated by software in application circuits.

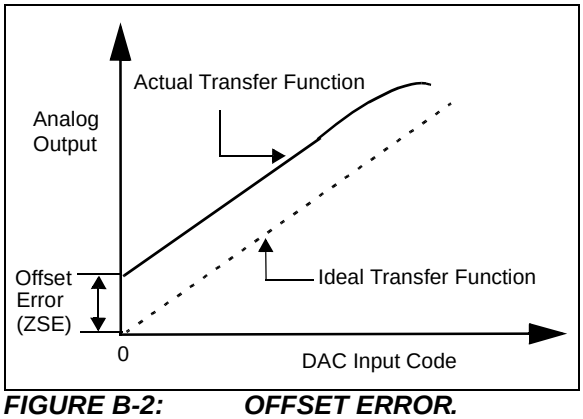


FIGURE B-2: OFFSET ERROR.

B.8 Offset Error Drift

The Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/^{o}C.

B.9 Gain Error

The Gain error (see Figure B-3) is the difference between the actual full-scale output voltage, from the ideal output voltage of the DAC transfer curve. The gain error is calculated after nullifying the offset error, or full scale error minus the offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full-scale range (% of FSR) or in LSb. The gain error is not calibrated at the factory and most of the gain error is contributed by the output buffer (op amp) saturation.

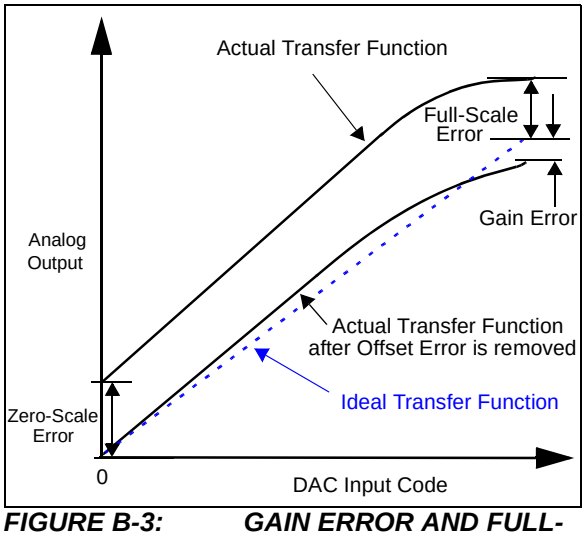


FIGURE B-3: GAIN ERROR AND FULL-SCALE ERROR EXAMPLE.

B.10 Gain Error Drift

The Gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/^{o}C.

B.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line).

In the MCP47A1, INL is calculated using two end points. The points used are Zero-Scale (00h) and Full-Scale - 1 (3Fh). INL can be expressed as a percentage of full scale range (FSR) or in a fraction of an LSb. INL is also called relative accuracy. Equation B-5 shows how to calculate the INL error in LSb and Figure B-4 shows an example of INL accuracy.

INL error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point after offset and gain errors have been removed. These endpoints are from 0x00 to 0x40 for the MCP47A1. Refer to Figure B-4.

Positive INL means higher V_{OUT} voltage than ideal. Negative INL means lower V_{OUT} voltage than ideal.

See Figure 2-1 through Figure 2-4 for INL characterization graphs.

EQUATION B-5: INL ERROR

$$INL_{LSb} = \frac{V_{OUT} - V_{IDEAL}}{V_S}$$

$$V_{IDEAL} = V_{ZS} + (V_S * DAC\ Code)$$

$$V_S = \frac{V_{(Code=63)} - V_{ZS}}{63}$$

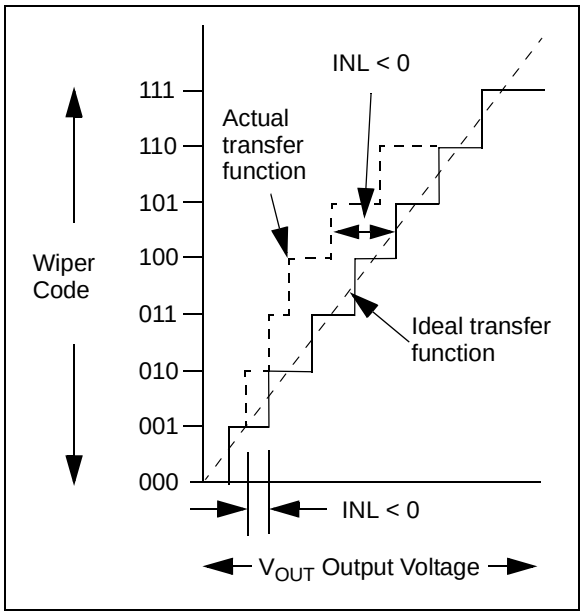


FIGURE B-4: INL ACCURACY.

B.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure B-5) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. The DNL error between any two adjacent codes is calculated as follows:

DNL error is the measure of variations in code widths from the ideal code width. A DNL error of zero would imply that every code is exactly 1 LSb wide.

See Figure 2-5 through Figure 2-8 for DNL characterization graphs.

EQUATION B-6: DNL ERROR

$$DNL_{LSb} = \frac{V_S - (V_{(Code = n)} - V_{(Code = n-1)})}{V_S}$$

$$V_S = \frac{V_{(Code=63)} - V_{ZS}}{63}$$

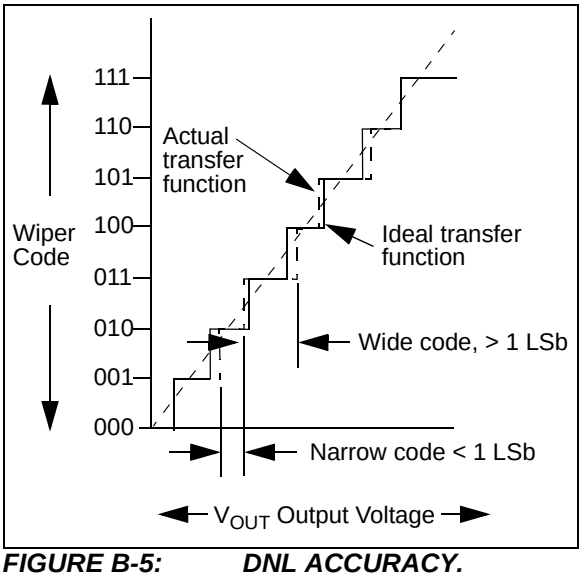


FIGURE B-5: DNL ACCURACY.

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B.13 Settling Time

The Settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition, to when the V_{OUT} voltage is within the specified accuracy.

In the MCP47A1, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC Register changes from 40h to 50h.

See Figure 2-36 through Figure 2-39 for Settling Time oscilloscope screen captures.

B.14 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec, and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: Wiper code changes from "011111" to "100000", or from "100000" to "011111").

B.15 Digital Feedthrough

The Digital feedthrough is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec, and is measured with a full scale change (Example: all 0s to all 1s and vice versa) on the digital input pins. The digital feedthrough is measured when the DAC is not being written to the output register.

B.16 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied +/- 10%, and expressed in dB or µV/V.

B.17 Ratiometric Temperature Coefficient

The ratiometric temperature coefficient quantifies the error in the ratio of the resistor setting (Resistance from VREF pin to Wiper position (R_{VREF-W}) and the Wiper position to Ground (R_{W-VSS}) due to temperature drift. This error also includes the drift of the output driver over temperature. This is typically the critical error when using a DAC.

See Figure 2-21 through Figure 2-24 for Tempco characterization graphs.

B.18 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (Nominal output voltage V_{OUT}) due to temperature drift. For a DAC, this error is typically not an issue, due to the ratiometric aspect of the output.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XXX	X	/XX
Device	I^2C Slave Address	Temperature Range	Package

Device:	MCP47A1T:	6-bit Single DAC with I^2C interface (Tape and Reel)
I^2C Slave Address	A0 = 5Ch A1 = 7Ch	
Temperature Range:	E = -40°C to +125°C	
Package:	LT = Plastic Small Outline Transistor (SC70), 6-lead	

Examples:

a) MCP47A1T-A0E/LT: 6-bit DAC, SC70-6, Address = 5Ch, Tape and Reel

b) MCP47A1T-A1E/LT: 6-bit DAC, SC70-6, Address = 7Ch, Tape and Reel

NOTES:

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