
MCP2518FD Silicon Errata and Data Sheet Clarification

The functionality of the MCP2518FD devices is described in the Device Data Sheet (DS20006027A), except for the anomalies described below.

1. Module: SPI Module

Incorrect CRC for certain READ_CRC commands

It is possible that there is a mismatch between the transmitted CRC and the actual CRC for the transmitted data when data is updated at a specific time during the SPI `READ_CRC` command. In these cases, the transmitted CRC is wrong and a glitch on the SDO line shorter than 1 bit in length occurs. The data transmitted is correct.

Fix/Workaround:

1) If a CRC mismatch occurs, re-issue the `READ_CRC` command.

Only bit 7/15/23/31 of the following registers can be affected:

CiTXIF
CiRXIF
CiCON
CiTBC
CiINT
CiRXOVIF
CiTXATIF
CiTXREQ
CiTREC
CiBDIAG0
CiBDIAG1
CiTXQSTA
CiFIFOSTAm

The occurrence can be minimized by not using FIFOs 7/15/23/31. In these cases, the registers CiTXIF, CiRXIF, CiRXOVIF, CiTXATIF and CiTXREQ are not affected.

Bit 31 of RAM reads with CRC can also be affected. This can be avoided by reading from a receive FIFO only after the message has been loaded into the FIFO, indicated by the receive flags. This is the recommended procedure independent of the issue described here.

MCP2518FD

Clarifications/Corrections to the Data Sheet:

In the MCP2518FD Data Sheet (DS20006027A), the following clarifications and corrections should be noted.

None.

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Initial Release of this Document.

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