

LIN Transceiver with Voltage Regulator

Features:

- Compliant with LIN Bus Specifications Version 1.3, 2.1 and with SAE J2602-2
- Supports Baud Rates up to 20 kBaud
- 43V Load Dump Protected
- Maximum Continuous Input Voltage: 30V
- Wide LIN-Compliant Supply Voltage: 6.0-18.0V
- Extended Temperature Range: -40°C to +125°C
- Interface to PIC® EUSART and Standard USARTs
- Wake-Up on LIN Bus Activity or Local Wake Input
- Local Interconnect Network (LIN) Bus Pin:
 - Internal Pull-Up Termination Resistor and Diode for Slave Node
 - Protected Against VBAT Shorts
 - Protected Against Loss of Ground
 - High-Current Drive
- TXD and LIN Bus Dominant Time-Out Function
- Two Low-Power Modes:
 - Transmitter Off: 90 μ A (typical)
 - Power Down: 4.5 μ A (typical)
- MCP2025 On-Chip Voltage Regulator:
 - Output Voltage of 5.0V or 3.3V at 70 mA Capability with Tolerances of $\pm 3\%$ Over the Temperature Range
 - Internal Short-Circuit Current Limit
 - External Components Limited to Filter Capacitor and Load Capacitor
- Automatic Thermal Shutdown
- High Electromagnetic Immunity (EMI), Low Electromagnetic Emission (EME)
- Robust ESD Performance: ± 15 kV for LBUS and VBB Pin (IEC61000-4-2)
- Transient Protection for LBUS and VBB pins in Automotive Environment (ISO7637)
- Meets Stringent Automotive Design Requirements, including "OEM Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications", Version 1.3, May 2012
- Multiple Package Options, Including Small 4x4 mm DFN Package

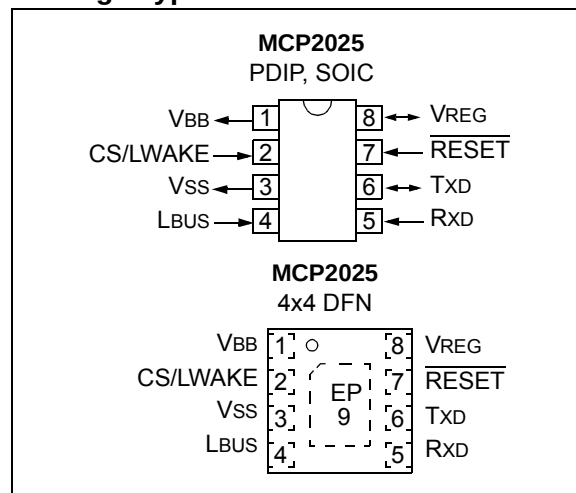
Description:

The MCP2025 provides a bidirectional, half-duplex communication physical interface to meet the LIN bus specification Revision 2.1 and SAE J2602-2. The device incorporates a voltage regulator with 5V or 3.3V at 70 mA regulated power supply output. The device has been designed to meet the stringent quiescent current requirements of the automotive industry, and will survive +43V load dump transients and double battery jumps.

The MCP2025 family members include:

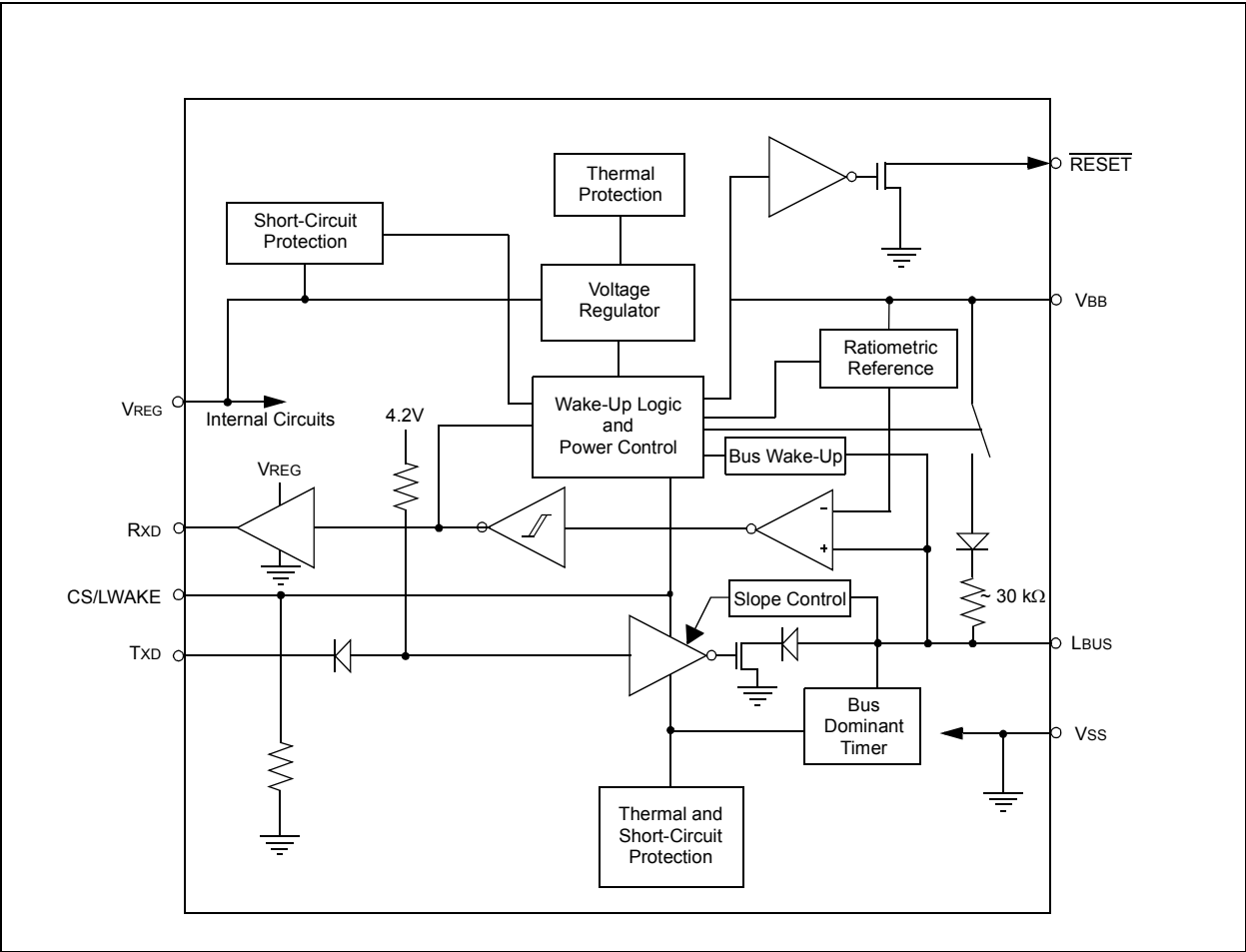
- MCP2025-500, 8-pin, LIN driver with 5.0V regulator
- MCP2025-330, 8-pin, LIN driver with 3.3V regulator

Package Types



MCP2025

MCP2025 Block Diagram



1.0 DEVICE OVERVIEW

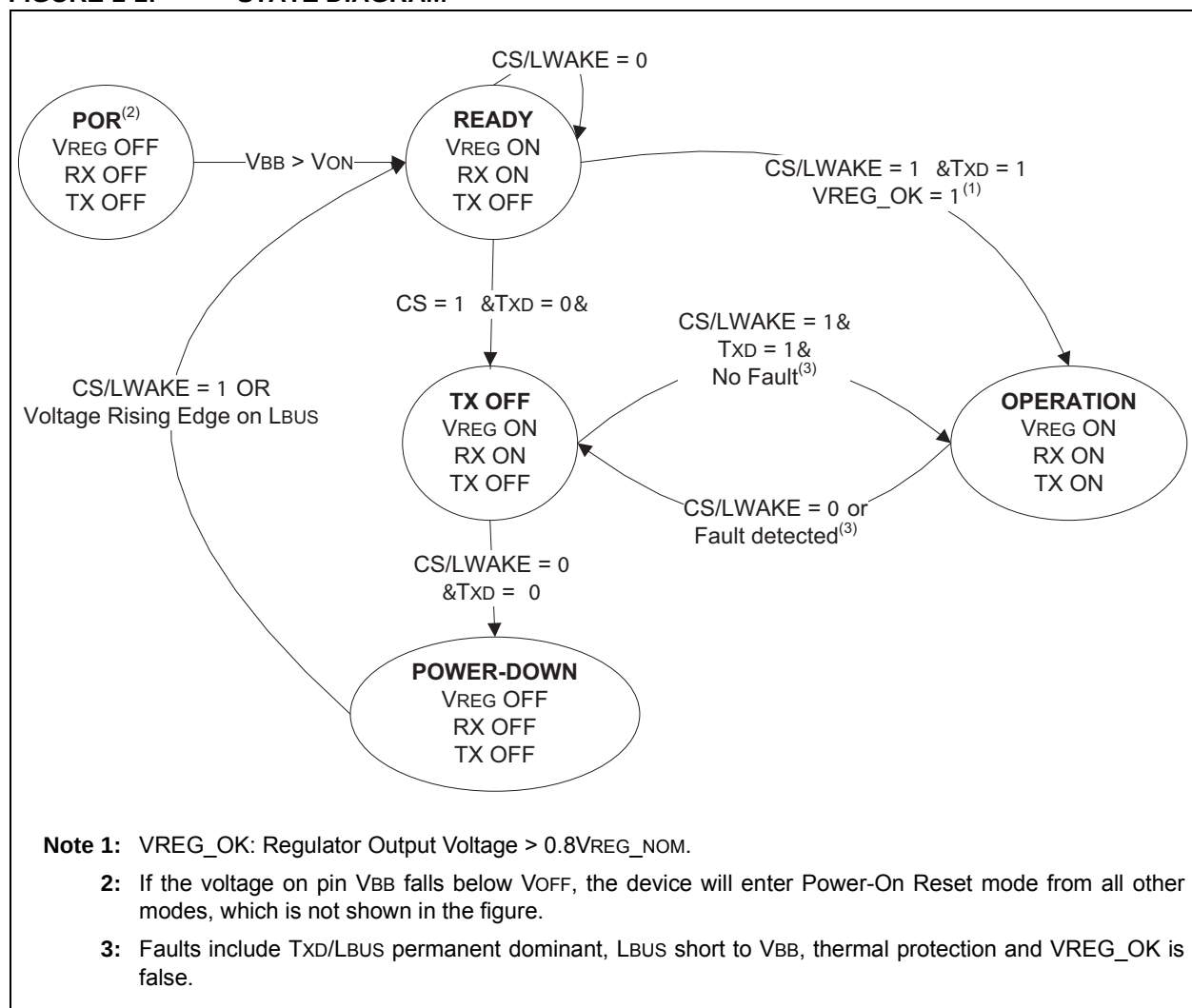
The MCP2025 provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus baud rates up to 20 kBaud. This device will translate the CMOS/TTL logic levels to LIN logic levels, and vice versa.

The device offers optimum EMI and ESD performance and it can withstand high voltage on the LIN bus. The device supports two low-power modes to meet automotive industry power consumption requirements. The MCP2025 also provides a +5V or 3.3V regulated power output at 70 mA.

1.1 Modes of Operation

The MCP2025 works in five modes: Power-On Reset, Power-Down, Ready, Operation and Transmitter Off. For an overview of all operational modes, please refer to [Table 1-1](#). For the operational mode transition, please refer to [Figure 1-1](#).

FIGURE 1-1: STATE DIAGRAM



1.1.1 POWER-ON RESET MODE

Upon application of VBB, or whenever the voltage on VBB is below the threshold of regulator turn-off voltage VOFF (typically 4.50V), the device enters Power-On Reset (POR) mode. During this mode, the device maintains the digital section in a Reset mode and waits until the voltage on the VBB pin rises above the threshold of regulator turn-on voltage VON (typically 5.75V) to enter Ready mode. In Power-On Reset mode, the LIN physical layer and voltage regulator are disabled and the RESET pin is switched to ground.

1.1.2 READY MODE

The device enters Ready mode from POR mode after the voltage on VBB rises above the threshold of regulator turn-on voltage VON, or from Power-Down mode when a remote or local wake-up event happens.

Upon entering Ready mode, the voltage regulator and the receiver section of the transceiver are powered-up. The transmitter remains in an off state. The device is ready to receive data, but not to transmit. In order to minimize the power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and it is thus slower. However, the 70 mA drive capability is unchanged.

The device stays in Ready mode until the output of the voltage regulator has stabilized and the CS/LWAKE pin is high ('1').

1.1.3 OPERATION MODE

If the CS/LWAKE pin changes to high while VREG is OK ($V_{REG} > 0.8 \cdot V_{REG_NOM}$) and the TXD pin is high, the part enters Operation mode from either Ready or Transmitter Off mode.

In this mode, all internal modules are operational. The internal pull-up resistor between LBUS and VBB is connected only in this mode.

The device goes into Transmitter Off mode at the falling edge on the CS/LWAKE pin or when a fault is detected.

Note:	The TXD pin needs to be set high before setting the CS/LWAKE pin to low in order to jump and stay in Transmitter Off mode. If the TXD pin is set or maintained low before setting the CS/LWAKE pin to low, the part will transition to Transmitter Off mode and then jump to Power-Down mode after a deglitch delay of about 20 μ s.
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1.1.4 TRANSMITTER OFF MODE

If VREG is OK ($V_{REG} > 0.8 \cdot V_{REG_NOM}$), the Transmitter Off mode can be reached from Ready mode by setting CS/LWAKE to high when the TXD pin is low, or from Operation mode by pulling down CS/LWAKE to low.

In Transmitter Off mode, the receiver is enabled but the LBUS transmitter is off. It is a lower-power mode.

In order to minimize power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and it is thus slower. However, the 70 mA drive capability is unchanged.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption on the bus during times of uncertain operation.

1.1.5 POWER-DOWN MODE

Power-Down mode is entered by pulling down both the CS/LWAKE pin and the TXD pin to low from Transmitter Off mode. In Power-Down mode, the transceiver and the voltage regulator are both off. Only the bus wake-up section and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest-power mode.

If any bus activity (e.g., a Break character) occurs or CS/LWAKE is set to high during Power-Down mode, the device will immediately enter Ready mode and enable the voltage regulator. Then, once the regulator output has stabilized (approximately 0.3 ms to 1.2 ms), it can go into either Operation mode or Transmitter Off mode. Refer to [Section 1.1.6 "Remote Wake-Up"](#) for more details.

1.1.6 REMOTE WAKE-UP

The Remote Wake-Up sub-module observes the LBUS in order to detect bus activity. In Power-Down mode, the normal LIN recessive/dominant threshold is disabled and the LIN bus wake-up voltage threshold VWK(LBUS) is used to detect bus activities. Bus activity is detected when the voltage on the LBUS falls below the LIN bus wake-up voltage threshold VWK(LBUS) (approximately 3.4V) for at least tBDB (a typical duration of 80 μ s) followed by a rising edge. Such a condition causes the device to leave Power-Down mode.

TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Internal Wake Module	Voltage Regulator	Operation	Comments
POR	OFF	OFF	OFF	OFF	Proceed to Ready mode after $V_{BB} > V_{ON}$.	—
Ready	OFF	ON	OFF	ON	If CS/LWAKE is high, then proceed to Operation or Transmitter Off mode.	Bus Off state
Operation	ON	ON	OFF	ON	If CS/LWAKE is low, then proceed to Transmitter Off mode.	Normal Operation mode
Power-Down	OFF	OFF	ON Activity Detect	OFF	On LIN bus rising edge or CS/LWAKE high level, go to Ready mode.	Lowest-Power mode
Transmitter Off	OFF	ON	OFF	ON	If TxD and CS/LWAKE are low, then proceed to Power-Down mode. If TxD and CS/LWAKE are high, then proceed to Operation mode.	Bus Off state, lower-power mode

1.2 Pin Descriptions

The descriptions of the pins are listed in [Table 1-2](#).

TABLE 1-2: PIN FUNCTION TABLE

Pin Name	Pin Number		Pin Type	Description
	8-lead PDIP	4x4 DFN		
VBB	1	1	Power	Battery
CS/LWAKE	2	2	TTL input, HV-tolerant	Chip Select and Local Wake-up Input
VSS	3	3	Power	Ground
LBUS	4	4	I/O, HV	LIN Bus
RxD	5	5	Output	Receive Data Output
TxD	6	6	Input, HV-tolerant	Transmit Data Input
$\overline{\text{RESET}}$	7	7	Open-drain output, HV-tolerant	Reset Output
VREG	8	8	Output	Voltage Regulator Output
EP	—	9	—	Exposed Thermal Pad

1.2.1 BATTERY POSITIVE SUPPLY VOLTAGE (VBB)

Battery Positive Supply Voltage pin. An external diode is connected in series to prevent the device from being reversely powered (refer to [Figure 1-7](#)).

1.2.2 CHIP SELECT AND LOCAL WAKE-UP INPUT (CS/LWAKE)

Chip Select and Local Wake-Up Input pin (TTL level, high-voltage tolerant). This pin controls the device state transition. Refer to [Figure 1-1](#).

An internal pull-down resistor will keep the CS/LWAKE pin low to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-On Reset and I/O initialization sequence. When CS/LWAKE is '1', a weak pull-down (~600 kΩ) is used to reduce current. When CS/LWAKE is '0', a stronger pull-down (~300 kΩ) is used to maintain the logic level.

This pin may also be used as a local wake-up input (see [Figure 1-7](#)). The microcontroller will set the I/O pin to control the CS/LWAKE. An external switch or another source can then wake up both the transceiver and the microcontroller.

Note: CS/LWAKE should NOT be tied directly to the VREG pin, as this could force the MCP2025 into Operation mode before the microcontroller is initialized.

1.2.3 GROUND (VSS)

Ground pin.

1.2.4 LIN BUS (LBUS)

LIN Bus pin. LBUS is a bidirectional LIN bus interface pin and is controlled by the signal TxD. It has an open collector output with a current limitation. To reduce electromagnetic emission, the slopes during signal changes are controlled and the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus and generates the output signal RxD that follows the state of the LBUS. A 1st degree 160 kHz low-pass input filter optimizes electromagnetic immunity.

1.2.5 RECEIVE DATA OUTPUT (RxD)

Receive Data Output pin. The RxD pin is a standard CMOS output pin and it follows the state of the LBUS pin.

1.2.6 TRANSMIT DATA INPUT (TxD)

Transmit Data Input pin (TTL level, HV-compliant, adaptive pull-up). The transmitter reads the data stream on the TxD pin and sends it to the LIN bus. The LBUS pin is low (dominant) when TxD is low, and high (recessive) when TxD is high.

TxD is internally pulled-up to approximately 4.2V. When TxD is '0', a weak pull-up (~900 kΩ) is used to reduce current. When TxD is '1', a stronger pull-up (~300 kΩ) is used to maintain the logic level. A series reverse-blocking diode allows applying TxD input voltages greater than the internally generated 4.2V and renders the TxD pin HV-compliant up to 30V (see [MCP2025 Block Diagram](#)).

1.2.7 $\overline{\text{RESET}}$

Reset output pin. This is an open-drain output pin. It indicates the internal voltage has reached a valid, stable level. As long as the internal voltage is valid (above 0.8 V_{REG}), this pin will present high impedance; otherwise, the $\overline{\text{RESET}}$ pin switches to ground.

1.2.8 POSITIVE SUPPLY VOLTAGE REGULATOR OUTPUT (V_{REG})

Positive Supply Voltage Regulator Output pin. An on-chip Low Dropout Regulator (LDO) gives +5.0 or +3.3V at 70 mA regulated voltage on this pin.

1.2.9 EXPOSED THERMAL PAD (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the VSS pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

1.3 Fail-Safe Features

1.3.1 GENERAL FAIL-SAFE FEATURES

- An internal pull-down resistor on the CS/LWAKE pin disables the transmitter if the pin is floating.
- An internal pull-up resistor on the TXD pin places TXD in high and the LBUS in recessive if the TXD pin is floating.
- High-Impedance and low-leakage current on LBUS during loss of power or ground.
- The current limit on LBUS protects the transceiver from being damaged if the pin is shorted to V_{BB} .

1.3.2 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

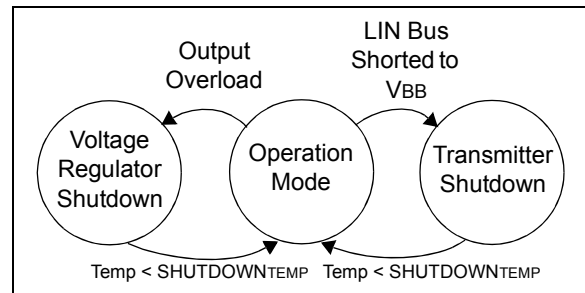
There are three causes for a thermal overload. A thermal shutdown can be triggered by any one, or a combination of, the following thermal overload conditions:

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

The recovery time from the thermal shutdown is equal to adequate cooling time.

Driving the TXD and checking the RXD pin make it possible to determine whether there is a bus contention (TXD = high, RXD = low) or a thermal overload condition (TXD = low, RXD = high).

FIGURE 1-2: THERMAL SHUTDOWN STATE DIAGRAMS



1.3.3 TXD/LBUS TIME-OUT TIMER

The LIN bus can be driven to a dominant level, either from the TXD pin or externally. An internal timer deactivates the LBUS transmitter if a dominant status (low) on the LIN bus lasts longer than Bus Dominant Time-Out Time, $t_{\text{TO(LIN)}}$ (approximately 20 milliseconds). At the same time, the RXD output is put in recessive (high) and the internal pull-up resistor between LBUS and V_{BB} is disconnected. The timer is reset on any recessive LBUS status or POR mode. The recessive status on LBUS can be caused either by the bus being externally pulled-up or by the TXD pin being returned high.

1.4 Internal Voltage Regulator

The MCP2025 has a positive regulator capable of supplying +5.00 or +3.30 VDC $\pm 3\%$ at up to 70 mA of load current over the entire operating temperature range of -40°C to $+125^{\circ}\text{C}$. The regulator uses an LDO design, is short-circuit-protected and will turn the regulator output off if its output falls below the shutdown voltage threshold, V_{SD} .

With a load current of 70 mA, the minimum input-to-output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 μA with a full 70 mA load current when the input-to-output voltage differential is greater than +3.00V.

Regarding the correlation between V_{BB} , V_{REG} and I_{DD} , please refer to [Figures 1-4](#) and [1-5](#). When the input voltage (V_{BB}) drops below the differential needed to provide stable regulation, the voltage regulator output, V_{REG} , will track the input down to approximately V_{OFF} , at which point the regulator will turn off the output. This will allow PIC[®] microcontrollers with internal POR circuits to generate a clean arming of the POR trip point. The MCP2025 will then monitor V_{BB} and turn on the regulator when V_{BB} is above the threshold of regulator turn-on voltage, V_{ON} .

In Power-Down mode, the V_{BB} monitor is turned off.

MCP2025

Under specific ambient temperature and battery voltage range, the voltage regulator can output as high as 150 mA current. For current load capability of the voltage regulator, refer to [Figures 2-8 and 2-9](#).

Note: The regulator has an overload current limit of approximately 250 mA. The regulator output voltage, VREG, is monitored. If output voltage VREG is lower than VSD, the voltage regulator will turn off. After a recovery time of about 3 ms, the VREG will be checked again. If there is no short circuit, (VREG > VSD), then the voltage regulator remains on.

The regulator requires an external output bypass capacitor for stability. See [Figure 2-1](#) for correct capacity and ESR for stable operation.

Note: A ceramic capacitor of at least 10 μF or a tantalum capacitor of at least 2.2 μF is recommended for stability.

In worst-case scenarios, the ceramic capacitor may derate by 50%, based on tolerance, voltage and temperature. Therefore, in order to ensure stability, ceramic capacitors smaller than 10 μF may require a small series resistance to meet the ESR requirements, as shown in [Table 1-3](#).

TABLE 1-3: RECOMMENDED SERIES RESISTANCE FOR CERAMIC CAPACITORS

Resistance	Capacitor
1 Ω	1 μF
0.47 Ω	2.2 μF
0.22 Ω	4.7 μF
0.1 Ω	6.8 μF

FIGURE 1-3: VOLTAGE REGULATOR BLOCK DIAGRAM

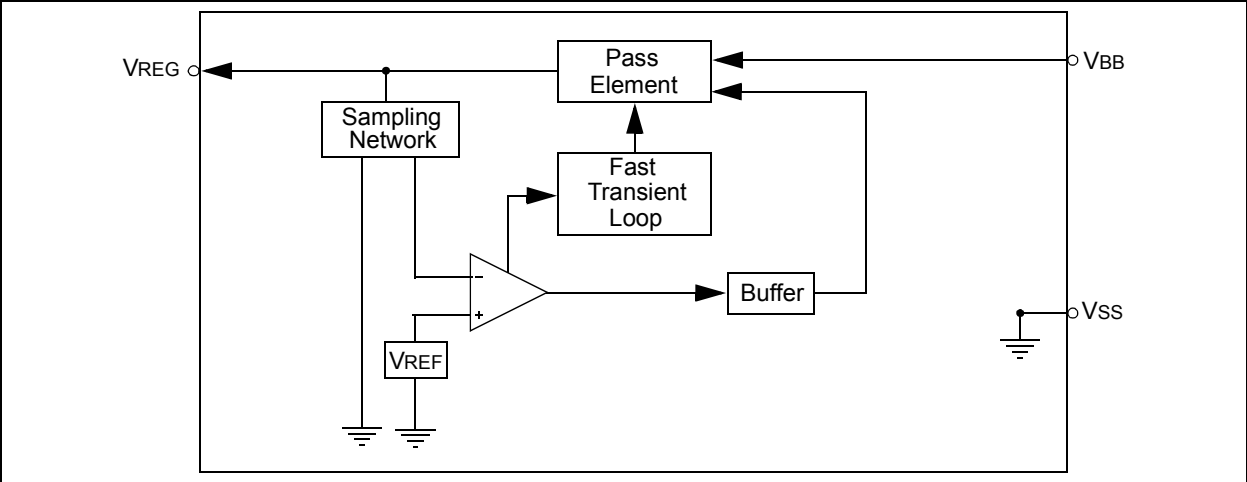


FIGURE 1-4: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET

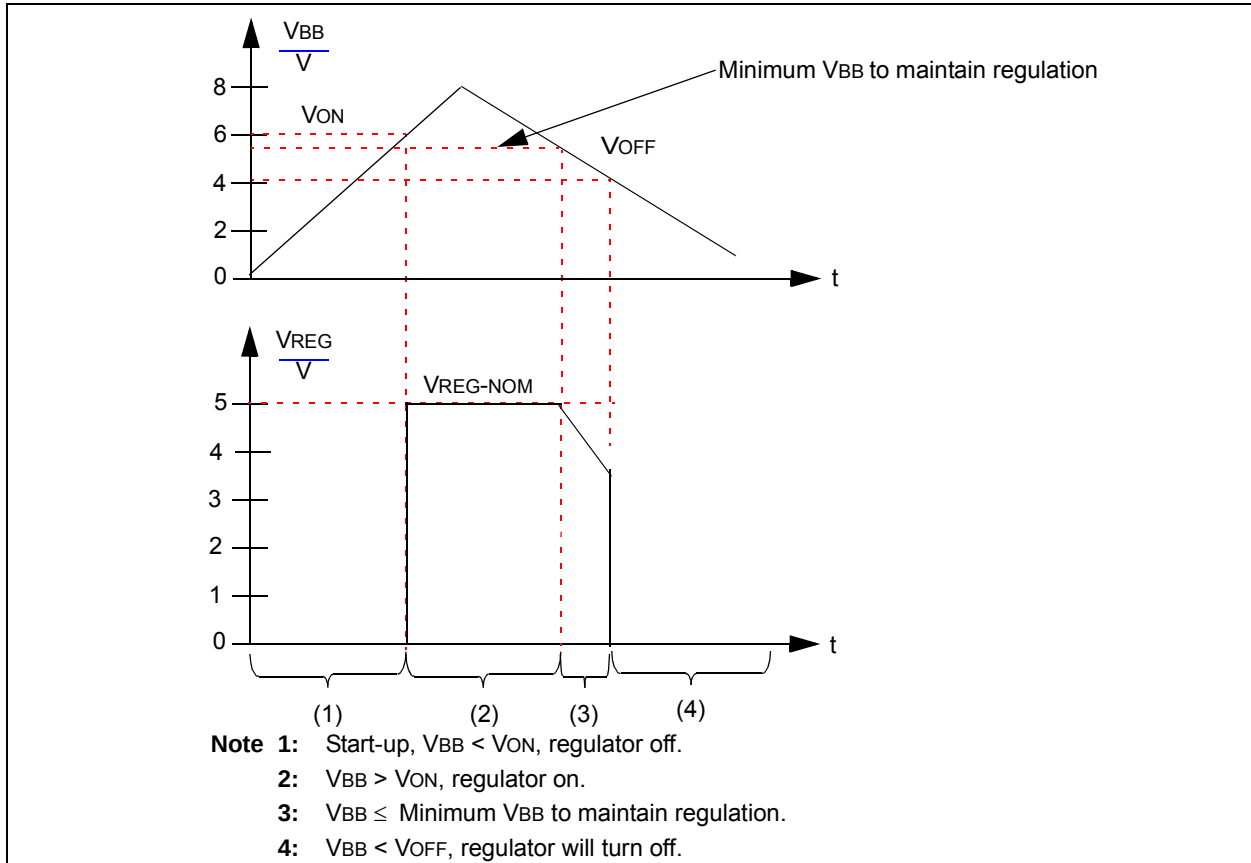
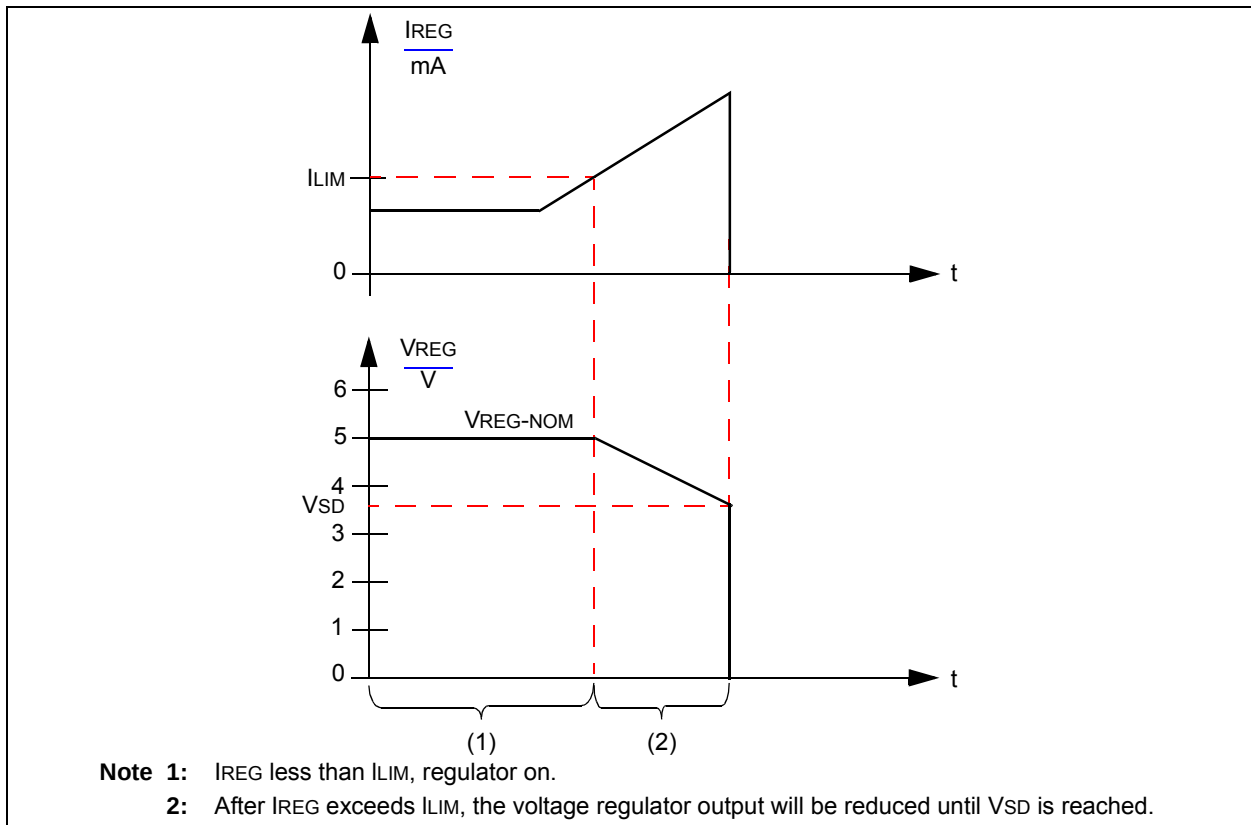


FIGURE 1-5: VOLTAGE REGULATOR OUTPUT ON OVERCURRENT SITUATION



1.5 Optional External Protection

1.5.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see [Figure 1-7](#)).

1.5.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between V_{BB} and ground, with a transient protection resistor (R_{TP}) in series with the battery supply and the V_{BB} pin, protects the device from power transients and ESD events greater than 43V (see [Figure 1-7](#)). The maximum value for the R_{TP} protection resistor depends upon two parameters: the minimum voltage the part will start at and the impacts of this R_{TP} resistor on the V_{BB} value, thus on the bus recessive level and slopes.

This leads to a set of three equations to fulfill.

[Equation 1-1](#) provides a maximum R_{TP} value according to the minimum battery voltage the user wants.

[Equation 1-2](#) provides a maximum R_{TP} value according to the maximum error on the recessive level, thus V_{BB}, since the part uses V_{BB} as the reference value for the recessive level.

[Equation 1-3](#) provides a maximum R_{TP} value according to the maximum relative variation the user can accept on the slope when I_{REG} varies.

Since both [Equations 1-1](#) and [1-2](#) must be fulfilled, the maximum allowed value for R_{TP} is thus the smaller of the two values found when solving [Equations 1-1](#) and [1-2](#).

Usually, [Equation 1-1](#) gives the higher constraint (smaller value) for R_{TP}, as shown in the following example where V_{BATMIN} is 8V.

However, the user needs to verify that the value found with [Equation 1-1](#) fulfills [Equations 1-2](#) and [1-3](#).

While this protection is optional, it should be considered as good engineering practice.

EQUATION 1-1:

$$R_{TP} \leq \frac{V_{BATMIN} - 5.5V}{250 \text{ mA}}$$

$$5.5V = V_{OFF} + 1.0V$$

Where:

250 mA = Peak current at power-on when V_{BB} = 5.5V

Assume that V_{BATMIN} = 8V. [Equation 1-1](#) gives 10Ω.

EQUATION 1-2:

$$R_{TP} \leq \frac{\Delta V_{RECESSIVE}}{I_{REGMAX}}$$

Where:

ΔV_{RECESSIVE} = Maximum variation tolerated on the recessive level

Assume that ΔV_{RECESSIVE} = 1V and I_{REGMAX} = 50 mA. [Equation 1-2](#) gives 20Ω.

EQUATION 1-3:

$$R_{TP} \leq \frac{\Delta \text{Slope} \times (V_{BATMIN} - 1V)}{I_{REGMAX}}$$

Where:

ΔSlope = Maximum variation tolerated on the slope level

I_{REGMAX} = Maximum current the current will provide to the load

V_{BATMIN} > V_{OFF} + 1.0V

Assume that ΔSlope = 15%, V_{BATMIN} = 8V and I_{REGMAX} = 50 mA. [Equation 1-3](#) gives 20Ω.

1.5.3 C_{BAT} CAPACITOR

Selecting C_{BAT} = 10 x C_{REG} is recommended. However, this leads to a high-value capacitor. Lower values for C_{BAT} capacitor can be used with respect to some rules. In any case, the voltage at the V_{BB} pin should remain above V_{OFF} when the device is turned on.

The current peak at start-up (due to the fast charge of the C_{REG} and C_{BAT} capacitors) may induce a significant drop on the V_{BB} pin. This drop is proportional to the impedance of the V_{BAT} connection (see [Figure 1-7](#)).

The V_{BAT} connection is mainly inductive and resistive. Therefore, it can be modeled as a resistor (R_{TOT}) in series with an inductor (L). R_{TOT} and L can be measured.

The following formula gives an indication of the minimum value of C_{BAT} using R_{TOT} and L:

EQUATION 1-4:

$$\frac{C_{BAT}}{C_{REG}} = \sqrt{\frac{100L^2 + R_{TOT}^2}{1 + L^2 + \frac{R_{TOT}^2}{100}}}$$

Where:

L = Inductor (measured in mH)

R_{TOT} = R_{LINE} + R_{TP} (measured in Ω)

[Equation 1-4](#) allows lower C_{BAT}/C_{REG} values than the 10x ratio we recommend.

Assume that we have a good quality VBAT connection with $R_{TOT} = 0.1\Omega$ and $L = 0.1$ mH.

Solving the equation gives $C_{BAT}/C_{REG} = 1$.

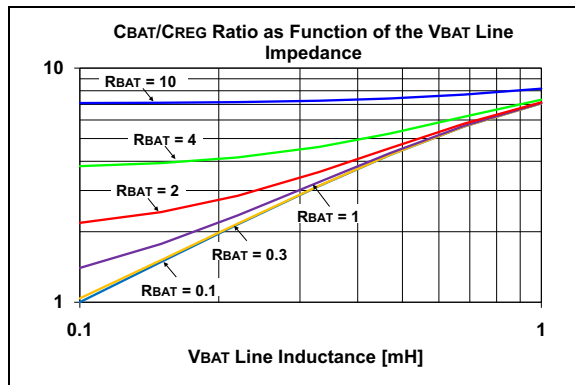
If we increase R_{TOT} up to 1Ω , the result becomes $C_{BAT}/C_{REG} = 1.4$. However, if the connection is highly resistive or highly inductive (poor connection), the C_{BAT}/C_{REG} ratio greatly increases.

TABLE 1-4: C_{BAT}/C_{REG} RATIO BY VBAT CONNECTION TYPE

Connection Type	R_{TOT}	L	C_{BAT}/C_{REG} Ratio
Good	0.1Ω	0.1 mH	1
Typical	1Ω	0.1 mH	1.4
Highly inductive	0.1Ω	1 mH	7
Highly resistive	10Ω	0.1 mH	7

Figure 1-6 shows the minimum recommended C_{BAT}/C_{REG} ratio as a function of the impedance of the VBAT connection.

FIGURE 1-6: Minimum Recommended C_{BAT}/C_{REG} Ratio



MCP2025

1.6 Typical Applications

FIGURE 1-7: TYPICAL APPLICATION CIRCUIT

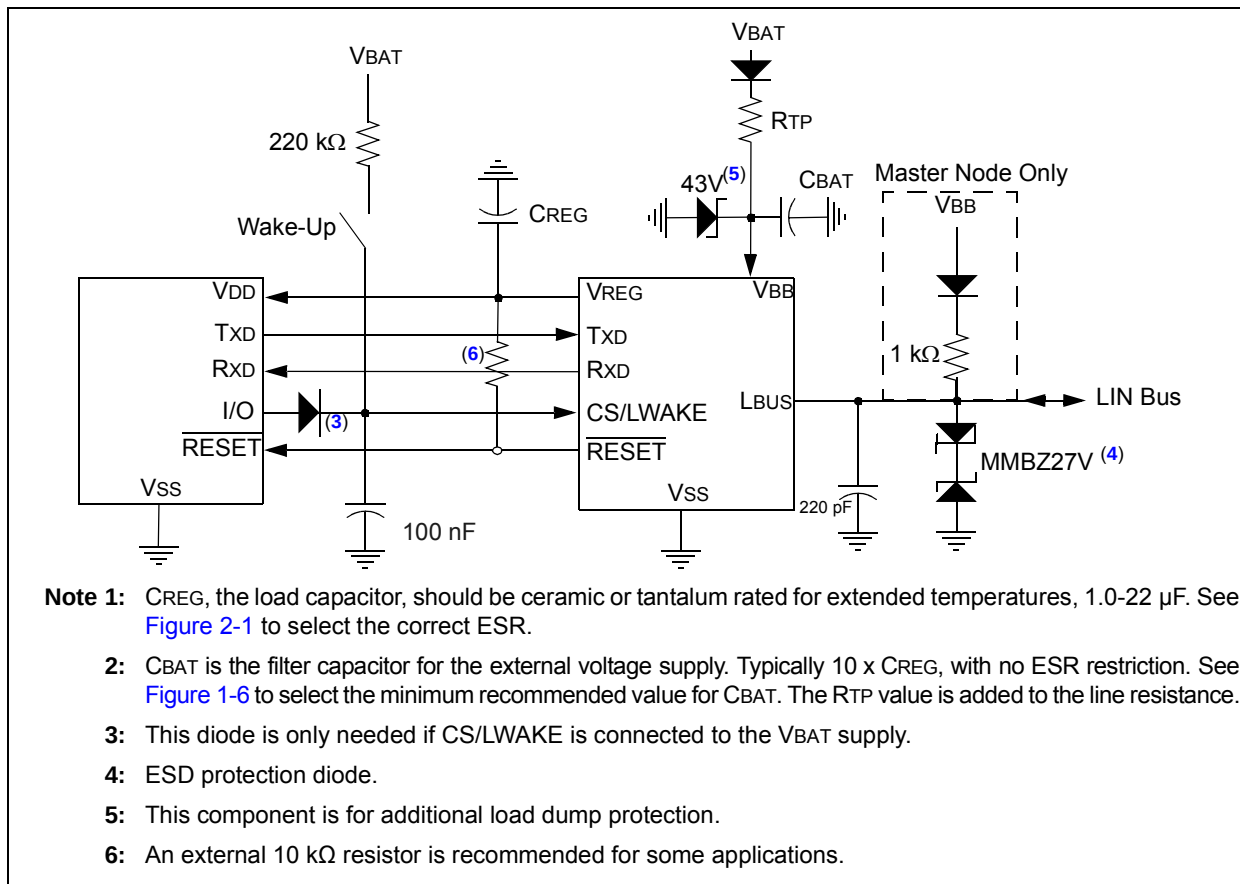
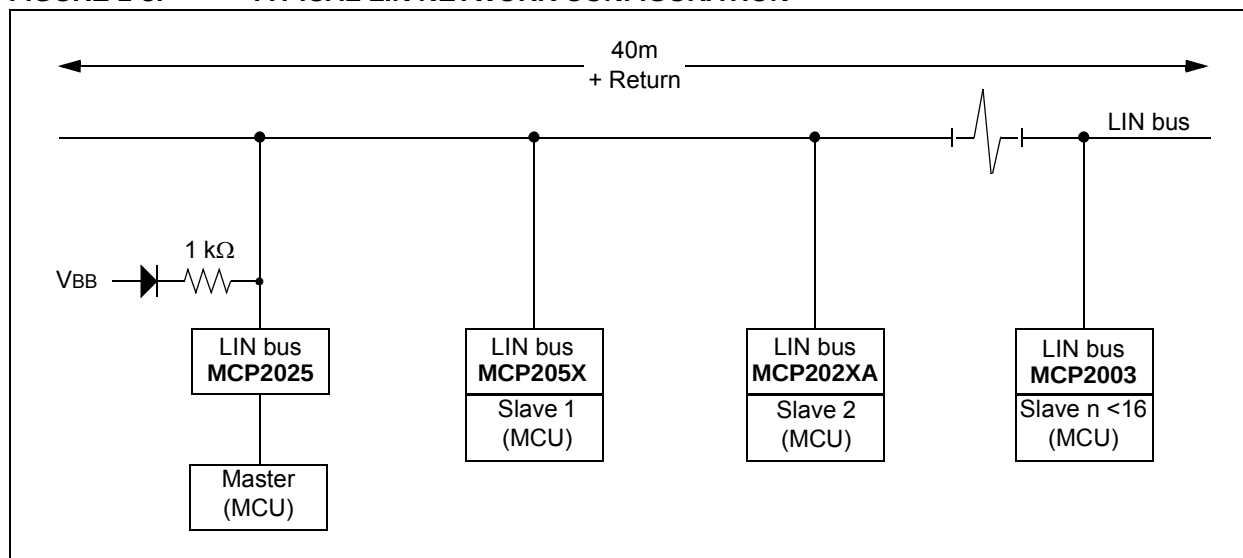


FIGURE 1-8: TYPICAL LIN NETWORK CONFIGURATION



1.7 ICSP™ Considerations

The following should be considered when the MCP2025 are connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller can be supplied from the programmer or from the MCP2025.

The voltage on the VREG pin should not exceed the maximum value of VREG in [DC Specifications](#).

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V _{IN} DC Voltage on RXD and $\overline{\text{RESET}}$	-0.3V to V _{REG} + 0.3
V _{IN} DC Voltage on TXD, CS/LWAKE	-0.3 to +40V
V _{BB} Battery Voltage, continuous, non-operating (Note 1)	-0.3 to +40V
V _{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) (Note 2)	-0.3 to +43V
V _{BB} Battery Voltage, transient ISO 7637 Test 1	-100V
V _{BB} Battery Voltage, transient ISO 7637 Test 2a	+75V
V _{BB} Battery Voltage, transient ISO 7637 Test 3a	-150V
V _{BB} Battery Voltage, transient ISO 7637 Test 3b	+100V
V _{LBUS} Bus Voltage, continuous	-18 to +30V
V _{LBUS} Bus Voltage, transient (Note 3)	-27 to +43V
I _{LBUS} Bus Short Circuit Current Limit	200 mA
ESD protection on LIN, V _{BB} (IEC 61000-4-2) (Note 4)	±15 V
ESD protection on LIN, V _{BB} (Human Body Model) (Note 5)	±8 kV
ESD protection on all other pins (Human Body Model) (Note 5)	±4 kV
ESD protection on all pins (Charge Device Model) (Note 6)	±1500V
ESD protection on all pins (Machine Model) (Note 7)	±200V
Maximum Junction Temperature	150°C
Storage Temperature	-65 to +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: LIN 2.x compliant specification.

2: SAE J2602-2 compliant specification.

3: ISO 7637/1 load dump compliant (t < 500 ms).

4: According to IEC 61000-4-2, 330Ω, 150 pF and Transceiver EMC Test Specifications [2] to [4].

5: According to AEC-Q100-002/JESD22-A114.

6: According to AEC-Q100-011B.

7: According to AEC-Q100-003/JESD22-A115.

2.2 Nomenclature Used in this Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term used in the following tables	Definition
VBAT	<i>not used</i>	ECU operating voltage
VSUP	V _{BB}	Supply voltage at device pin
VBUS_LIM	I _{SC}	Current limit of driver
VBUSREC	V _{IH} (LBUS)	Recessive state
VBUSDOM	V _{IL} (LBUS)	Dominant state

2.3 DC Specifications

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_{REG} = 10 \mu F$.				
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power						
VBB Quiescent Operating Current	IBBQ	—	—	200	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 5.0V$
		—	—	200	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 3.3V$
VBB Ready Current	IBBRD	—	—	100	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 5.0V$
		—	—	100	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 3.3V$
VBB Transmitter-Off Current with Watchdog Disabled	IBBTO	—	—	100	μA	With voltage regulator on, transmitter off, receiver on, $CS = V_{IH}$, $V_{REG} = 5.0V$
		—	—	100	μA	With voltage regulator on, transmitter off, receiver on, $CS = V_{IH}$, $V_{REG} = 3.3V$
VBB Power-Down Current	IBBPD	—	4.5	8	μA	With voltage regulator off, receiver on and transmitter off, $CS = V_{IL}$
VBB Current with VSS Floating	IBBNOGND	-1	—	1	mA	$V_{BB} = 12V$, GND to VBB, $V_{LIN} = 0 - 18V$
Microcontroller Interface						
High-Level Input Voltage (TXD)	V_{IH}	2.0	—	30	V	
Low-Level Input Voltage (TXD)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (TXD)	I_{IH}	-2.5	—	0.4	μA	Input voltage = 4.0V ~800 k Ω internal adaptive pull-up
Low-Level Input Current (TXD)	I_{IL}	-10	—	—	μA	Input voltage = 0.5V ~800 k Ω internal adaptive pull-up
High-Level Input Voltage (CS/LWAKE)	V_{IH}	2	—	30	V	Through a current-limiting resistor
Low-Level Input Voltage (CS/LWAKE)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (CS/LWAKE)	I_{IH}	—	—	8.0	μA	Input voltage = 0.8 V_{REG} ~1.3 M Ω internal pull-down to VSS

Note 1: Internal current limited. 2.0 ms maximum recovery time ($R_{LBUS} = 0\Omega$, $TX = 0$, $V_{LBUS} = V_{BB}$).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; $V_{WK}(LBUS)$ is used to detect bus activities.

2.3 DC Specifications (Continued)

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_{REG} = 10 \mu F$.				
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Low-Level Input Current (CS/LWAKE)	IIL	—	—	5.0	μA	Input voltage = $0.2V_{REG}$ ~1.3 M Ω internal pull-down to VSS
Low-Level Output Voltage (RXD)	VOLRXD	—	—	$0.2V_{REG}$	V	IOL = 2 mA
High-Level Output Voltage (RXD)	VOHRXD	$0.8V_{REG}$	—	—	V	IOH = 2 mA
Bus Interface						
High-Level Input Voltage	VIH(LBUS)	$0.6 V_{BB}$	—	—	V	Recessive state
Low-Level Input Voltage	VIL(LBUS)	-8	—	$0.4 V_{BB}$	V	Dominant state
Input Hysteresis	VHYS	—	—	$0.175 V_{BB}$	V	VIH(LBUS) – VIL(LBUS)
Low-Level Output Current	IOL(LBUS)	40	—	200	mA	Output voltage = $0.1 V_{BB}$, $V_{BB} = 12V$
Pull-Up Current on Input	IPU(LBUS)	-180	—	-72	μA	~30 k Ω internal pull-up @ VIH(LBUS) = $0.7 V_{BB}$, $V_{BB} = 12V$
Short Circuit Current Limit	ISC	50	—	200	mA	Note 1
High-Level Output Voltage	VOH(LBUS)	$0.8 V_{BB}$	—	V_{BB}	V	
Driver Dominant Voltage	V_LOSUP	—	—	1.1	V	$V_{BB} = 7.3V$ RLOAD = 1000 Ω
	V_HISUP	—	—	1.2	V	$V_{BB} = 18V$ RLOAD = 1000 Ω
Input Leakage Current (at the receiver during dominant bus level)	IBUS_PAS_DOM	-1	—	—	mA	Driver off $V_{BUS} = 0V$ $V_{BB} = 12V$
Input Leakage Current (at the receiver during recessive bus level)	IBUS_PAS_REC	-20	—	20	μA	Driver off $8V < V_{BB} < 18V$ $8V < V_{BUS} < 18V$ $V_{BUS} \geq V_{BB}$
Leakage Current (disconnected from ground)	IBUS_NO_GND	-10	—	+10	μA	GNDDEVICE = V_{BB} $0V < V_{BUS} < 18V$ $V_{BB} = 12V$
Leakage Current (disconnected from VBB)	IBUS_NO_PWR	-10	—	+10	μA	$V_{BB} = GND$ $0 < V_{BUS} < 18V$
Receiver Center Voltage	VBUS_CNT	$0.475 V_{BB}$	$0.5 V_{BB}$	$0.525 V_{BB}$	V	$V_{BUS_CNT} = (V_{IL}(LBUS) + V_{IH}(LBUS))/2$
Slave Termination	RSLAVE	20	30	47	k Ω	Note 2
Capacitance of Slave Node	CSLAVE	—	—	50	pF	Note 2
Wake-Up Voltage Threshold on LIN Bus	VWK(LBUS)	—	—	3.4	V	Wake up from Power-Down mode (Note 3)

Note 1: Internal current limited. 2.0 ms maximum recovery time ($R_{LBUS} = 0\Omega$, $T_X = 0$, $V_{LBUS} = V_{BB}$).

Note 2: Characterized, not 100% tested.

Note 3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; VWK(LBUS) is used to detect bus activities.

2.3 DC Specifications (Continued)

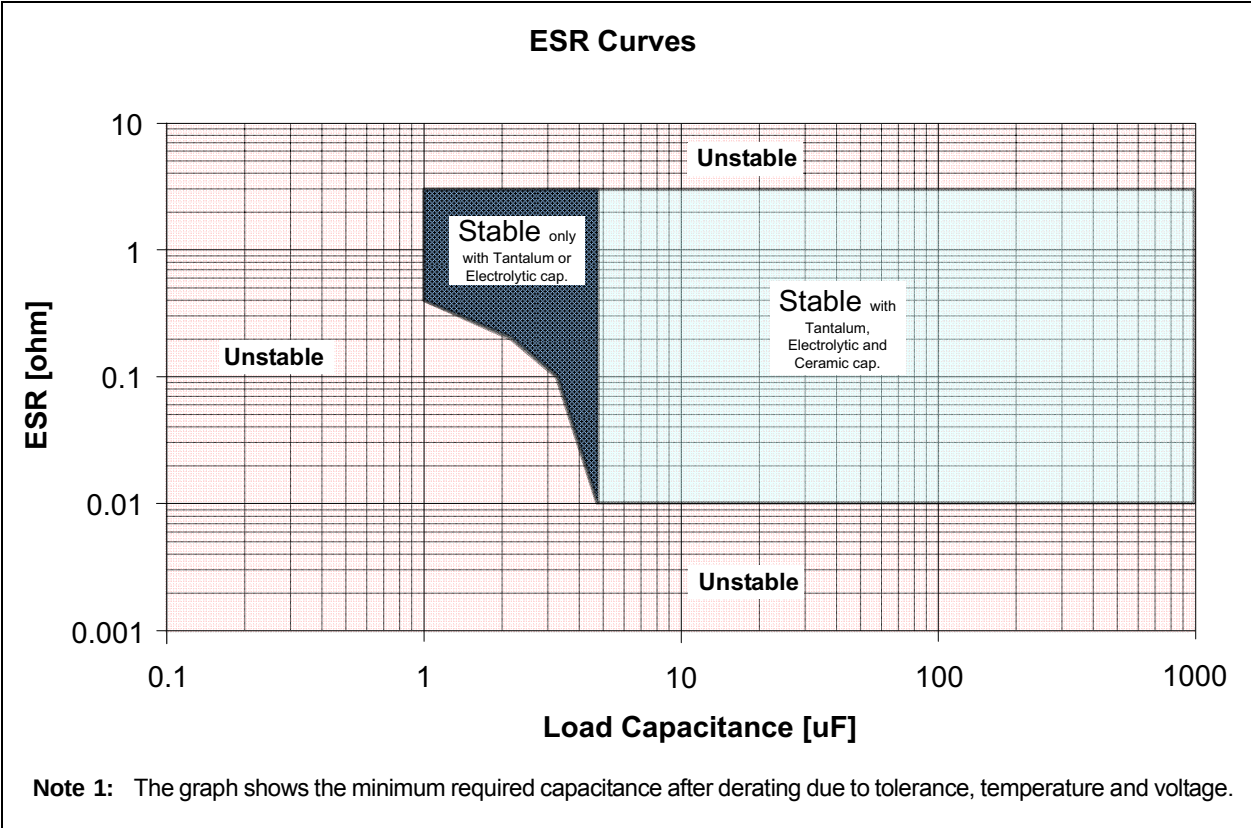
DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_{REG} = 10 \mu F$.				
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Voltage Regulator – 5.0V						
Output Voltage Range	V_{REG}	4.85	5.00	5.15	V	$0 \text{ mA} < I_{OUT} < 70 \text{ mA}$
Line Regulation	ΔV_{OUT1}	—	10	50	mV	$I_{OUT} = 1 \text{ mA}$ $6.0V < V_{BB} < 18V$
Load Regulation	ΔV_{OUT2}	—	10	50	mV	$5 \text{ mA} < I_{OUT} < 70 \text{ mA}$ $6.0V < V_{BB} < 12V$
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 VPP @ 10-20 kHz $I_{LOAD} = 20 \text{ mA}$
Output Noise Voltage	eN	—	—	100	μV_{RMS}	10 Hz – 40 MHz $C_{FILTER} = 10 \mu F$ $C_{BP} = 0.1 \mu F$ $I_{LOAD} = 20 \text{ mA}$
Shutdown Voltage Threshold	V_{SD}	3.5	—	4.0	V	See Figure 1-5 (Note 2)
Input Voltage to Turn-Off Output	V_{OFF}	3.9	—	4.5	V	—
Input Voltage to Turn-On Output	V_{ON}	5.25	—	6.0	V	—
Voltage Regulator – 3.3V						
Output Voltage	V_{REG}	3.20	3.30	3.40	V	$0 \text{ mA} < I_{OUT} < 70 \text{ mA}$
Line Regulation	ΔV_{OUT1}	—	10	50	mV	$I_{OUT} = 1 \text{ mA}$ $6.0V < V_{BB} < 18V$
Load Regulation	ΔV_{OUT2}	—	10	50	mV	$5 \text{ mA} < I_{OUT} < 70 \text{ mA}$ $6.0V < V_{BB} < 12V$
Power Supply Ripple Reject	PSRR	—	50	—	dB	1 VPP @ 10-20 kHz $I_{LOAD} = 20 \text{ mA}$
Output Noise Voltage	eN	—	—	100	μV_{RMS} $/\sqrt{Hz}$	10 Hz – 40 MHz $C_{FILTER} = 10 \mu F$ $C_{BP} = 0.1 \mu F$ $I_{LOAD} = 20 \text{ mA}$
Shutdown Voltage	V_{SD}	2.5	—	2.7	V	See Figure 1-5 (Note 2)
Input Voltage to Turn-Off Output	V_{OFF}	3.9	—	4.5	V	—
Input Voltage to Turn-On Output	V_{ON}	5.25	—	6	V	—

Note 1: Internal current limited. 2.0 ms maximum recovery time ($R_{LBUS} = 0\Omega$, $TX = 0$, $V_{LBUS} = V_{BB}$).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled; $V_{WK}(LBUS)$ is used to detect bus activities.

FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION



2.4 AC Specifications

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$.				
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Bus Interface – Constant Slope Time Parameters						
Slope Rising and Falling Edges	t_{SLOPE}	3.5	—	22.5	μs	$7.3V \leq V_{BB} \leq 18V$
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	6.0	μs	$t_{TRANSPD} = \max.$ ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	μs	$t_{RECPD} = \max.$ (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	t_{RECSYM}	-2.0	—	2.0	μs	$t_{RECSYM} = \max.$ ($t_{RECPDF} - t_{RECPDR}$) $R_{RXD} = 2.4 k\Omega$ to V_{CC} $C_{RXD} = 20 pF$
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	$t_{TRANSSYM}$	-2.0	—	2.0	μs	$t_{TRANSSYM} = \max.$ ($t_{TRANSPDF} - t_{TRANSPDR}$)
Bus Dominant Time-Out Time	$t_{TO(LIN)}$	—	25	—	mS	—
Duty Cycle 1 @ 20.0 kbps	—	0.396	—	—	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC}(MAX) = 0.744 \times V_{BB}$, $TH_{DOM}(MAX) = 0.581 \times V_{BB}$, $V_{BB} = 7.0V - 18V$; $t_{BIT} = 50 \mu s$. $D1 = t_{BUS_REC}(MIN)/2 \times t_{BIT}$
Duty Cycle 2 @ 20.0 kbps	—	—	—	0.581	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC}(MAX) = 0.284 \times V_{BB}$, $TH_{DOM}(MAX) = 0.422 \times V_{BB}$, $V_{BB} = 7.6V - 18V$; $t_{BIT} = 50 \mu s$. $D2 = t_{BUS_REC}(MAX)/2 \times t_{BIT}$
Duty Cycle 3 @ 10.4 kbps	—	0.417	—	—	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC}(MAX) = 0.778 \times V_{BB}$, $TH_{DOM}(MAX) = 0.616 \times V_{BB}$, $V_{BB} = 7.0V - 18V$; $t_{BIT} = 96 \mu s$. $D3 = t_{BUS_REC}(MIN)/2 \times t_{BIT}$
Duty Cycle 4 @ 10.4 kbps	—	—	—	0.590	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC}(MAX) = 0.251 \times V_{BB}$, $TH_{DOM}(MAX) = 0.389 \times V_{BB}$, $V_{BB} = 7.6V - 18V$; $t_{BIT} = 96 \mu s$. $D4 = t_{BUS_REC}(MAX)/2 \times t_{BIT}$

Note 1: Time depends on external capacitance and load. Test condition: $C_{REG} = 4.7 \mu F$, no resistor load.

2: Characterized, not 100% tested.

MCP2025

2.4 AC Specifications (Continued)

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$.				
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Voltage Regulator						
Bus Activity Debounce Time	tBDB	30	80	250	μs	—
Bus Activity to Voltage Regulator Enabled	tBACTIVE	35	—	200	μs	—
Voltage Regulator Enabled to Ready	tVEVR	300	—	1200	μs	Note 1
Chip Select to Ready Mode	tCSR	—	—	230	μs	—
Chip Select to Power-Down	tCSPD	—	—	300	μs	Note 2
Short Circuit to Shutdown	tSHUTDOWN	20	—	100	μs	—
RESET Timing						
VREG OK Detect to RESET Inactive	tRPU	—	—	60.0	μs	Note 2
VREG Not OK Detect to RESET Active	tRPD	—	—	60.0	μs	Note 2

Note 1: Time depends on external capacitance and load. Test condition: $C_{REG} = 4.7 \mu F$, no resistor load.

Note 2: Characterized, not 100% tested.

2.5 Thermal Specifications

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Specified Temperature Range	T_A	-40	—	+125	$^{\circ}C$	—
Maximum Junction Temperature	T_J	—	—	+150	$^{\circ}C$	—
Storage Temperature Range	T_A	-65	—	+150	$^{\circ}C$	—
Recovery Temperature	$\theta_{RECOVERY}$	—	+140	—	$^{\circ}C$	—
Shutdown Temperature	$\theta_{SHUTDOWN}$	—	+150	—	$^{\circ}C$	—
Short Circuit Recovery Time	tTHERM	—	1.5	5.0	ms	—
Thermal Package Resistances						
Thermal Resistance, 8-PDIP	θ_{JA}	—	89.3	—	$^{\circ}C/W$	—
Thermal Resistance, 8-SOIC	θ_{JA}	—	149.5	—	$^{\circ}C/W$	—
Thermal Resistance, 8L-DFN	θ_{JA}	—	48.0	—	$^{\circ}C/W$	—

Note 1: The maximum power dissipation is a function of T_{JMAX} , θ_{JA} and ambient temperature, T_A . The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A) \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above $150^{\circ}C$ and the MCP2025 will go into thermal shutdown.

2.6 Typical Performance Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{BB} = 6.0V$ to $18.0V$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$.

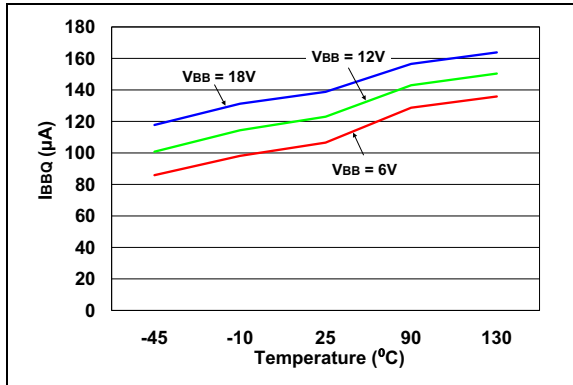


FIGURE 2-2: Typical $IBBQ$ vs. Temperature – 5.0V.

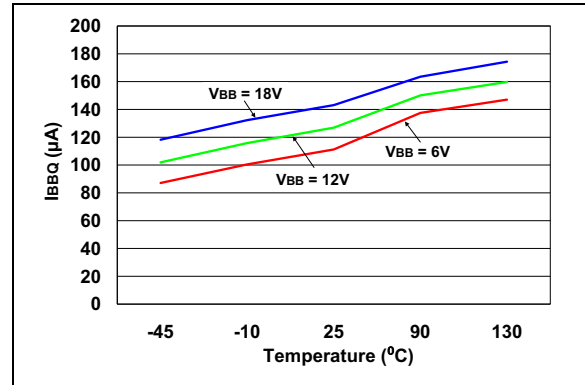


FIGURE 2-5: Typical $IBBQ$ vs. Temperature – 3.3V.

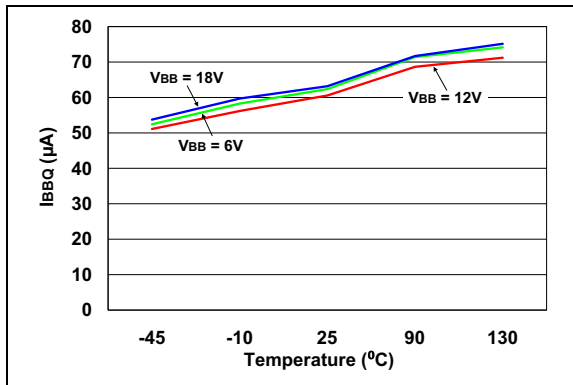


FIGURE 2-3: $IBBQ$ Transmitter-Off vs. Temperature – 5.0V.

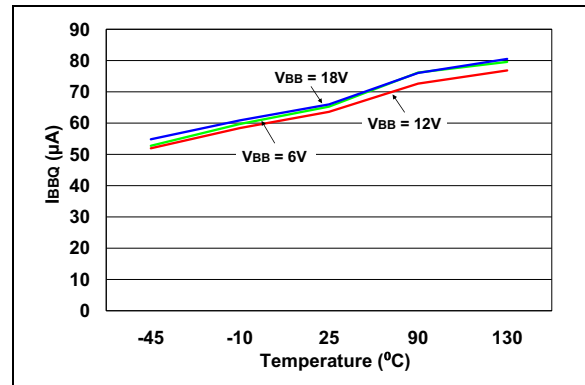


FIGURE 2-6: $IBBQ$ Transmitter-Off vs. Temperature – 3.3V.

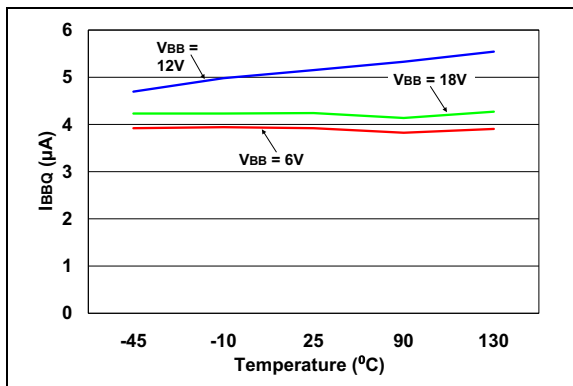


FIGURE 2-4: $IBBQ$ Power-Down vs. Temperature – 5.0V.

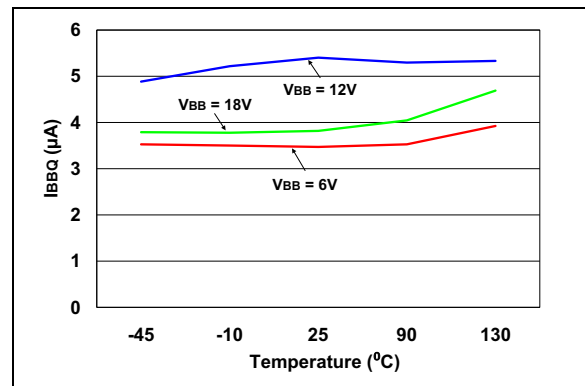


FIGURE 2-7: $IBBQ$ Power-Down vs. Temperature – 3.3V.

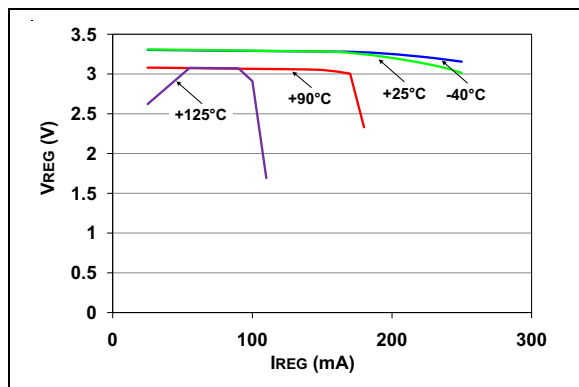


FIGURE 2-8: 5.0V V_{REG} vs. I_{REG} at $V_{BB} = 12V$.

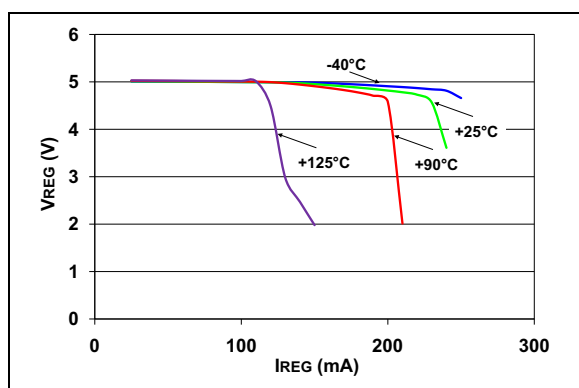


FIGURE 2-9: 3.3V V_{REG} vs. I_{REG} at $V_{BB} = 12V$.

2.7 Timing Diagrams and Specifications

FIGURE 2-10: BUS TIMING DIAGRAM

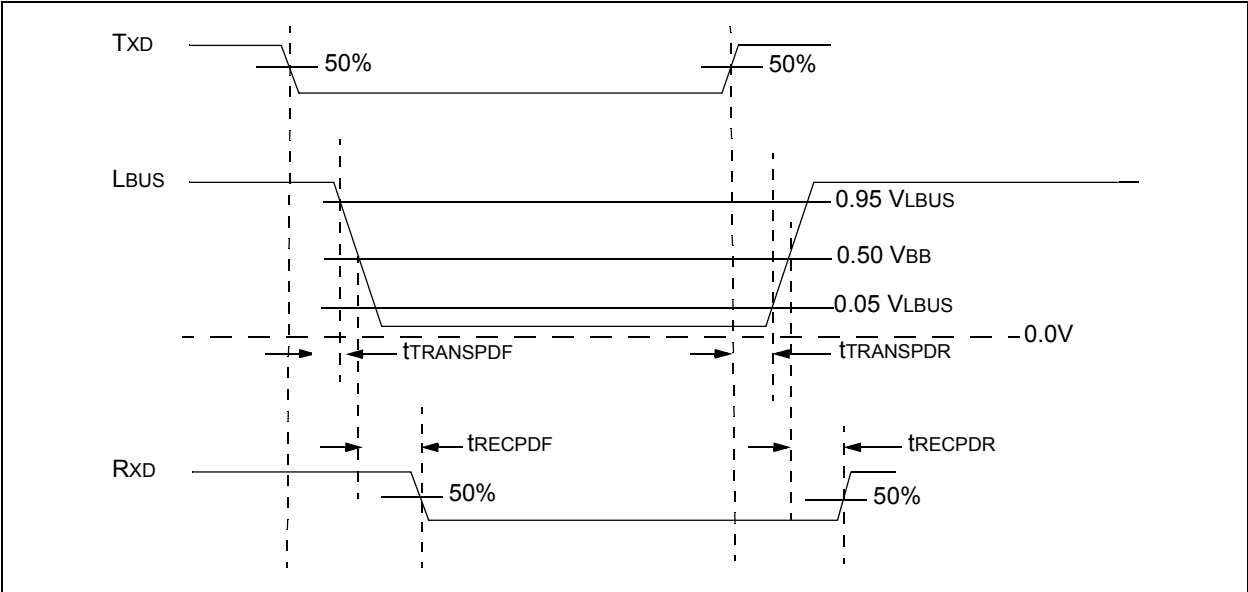


FIGURE 2-11: REGULATOR BUS WAKE TIMING DIAGRAM

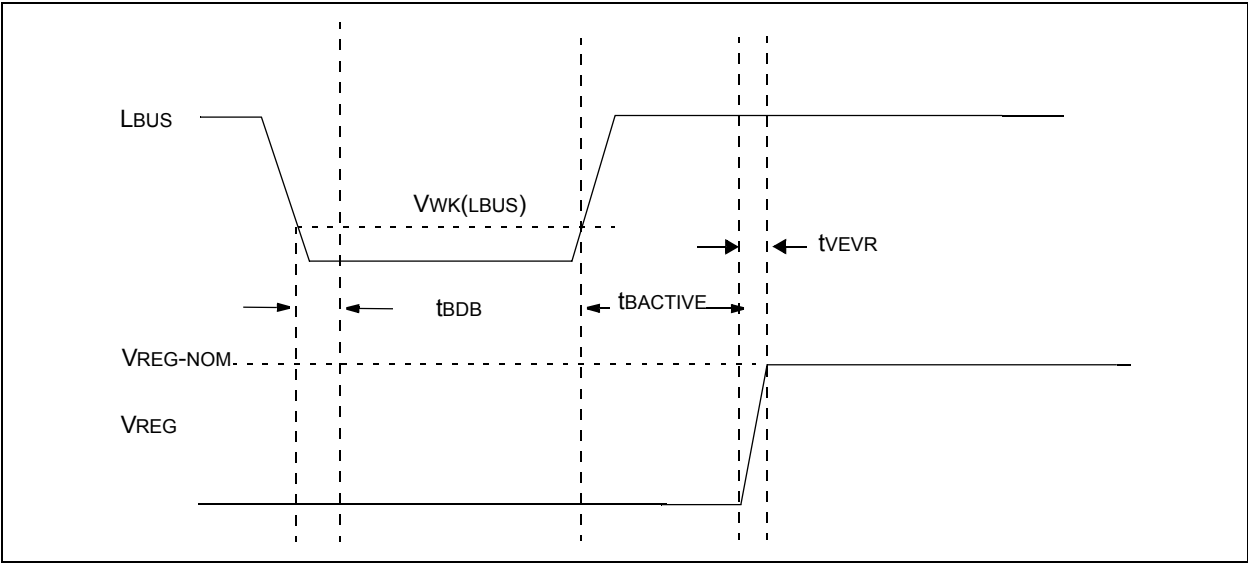
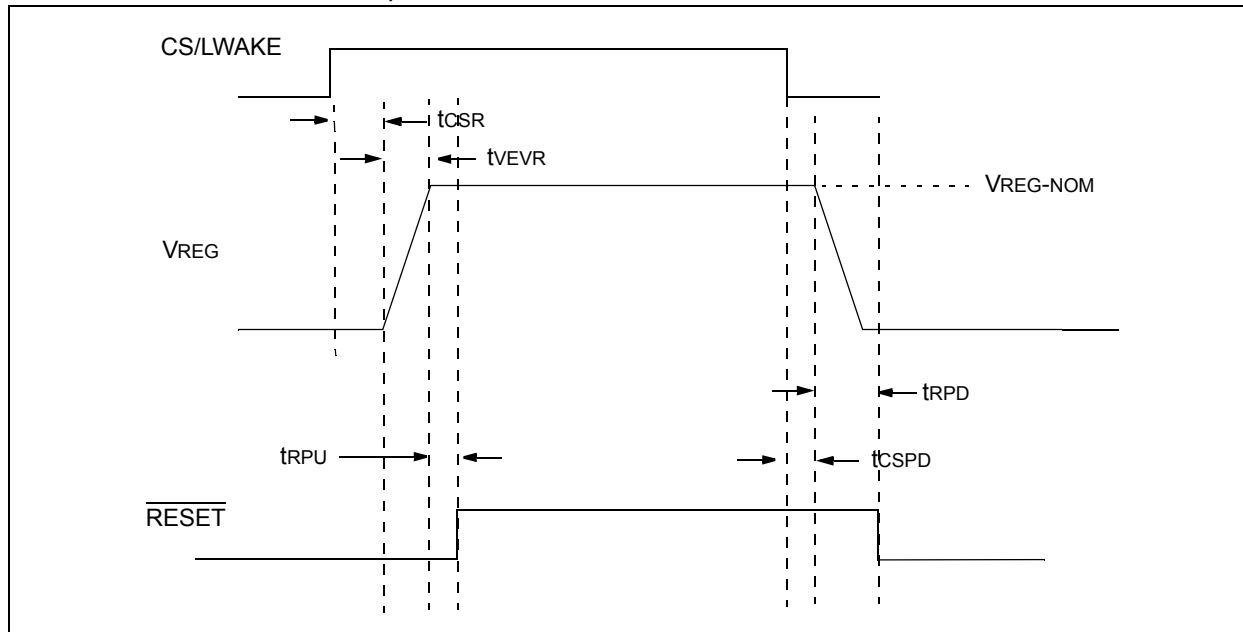


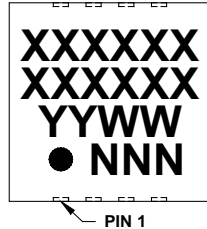
FIGURE 2-12: CS/LWAKE, REGULATOR AND RESET TIMING DIAGRAM



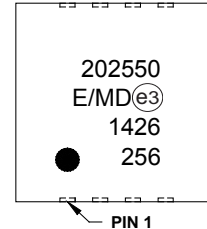
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

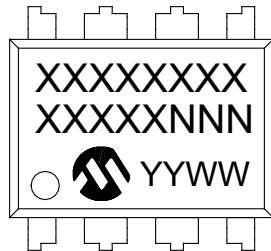
8-Lead DFN (4x4x0.9 mm)



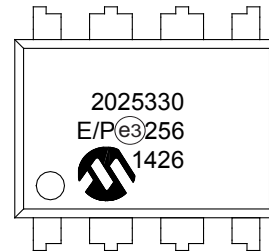
Example



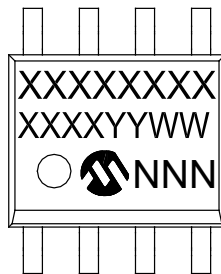
8-Lead PDIP (300 mil)



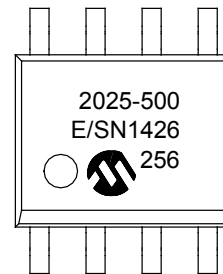
Example



8-Lead SOIC (3.90 mm)



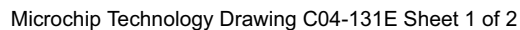
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

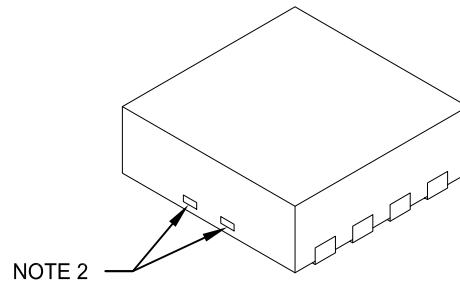
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		0.80 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Length	D		4.00 BSC		
Exposed Pad Width	E2		2.60	2.70	2.80
Overall Width	E		4.00 BSC		
Exposed Pad Length	D2		3.40	3.50	3.60
Contact Width	b		0.25	0.30	0.35
Contact Length	L		0.30	0.40	0.50
Contact-to-Exposed Pad	K		0.20	-	-

Notes:

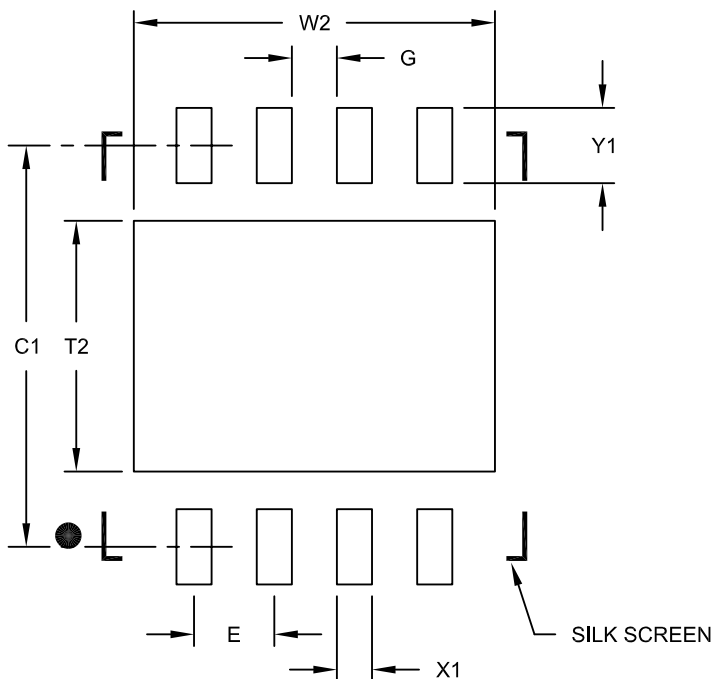
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

MCP2025

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

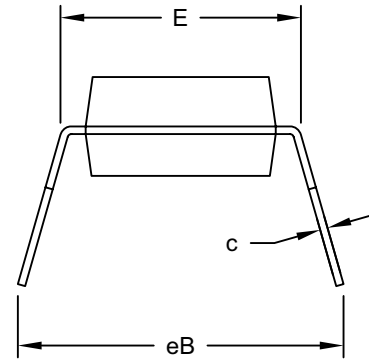
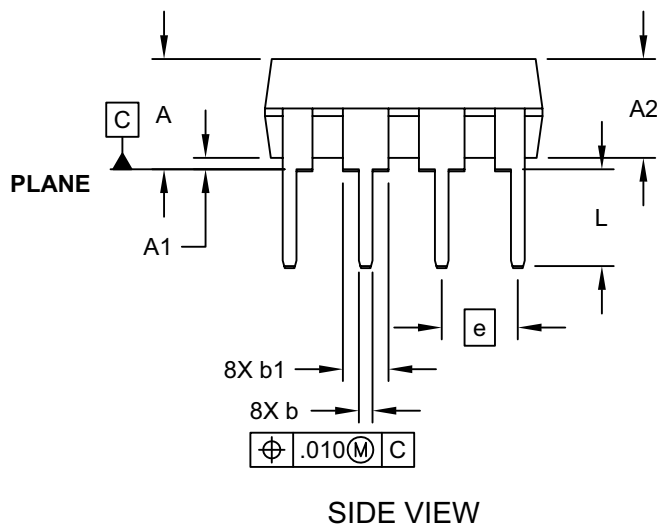
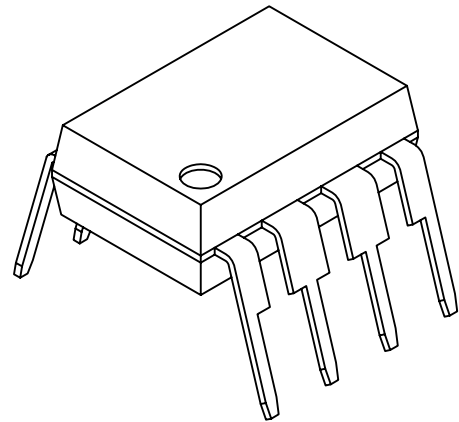
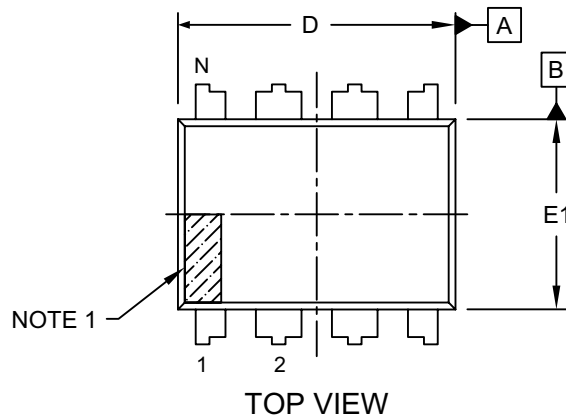
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

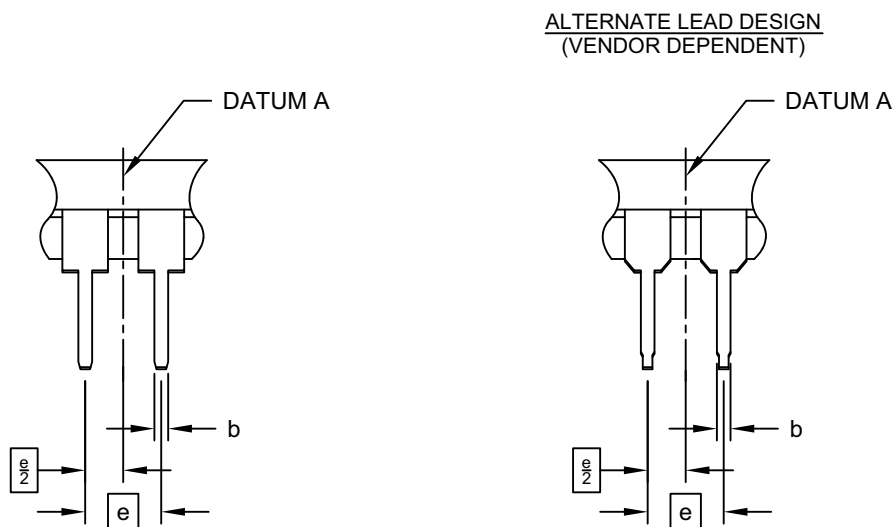
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing	§ eB	-	-	.430

Notes:

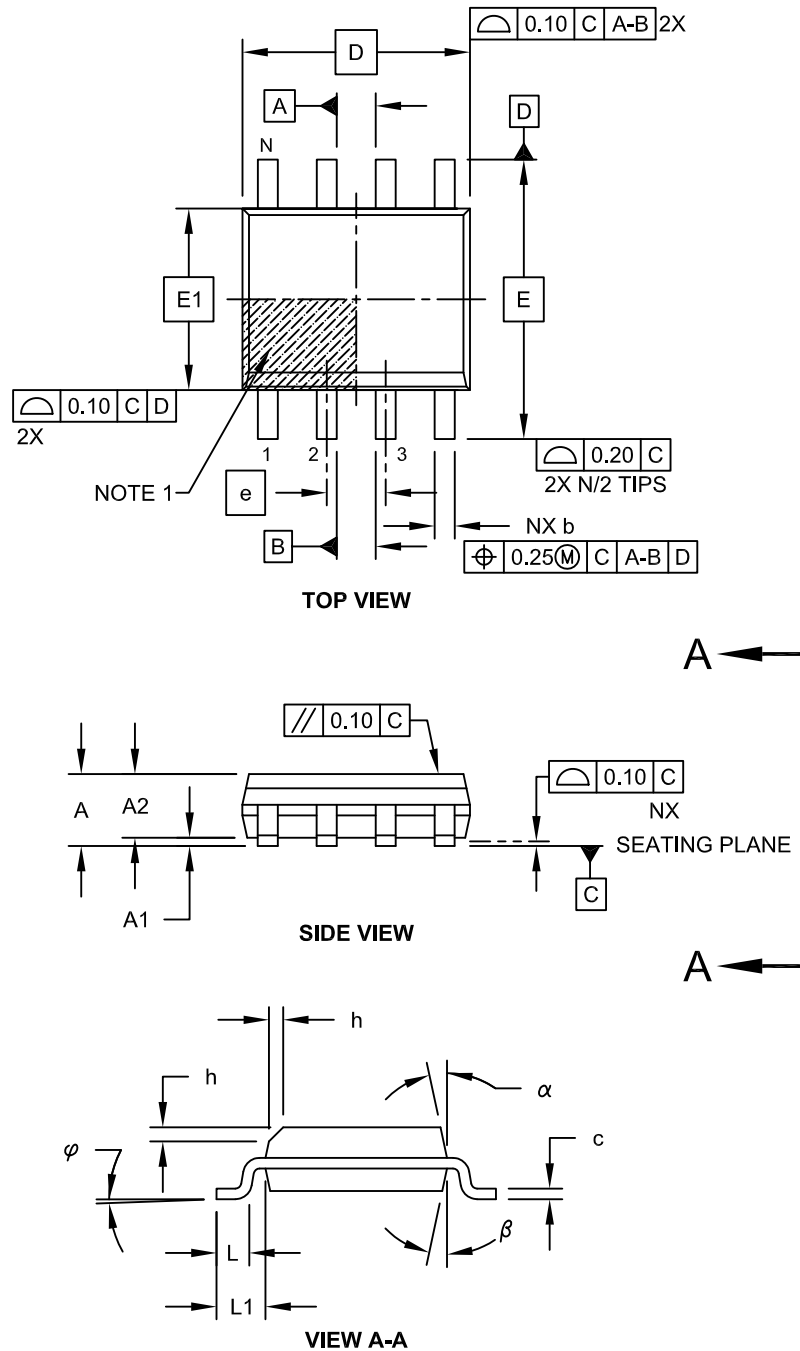
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

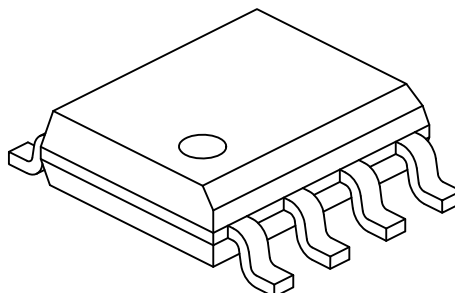


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

MCP2025

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A		-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		4.90 BSC		
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1		1.04 REF		
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.17	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

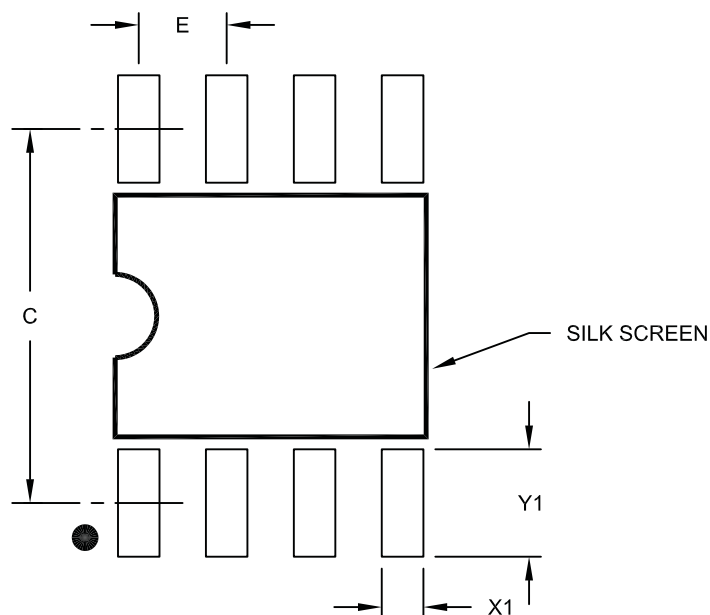
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (August 2014)

The following is the list of modifications:

1. Clarified CREG selection.
2. Updated **Section 1.6 “Typical Applications”** with values used during ESD tests.
3. Minor typographical corrections.

Revision A (June 2012)

- Original Release of this Document.

MCP2025

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-X</u>	<u>X</u>	<u>/XX</u>
Device	Voltage	Temperature Range	Package
Device:	MCP2025: LIN Transceiver with Voltage Regulator MCP2025T: LIN Transceiver with Voltage Regulator (Tape and Reel)		
Voltage:	330 = 3.3V 500 = 5.0V		
Temperature Range:	E = -40°C to +125°C		
Package:	MD = 8LD Plastic Dual Flat, No Lead – 4x4x0.8 mm Body P = 8LD/14LD Plastic Dual In-Line – 300 mil Body SN = 8LD Plastic Small Outline – Narrow, 3.90 mm Body		

Examples:

- a) MCP2025-330E/MD: 3.3V, 8-lead DFN package
- b) MCP2025-500E/MD: 5.0V, 8-lead DFN package
- c) MCP2025T-330E/MD: 3.3V, 8-lead DFN package, Tape and Reel
- d) MCP2025T-500E/MD: 5.0V, 8-lead DFN package, Tape and Reel
- e) MCP2025-330E/P: 3.3V, 8-lead PDIP package
- f) MCP2025-500E/P: 5.0V, 8-lead PDIP package
- g) MCP2025-330E/SN: 3.3V, 8-lead SOIC package
- h) MCP2025-500E/SN: 5.0V, 8-lead SOIC package
- i) MCP2025T-330E/SN: 3.3V, 8-lead SOIC package, Tape and Reel
- j) MCP2025T-500E/SN: 5.0V, 8-lead SOIC package, Tape and Reel

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ISBN: 978-1-63276-499-7

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