MC9S08PA60 Reference Manual

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Chapter 1
Device Overview

1.1 Introduction

These devices are members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 central processor unit and are available with a variety of modules, memory sizes and types, and package types. The following table summarizes the peripheral availability per package type for the devices available.

Table 1-1. Memory and package availability

Feature	MC9S08PA60	MC9S08PA32
Flash size (bytes)	60,864	32,768
EEPROM size (bytes)	256	256
RAM size (bytes)	4,096	4,096
LQFP-64	Yes	Yes
QFP-64	Yes	Yes
LQFP-48	Yes	Yes
LQFP-44	Yes	Yes
LQFP-32	Yes	Yes

Table 1-2. Feature availability

Pin number	64-pin	48-pin	44-pin	32-pin
Bus frequency (MHz)	20	20	20	20
IRQ	Yes			
WDOG	Yes			
DBG	Yes			
IPC	Yes			
CRC	Yes			
ICS	Yes			

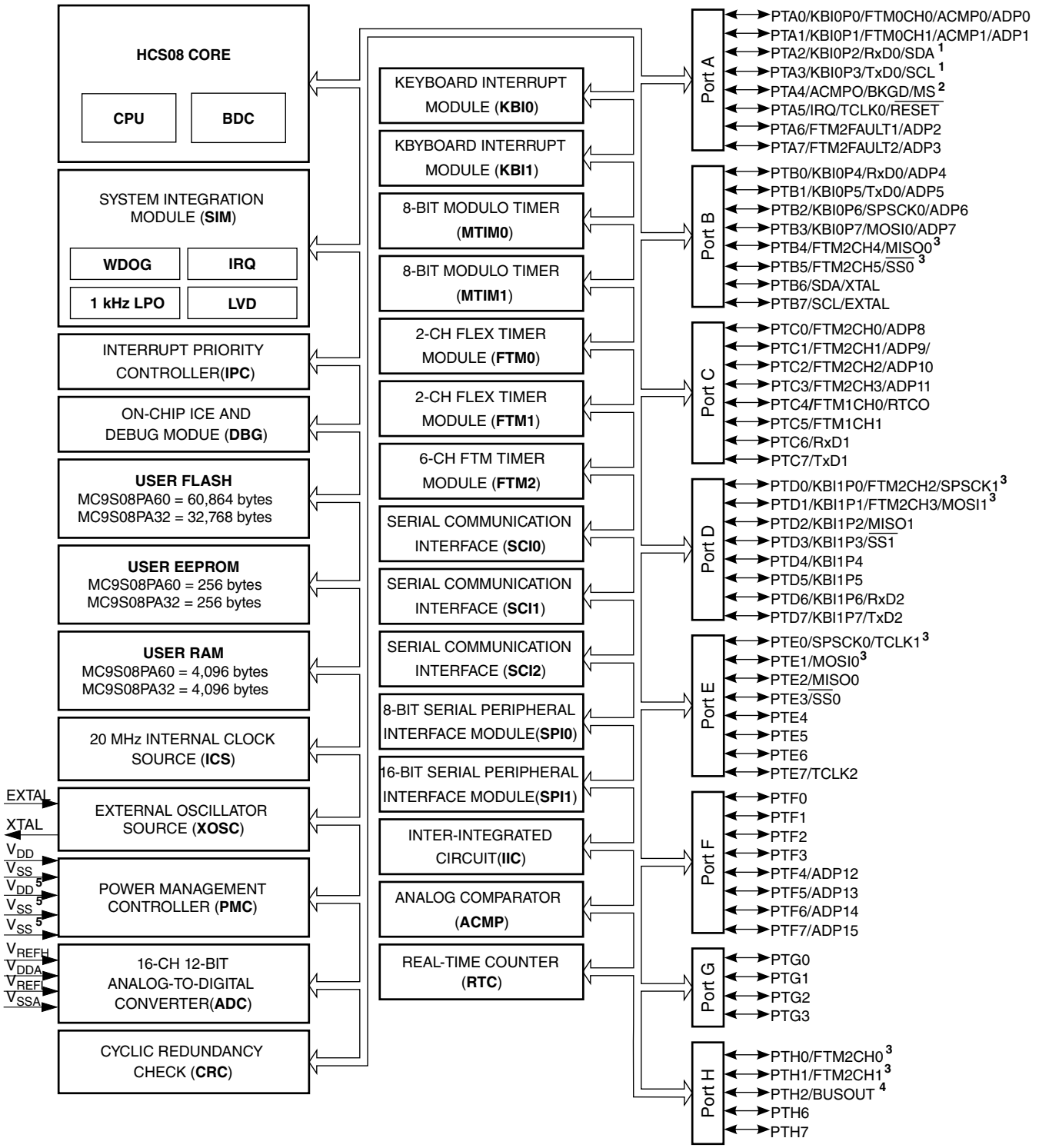
Table continues on the next page...

Table 1-2. Feature availability (continued)

Pin number	64-pin	48-pin	44-pin	32-pin
XOSC	Yes			
RTC	Yes			
FTM0 channels	2-ch			
FTM1 channels	2-ch			
FTM2 channels	6-ch			
MTIM0	Yes			
MTIM1	Yes			
SPI0 (8-bit)	Yes			
SPI1 (16-bit)	Yes			
IIC	Yes			
ACMP	Yes			
SCI0	Yes			
SCI1	Yes			
SCI2	Yes			No
ADC channels	16	12	12	12
KBI pins	16	16	12	12
GPIO	57	41	37	28

1.2 MCU block diagram

The block diagram below shows the structure of the MCUs.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 1-1. MCU block diagram

1.3 System clock distribution

These series contain three on-chip clock sources:

- Internal clock source (ICS) module — The main clock source generator providing bus clock and other reference clocks to peripherals
- External oscillator (XOSC) module — The external oscillator providing reference clock to internal clock source (ICS), the real-time clock counter clock module (RTC) and other MCU sub-systems.
- Low-power oscillator (LPO) module — The on-chip low-power oscillator providing 1 kHz reference clock to RTC and watchdog (WDOG).

NOTE

For this device, the system clock is the bus clock.

The following figure shows a simplified clock connection diagram.

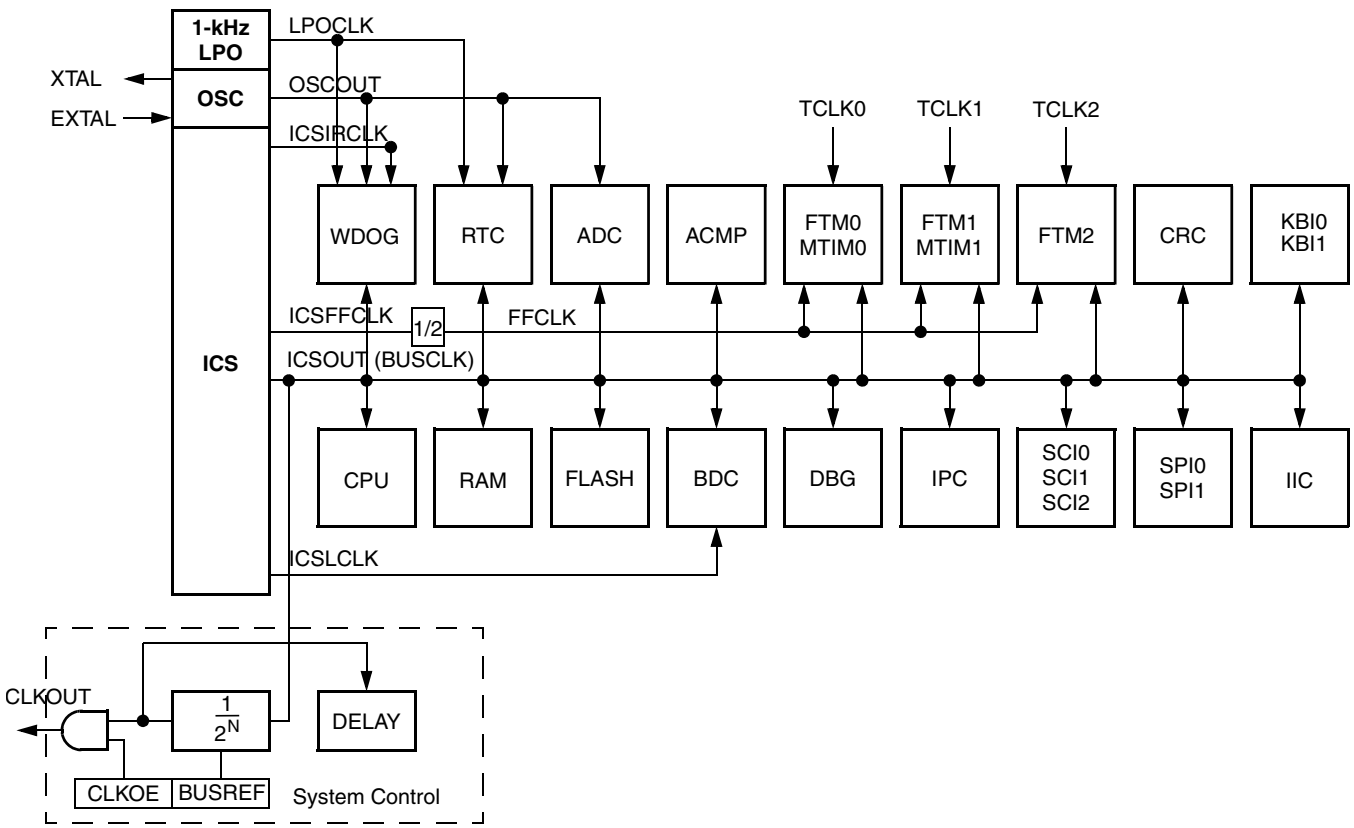


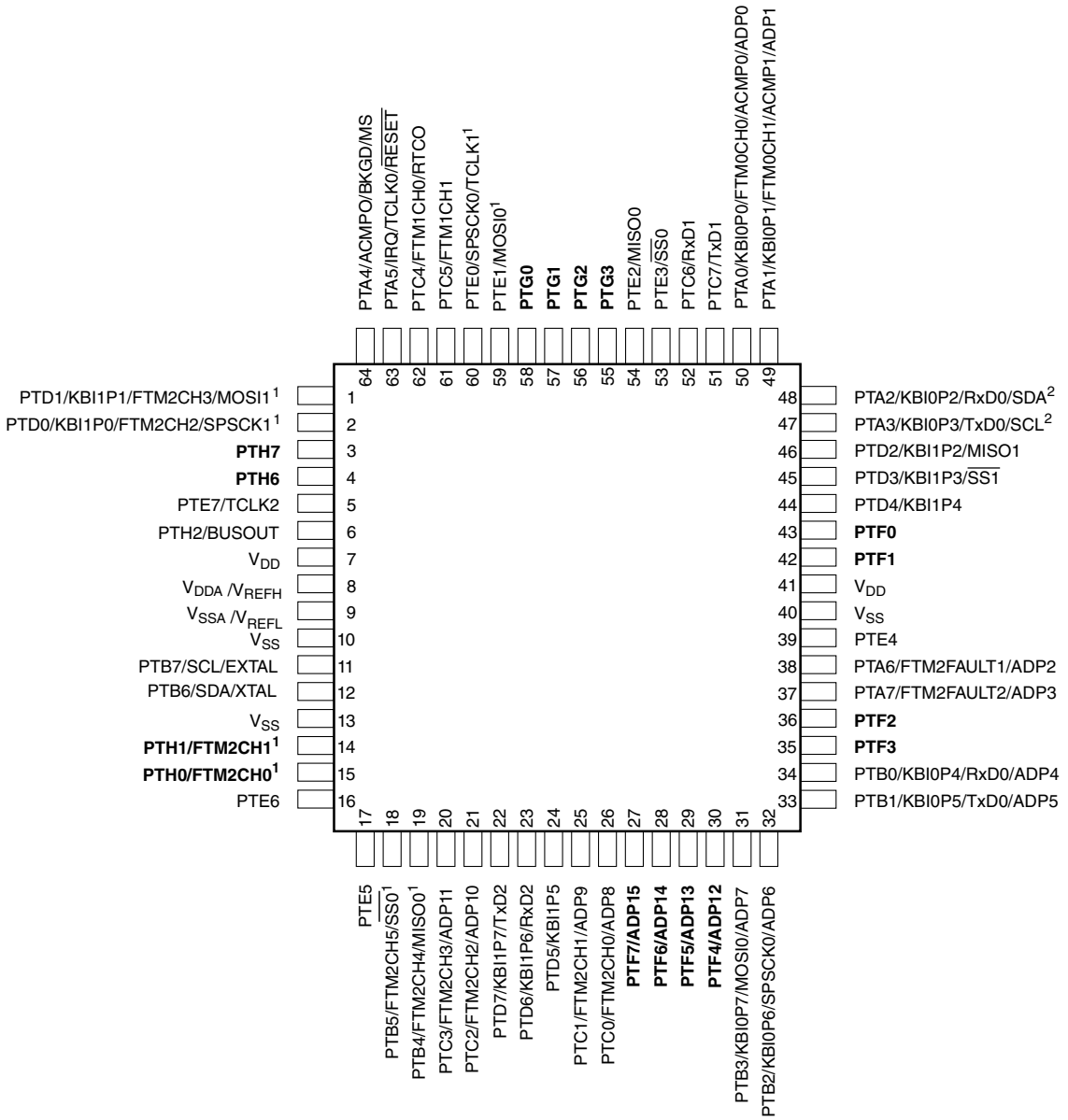
Figure 1-2. System clock distribution diagram

The clock system supplies:

- ICSOUT(BUSCLK) — This up to 20 MHz clock source is used as the bus clock that is the reference to CPU and all peripherals. Control bits in the ICS control registers determine which of the clock sources is connected:
  - Internal reference clock
  - External reference clock
  - Frequency-locked loop (FLL) output
- ICSLCLK — This clock source is derived from the digitally controlled oscillator (DCO) of the ICS when the ICS is configured to run off of the internal or external reference clock. Development tools can select this internal self-clocked source (8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICSIRCLK — This is the internal reference clock and can be selected as the clock source to the WDOG module.
- ICSFFCLK — This is the reference clock of the FLL. Its frequency is determined by the setting of the ICS. ICSFFCLK is also used to generate the fixed frequency clock (FFCLK).
- FFCLK — This is the fixed frequency clock which can be selected as the clock source to the FTM and MTIM modules. It is generated by the ICSFFCLK after being synchronized to the bus clock, so the frequency of FFCLK is half of ICSFFCLK.
- LPOCLK — This clock is generated from an internal low power oscillator (≈1 kHz) that is completely independent of the ICS module. The LPOCLK can be selected as the clock source to the RTC or WDOG modules.
- OSCOUT — This is the direct output of the external oscillator module and can be selected as the clock source for RTC, WDOG and ADC.
- TCLK0 — This is an optional external clock source for the FTM0 and MTIM0 modules. The TCLK0 must be limited to 1/4th frequency of the bus clock for synchronization.
- TCLK1 — This is an optional external clock source for the FTM1 and MTIM1 modules. The TCLK1 must be limited to 1/4th frequency of the bus clock for synchronization.
- TCLK2 — This is an optional external clock source for the FTM2 module. The TCLK2 must be limited to 1/4th frequency of the bus clock for synchronization.

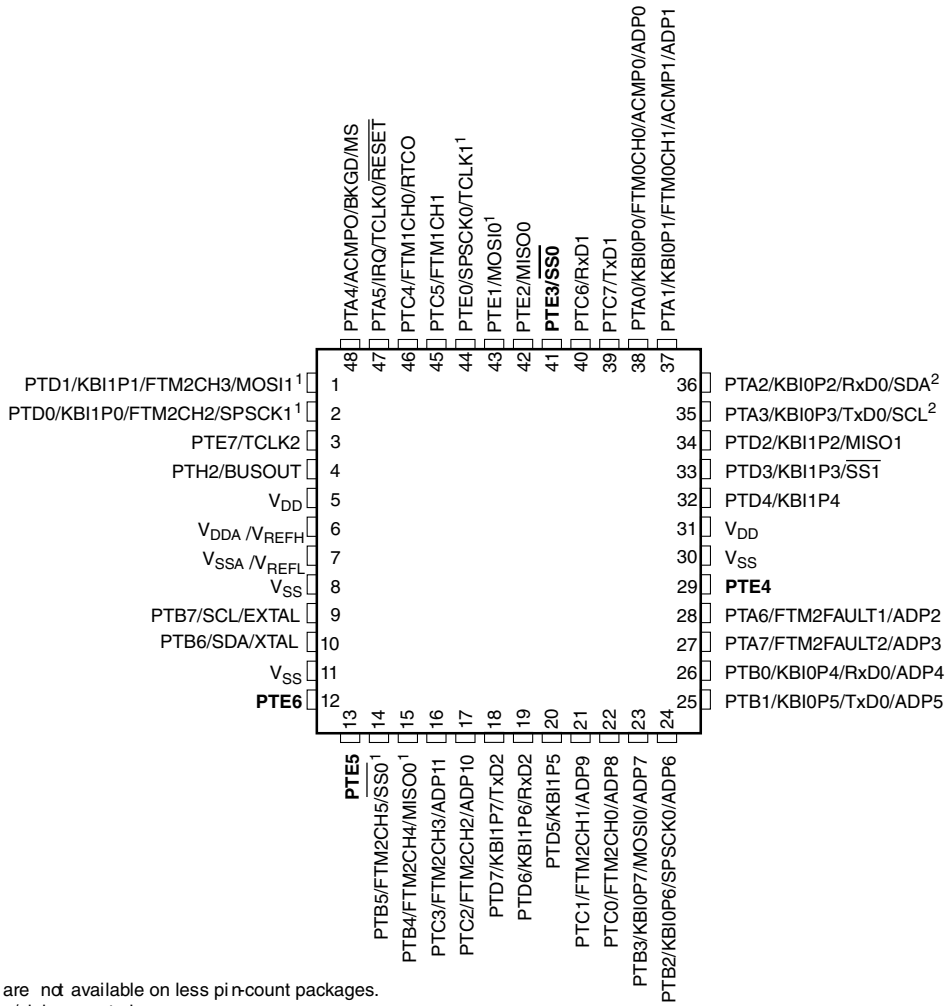
Chapter 2
Pins and connections

2.1 Device pin assignment



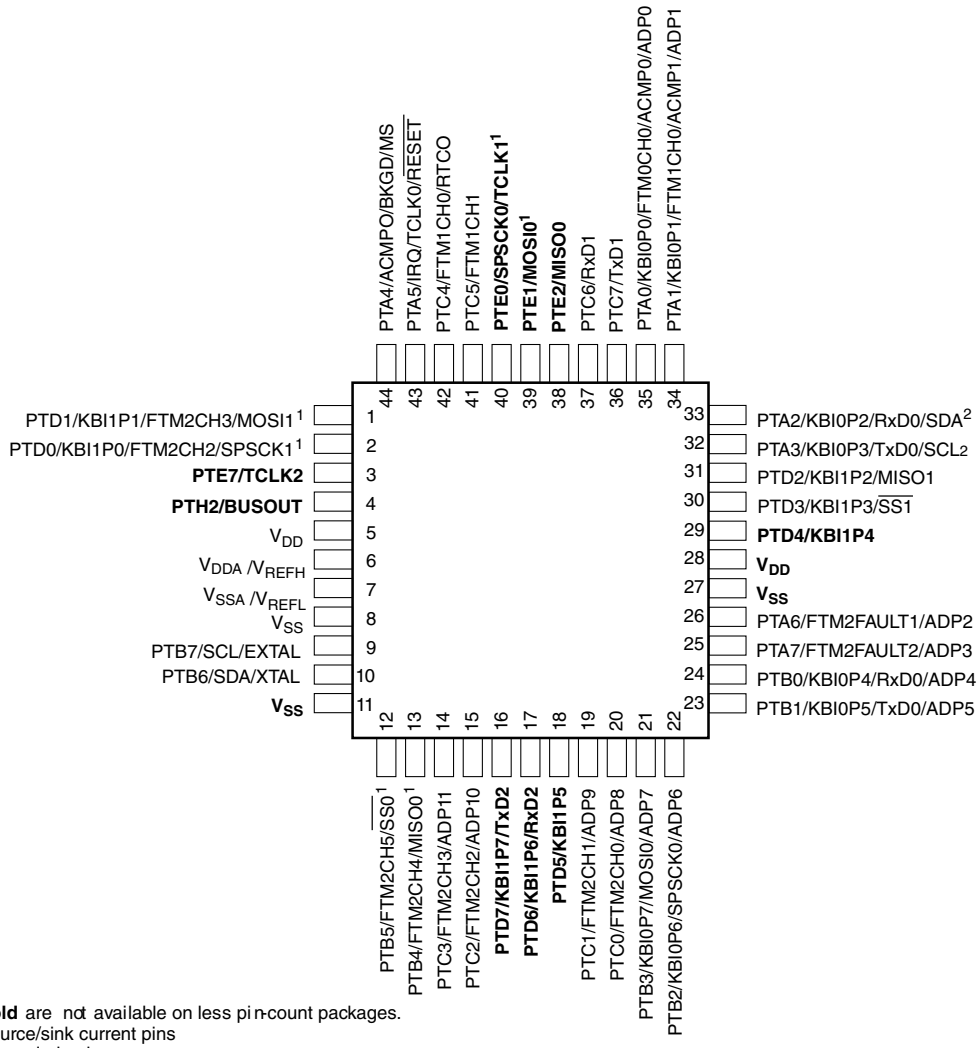
Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 2-1. MC9S08PA60 64-pin QFP and LQFP package



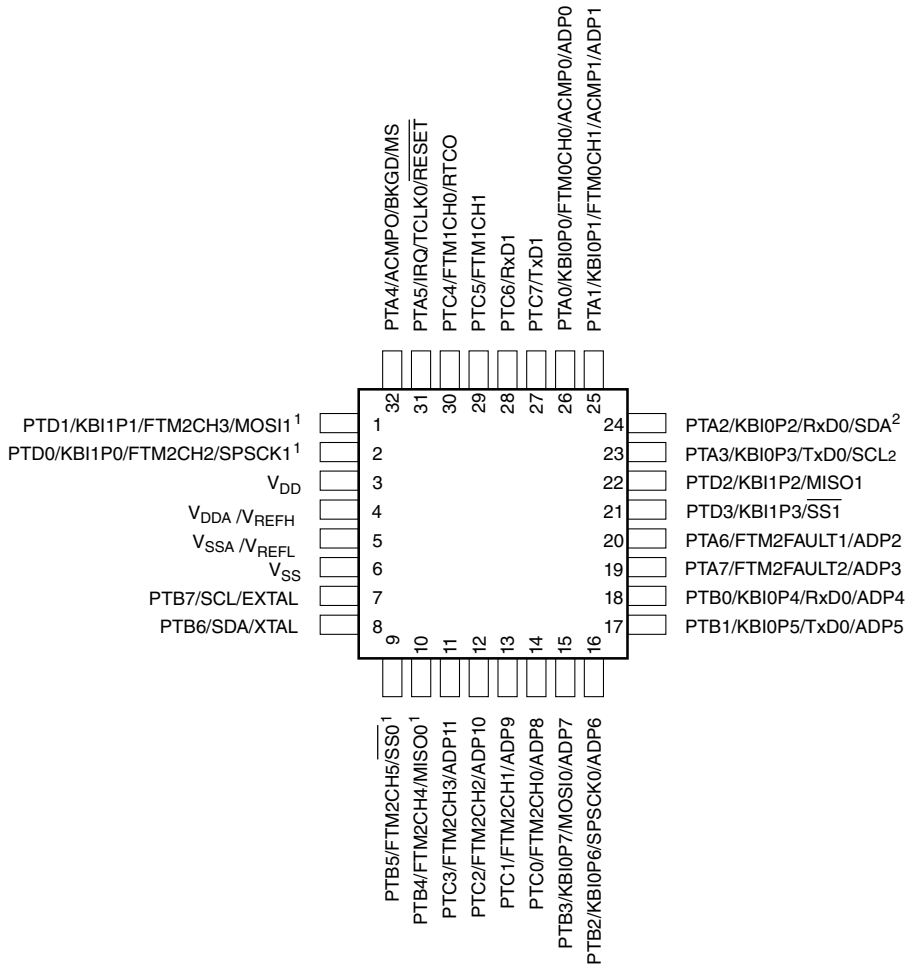
Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 2-2. MC9S08PA60 48-pin LQFP package



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 2-3. MC9S08PA60 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 2-4. MC9S08PA60 32-pin LQFP package

2.2 Pin functions

2.2.1 Power (V_{DD}, V_{SS})

V_{DD} and V_{SS} are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides a regulated lower-voltage source to the CPU and to the MCU's other internal circuitry.

Typically, application systems have two separate capacitors across the power pins. In this case, there should be a bulk electrolytic capacitor, such as a 10 µF tantalum capacitor, that provides bulk charge storage for the overall system and a 0.1 µF ceramic bypass capacitor located as near to the paired V_{DD} and V_{SS} power pins as practical to suppress high-frequency noise.

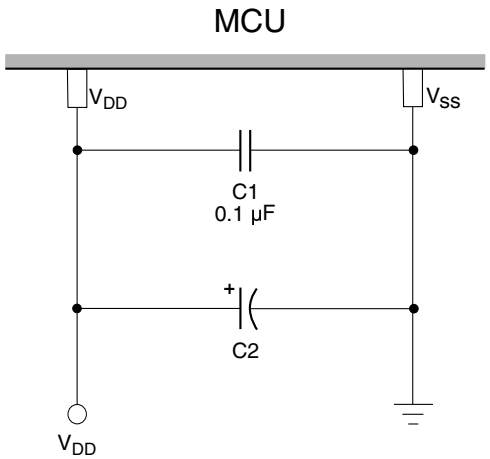


Figure 2-5. Power supply bypassing

2.2.2 Analog power supply and reference pins (V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Connect the V_{DDA} pin to the same voltage potential as V_{DD}, and the V_{SSA} pin to the same voltage potential as V_{SS}.

De-coupling of these pins should be as per the digital supply. A 0.1 µF ceramic bypass capacitor should be located as near to the MCU power pins as practical to suppress high-frequency noise.

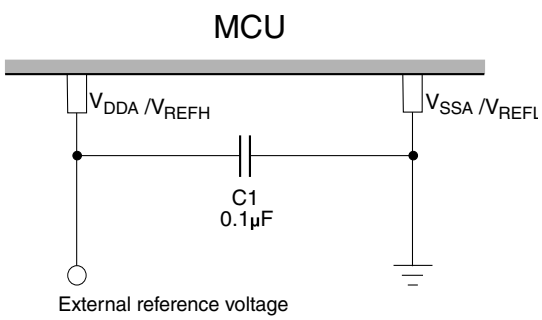


Figure 2-6. Analog power supply bypassing

V_{REFH} is the high reference supply for the ADC, and is internally connected to V_{DDA}. V_{REFL} is the low reference supply for the ADC, and is internally connected to V_{SSA}.

2.2.3 Oscillator (XTAL, EXTAL)

The XTAL and EXTAL pins are used to provide the connections for the on-chip oscillator. The oscillator (XOSC) in this MCU is a Pierce oscillator that can accommodate a crystal or ceramic resonator. Optionally, an external clock source can be connected to the EXTAL input pin. The oscillator can be configured to run in stop3 mode.

Refer to the following figure, R_S (when used) and R_F must be low-inductance resistors such as carbon composition resistors. Wire-wound resistors, and some metal film resistors, have too much inductance. C1 and C2 normally must be high-quality ceramic capacitors that are specifically designed for high-frequency applications.

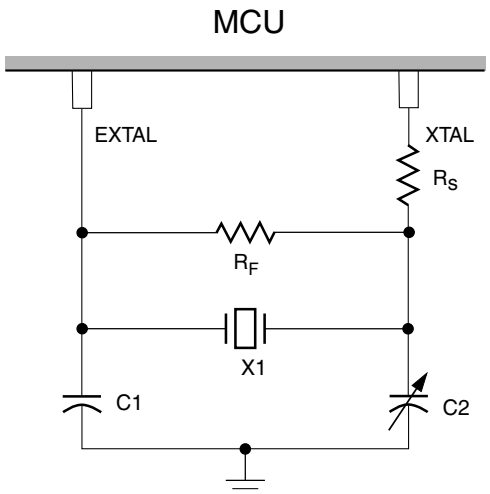


Figure 2-7. Typical crystal or resonator circuit

R_F is used to provide a bias path to keep the EXTAL input in its linear range during crystal startup; its value is not generally critical. Typical systems use 1 M to 10 M. Higher values are sensitive to humidity and lower values reduce gain and (in extreme cases) could prevent startup.

C1 and C2 are typically in the 5 pF to 25 pF range and are chosen to match the requirements of a specific crystal or resonator. Take into account printed circuit board (PCB) capacitance and MCU pin capacitance when selecting C1 and C2. The crystal manufacturer typically specifies a load capacitance, which is the series combination of C1 and C2 (which are usually the same size). As a first-order approximation, use 10 pF as an estimate of combined pin and PCB capacitance for each oscillator pin (EXTAL and XTAL).

2.2.4 External reset pin ($\overline{\text{RESET}}$)

A low on the $\overline{\text{RESET}}$ pin forces the MCU to an known startup state. $\overline{\text{RESET}}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor.

2.2.5 Background/mode select (BKGD/MS)

During a power-on-reset (POR) or background debug force reset, the PTA4/ACMPO/ BKGD/MS pin functions as a mode select pin. Immediately after internal reset rises the pin functions as the background pin and can be used for background debug communication. While the pin functions as a background/mode selection pin, it includes an internal pullup device and a standard output driver.

The background debug communication function is enabled when SOPT1[BKGDPE] bit is set. SOPT1[BKGDPE] is set following any reset of the MCU and must be cleared to use the PTA4/ACMPO/BKGD/MS pin's alternative pin functions.

If this pin is floating, the MCU will enter normal operating mode at the rising edge of reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during the POR or immediately after issuing a background debug force reset, which will force the MCU into active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU's BDC clock per bit time. The target MCU's BDC clock can run as fast as the bus clock, so there should never be any significant capacitance connected to the BKGD/MS pin that interferes with background serial communications. When the pin performs output only PTA4, it can drive only capacitance-limited MOSFET. Driving a bipolar transistor directly by PTA4 is prohibited because this can cause mode entry fault and BKGD errors.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise time. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall time on the BKGD pin.

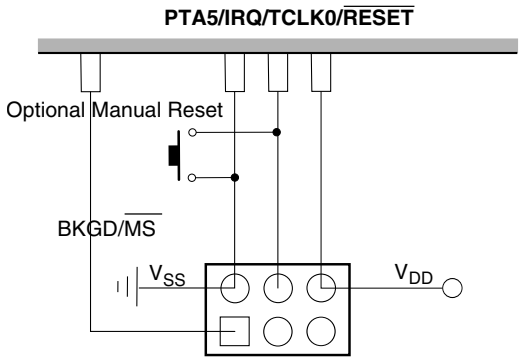


Figure 2-8. Typical debug circuit

2.2.6 Port A input/output (I/O) pins (PTA–PTA0)

PTA–PTA0 except PTA4 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode except PTA4. The pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode except when PTA2 and PTA3 are used as SDA and SCL function.

PTA3 and PTA2 provide true open drain when operated as output.

2.2.7 Port B input/output (I/O) pins (PTB7–PTB0)

PTB7–PTB0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.8 Port C input/output (I/O) pins (PTC–PTC0)

PTC–PTC0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, and the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.9 Port D input/output (I/O) pins (PTD7–PTD0)

PTD7–PTD0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.10 Port E input/Output (I/O) pins (PTE7-PTE0)

PTE7-PTE0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.11 Port F input/output (I/O) pins (PTF7–PTF0)

PTF7–PTF0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.12 Port G input/output (I/O) pins (PTG3–PTG0)

PTG3–PTG0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pull-up devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.13 Port H input/output (I/O) pins (PTH7–PTH6, PTH2–PTH0)

PTH7–PTH6, PTH2–PTH0 are general-purpose, bidirectional I/O port pins. These port pins also have selectable pullup devices when configured for input mode, the pullup devices are selectable on an individual port bit basis. The pulling devices are disengaged when configured for output mode.

2.2.14 True open drain pins (PTA3–PTA2)

PTA3 and PTA2 operate in true open drain mode.

NOTE

When configuring IIC to use SDA(PTA2) and SCL(PTA3) pins, if an application uses internal pullups instead of external pullups, the internal pullups remain present setting when the pins are configured as outputs, but they are automatically disabled to save power when the output values are low.

2.2.15 High current drive pins (PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, PTH1)

When high current function is enabled, PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can drive output current. Each high current drive pin can drive higher sink/source current than the other normal pins, please refer to data sheet for the drive capacity.

2.3 Peripheral pinouts

These MCUs support up to 57 general-purpose I/O pins, which are shared with on-chip peripheral functions (FTM, ACMP, ADC, SCI, SPI, IIC, KBI, etc.). These 57 general-purpose I/O pins include one output-only pin (PTA4).

When a port pin is configured as general-purpose input, or when a peripheral uses the port pin as an input, the software can enable a pullup device.

When a high current drive port pin is configured as general-purpose output or when a peripheral uses the port pin as an output, software can select alternative drive strengths.

For information about controlling these pins as general-purpose I/O pins, see the Parallel input/output. For information about how and when on-chip peripheral systems use these pins, see the appropriate module chapter.

Immediately after reset, all pins are configured as high-impedance general-purpose IO with internal pullup devices disabled.

Table 2-1. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	1	PTD1[1]	KBI1P1	FTM2CH3	MOSI1	—
2	2	2	2	PTD0[1]	KBI1P0	FTM2CH2	SPSCK1	—
3	—	—	—	PTH7	—	—	—	—
4	—	—	—	PTH6	—	—	—	—
5	3	3	—	PTE7	—	TCLK2	—	—
6	4	4	—	PTH2	—	BUSOUT	—	—
7	5	5	3	—	—	—	—	V_{DD}
8	6	6	4	—	—	—	V_{DDA}	V_{REFH}
9	7	7	5	—	—	—	V_{SSA}	V_{REFL}
10	8	8	6	—	—	—	—	V_{SS}
11	9	9	7	PTB7	—	SCL	—	EXTAL
12	10	10	8	PTB6	—	SDA	—	XTAL
13	11	11	—	—	—	—	—	V_{SS}
14	—	—	—	PTH1[1]	—	FTM2CH1	—	—
15	—	—	—	PTH0[1]	—	FTM2CH0	—	—
16	12	—	—	PTE6	—	—	—	—
17	13	—	—	PTE5	—	—	—	—
18	14	12	9	PTB5[1]	FTM2CH5	$\overline{SS0}$	—	—
19	15	13	10	PTB4[1]	FTM2CH4	MISO0	—	—
20	16	14	11	PTC3	FTM2CH3	—	ADP11	—
21	17	15	12	PTC2	FTM2CH2	—	ADP10	—
22	18	16	—	PTD7	KBI1P7	TXD2	—	—
23	19	17	—	PTD6	KBI1P6	RXD2	—	—
24	20	18	—	PTD5	KBI1P5	—	—	—
25	21	19	13	PTC1	—	FTM2CH1	ADP9	—
26	22	20	14	PTC0	—	FTM2CH0	ADP8	—
27	—	—	—	PTF7	—	—	ADP15	—
28	—	—	—	PTF6	—	—	ADP14	—
29	—	—	—	PTF5	—	—	ADP13	—
30	—	—	—	PTF4	—	—	ADP12	—
31	23	21	15	PTB3	KBI0P7	MOSI0	ADP7	—
32	24	22	16	PTB2	KBI0P6	SPSCK0	ADP6	—
33	25	23	17	PTB1	KBI0P5	TXD0	ADP5	—
34	26	24	18	PTB0	KBI0P4	RXD0	ADP4	—
35	—	—	—	PTF3	—	—	—	—
36	—	—	—	PTF2	—	—	—	—
37	27	25	19	PTA7	FTM2FAULT2	—	ADP3	—

Table continues on the next page...

Table 2-1. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
38	28	26	20	PTA6	FTM2FAULT1	—	ADP2	—
39	29	—	—	PTE4	—	—	—	—
40	30	27	—	—	—	—	—	V_{SS}
41	31	28	—	—	—	—	—	V_{DD}
42	—	—	—	PTF1	—	—	—	—
43	—	—	—	PTF0	—	—	—	—
44	32	29	—	PTD4	KBI1P4	—	—	—
45	33	30	21	PTD3	KBI1P3	$\overline{SS1}$	—	—
46	34	31	22	PTD2	KBI1P2	MISO1	—	—
47	35	32	23	PTA3[2]	KBI0P3	TXD0	SCL	—
48	36	33	24	PTA2[2]	KBI0P2	RXD0	SDA	—
49	37	34	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	35	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	36	27	PTC7	—	TxD1	—	—
52	40	37	28	PTC6	—	RxD1	—	—
53	41	—	—	PTE3	—	$\overline{SS0}$	—	—
54	42	38	—	PTE2	—	MISO0	—	—
55	—	—	—	PTG3	—	—	—	—
56	—	—	—	PTG2	—	—	—	—
57	—	—	—	PTG1	—	—	—	—
58	—	—	—	PTG0	—	—	—	—
59	43	39	—	PTE1[1]	—	MOSI0	—	—
60	44	40	—	PTE0[1]	—	SPSCK0	TCLK1	—
61	45	41	29	PTC5	—	FTM1CH1	—	—
62	46	42	30	PTC4	—	FTM1CH0	RTCO	—
63	47	43	31	PTA5	IRQ	TCLK0	—	$\overline{RESET}$
64	48	44	32	PTA4	—	ACMPO	BKGD	MS

1. This is a high current drive pin when operated as output. Please see High current drive for more information.
2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function

already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

Chapter 3
Power management

3.1 Introduction

The operating modes of the device are described in this chapter. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

3.2 Features

These MCUs feature the following power modes:

- Run mode
- Wait mode
  - CPU shuts down to conserve power
  - Bus clocks are running
  - Full voltage regulation is maintained
- Stop3 modes
  - System clocks stopped; voltage regulator in standby
  - all internal circuits powered for fast recovery

3.2.1 Run mode

This is the normal operating mode. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at 0xFFFE: 0xFFFF after reset. The power supply is fully regulating and all peripherals can be active in run mode.

3.2.2 Wait mode

Wait mode is entered by executing a WAIT instruction. Upon execution of the WAIT instruction, the CPU enters a low-power state in which it is not clocked. The I bit in CCR is cleared when the CPU enters the wait mode, enabling interrupts. When an interrupt request occurs, the CPU exits the wait mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

While the MCU is in wait mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available when the MCU is in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from wait mode and enter active background mode.

3.2.3 Stop3 mode

To enter stop3, the user must execute a STOP instruction with stop mode enabled (SOPT1[STOPE] = 1). Upon entering the stop3 mode, all of the clocks in the MCU are halted by default, but OSC clock and internal reference clock can be turned on by setting the ICS control registers. The ICS enters its standby state, as does the voltage regulator and the ADC. The states of all of the internal registers and logic, as well as the RAM content, are maintained. The I/O pin states are not latched at the pin. Instead they are maintained by virtue of the states of the internal logic driving the pins being maintained.

Exit from stop3 is done by asserting reset or through an interrupt. The interrupt include the asynchronous interrupt from the IRQ or KBI pins, the SCI receive interrupt, the ADC, ACMP, IIC or LVI interrupt and the real-time interrupt.

If stop3 is exited by means of the $\overline{\text{RESET}}$ pin, then the MCU will be reset and operation will resume after taking the reset vector. Exit by means of an asynchronous interrupt or the real-time interrupt will result in the MCU taking the appropriate interrupt vector.

The LPO (≈1 kHz) for the real-time counter clock allows a wakeup from stop3 mode with no external components. When RTC_SC2[RTCPS] is clear, the real-time counter clock function is disabled.

3.2.4 Active BDM enabled in stop3 mode

Entry into the active background mode from run mode is enabled if the BDC_SCR[ENBDM] bit is set. This register is described in the development support. If BDC_SCR[ENBDM] is set when the CPU executes a STOP instruction, the system clocks to the background debug logic remain active when the MCU enters stop mode, so background debug communication is still possible. In addition, the voltage regulator does not enter its low-power standby state but maintains full internal regulation.

Most background commands are not available in stop mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the MCU is in either stop or wait mode. The BACKGROUND command can be used to wake the MCU from stop and enter active background mode if the BDC_SCR[ENBDM] bit is set. After entering background debug mode, all background commands are available.

3.2.5 LVD enabled in stop mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop3 mode.

3.2.6 Power modes behaviors

Executing the WAIT or STOP command puts the MCU in a low power consumption mode for standby situations. The system integration module (SIM) holds the CPU in a non-clocked state. The operation of each of these modes is described in the following subsections. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupt to occur. The following table shows the low power mode behaviors.

Table 3-1. Low power mode behavior

Peripheral	Mode		
	Run	Wait	Stop3
PMC	Full regulation	Full regulation	Loose regulation
ICS	On	On	Optional on
XOSC	On	On	Optional on
LPO	On	On	On
CPU	On	Standby	Standby

Table continues on the next page...

Table 3-1. Low power mode behavior (continued)

Peripheral	Mode		
	Run	Wait	Stop3
FLASH	On	On	Standby
RAM	On	Standby	Standby
ADC	On	On	Optional on
ACMP	On	On	Optional on
I/O	On	On	States held
SCI	On	On	Standby
SPI	On	On	Standby
IIC	On	On	Standby
FTM	On	On	Standby
MTIM	On	On	Standby
WDOG	On	On	Optional on
DBG	On	On	Standby
IPC	On	On	Standby
CRC	On	On	Standby
RTC	On	On	Optional on
LVD	On	On	Optional on

3.3 Low voltage detect (LVD) system

This device includes a system to protect against low voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. This system consists of a power-on reset (POR) circuit and an LVD circuit with a user selectable trip voltage, either high (V_{LVDH}) or low (V_{LVDL}). The LVD circuit is enabled when SPMSC1[LVDE] is set and the trip voltage is selected by SPMSC2[LVDV]. The LVD is disabled upon entering the stop modes unless the SPMSC1[LVDSE] bit is set or active BDM enabled (BDCSCR[ENBDM]=1). If SPMSC1[LVDSE] and SPMSC1[LVDE] are both set, the current consumption in stop3 with the LVD enabled will be greater.

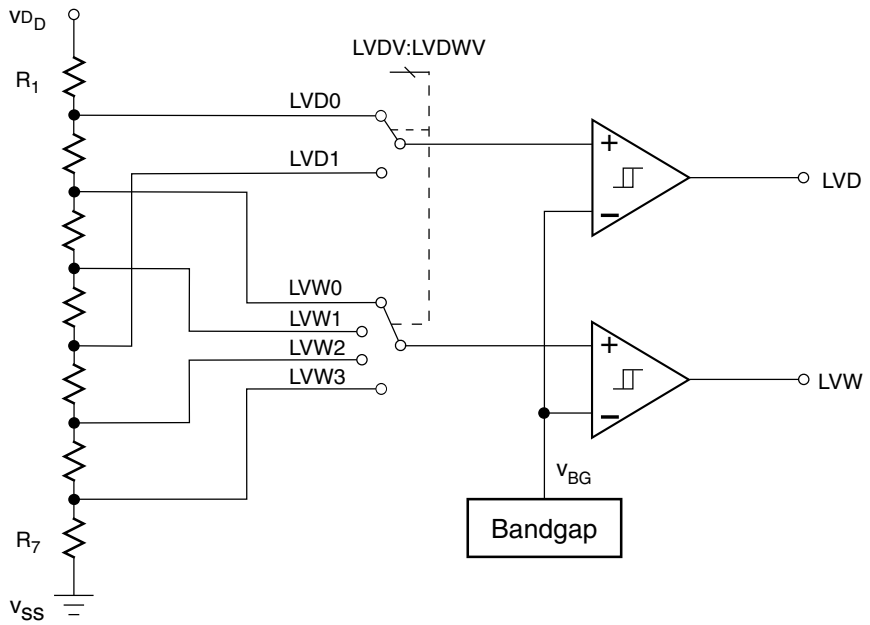


Figure 3-1. Low voltage detect (LVD) block diagram

3.3.1 Power-on reset (POR) operation

When power is initially applied to the MCU, or when the supply voltage drops below the V_{POR} level, the POR circuit will cause a reset condition. As the supply voltage rises, the LVD circuit will hold the chip in reset until the supply has risen above the V_{LVDL} level. Both the SRS[POR] and SRS[LVD] are set following a POR.

3.3.2 LVD reset operation

The LVD can be configured to generate a reset upon detection of a low voltage condition by setting SPMSC1[LVDRE] to 1. After an LVD reset has occurred, the LVD system will hold the MCU in reset until the supply voltage has risen above the level determined by LVDV. The SRS[LVD] bit is set following either an LVD reset or POR.

3.3.3 Low-voltage warning (LVW)

The LVD system has a low voltage warning flag to indicate that the supply voltage is approaching the LVD voltage. When a low voltage condition is detected and the LVD circuit is configured for interrupt operation (SPMSC1[LVDE] set, SPMSC1[LVWIE] set), SPMSC1[LVWF] will be set and LVW interrupt will occur. There are four user-selectable trip voltages for the LVW upon each LVDV configuration. The trip voltage is selected by SPMSC2[LVWV].

3.4 Bandgap reference

This device includes an on-chip bandgap reference (≈1.2V) connected to ADC channel and ACMP. The bandgap reference voltage will not drop under the full operating voltage even when the operating voltage is falling. This reference voltage acts as an ideal reference voltage for accurate measurements.

3.5 Power management control bits and registers

PMC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3040	System Power Management Status and Control 1 Register (PMC_SPMSC1)	8	R/W	1Ch	3.5.1/58
3041	System Power Management Status and Control 2 Register (PMC_SPMSC2)	8	R/W	00h	3.5.2/60

3.5.1 System Power Management Status and Control 1 Register (PMC_SPMSC1)

This high page register contains status and control bits to support the low-voltage detection function, and to enable the bandgap voltage reference for use by the ADC module. This register should be written during the user's reset initialization program to set the desired controls, even if the desired settings are the same as the reset settings.

Address: 3040h base + 0h offset = 3040h

Bit	7	6	5	4	3	2	1	0
Read	LVWF	0	LVWIE	LVDRE	LVDSE	LVDE	BGBDS	BGBE
Write		LVWACK						
Reset	0	0	0	1	1	1	0	0

PMC_SPMSC1 field descriptions

Field	Description
7 LVWF	Low-Voltage Warning Flag The LVWF bit indicates the low-voltage warning status.

Table continues on the next page...

PMC_SPMSC1 field descriptions (continued)

Field	Description
	NOTE: LVWF will be set in the case when V_{Supply} transitions below the trip point or after reset and V_{Supply} is already below V_{LVW}. LVWF bit may be 1 after power on reset, therefore, to use LVW interrupt function, before enabling LVWIE, LVWF must be cleared by writing LVWACK first. 0 Low-voltage warning is not present. 1 Low-voltage warning is present or was present.
6 LVWACK	Low-Voltage Warning Acknowledge If LVWF = 1, a low-voltage condition has occurred. To acknowledge this low-voltage warning, write 1 to LVWACK, which automatically clears LVWF to 0 if the low-voltage warning is no longer present.
5 LVWIE	Low-Voltage Warning Interrupt Enable This bit enables hardware interrupt requests for LVWF. 0 Hardware interrupt disabled (use polling). 1 Request a hardware interrupt when LVWF = 1.
4 LVDRE	Low-Voltage Detect Reset Enable This write-once bit enables LVD events to generate a hardware reset (provided LVDE = 1). **NOTE:** This bit can be written only one time after reset. Additional writes are ignored. 0 LVD events do not generate hardware resets. 1 Force an MCU reset when an enabled low-voltage detect event occurs.
3 LVDSE	Low-Voltage Detect Stop Enable Provided LVDE = 1, this read/write bit determines whether the low-voltage detect function operates when the MCU is in stop mode. 0 Low-voltage detect disabled during stop mode. 1 Low-voltage detect enabled during stop mode.
2 LVDE	Low-Voltage Detect Enable This write-once bit enables low-voltage detect logic and qualifies the operation of other bits in this register. **NOTE:** This bit can be written only one time after reset. Additional writes are ignored. 0 LVD logic disabled. 1 LVD logic enabled.
1 BGBDS	Bandgap Buffer Drive Select This bit is used to select the high drive mode of the bandgap buffer. 0 Bandgap buffer enabled in low drive mode if BGBE = 1. 1 Bandgap buffer enabled in high drive mode if BGBE = 1.
0 BGBE	Bandgap Buffer Enable This bit enables an internal buffer for the bandgap voltage reference for use by the ADC module on one of its internal channels. 0 Bandgap buffer disabled. 1 Bandgap buffer enabled.

3.5.2 System Power Management Status and Control 2 Register (PMC_SPMSC2)

This register is used to report the status of the low-voltage warning function, and to configure the stop mode behavior of the MCU. This register should be written during the user's reset initialization program to set the desired controls, even if the desired settings are the same as the reset settings.

Address: 3040h base + 1h offset = 3041h

Bit	7	6	5	4	3	2	1	0
Read	0	LVDV	LVWV		0			
Write								
Reset	0	0	0	0	0	0	0	0

PMC_SPMSC2 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 LVDV	Low-Voltage Detect Voltage Select This write-once bit selects the low-voltage detect (LVD) trip point setting. See data sheet for details. 0 Low trip point selected ($V_{LVD} = V_{LVDL}$). 1 High trip point selected ($V_{LVD} = V_{LVDH}$).
5–4 LVWV	Low-Voltage Warning Voltage Select This bit selects the low-voltage warning (LVW) trip point voltage. See data sheet for details. 00 Low trip point selected ($V_{LVW} = V_{LVW1}$). 01 Middle 1 trip point selected ($V_{LVW} = V_{LVW2}$). 10 Middle 2 trip point selected ($V_{LVW} = V_{LVW3}$). 11 High trip point selected ($V_{LVW} = V_{LVW4}$).
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Chapter 4
Memory map

4.1 Memory map

The HCS08 core processor can address 64 KB of memory space. The memory map, shown in the following figure, includes:

- User flash memory (flash)
  - MC9S08PA60: 60,864 bytes; 119 pages of 512 bytes each
  - MC9S08PA32: 32,768 bytes; 64 pages of 512 bytes each
- Random-access memory (RAM)
  - MC9S08PA60: 4,096 bytes
  - MC9S08PA32: 4,096 bytes
- Electrically erasable programmable read-only memory (EEPROM)
  - MC9S08PA60: 256 bytes; 128 pages of 2 bytes each
  - MC9S08PA32: 256 bytes; 128 pages of 2 bytes each
- Direct-page registers (0x0000 through 0x003F)
- High-page registers (0x3000 through 0x30FF)

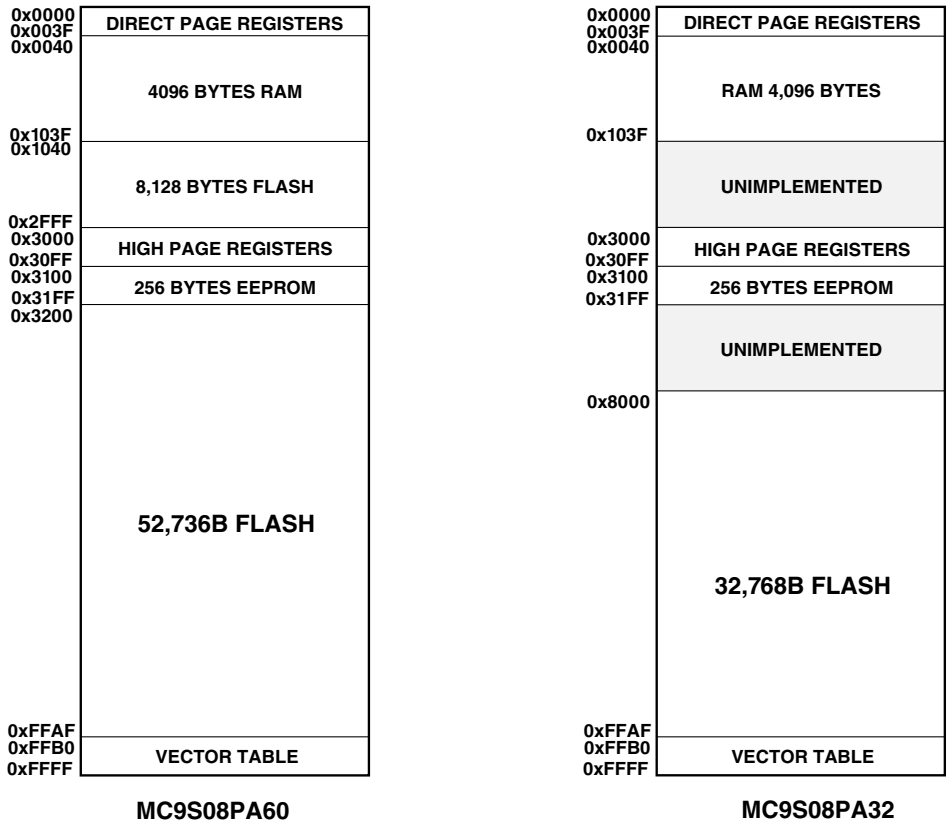


Figure 4-1. Memory map

4.2 Reset and interrupt vector assignments

The following table shows address assignments for reset and interrupt vectors. The vector names shown in this table are the labels used in the header files for the device.

Table 4-1. Reset and interrupt vectors

Address (high/low)	Vector	Vector name
0xFFB0:FFB1	NVM	Vnvm
0xFFB2:FFB3	KBI1	Vkbi1
0xFFB4:FFB5	KBI0	Vkbi0
0xFFB6:FFB7	Reserved	Reserved
0xFFB8:FFB9	RTC	Vrtc
0xFFBA:FFBB	IIC	Viic
0xFFBC:FFBD	SPI1	Vspi1
0xFEBE:FFBF	SPI0	Vspi0
0xFFC0:FFC1	SCI2 transmit	Vsci2txd
0xFFC2:FFC3	SCI2 receive	Vsci2rxd

Table continues on the next page...

Table 4-1. Reset and interrupt vectors (continued)

Address (high/low)	Vector	Vector name
0xFFC4:FFC5	SCI2 error	Vsci2err
0xFFC6:FFC7	SCI1 transmit	Vsci1txd
0xFFC8:FFC9	SCI1 receive	Vsci1rxd
0xFFCA:FFCB	SCI1 error	Vsci1err
0xFFCC:FFCD	SCI0 transmit	Vsci0txd
0xFFCE:FFCF	SCI0 receive	Vsci0rxd
0xFFD0:FFD1	SCI0 error	Vsci0err
0xFFD2:FFD3	ADC	Vadc
0xFFD4:FFD5	ACMP	Vacmp
0xFFD6:FFD7	MTIM1	Vmtim1
0xFFD8:FFD9	MTIM0	Vmtim0
0xFFDA:FFDB	FTM0 overflow	Vftm0ovf
0xFFDC:FFDD	FTM0 channel 1	Vftm0ch1
0xFFDE:FFDF	FTM0 channel 0	Vftm0ch0
0xFFE0:FFE1	FTM1 overflow	Vftm1ovf
0xFFE2:FFE3	FTM1 channel 1	Vftm1ch1
0xFFE4:FFE5	FTM1 channel 0	Vftm1ch0
0xFFE6:FFE7	FTM2 overflow	Vftm2ovf
0xFFE8:FFE9	FTM2 channel 5	Vftm2ch5
0xFFEA:FFEB	FTM2 channel 4	Vftm2ch4
0xFFEC:FFED	FTM2 channel 3	Vftm2ch3
0xFFEE:FFEF	FTM2 channel 2	Vftm2ch2
0xFFF0:FFF1	FTM2 channel 1	Vftm2ch1
0xFFF2:FFF3	FTM2 channel 0	Vftm2ch0
0xFFF4:FFF5	FTM2 fault	Vftm2flt
0xFFF6:FFF7	Clock loss of lock	Vclk
0xFFF8:FFF9	Low voltage warning	Vlvw
0xFFFA:FFFB	IRQ or Watchdog	Virq_wdog
0xFFFC:FFFD	SWI	Vswi
0xFFFE:FFFF	Reset	Vreset

4.3 Register addresses and bit assignments

The register definitions vary in different memory sizes. The register addresses of unused peripherals are reserved. The following table shows the register availability of the devices.

Table 4-2. Peripheral registers availability

Address	Bytes	Peripheral registers
0x0000—0x0007	8	Port data
0x0010—0x0017	8	ADC
0x0018—0x001B	4	MTIM0
0x001C—0x001F	4	MTIM1
0x0020—0x002A	11	FTM0
0x002C—0x002F	4	ACMP
0x0030—0x003A	11	FTM1
0x003B—0x003B	1	IRQ
0x003C—0x003C	1	KBI0
0x003D—0x003D	1	KBI1
0x003E—0x003F	2	IPC
0x3000—0x300B	12	SIM
0x300C—0x300F	4	SCG
0x3010—0x301F	16	DBG
0x3020—0x302C	13	NVM
0x3030—0x3037	8	WDOG
0x3038—0x303E	7	ICS, XOSC
0x3040—0x3041	2	PMC
0x304A—0x304B	2	SYS
0x3050—0x3059	10	IPC
0x3060—0x3068	9	CRC
0x306A—0x306F	6	RTC
0x3070—0x307B	12	IIC
0x307C—0x307D	2	KBI0
0x307E—0x307F	2	KBI1
0x3080—0x3087	8	SCI0
0x3088—0x308F	8	SCI1
0x3090—0x3097	8	SCI2
0x3098—0x309F	8	SPI0
0x30A0—0x30A9	10	SPI1
0x30AC—0x30AD	2	ADC
0x30AF—0x30AF	1	Port high drive enable
0x30B0—0x30B7	8	Port output enable
0x30B8—0x30BF	8	Port input enable
0x30C0—0x30EA	43	FTM2
0x30EC—0x30EF	4	Port filter
0x30F0—0x30F7	8	Port pullup
0x30F8—0x30FF	8	SYS

The registers in the devices are divided into two groups:

- Direct-page registers are located in the first 64 locations in the memory map, so they can be accessed with efficient direct addressing mode instructions.
- High-page registers are used much less often, so they are located above 0x3000 in the memory map. This leaves room in the direct page for more frequently used registers and variables.

Direct-page registers can be accessed with efficient direct addressing mode instructions. Bit manipulation instructions can be used to access any bit in a direct-page register.

The direct page registers can use the more efficient direct addressing mode, which requires only the lower byte of the address.

The following tables are summaries of all user-accessible direct-page and high-page registers and control bits. Cells that are not associated with named bits are shaded. A shaded cell with a 0 indicates this unused bit always reads as a 0; and a shaded cell with a 1 indicates this unused bit always reads as a 1. Shaded cells with dashes indicate unused or reserved bit locations that could read as 1s or 0s.

Table 4-3. Direct-page register allocation

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x0000	PORT_PTAD	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
0x0001	PORT_PTBD	PTBD7	PTBD6	PTBD5	PTBD4	PTBD3	PTBD2	PTBD1	PTBD0
0x0002	PORT_PTCD	PTCD7	PTCD6	PTCD5	PTCD4	PTCD3	PTCD2	PTCD1	PTCD0
0x0003	PORT_PTDD	PTDD7	PTDD6	PTDD5	PTDD4	PTDD3	PTDD2	PTDD1	PTDD0
0x0004	PORT_PTED	PTED7	PTED6	PTED5	PTED4	PTED3	PTED2	PTED1	PTED0
0x0005	PORT_PTFD	PTFD7	PTFD6	PTFD5	PTFD4	PTFD3	PTFD2	PTFD1	PTFD0
0x0006	PORT_PTGD	—	—	—	—	PTGD3	PTGD2	PTGD1	PTGD0
0x0007	PORT_PTHD	PTHD7	PTHD6	—	—	—	PTHD2	PTHD1	PTHD0
0x0008-0x000F	Reserved	—	—	—	—	—	—	—	—
0x0010	ADC_SC1	COCO	AIEN	ADCO	ADCH				
0x0011	ADC_SC2	ADACT	ADTRG	ACFE	ACFGT	FEMPTY	FFULL	—	—
0x0012	ADC_SC3	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
0x0013	ADC_SC4	—	ASCANE	ACFSEL	—	—	AFDEP		
0x0014	ADC_RH	—	—	—	—	11	10	9	Bit 8
0x0015	ADC_RL	Bit 7	6	5	4	3	2	1	Bit 0
0x0016	ADC_CVH	—	—	—	—	11	10	9	Bit 8
0x0017	ADC_CVL	Bit 7	6	5	4	3	2	1	Bit 0
0x0018	MTIM0_SC	TOF	TOIE	TRST	TSTP	—	—	—	—
0x0019	MTIM0_CLK	—	—	CLKS		PS			

Table continues on the next page...

Table 4-3. Direct-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x001A	MTIM0_CNT	COUNT							
0x001B	MTIM0_MOD	MOD							
0x001C	MTIM1_SC	TOF	TOIE	TRST	TSTP	—	—	—	—
0x001D	MTIM1_CLK	—	—	CLKS		PS			
0x001E	MTIM1_CNT	COUNT							
0x001F	MTIM1_MOD	MOD							
0x0020	FTM0_SC	TOF	TOIE	CPWMS	CLKS1	CLKS0	PS2	PS1	PS0
0x0021	FTM0_CNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x0022	FTM0_CNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x0023	FTM0_MODH	Bit 15	14	13	12	11	10	9	Bit 8
0x0024	FTM0_MODL	Bit 7	6	5	4	3	2	1	Bit 0
0x0025	FTM0_C0SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x0026	FTM0_C0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0027	FTM0_C0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0028	FTM0_C1SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x0029	FTM0_C1VH	Bit 15	14	13	12	11	10	9	Bit 8
0x002A	FTM0_C1VL	Bit 7	6	5	4	3	2	1	Bit 0
0x002B	Reserved	—	—	—	—	—	—	—	—
0x002C	ACMP_CS	ACE	HYST	ACF	ACIE	ACO	ACOPE	ACMOD	
0x002D	ACMP_C0	—	—	ACPSEL		—	—	ACNSEL	
0x002E	ACMP_C1	DACEN	DACREF	DACVAL					
0x002F	ACMP_C2	—	—	—	—	—	ACIPE2	ACIPE1	ACIPE0
0x0030	FTM1_SC	TOF	TOIE	CPWMS	CLKS1	CLKS0	PS2	PS1	PS0
0x0031	FTM1_CNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x0032	FTM1_CNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x0033	FTM1_MODH	Bit 15	14	13	12	11	10	9	Bit 8
0x0034	FTM1_MODL	Bit 7	6	5	4	3	2	1	Bit 0
0x0035	FTM1_C0SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x0036	FTM1_C0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x0037	FTM1_C0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x0038	FTM1_C1SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x0039	FTM1_C1VH	Bit 15	14	13	12	11	10	9	Bit 8
0x003A	FTM1_C1VL	Bit 7	6	5	4	3	2	1	Bit 0
0x003B	IRQ_SC	—	IRQPDD	IRQEDG	IRQPE	IRQF	IRQACK	IRQIE	IRQMOD
0x003C	KBI0_SC	—	—	—	—	KBF	KBACK	KBIE	KBMOD
0x003D	KBI1_SC	—	—	—	—	KBF	KBACK	KBIE	KBMOD
0x003E	IPC_SC	IPCE	—	PSE	PSF	PULIPM	—	IPM	
0x003F	IPC_IPMPS	IPM3		IPM2		IPM1		IPM0	

Table 4-4. High-page register allocation

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x3000	SYS_SRS	POR	PIN	WDOG	ILOP	ILAD	LOC	LVD	—
0x3001	SYS_SBDFR	—	—	—	—	—	—	—	BDFR
0x3002	SYS_SDIDH	—	—	—	—	ID11	ID10	ID9	ID8
0x3003	SYS_SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0x3004	SYS_SOPT1	SCI0PS	SPI0PS	IICPS	FTM2PS	BKGDPE	RSTPE	FWAKE	STOPE
0x3005	SYS_SOPT2	TXDME	FTMSYNC	RXDFE	RXDCE	ACIC	RTCC	ADHWTS	
0x3006	SYS_SOPT3	DLYACT	—	—	—	CLKOE	BUSREF		
0x3007	SYS_SOPT4	DELAY							
0x3008-0x300B	Reserved	—	—	—	—	—	—	—	—
0x300C	SCG_C1	FTM2	FTM1	FTM0	—	—	MTIM1	MTIM0	RTC
0x300D	SCG_C2	—	—	DBG	NVM	IPC	CRC	—	—
0x300E	SCG_C3	—	SCI2	SCI1	SCI0	SPI1	SPI0	IIC	—
0x300F	SCG_C4	ACMP	—	ADC	—	IRQ	—	KBI1	KBI0
0x3010	DBG_CAH	Bit 15	14	13	12	11	10	9	Bit 8
0x3011	DBG_CAL	Bit 7	6	5	4	3	2	1	Bit 0
0x3012	DBG_CBH	Bit 15	14	13	12	11	10	9	Bit 8
0x3013	DBG_CBL	Bit 7	6	5	4	3	2	1	Bit 0
0x3014	DBG_CCH	Bit 15	14	13	12	11	10	9	Bit 8
0x3015	DBG_CCL	Bit 7	6	5	4	3	2	1	Bit 0
0x3016	DBG_FH	Bit 15	14	13	12	11	10	9	Bit 8
0x3017	DBG_FL	Bit 7	6	5	4	3	2	1	Bit 0
0x3018	DBG_CAX	RWAEN	RWA	—	—	—	—	—	—
0x3019	DBG_CBX	RWBEN	RWB	—	—	—	—	—	—
0x301A	DBG_CCX	RWCEN	RWC	—	—	—	—	—	—
0x301B	DBG_FX	PPACC	—	—	—	—	—	—	Bit 16
0x301C	DBG_C	DBGEN	ARM	TAG	BRKEN	—	—	—	LOOP1
0x301D	DBG_T	TRGSEL	BEGIN	—	—	TRG			
0x301E	DBG_S	AF	BF	CF	—	—	—	—	ARMF
0x301F	DBG_CNT	—	—	—	—	CNT			
0x3020	NVM_FCLKDIV	FDIVLD	FDIVLCK	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
0x3021	NVM_FSEC	KEYEN1	KEYEN0	1	1	1	1	SEC1	SEC0
0x3022	NVM_FCCOBIX	—	—	—	—	—	CCOBIX2	CCOBIX1	CCOBIX0
0x3023	Reserved	—	—	—	—	—	—	—	—
0x3024	NVM_FCNFG	CCIE	—	—	IGNSF	—	—	FDFD	FSFD
0x3025	NVM_FERCNFG	—	—	—	—	—	—	DFDIE	SFDIE

Table continues on the next page...

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x3026	NVM_FSTAT	CCIF	—	ACCERR	FPVIOL	MGBUSY	—	MGSTAT1	MGSTAT0
0x3027	NVM_FERSTAT	—	—	—	—	—	—	DFDIF	SFDIF
0x3028	NVM_FPROT	FPOEN	—	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
0x3029	NVM_EEPROT	DPOPEN	—	—	—	—	DPS2	DPS1	DPS0
0x302A	NVM_FCCOBHI	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
0x302B	NVM_FCCOBLO	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
0x302C	NVM_FOPT	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
0x302D-0x302F	Reserved	—	—	—	—	—	—	—	—
0x3030	WDOG_CS1	EN	INT	UPDATE	TST		DBG	WAIT	STOP
0x3031	WDOG_CS2	WIN	FLG	—	PRES	—	—	CLK	
0x3032	WDOG_CNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x3033	WDOG_CNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x3034	WDOG_TOVALH	Bit 15	14	13	12	11	10	9	Bit 8
0x3035	WDOG_TOVALL	Bit 7	6	5	4	3	2	1	Bit 0
0x3036	WDOG_WINH	Bit 15	14	13	12	11	10	9	Bit 8
0x3037	WDOG_WINL	Bit 7	6	5	4	3	2	1	Bit 0
0x3038	ICS_C1	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
0x3039	ICS_C2	BDIV			LP	—	—	—	—
0x303A	ICS_C3	SCTRIM							
0x303B	ICS_C4	LOLIE	—	CME	—	—	—	—	SCFTRIM
0x303C	ICS_S	LOLS	LOCK	—	IREFST	CLKST		—	—
0x303D	Reserved	—	—	—	—	—	—	—	—
0x303E	ICS_OSCSC	OSCEN	—	OSCSTEN	OSCOS	—	RANGE	HGO	OSCINIT
0x303F	Reserved	—	—	—	—	—	—	—	—
0x3040	PMC_SPMSC1	LVWF	LVWACK	LVWIE	LVDRE	LVDSE	LVDE	BGBDS	BGBE
0x3041	PMC_SPMSC2	—	LVDV	LVWV		—	—	—	—
0x3042-0x3049	Reserved	—	—	—	—	—	—	—	—
0x304A	SYS_ILLAH	Bit 15	14	13	12	11	19	9	Bit 8
0x304B	SYS_ILLAL	Bit 7	6	5	4	3	2	1	Bit 0
0x304C-0x304F	Reserved	—	—	—	—	—	—	—	—
0x3050	IPC_ILRS0	ILR3		ILR2		ILR1		ILR0	
0x3051	IPC_ILRS1	ILR7		ILR6		ILR5		ILR4	
0x3052	IPC_ILRS2	ILR11		ILR10		ILR9		ILR8	
0x3053	IPC_ILRS3	ILR15		ILR14		ILR13		ILR12	

Table continues on the next page...

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x3054	IPC_ILRS4	ILR19		ILR18		ILR17		ILR16	
0x3055	IPC_ILRS5	ILR23		ILR22		ILR21		ILR20	
0x3056	IPC_ILRS6	ILR27		ILR26		ILR25		ILR24	
0x3057	IPC_ILRS7	ILR31		ILR30		ILR29		ILR28	
0x3058	IPC_ILRS8	ILR35		ILR34		ILR33		ILR32	
0x3059	IPC_ILRS9	ILR39		ILR38		ILR37		ILR36	
0x305A-0x305F	Reserved	—	—	—	—	—	—	—	—
0x3060	CRC_D0	Bit 31	30	29	28	27	26	25	Bit 24
0x3061	CRC_D1	Bit 23	22	21	20	19	18	17	Bit 16
0x3062	CRC_D2	Bit 15	14	13	12	11	10	9	Bit 8
0x3063	CRC_D3	Bit 7	6	5	4	3	2	1	Bit 0
0x3064	CRC_P0	Bit 31	30	29	28	27	26	25	Bit 24
0x3065	CRC_P1	Bit 23	22	21	20	19	18	17	Bit 16
0x3066	CRC_P2	Bit 15	14	13	12	11	10	9	Bit 8
0x3067	CRC_P3	Bit 7	6	5	4	3	2	1	Bit 0
0x3068	CRC_CTRL	TOT		TOTR		0	FXOR	WAS	TCRC
0x3069	Reserved	—	—	—	—	—	—	—	—
0x306A	RTC_SC1	RTIF	RTIE	—	RTCO	—	—	—	—
0x306B	RTC_SC2	RTCLKS		—	—	—	RTCPS		
0x306C	RTC_MODH	MODH							
0x306D	RTC_MODL	MODL							
0x306E	RTC_CNTH	CNTH							
0x306F	RTC_CNTL	CNTL							
0x3070	I2C_A1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
0x3071	I2C_F	MULT		ICR					
0x3072	I2C_C1	IICEN	IICIE	MST	TX	TXAK	RSTA	WUEN	—
0x3073	I2C_S	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
0x3074	I2C_D	DATA							
0x3075	I2C_C2	GCAEN	ADEXT	—	—	RMEN	AD10	AD9	AD8
0x3076	I2C_FLT	—	—	—	FLT4	FLT3	FLT2	FLT1	FLT0
0x3077	I2C_RA	RAD							—
0x3078	I2C_SMB	FACK	ALERTEN	SIICAEN	TCKSEL	SLTF	SHTF1	SHTF2	SHTF2IE
0x3079	I2C_A2	SAD7	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	—
0x307A	I2C_SLTH	SSLT15	SSLT14	SSLT13	SSLT12	SSLT11	SSLT10	SSLT9	SSLT8
0x307B	I2C_SLTL	SSLT7	SSLT6	SSLT5	SSLT4	SSLT3'	SSLT2	SSLT1	SSLT0
0x307C	KBI0_PE	KBIPE7	KBIPE6	KBIPE5	KBIPE4	KBIPE3	KBIPE2	KBIPE1	KBIPE0
0x307D	KBI0_ES	KBEDG7	KBEDG6	KBEDG5	KBEDG4	KBEDG3	KBEDG2	KBEDG1	KBEDG0
0x307E	KBI1_PE	KBIPE7	KBIPE6	KBIPE5	KBIPE4	KBIPE3	KBIPE2	KBIPE1	KBIPE0

Table continues on the next page...

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x307F	KBI1_ES	KBEDG7	KBEDG6	KBEDG5	KBEDG4	KBEDG3	KBEDG2	KBEDG1	KBEDG0
0x3080	SCI0_BDH	LBKDIE	RXEDGIE	SBNS	SBR12	SBR11	SBR10	SBR9	SBR8
0x3081	SCI0_BDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x3082	SCI0_C1	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x3083	SCI0_C2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x3084	SCI0_S1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x3085	SCI0_S2	LBKDIF	RXEDGIF	—	RXINV	RWUID	BRK13	LBKDE	RAF
0x3086	SCI0_C3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
0x3087	SCI0_D	D7	D6	D5	D4	D3	D2	D1	D0
0x3088	SCI1_BDH	LBKDIE	RXEDGIE	SBNS	SBR12	SBR11	SBR10	SBR9	SBR8
0x3089	SCI1_BDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x308A	SCI1_C1	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x308B	SCI1_C2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x308C	SCI1_S1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x308D	SCI1_S2	LBKDIF	RXEDGIF	—	RXINV	RWUID	BRK13	LBKDE	RAF
0x308E	SCI1_C3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
0x308F	SCI1_D	D7	D6	D5	D4	D3	D2	D1	D0
0x3090	SCI2_BDH	LBKDIE	RXEDGIE	SBNS	SBR12	SBR11	SBR10	SBR9	SBR8
0x3091	SCI2_BDL	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x3092	SCI2_C1	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x3093	SCI2_C2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
0x3094	SCI2_S1	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
0x3095	SCI2_S2	LBKDIF	RXEDGIF	—	RXINV	RWUID	BRK13	LBKDE	RAF
0x3096	SCI2_C3	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
0x3097	SCI2_D	D7	D6	D5	D4	D3	D2	D1	D0
0x3098	SPI0_C1	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
0x3099	SPI0_C2	SPMIE	—	—	MODFEN	BIDIROE	—	SPISWAI	SPC0
0x309A	SPI0_BR	—	SPPR2	SPPR1	SPPR0	SPR3	SPR2	SPR1	SPR0
0x309B	SPI0_S	SPRF	SPMF	SPTEF	MODF	—	—	—	—
0x309C	Reserved	—	—	—	—	—	—	—	—
0x309D	SPI0_D	Bit 7	6	5	4	3	2	1	Bit 0
0x309E	Reserved	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x309F	SPI0_M	Bit 7	6	5	4	3	2	1	Bit 0
0x30A0	SPI1_C1	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
0x30A1	SPI1_C2	SPMIE	SPIMODE	—	MODFEN	BIDIROE	—	SPISWAI	SPC0
0x30A2	SPI1_BR	—	SPPR2	SPPR1	SPPR0	SPR3	SPR2	SPR1	SPR0
0x30A3	SPI1_S	SPRF	SPMF	SPTEF	MODF	RNFULLF	TNEAREF	TXFULLF	RFIFOEF
0x30A4	SPI1_DH	Bit 15	14	13	12	11	10	9	Bit 8
0x30A5	SPI1_DL	Bit 7	6	5	4	3	2	1	Bit 0
0x30A6	SPI1_MH	Bit 15	14	13	12	11	10	9	Bit 8
0x30A7	SPI1_ML	Bit 7	6	5	4	3	2	1	Bit 0
0x30A8	SPI1_C3	—	—	TNEAREF_MARK	RNFULLF_MARK	INTCLR	TNEARIEN	RNFULLIEN	FIFOMODE
0x30A9	SPI1_CI	TXFERR	RXFERR	TXFOF	RXFOF	TNEAREFCI	RNFULLFCI	SPTEFCI	SPRFCI
0x30AA-0x30AB	Reserved	—	—	—	—	—	—	—	—
0x30AC	ADC_APCTL1	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0
0x30AD	ADC_APCTL2	ADPC15	ADPC14	ADPC13	ADPC12	ADPC11	ADPC10	ADPC9	ADPC8
0x30AE	Reserved	—	—	—	—	—	—	—	—
0x30AF	PORT_HDRVE	PTH1	PTH0	PTE1	PTE0	PTD1	PTD0	PTB5	PTB4
0x30B0	PORT_PTAOE	PTAOE7	PTAOE6	PTAOE5	PTAOE4	PTAOE3	PTAOE2	PTAOE1	PTAOE0
0x30B1	PORT_PTBOE	PTBOE7	PTBOE6	PTBOE5	PTBOE4	PTBOE3	PTBOE2	PTBOE1	PTBOE0
0x30B2	PORT_PTCOE	PTCOE7	PTCOE6	PTCOE5	PTCOE4	PTCOE3	PTCOE2	PTCOE1	PTCOE0
0x30B3	PORT_PTDOE	PTDOE7	PTDOE6	PTDOE5	PTDOE4	PTDOE3	PTDOE2	PTDOE1	PTDOE0
0x30B4	PORT_PTEOE	PTEOE7	PTEOE6	PTEOE5	PTEOE4	PTEOE3	PTEOE2	PTEOE1	PTEOE0
0x30B5	PORT_PTFOE	PTFOE7	PTFOE6	PTFOE5	PTFOE4	PTFOE3	PTFOE2	PTFOE1	PTFOE0
0x30B6	PORT_PTGOE	—	—	—	—	PTGOE3	PTGOE2	PTGOE1	PTGOE0
0x30B7	PORT_PTHOE	PTHOE7	PTHOE6	—	—	—	PTHOE2	PTHOE1	PTHOE0
0x30B8	PORT_PTAIE	PTAIE7	PTAIE6	PTAIE5	—	PTAIE3	PTAIE2	PTAIE1	PTAIE0
0x30B9	PORT_PTBIE	PTBIE7	PTBIE6	PTBIE5	PTBIE4	PTBIE3	PTBIE2	PTBIE1	PTBIE0
0x30BA	PORT_PTCIE	PTCIE7	PTCIE6	PTCIE5	PTCIE4	PTCIE3	PTCIE2	PTCIE1	PTCIE0
0x30BB	PORT_PTDIE	PTDIE7	PTDIE6	PTDIE5	PTDIE4	PTDIE3	PTDIE2	PTDIE1	PTDIE0
0x30BC	PORT_PTEIE	PTEIE7	PTEIE6	PTEIE5	PTEIE4	PTEIE3	PTEIE2	PTEIE1	PTEIE0
0x30BD	PORT_PTFIE	PTFIE7	PTFIE6	PTFIE5	PTFIE4	PTFIE3	PTFIE2	PTFIE1	PTFIE0
0x30BE	PORT_PTGIE	—	—	—	—	PTGIE3	PTGIE2	PTGIE1	PTGIE0
0x30BF	PORT_PTHIE	PTHIE7	PTHIE6	—	—	—	PTHIE2	PTHIE1	PTHIE0
0x30C0	FTM2_SC	TOF	TOIE	CPWMS	CLKS1	CLKS0	PS2	PS1	PS0

Table continues on the next page...

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x30C1	FTM2_CNTH	Bit 15	14	13	12	11	10	9	Bit 8
0x30C2	FTM2_CNTL	Bit 7	6	5	4	3	2	1	Bit 0
0x30C3	FTM2_MODH	Bit 15	14	13	12	11	10	9	Bit 8
0x30C4	FTM2_MODL	Bit 7	6	5	4	3	2	1	Bit 0
0x30C5	FTM2_C0SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x30C6	FTM2_C0VH	Bit 15	14	13	12	11	10	9	Bit 8
0x30C7	FTM2_C0VL	Bit 7	6	5	4	3	2	1	Bit 0
0x30C8	FTM2_C1SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x30C9	FTM2_C1VH	Bit 15	14	13	12	11	10	9	Bit 8
0x30CA	FTM2_C1VL	Bit 7	6	5	4	3	2	1	Bit 0
0x30CB	FTM2_C2SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x30CC	FTM2_C2VH	Bit 15	14	13	12	11	10	9	Bit 8
0x30CD	FTM2_C2VL	Bit 7	6	5	4	3	2	1	Bit 0
0x30CE	FTM2_C3SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x30CF	FTM2_C3VH	Bit 15	14	13	12	11	10	9	Bit 8
0x30D0	FTM2_C3VL	Bit 7	6	5	4	3	2	1	Bit 0
0x30D1	FTM2_C4SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x30D2	FTM2_C4VH	Bit 15	14	13	12	11	10	9	Bit 8
0x30D3	FTM2_C4VL	Bit 7	6	5	4	3	2	1	Bit 0
0x30D4	FTM2_C5SC	CHF	CHIE	MSB	MSA	ELSB	ELSA	—	—
0x30D5	FTM2_C5VH	Bit 15	14	13	12	11	10	9	Bit 8
0x30D6	FTM2_C5VL	Bit 7	6	5	4	3	2	1	Bit 0
0x30D7	FTM2_CNTINH	Bit 15	14	13	12	11	10	9	Bit 8
0x30D8	FTM2_CNTINL	Bit 7	6	5	4	3	2	1	Bit 0
0x30D9	FTM2_STATUS	CH7F	CH6F	CH5F	CH4F	CH3F	CH2F	CH1F	CH0F
0x30DA	FTM2_MODE	FAULTIE	FAULTM		CAPTEST	PWMSYNC	WPDIS	INIT	FTMEN
0x30DB	FTM2_SYNC	SWSYNC	TRIG2	TRIG1	TRIG0	SYNCHOM	REINIT	CNTMAX	CNTMIN
0x30DC	FTM2_OUTINIT	CH7OI	CH6OI	CH5OI	CH4OI	CH3OI	CH2OI	CH1OI	CH0OI
0x30DD	FTM2_OUTMASK	CH7OM	CH6OM	CH5OM	CH4OM	CH3OM	CH2OM	CH1OM	CH0OM
0x30DE	FTM2_COMBINE0	—	FAULTEN	SYNCEN	DTEN	DECAP	DECAPEN	COMP	COMBINE
0x30DF	FTM2_COMBINE1	—	FAULTEN	SYNCEN	DTEN	DECAP	DECAPEN	COMP	COMBINE
0x30E0	FTM2_COMBINE2	—	FAULTEN	SYNCEN	DTEN	DECAP	DECAPEN	COMP	COMBINE
0x30E1	FTM2_COMBINE3	—	FAULTEN	SYNCEN	DTEN	DECAP	DECAPEN	COMP	COMBINE
0x30E2	FTM2_DEATIME	DTPS		DTVAL					

Table continues on the next page...

Table 4-4. High-page register allocation (continued)

Address	Register name	Bit 7	6	5	4	3	2	1	Bit 0
0x30E3	FTM2_EXTTRIG	TRIGF	INITTRIGEN	CH1TRIG	CH0TRIG	CH5TRIG	CH4TRIG	CH3TRIG	CH2TRIG
0x30E4	FTM2_POL	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
0x30E5	FTM2_FMS	FAULTF	WPEN	FAULTIN	—	—	FAULTF2	FAULTF1	FAULTF0
0x30E6	FTM2_FILTER0	CHoddFVAL				CHevenFVAL			
0x30E7	FTM2_FILTER1	CHoddFVAL				CHevenFVAL			
0x30E8	FTM2_FLTFILTER	—	—	—	—	FFVAL			
0x30E9	FTM2_FLTCTRL	FFLTR3EN	FFLTR2EN	FFLTR1EN	FFLTR0EN	FAULT3EN	FAULT2EN	FAULT1EN	FAULT0EN
0x30EA-0x30EB	Reserved	—	—	—	—	—	—	—	—
0x30EC	PORT_IOFLT0	FLTD		FLTC		FLTB		FLTA	
0x30ED	PORT_IOFLT1	FLTH		FLTG		FLTF		FLTE	
0x30EE	PORT_IOFLT2	—	—	FLTKBI1		FLTKBI0		FLTRST	
0x30EF	PORT_FCLKDIV	FLTDIV3			FLTDIV2			FLTDIV1	
0x30F0	PORT_PTAPE	PTAPE7	PTAPE6	PTAPE5	—	PTAPE3	PTAPE2	PTAPE1	PTAPE0
0x30F1	PORT_PTBPE	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
0x30F2	PORT_PTCPE	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
0x30F3	PORT_PTDPE	PTDPE7	PTDPE6	PTDPE5	PTDPE4	PTDPE3	PTDPE2	PTDPE1	PTDPE0
0x30F4	PORT_PTEPE	PTEPE7	PTEPE6	PTEPE5	PTEPE4	PTEPE3	PTEPE2	PTEPE1	PTEPE0
0x30F5	PORT_PTFPE	PTFPE7	PTFPE6	PTFPE5	PTFPE4	PTFPE3	PTFPE2	PTFPE1	PTFPE0
0x30F6	PORT_PTGPE	—	—	—	—	PTGPE3	PTGPE2	PTGPE1	PTGPE0
0x30F7	PORT_PTHPE	PTHPE7	PTHPE6	—	—	—	PTHPE2	PTHPE1	PTHPE0
0x30F8	SYS_UUID1	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56
0x30F9	SYS_UUID2	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
0x30FA	SYS_UUID3	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
0x30FB	SYS_UUID4	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
0x30FC	SYS_UUID5	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
0x30FD	SYS_UUID6	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
0x30FE	SYS_UUID7	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
0x30FF	SYS_UUID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Several reserved flash memory locations, shown in the following table, are used for storing values used by several registers. These registers include an 8-byte backdoor key, NV_BACKKEY, which can be used to gain access to secure memory resources. During reset events, the contents of NVPROT and NVOPT in the reserved flash memory are transferred into corresponding FPROT and FOPT registers in the high-page registers area to control security and block protection options.

The factory ICS trim value is stored in the flash information row (IFR[1]) and will be loaded into the ICS_C3 and ICS_C4 registers after any reset. The internal reference trim values (SCTRIM and SCFTRIM) stored in reserved flash registers, NV_ICSTRM and NV_FTRIM, can be programmed by third party programmers and must be copied into the corresponding ICS registers by user code to override the factory trim.

NOTE

When the MCU is in active BDM, the trim value in the IFR will not be loaded. Instead, the ICS_C3 register will reset to 0x80 and the SCFTRIM bit in the ICS_C4 register will be reset to 0.

Table 4-5. Reserved flash memory addresses

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0xFF6E	NV_FTRIM	—	—	—	—	—	—	—	SCFTRIM
0xFF6F	NV_ICSTRM	SCTRIM							
0xFF70	NV_BACKKEY0	BACKKEY0							
0xFF71	NV_BACKKEY1	BACKKEY1							
0xFF72	NV_BACKKEY2	BACKKEY2							
0xFF73	NV_BACKKEY3	BACKKEY3							
0xFF74	NV_BACKKEY4	BACKKEY4							
0xFF75	NV_BACKKEY5	BACKKEY5							
0xFF76	NV_BACKKEY6	BACKKEY6							
0xFF77	NV_BACKKEY7	BACKKEY7							
0xFF78	Reserved	—	—	—	—	—	—	—	—
0xFF79	Reserved	—	—	—	—	—	—	—	—
0xFF7A	Reserved	—	—	—	—	—	—	—	—
0xFF7B	Reserved	—	—	—	—	—	—	—	—
0xFF7C	NV_FPROT	FPOPEN	—	FPHDIS	FPHS		FPLDIS	FPLS	
0xFF7D	NV_EEPROT	DPOPEN	—				DPS		
0xFF7E	NV_FOPT	NV							
0xFF7F	NV_FSEC	KEYEN		1	1	1	1	SEC	

The 8-byte comparison key can be used to temporarily disengage memory security provided the key enable field, NV_FSEC[KEYEN], is 10b. This key mechanism can be accessed only through user code running in secure memory. A security key cannot be entered directly through background debug commands. This security key can be disabled completely by programming the NV_FSEC[KEYEN] field to 00b, 01b, or 11b. If the

1. IFR — Nonvolatile information memory that can be only accessed during production test. During production test, system initialization, configuration and test information is stored in the IFR. This information cannot be read or modified in normal user or background debug modes.

security key is disabled, the only way to disengage security is by mass erasing the flash if needed, normally through the background debug interface and verifying that flash is blank. To avoid returning to secure mode after the next reset, program the security bits, NV_FSEC[SEC], to the unsecured state (10b).

4.4 Random-access memory (RAM)

This section describes the 4,096 bytes of RAM (random-access memory).

These devices include static RAM. The locations in RAM below 0x0100 can be accessed using the more efficient direct addressing mode. Any single bit in this area can be accessed with the bit manipulation instructions (BCLR, BSET, BRCLR, and BRSET).

The RAM retains data when the MCU is in low-power wait, or stop3 mode. At power-on, the contents of RAM are uninitialized. RAM data is unaffected by any reset provided that the supply voltage does not drop below the minimum value for RAM retention.

For compatibility with older M68HC05 MCUs, the HCS08 resets the stack pointer to 0x00FF. In this series, re-initialize the stack pointer to the top of the RAM so that the direct-page RAM can be used for frequently accessed RAM variables and bit-addressable program variables. Include the following 2-instruction sequence in your reset initialization routine (where RamLast is equated to the highest address of the RAM in the equate file).

```
LDHX     #RamLast+1    ;point one past RAM
TXS                    ;SP<-(H:X-1)
```

When security is enabled, the RAM is considered a secure memory resource and is not accessible through BDM or code executing from non-secure memory.

4.5 Flash and EEPROM

4.5.1 Overview

This device includes various configuration of flash and EEPROM. The controller for flash and EEPROM is ideal for single-supply applications for field programming without external high voltage sources for program or erase operations.

The flash memory is ideal for single-supply applications that allow for field reprogramming without requiring external high voltage sources for program or erase operations. The flash module includes a memory controller that executes commands to modify flash memory contents. The user interface to the memory controller consists of

the indexed flash common command object (FCCOB) register, which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register is written to with a new command.

CAUTION

A flash byte or longword must be in the erased state before being programmed. Cumulative programming of bits within a flash byte or longword is not allowed.

The flash memory is read as bytes. Read access time is one bus cycle for bytes. For flash memory, an erased bit reads 1 and a programmed bit reads 0. It is possible to read from flash memory while commands are being executed on EEPROM memory. It is not possible to read from EEPROM memory while a command (erase/program) is executing on flash memory. Simultaneous EEPROM memory are implemented with error correction codes (ECC) that can resolve single bit faults and detect double bit faults.

The following figure shows the block diagram of the flash and EEPROM module.

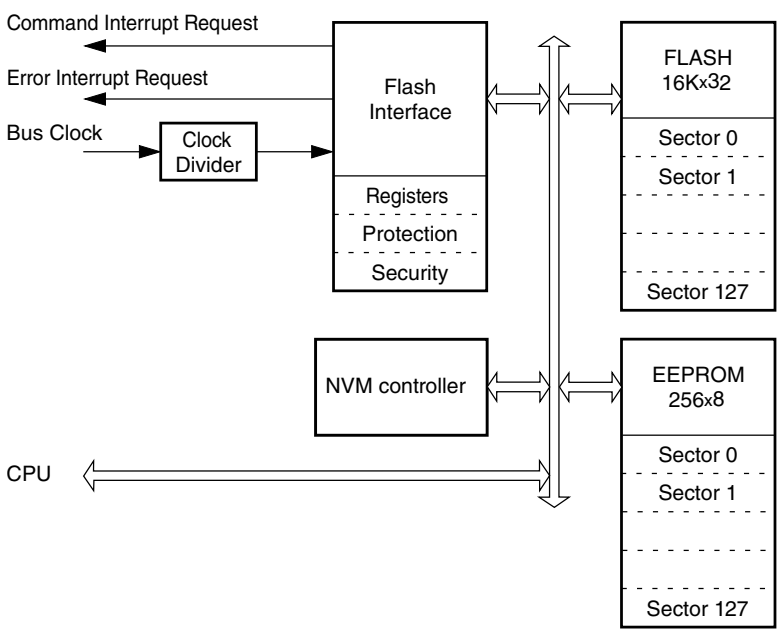


Figure 4-2. Flash and EEPROM block diagram

Flash features:

- 64 KB of flash memory composed of one 64 KB flash block divided into 128 sectors of 512 bytes
- Automated program and erase algorithm with verification

- Fast sector erase and longword program operation
- Ability to read the flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of flash memory

EEPROM features:

- 256 bytes of EEPROM memory composed of one 256 byte EEPROM block divided into sectors of 2 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verification and generation of ECC parity bits
- Fast sector erase and byte program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four bytes in a burst sequence

Other features

- No external high-voltage power supply required for flash memory program and erase operations
- Interrupt generation on flash command completion and flash error detection
- Security mechanism to prevent unauthorized access to the flash memory

4.5.2 Function descriptions

4.5.2.1 Modes of operation

The flash and EEPROM module provides the normal user mode of operation. The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers.

4.5.2.1.1 Wait mode

The flash and EEPROM module is not affected if the MCU enters wait mode. The flash module can recover the MCU from wait via the CCIF interrupt. See Flash and EEPROM interrupts.

4.5.2.1.2 Stop mode

If a flash and EEPROM command is active, that is, FSTAT[CCIF] = 0, when the MCU requests stop mode, the current NVM operation will be completed before the MCU is allowed to enter stop mode.

4.5.2.2 Flash and EEPROM memory map

The MCU places the flash memory between global address 0x0000 and 0xFFFF as shown in the following table. Not all flash are available to users because some addresses are overlapped with RAM, EEPROM, and registers.

MC9S08PA60 contains a piece of 64 KB flash in which only 60,864 bytes flash are available for users. This flash block is divided into 128 sectors of 512 bytes. MC9S08PA32 contains a piece of 32 KB flash that is fully available for users. This flash block is divided into 64 sectors of 512 bytes.

Table 4-6. Flash memory addressing

Device	Global address	Size (Bytes)	Description	User availability
MC9S08PA60	0x0000 — 0xFFFF	64 KB	Flash block contains flash configuration field	Sector [0:7]: N/A Sector [8]: Last 448 bytes available Sector [9:23]: fully available Sector [24]: N/A Sector [25:127]: fully available
MC9S08PA32	0x8000 — 0xFFFF	32 KB	Flash block contains flash configuration field	Sector [64:127]: fully available

4.5.2.3 Flash and EEPROM initialization after system reset

On each system reset, the flash and EEPROM module executes an initialization sequence that establishes initial values for the flash and EEPROM block configuration parameters, the FPROT and EEPROT protection registers, and the FOPT and FSEC registers. The initialization routine reverts to built-in default values that leave the module in a fully protected and secured state if errors are encountered during execution of the reset sequence. If a double bit fault is detected during the reset sequence, both FSTAT[MGSTAT] bits will be set.

FSTAT[CCIF] is cleared throughout the initialization sequence. The NVM module holds off all CPU access for a portion of the initialization sequence. Flash and EEPROM reads are allowed after the hold is removed. Completion of the initialization sequence is marked by setting FSTAT[CCIF] high, which enables user commands.

If a reset occurs while any flash or EEPROM command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

4.5.2.4 Flash and EEPROM command operations

Flash and EEPROM command operations are used to modify flash and EEPROM memory contents.

The command operations contain three steps:

1. Configure the clock for flash or EEPROM program and erase command operations.
2. Use command write sequence to set flash and EEPROM command parameters and launch execution.
3. Execute valid flash and EEPROM commands according to MCU functional mode and MCU security state.

The figure below shows a general flowchart of the flash or EEPROM command write sequence.

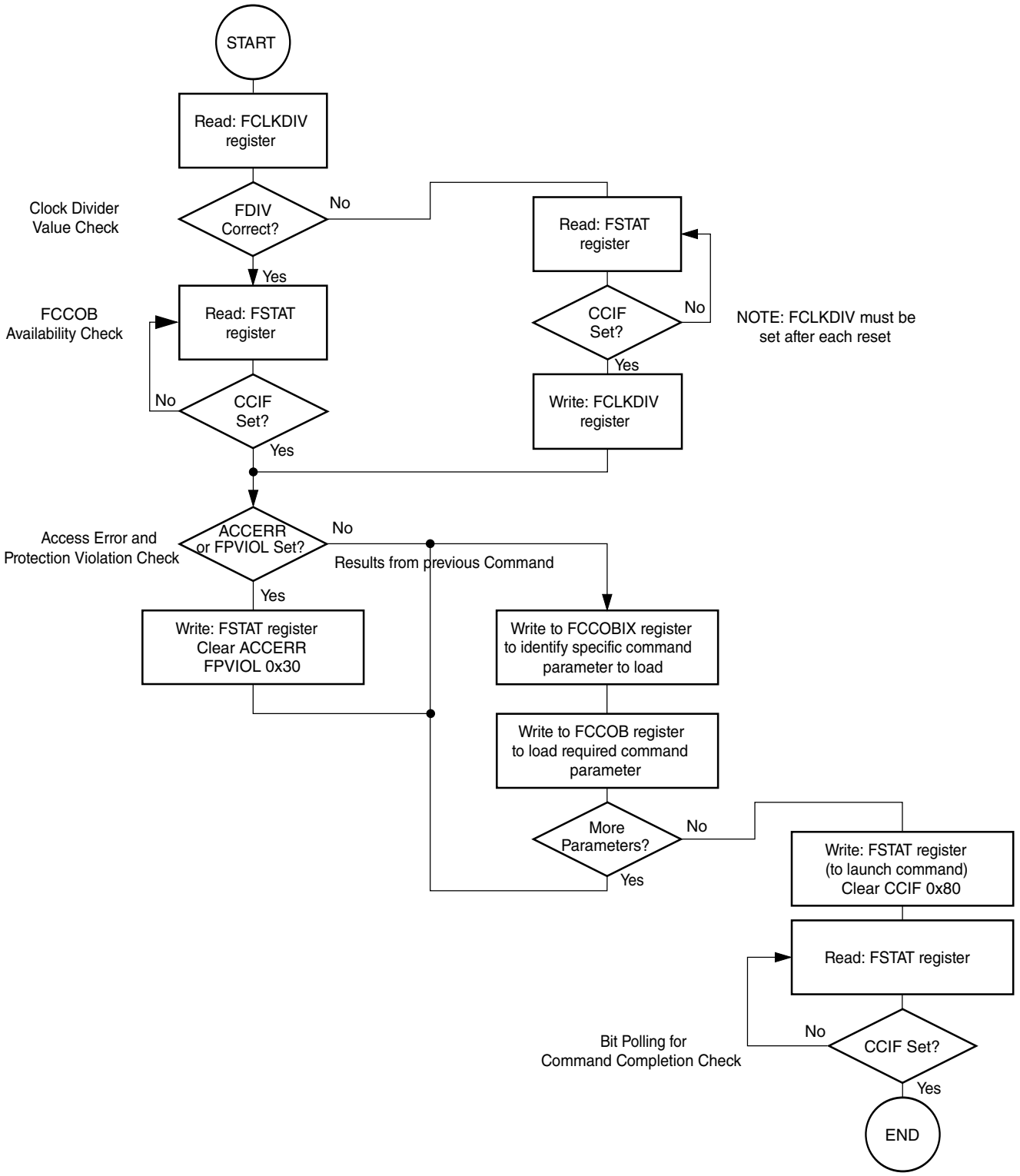


Figure 4-3. Generic flash and EEPROM command write sequence flowchart

4.5.2.4.1 Writing the FCLKDIV register

Prior to issuing any flash and EEPROM program or erase command after a reset, the user is required to write the FCLKDIV register to divide BUSCLK down to a target FCLK of 1MHz. The following table shows recommended values for the FDIV field based on BUSCLK frequency.

Table 4-7. FDIV values for various BUSCLK frequencies

BUSCLK frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]	
1.0	1.6	0x00
1.6	2.6	0x01
2.6	3.6	0x02
3.6	4.6	0x03
4.6	5.6	0x04
5.6	6.6	0x05
6.6	7.6	0x06
7.6	8.6	0x07
8.6	9.6	0x08
9.6	10.6	0x09
10.6	11.6	0x0A
11.6	12.6	0x0B
12.6	13.6	0x0C
13.6	14.6	0x0D
14.6	15.6	0x0E
15.6	16.6	0x0F
16.6	17.6	0x10
17.6	18.6	0x11
18.6	19.6	0x12
19.6	20.0	0x13

1. BUSCLK is greater than this value
2. BUSCLK is less than or equal to this value

CAUTION

Programming or erasing the flash and EEPROM memory cannot be performed if the bus clock runs at less than 0.8 MHz. Setting FCLKDIV[FDIV] too high can destroy the flash and EEPROM memory due to overstress. Setting FCLKDIV[FDIV] too low can result in incomplete programming or erasure of the flash and EEPROM memory cells.

When the FCLKDIV register is written, the FCLKDIV[FDIVLD] bit is set automatically. If the FCLKDIV[FDIVLD] bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any flash and EEPROM program or erase command loaded during a command write sequence will not execute and the FSTAT[ACCERR] bit will be set.

4.5.2.4.2 Command write sequence

The memory controller will launch all valid flash and EEPROM commands entered using a command write sequence.

Before launching a command, the FSTAT[ACCERR] and FSTAT[FPVIOL] bits must be clear and the FSTAT[CCIF] flag will be tested to determine the status of the current command write sequence. If FSTAT[CCIF] is 0, indicating that the previous command write sequence is still active, a new command write sequence cannot be started and all writes to the FCCOB register are ignored.

The FCCOB parameter fields must be loaded with all required parameters for the flash and EEPROM command being executed. Access to the FCCOB parameter fields is controlled via FCCOBIX[CCOBIX] bits.

Flash and EEPROM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the memory controller. First, the user must set up all required FCCOB field. Then they can initiate the command's execution by writing a 1 to the FSTAT[CCIF] bit. This action clears the CCIF command completion flag to 0. When the user clears the FSTAT[CCIF] bit all FCCOB parameter field are locked and cannot be changed by the user until the command completes (evidenced by the memory controller returning FSTAT[CCIF] to1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in flash and EEPROM command mode is shown in the following table. The return values are available for reading after the FSTAT[CCIF] flag has been returned to 1 by the memory controller. Writes to the unimplemented parameter fields, FCCOBIX[CCOBIX] =110b and FCCOBIX[CCOBIX] = 111b, are ignored with read from these fields returning 0x0000.

The table below shows the generic flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific flash command. For details on the FCCOB settings required by each command, see the flash command descriptions in Flash and EEPROM command summary .

Table 4-8. FCCOB – flash and EEPROM command mode typical usage

CCOBIX[2:0]	Byte	FCCOB parameter fields in flash and EEPROM command mode
000	HI	FCMD[7:0] defining flash command
	LO	Global address [23:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]
011	HI	Data 1 [15:8]
	LO	Data 1 [7:0]
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

The contents of the FCCOB parameter fields are transferred to the memory controller when the user clears the FSTAT[CCIF] command completion flag by writing 1. The CCIF flag will remain clear until the flash and EEPROM command has completed. Upon completion, the memory controller will return FSTAT[CCIF] to 1 and the FCCOB register will be used to communicate any results.

The following table presents the valid flash and EEPROM commands, as enabled by the combination of the functional MCU mode with the MCU security state of unsecured or secured.

MCU secured state is selected by NVM_FSEC[SEC].

Table 4-9. Flash and EEPROM commands by mode and security state

FCMD	Command	Unsecured	Secured
		U[1]	U[2]
0x01	Erase verify all blocks	*	*
0x02	Erase verify block	*	*
0x03	Erase verify flash section	*	N/A
0x04	Read once	*	N/A
0x06	Program flash	*	N/A
0x07	Program once	*	N/A
0x08	Erase all block	*	*
0x09	Erase flash block	*	*
0x0A	Erase flash sector	*	N/A
0x0B	Unsecure NVM	N/A	*
0x0C	Verify backdoor access key	*	*

Table continues on the next page...

Table 4-9. Flash and EEPROM commands by mode and security state (continued)

FCMD	Command	Unsecured	Secured
		U[1]	U[2]
0x0D	Set user margin level	*	N/A
0x10	Erase verify EEPROM section	*	*
0x11	Program EEPROM	*	N/A
0x12	Erase EEPROM sector	*	N/A

1. Unsecured User mode
2. Secured User mode

4.5.2.5 Flash and EEPROM interrupts

The flash and EEPROM module can generate an interrupt when a flash command operation has completed or when a flash and EEPROM command operation has detected an ECC fault.

Table 4-10. Flash interrupt source

Interrupt source	Interrupt flag	Local enable	Global (CCR) mask
Flash and EEPROM command complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC double bit fault on flash and EEPROM read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC single bit fault on flash and EEPROM read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

4.5.2.5.1 Description of flash and EEPROM interrupt operation

The flash module uses the FSTAT[CCIF] flag in combination with the FCNFG[CCIE] interrupt enable bit to generate the flash command interrupt request. The flash module uses the DFDIF and SFDIF flags in combination with the FERSTAT[DFDIE] and FERSTAT[SFDIE] interrupt enable bits to generate the flash error interrupt request.

The logic used for generating the flash module interrupts is shown in the following figure.

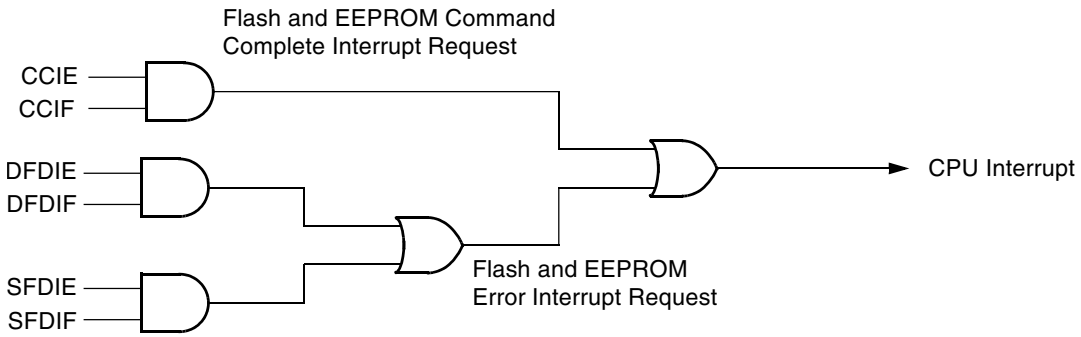


Figure 4-4. Flash and EEPROM module interrupts implementation

4.5.2.6 Protection

The FPROT register can be set to protect regions in the flash memory from accidental programming or erasing. Three separate memory regions, one growing upward from global address 0x8000 in the flash memory, called the lower region; one growing downward from global address 0xFFFF in the flash memory, called the higher region; and the remaining addresses in the flash memory, can be activated for protection. The flash memory addresses covered by these protectable regions are shown in the flash memory map. The higher address region is mainly targeted to hold the boot loader code because it covers the vector space.

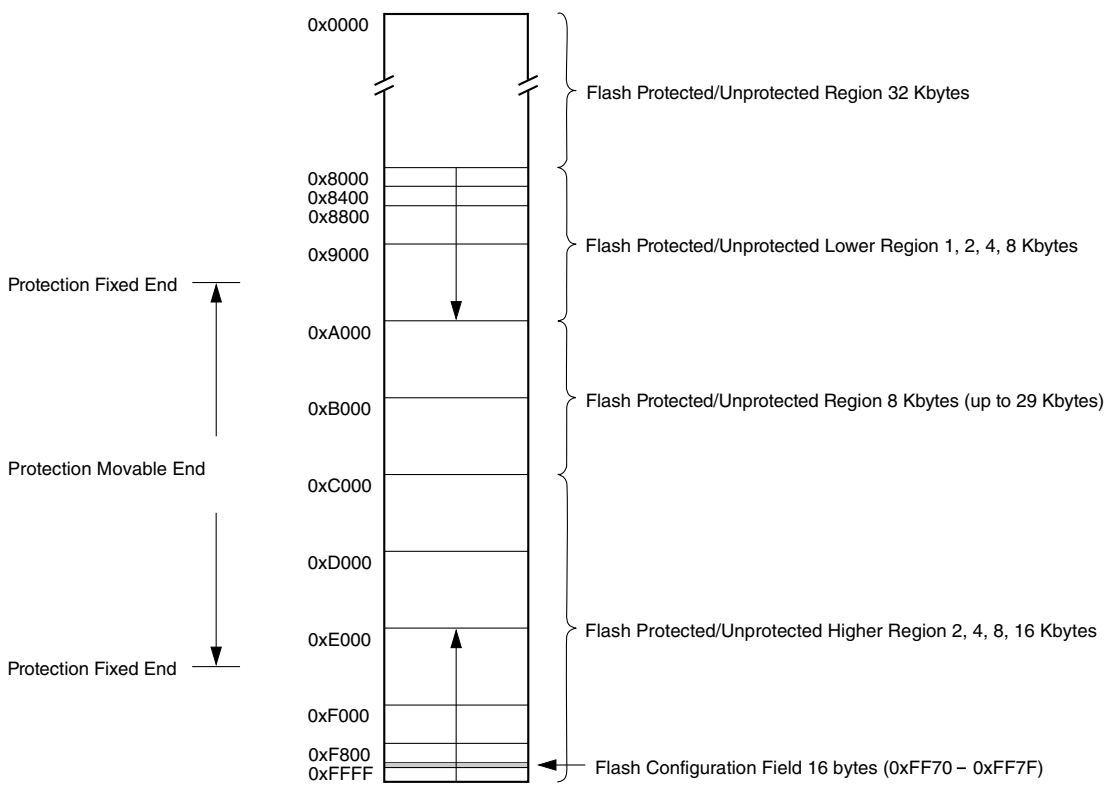


Figure 4-5. Flash protection memory map

Default protection settings as well as security information that allows the MCU to restrict access to the flash module are stored in the flash configuration field as described in the table below.

Table 4-11. Flash configuration field

Global address	Size (Bytes)	Description
0xFF70 — 0xFF77	8	Backdoor comparison key. See Verify backdoor access key command and Unsecuring the MCU using backdoor key access.
0xFF78 — 0xFF7B[1]	4	Reserved
0xFF7C[1]	1	Flash protection byte
0xFF7D[1]	1	EEPROM protection byte
0xFF7E[1]	1	Flash nonvolatile byte
0xFF7F[1]	1	Flash security byte

1. 0xFF78–0xFF7F for a flash phrase and must be programmed in a single command write sequence. Each byte in the 0xFF78-0xFF7B reserved field must be programmed to 0xFF.

The flash and EEPROM module provides protection to the MCU. During the reset sequence, the FPROT register is loaded with the contents of the flash protection byte in the flash configuration field at global address 0xFF7C in flash memory. The protection functions depend on the configuration of bit settings in FPORT register.

Table 4-12. Flash protection function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No flash protection
1	1	0	Protected low range
1	0	1	Protected high range
1	0	0	Protected high and low ranges
0	1	1	Full p-flash memory protected
0	1	0	Unprotected low range
0	0	1	Unprotected high range
0	0	0	Unprotected high and low ranges

1. For range sizes, see Table 4 and Table 5

The flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

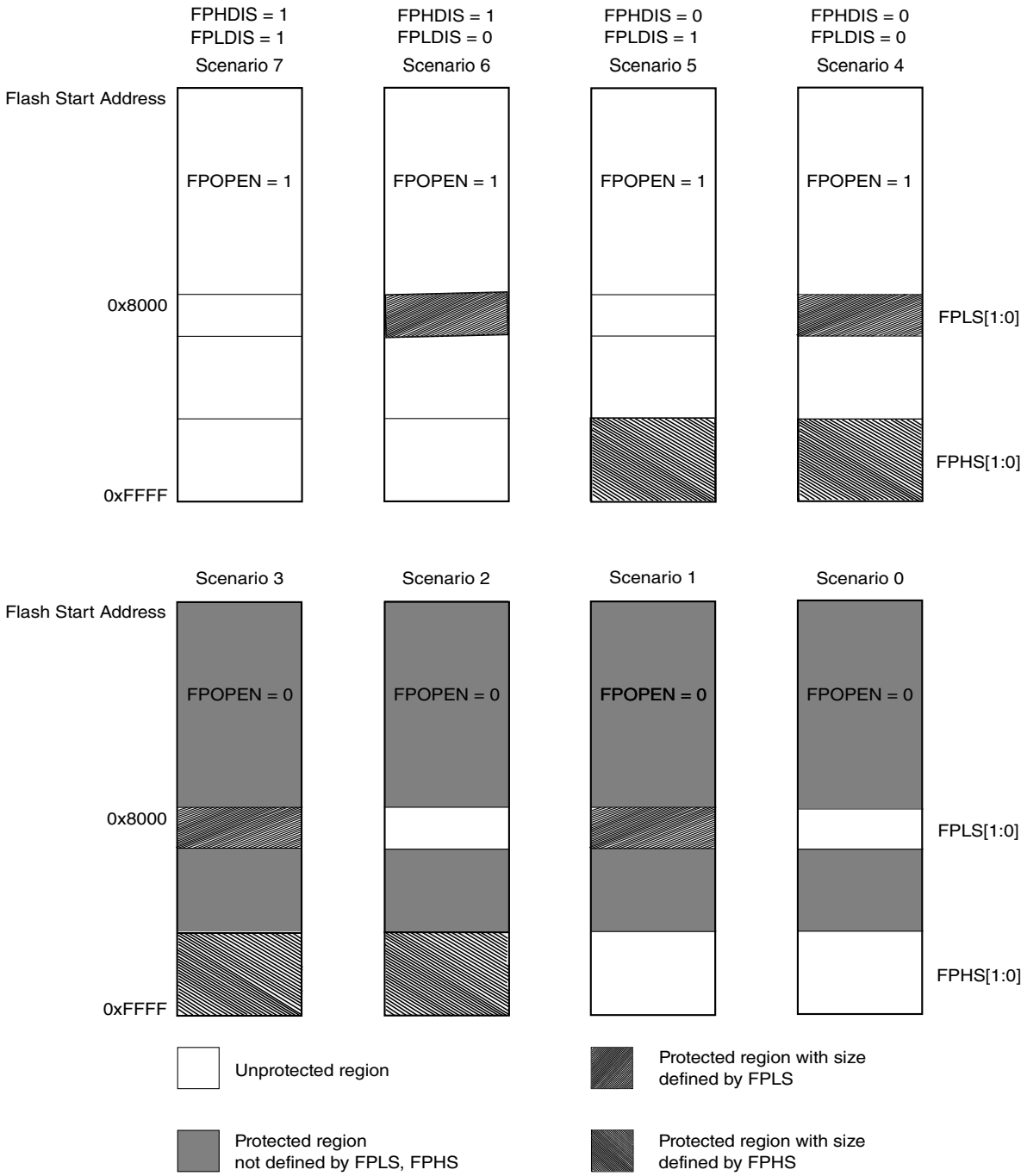


Figure 4-6. Flash protection scenarios

The general guideline is that flash protection can only be added and not removed. The following table specifies all valid transitions between flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPROT[FPHS] and FPROT[FPLS] bit descriptions for additional restrictions.

Table 4-13. Flash protection scenario transitions

From protection scenario	To protection scenario							
	0	1	2	3	4	5	6	7
0	×	×	×	×				
1		×		×				
2			×	×				
3				×				
4				×	×			
5			×	×	×	×		
6		×		×	×		×	
7	×	×	×	×	×	×	×	×

The flash protection address range is listed in the following two tables regarding the scenarios in the table above.

Table 4-14. Flash protection higher address range

FPHS[1:0]	Global address range	Protected size
00	0xF800 – 0xFFFF	2 Kbytes
01	0xF000 – 0xFFFF	4 Kbytes
10	0xE000 – 0xFFFF	8 Kbytes
11	0xC000 – 0xFFFF	16 Kbytes

Table 4-15. Flash protection lower address range

FPLS[1:0]	Global address range	Protected size
00	0x8000 – 0x83FF	1 Kbytes
01	0x8000 – 0x87FF	2 Kbytes
10	0x8000 – 0x8FFF	4 Kbytes
11	0x8000 – 0x9FFF	8 Kbytes

During the reset sequence, fields NVM_EEPROT[DPOPEN] and NVM_EEPROT[DPS] are loaded with the contents of the EEPROM protection byte in the flash configuration field at global address 0xFF7D located in flash memory. EEPROM protection address range is specified by the NVM_EEPROT[DPS].

Table 4-16. EEPROM protection address range

DPS[2:0]	Global address range	Protected size
000	0x3100 – 0x311F	32 bytes
001	0x3100 – 0x313F	64 bytes
010	0x3100 – 0x315F	96 bytes

Table continues on the next page...

Table 4-16. EEPROM protection address range (continued)

DPS[2:0]	Global address range	Protected size
011	0x3100 – 0x317F	128 bytes
100	0x3100 – 0x319F	160 bytes
101	0x3100 – 0x31BF	192 bytes
110	0x3100 – 0x31DF	224 bytes
111	0x3100 – 0x31FF	256 bytes

All possible flash protection scenarios are shown in Figure 4-6. Although the protection scheme is loaded from the flash memory at global address 0xFF7C during the reset sequence, it can be changed by the user.

4.5.2.7 Security

The flash and EEPROM module provides security information to the MCU. The flash security state is defined by the NVM_FSEC[SEC] bits. During reset, the flash module initializes the NVM_FSEC register using data read from the security byte of the flash and EEPROM configuration field at global address 0xFF7F. The security state out of reset can be permanently changed by programming the security byte, assuming that the MCU is starting from a mode where the necessary flash and EEPROM erase and program commands are available and that the upper region of the flash is unprotected. If the flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using backdoor key access
- Unsecuring the MCU using BDM
- Mode and security effects on flash and EEPROM command availability

4.5.2.7.1 Unsecuring the MCU using backdoor key access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys, which are four 16-bit words programmed at addresses 0xFF70–0xFF77. If the KEYEN[1:0] bits are in the enabled state, the verify backdoor access key command – see Verify backdoor access key command, allows the user to present four prospective keys for comparison to the keys stored in the flash and EEPROM memory via the memory controller. If the keys presented in the verify backdoor access key command match the backdoor keys stored in

the flash and EEPROM memory, the FSEC[SEC] bits will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, flash memory and EEPROM memory will not be available for read access and will return invalid data.

The user code stored in the flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state, the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the verify backdoor access key command as explained in Verify backdoor access key command.
2. If the verify backdoor access key command is successful, the MCU is unsecured and the FSEC[SEC] bits are forced to the unsecure state of 10.

The verify backdoor access key command is monitored by the memory controller and an illegal key will prohibit future use of the verify backdoor access key command. A reset of the MCU is the only method to re-enable the verify backdoor access key command. The security as defined in the flash and EEPROM security byte (0xFF7F) is not changed by using the verify backdoor access key command sequence. The backdoor keys stored in addresses 0xFF70–0xFF77 are unaffected by the verify backdoor access key command sequence. The verify backdoor access key command sequence has no effect on the program and erase protections defined in the flash and EEPROM protection register, FPORT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the flash and EEPROM security byte can be erased and the flash and EEPROM security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF70–0xFF77 in the flash configuration field.

4.5.2.7.2 Unsecuring the MCU using BDM

A secured MCU can be unsecured by using the following method to erase the flash and EEPROM memory:

1. Reset the MCU.
2. Set FCDIV register as described in Writing the FCLKDIV register.

3. Configure registers NVM_FERSTAT and NVM_FPROT to disable protection in the flash and EEPROM memory.
4. Execute the erase all blocks command write sequence to erase the flash and EEPROM memory. Alternately, the unsecure NVM command can be executed.

   If the flash and EEPROM memory are verified as erased, the MCU will be unsecured. All BDM. commands will now be enabled and the flash security byte may be programmed to the unsecure state by continuing with the steps that follow.
5. Execute the program flash command write sequence to program the flash security byte to the unsecured state.
6. Reset the MCU.

4.5.2.7.3 Mode and security effects on flash and EEPROM command availability

The availability of flash and EEPROM module commands depends on the MCU operating mode and security state as shown in Table 4-9.

4.5.2.8 Flash and EEPROM commands

4.5.2.8.1 Flash commands

The following table summarizes the valid flash commands as well as the effects of the commands on the flash block and other resources within the flash and EEPROM module.

Table 4-17. Flash commands

FCMD	Command	Function on flash memory
0x01	Erase verify all blocks	Verify that all flash (and EEPROM) blocks are erased
0x02	Erase verify block	Verify that a flash block is erased
0x03	Erase verify flash section	Verify that a given number of words starting at the address provided are erased
0x04	Read Once	Read a dedicated 64 byte field in the nonvolatile information register in flash block that was previously programmed using the program once command
0x06	Program flash	Program up to two longwords in a flash block
0x07	Program once	Program a dedicated 64 byte field in the nonvolatile information register in flash block that is allowed to be programmed only once
0x08	Erase all block	Erase all flash and EEPROM blocks An erase of all flash blocks is possible only when the FPROT[FPLDIS], FPROT[FPHDIS], and FPROT[FPOEN] bits and the EEPROT[DPOPEN] bit are set prior to launching the command
0x09	Erase flash block	Erase a flash or EEPROM block

Table continues on the next page...

Table 4-17. Flash commands (continued)

FCMD	Command	Function on flash memory
		An erase of the full flash block is possible only when FPROT[FPLDIS], FPROT[FPHDIS], and FPROT[FPOEN] bits are set prior to launching the command
0x0A	Erase flash sector	Erase all bytes in a flash sector
0x0B	Unsecure flash	Supports a method of releasing MCU security by erasing all flash (and EEPROM) blocks and verifying that all flash (and EEPROM) blocks are erased
0x0C	Verify backdoor access key	Supports a method of releasing MCU security by verifying a set of security keys
0x0D	Set user margin level	Specifies a user margin read level for all flash blocks

4.5.2.8.2 EEPROM commands

The following table summarizes the valid EEPROM commands along with the effects of the commands on the EEPROM block.

Table 4-18. EEPROM commands

FCMD	Command	Function on flash memory
0x01	Erase verify all blocks	Verify that all EEPROM (and flash) blocks are erased.
0x02	Erase verify block	Verify that an EEPROM block is erased.
0x08	Erase all block	Erase all EEPROM and flash blocks An erase of all EEPROM blocks is possible only when the FPROT[FPLDIS], FPROT[FPHDIS], and FPROT[FPOEN] bits and the DPOPEN bit in the EEPORT register are set prior to launching the command.
0x09	Erase EEPROM Block	Erase a EEPROM and flash block An erase of the full flash block is possible only when FPROT[FPLDIS], FPROT[FPHDIS] and FPROT[FPOPEN] bits are set prior to launching the command.
0x0B	Unsecure EEPROM	Supports a method of releasing MCU security by erasing all EEPROM and flash blocks and verifying that all EEPROM and flash blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for all flash blocks.
0x10	Erase Verify EEPROM Section	Verify that a given number of bytes starting at the address provided are erased.
0x11	Program EEPROM	Program up to four bytes in the EEPROM block.
0x12	Erase EEPROM Sector	Erase all bytes in a sector of the EEPROM block.

4.5.2.8.3 Allowed simultaneous flash and EEPROM operations

Only the operations marked 'OK' in the following table are permitted to be run simultaneously on the flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting flash reads while program and erase operations execute on the EEPROM, providing read (flash) while write (EEPROM) functionality.

Table 4-19. Allowed simultaneous flash and EEPROM operations

Program flash	EEPROM				
	Read	Margin read	Program	Sector erase	Mass erase
Read		OK	OK	OK	
Margin Read[1]					
Program					
Sector Erase					
Mass Erase[2]					OK

1. A 'Margin read' is any read after executing the margin setting commands 'Set user margin level' or 'Set field margin level' with anything but the 'normal' level specified. See the Note on margin settings in
2. The 'Mass erase' operations are commands 'Erase all blocks' and 'Erase flash block'

4.5.2.9 Flash and EEPROM command summary

This section provides details of all available flash commands launched by a command write sequence. The FSTAT[ACCERR] bit will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the memory controller:

- Starting any command write sequence that programs or erases flash memory before initializing the FLCKDIV register.
- Writing an invalid command as part of the command write sequence.
- For additional possible errors, refer to the error handling table provided for each command.

If a flash block is read during the execution of an algorithm (FSTAT[CCIF] = 0) on that same block, the read operation will return invalid data if both flags FERSTAT[SFDIF] and FERSTAT[DFDIF] are set. If the FERSTAT[SFDIF] or FERSTAT[DFDIF] flags were not previously set when the invalid read operation occurred, both the FERSTAT[SFDIF] and FERSTAT[DFDIF] flags will be set.

If the FSTAT[ACCERR] or FSTAT[FPVIOL] bits are set, the user must clear these bits before starting any command write sequence.

CAUTION

An EEPROM byte or flash longword must be in the erased state before being programmed. Cumulative programming of bits within an EEPROM byte or flash longword is not allowed.

4.5.2.9.1 Erase verify all blocks command

The erase verify all blocks command will verify that all flash and EEPROM blocks have been erased.

Table 4-20. Erase verify all blocks command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x01	Not required

Upon clearing NVM_FSTAT[CCIF] to launch the erase verify all blocks command, the memory controller will verify that the entire flash memory space is erased. The NVM_FSTAT[CCIF] flag will set after the erase verify all blocks operation has completed. If all blocks are not erased, it means blank check failed and both NVM_FSTAT[MGSTAT] bits will be set.

Table 4-21. Erase verify all blocks command error handling

Register	Error bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[1] or if blank check failed
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed

1. As found in the memory map for NVM

4.5.2.9.2 Erase verify block command

The erase verify block command allows the user to verify that an entire flash or EEPROM block has been erased. The FCCOB global address [23:0] bits determine which block must be verified.

Table 4-22. Erase verify block command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x02	Global address [23:16] to identify Flash block[1]
001	Global address [15:0] in flash block to be verified	

1. Global address [23] selects between flash (0) or EEPROM (1) block, that can otherwise eventually share the same address on the MCU global memory map.

Upon clearing NVM_FSTAT[CCIF] to launch the erase verify block command, the memory controller will verify that the selected flash or EEPROM block is erased. The NVM_FSTAT[CCIF] flag will set after the erase verify block operation has completed. If the block is not erased, it means blank check failed and both NVM_FSTAT[MGSTAT] bits will be set.

Table 4-23. Erase verify block command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid global address [23:0] is supplied[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed

1. As found in the memory map for NVM

4.5.2.9.3 Erase verify flash section command

The erase verify flash section command will verify that a section of code in the flash memory is erased. The erase verify flash section command defines the starting point of the code to be verified and the number of longwords.

Table 4-24. Erase verify flash section command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x03	Global address [23:16] of flash block
001	Global address [15:0] of the first longwords to be verified	
010	Number of long words to be verified	

Upon clearing NVM_FSTAT[CCIF] to launch the erase verify flash section command, the memory controller will verify that the selected section of flash memory is erased. The NVM_FSTAT[CCIF] flag will set after the erase verify flash section operation has completed. If the section is not erased, it means blank check failed and both FSTAT[MGSTAT] bits will be set.

Table 4-25. Erase verify flash section command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch

Table continues on the next page...

Table 4-25. Erase verify flash section command error handling (continued)

Register	Error bit	Error condition
		Set if command not available in current mode (see Table 4-9)
		Set if an invalid global address [23:0] is supplied (see Table 4-6)[1]
		Set if a misaligned long words address is supplied (global address[1:0] != 00)
		Set if the requested section crosses flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed

1. As defined by the memory map for NVM
2. As found in the memory map for NVM

4.5.2.9.4 Read once command

The read once command provides read access to a reserved 64 byte field (8 phrase) located in the nonvolatile information register of flash. The read once field can only be programmed once and can not be erased. It can be used to store the product ID or any other information that can be written only once. It is programmed using the program once command described in Program once command. To avoid code runaway, the read once command must not be executed from the flash block containing the program once reserved field.

Table 4-26. Read once command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x04	Not required
001	Read once phrase index (0x0000 – 0x0007)	
010	Read once word 0 value	
011	Read once word 1 value	
100	Read once word 2 value	
101	Read once word 3 value	

Upon clearing FSTAT[CCIF] to launch the read once command, a read once phrase is fetched and stored in the FCCOB indexed register. The FSTAT[CCIF] flag will set after the read once operation has completed. Valid phrase index values for the read once command range from 0x0000 to 0x0007. During execution of the read once command, any attempt to read addresses within flash block will return invalid data.

Table 4-27. Read once command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command is not available in current mode (see Table 4-9)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

4.5.2.9.5 Program flash command

The program flash operation will program up to two previously erased longwords in the flash memory using an embedded algorithm.

Note

A flash phrase must be in the erased state before being programmed. Cumulative programming of bits within a flash phrase is not allowed.

Table 4-28. Program flash command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x06	Global address [23:16] to identify flash block
001	Global address [15:0] of longwords location to be programmed[1]	
010	Word 0 (longword 0) program value	
011	Word 1 (longword 0) program value	
100	Word 2 (longword 1) program value	
101	Word 3 (longword 1) program value	

1. Global address [1:0] must be 00.

Upon clearing NVM_FSTAT[CCIF] to launch the program flash command, the memory controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The NVM_FSTAT[CCIF] flag will set after the program flash operation has completed.

Table 4-29. Program flash command error handling

Register	Error bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 011 or 101 at command launch
		Set if command not available in current mode (see Table 4-9)
		Set if an invalid global address [23:0] is supplied (see Table 4-6)[1]

Table continues on the next page...

Table 4-29. Program flash command error handling (continued)

Register	Error bit	Error condition
		Set if a misaligned longword address is supplied (global address [1:0] != 00)
		Set if the requested group of words breaches the end of the flash block.
	FPVIOL	Set if the global address [23:0] points to a protected data
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1. As defined by the memory map of NVM

4.5.2.9.6 Program once command

The program once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in flash. The program once reserved field can be read using the read once command as described in Read once command. The program once command must be issued only because the nonvolatile information register in flash cannot be erased. To avoid code runaway, the read once command must not be executed from the flash block containing the program once reserved field.

Table 4-30. Program once command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x07	Not required
001	Program Once phrase index (0x000 – 0x0007)	
010	Program once Word 0 value	
011	Program once Word 1value	
100	Program once Word 2 value	
101	Program once Word 3 value	

Upon clearing FSTAT[CCIF] to launch the program once command, the memory controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The FSTAT[CCIF] flag will remain clear, setting only after the program once operation has completed.

The reserved nonvolatile information register accessed by the program once command cannot be erased, and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the program once command range from 0x0000 to 0x0007. During execution of the program once command, any attempt to read addresses within flash will return invalid data.

Table 4-31. Program once command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 4-9)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1. If a program once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the program once command will be allowed to execute again on that same phrase.

4.5.2.9.7 Erase all blocks command

The erase all blocks operation will erase the entire flash and EEPROM memory space.

Table 4-32. Erase all blocks command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x08	Not required

Upon clearing NVM_FSTAT[CCIF] to launch the erase all blocks command, the memory controller will erase the entire NVM memory space and verify that it is erased. If the memory controller verifies that the entire NVM memory space was properly erased, security will be released. Therefore, the device is in unsecured state. During the execution of this command (NVM_FSTAT[CCIF] = 0) the user must not write to any NVM module register. The NVM_FSTAT[CCIF] flag will set after the erase all blocks operation has completed.

Table 4-33. Erase all blocks command error handling

Register	Error bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 000 at command launch
		Set if command not available in current mode (see Table 4-9)
	FPVIOL	Set if any area of the flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[1]

1. As found in the memory map for NVM

4.5.2.9.8 Erase flash block command

The erase flash block operation will erase all addresses in a flash or EEPROM block.

Table 4-34. Erase flash block command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x09	Global address [23:16] to identify flash block[1]
001	Global address[15:0] in flash block to be erased	

1. Global address [23] selects between flash (0) or EEPROM (1) block, that can otherwise eventually share the same address on the MCU global memory map.

Upon clearing FSTAT[CCIF] to launch the erase flash block command, the memory controller will erase the selected flash block and verify that it is erased. The FSTAT[CCIF] flag will set after the erase flash block operation has completed.

Table 4-35. Erase flash block command error handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 4-9)
		Set if an invalid global address [23:16] is supplied[1]
	FPVIOL	Set if an area of the selected flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[2]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[2]

1. As defined by the memory map for NVM
2. As found in the memory map for NVM

4.5.2.9.9 Erase flash sector command

The erase flash sector operation will erase all addresses in a flash sector.

Table 4-36. Erase flash sector command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x0A	Global address [23:16] to identify flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Overview for the flash sector size	

Upon clearing FSTAT[CCIF] to launch the erase flash sector command, the memory controller will erase the selected flash sector and then verify that it is erased. The FSTAT[CCIF] flag will be set after the erase flash sector operation has completed.

Table 4-37. Erase flash sector command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 4-9)
		Set if an invalid global address [23:16] is supplied.[1] (see Table 4-6)
		Set if a misaligned longword address is supplied (global address [1:0] != 00)
	FPVIOL	Set if the selected flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1. As defined by the memory map for NVM

4.5.2.9.10 Unsecure flash command

The unsecure flash command will erase the entire flash and EEPROM memory space, and if the erase is successful, will release security.

Table 4-38. Unsecure flash command FCCOB requirements

CCOBIX[2:0]	FCCOB parameters	
000	0x0B	Not required

Upon clearing FSTAT[CCIF] to launch the unsecure flash command, the memory controller will erase the entire flash and EEPROM memory space and verify that it is erased. If the memory controller verifies that the entire flash and EEPROM memory space was properly erased, security will be released. If the erase verify is not successful, the unsecure flash operation sets FSTAT[MGSTAT1] and terminates without changing the security state. During the execution of this command (FSTAT[CCIF] = 0), the user must not write to any flash and EEPROM module register. The FSTAT[CCIF] flag is set after the unsecure flash operation has completed.

Table 4-39. Unsecure flash command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command is not available in current mode (see Table 4-9)
	FPVIOL	Set if any area of the flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[1]

1. As found in the memory map for NVM

4.5.2.9.11 Verify backdoor access key command

The verify backdoor access key command will execute only if it is enabled by the NVM_FSEC[KEYEN] bits. The verify backdoor access key command releases security if user-supplied keys match those stored in the flash security bytes of the flash configuration field. See Table 4-6 for details. The code that performs verifying backdoor access command must be running from RAM or EEPROM.

Table 4-40. Verify backdoor access key command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing NVM_FSTAT[CCIF] to launch the verify backdoor access key command, the memory controller will check the NVM_FSEC[KEYEN] bits to verify that this command is enabled. If not enabled, the memory controller sets the NVM_FSTAT[ACCERR] bit. If the command is enabled, the memory controller compares the key provided in FCCOB to the backdoor comparison key in the flash configuration field with Key 0 compared to 0xFF70, and so on. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the verify backdoor access key command are aborted (set NVM_FSTAT[ACCERR]) until a reset occurs. The NVM_FSTAT[CCIF] flag is set after the verify backdoor access key operation has completed.

Table 4-41. Verify backdoor access key command error handling

Register	Error bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] ≠ 10
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

4.5.2.9.12 Set user margin level command

The user margin is a small delta to the normal read reference level and, in effect, is a minimum safety margin. That is, if the reads pass at the tighter tolerances of the user margins, the normal reads have at least that much safety margin before users experience data loss.

The set user margin level command causes the memory controller to set the margin level for future read operations of the flash or EEPROM block.

Table 4-42. Set user margin level command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x0D	Global address [23:16] to identify flash block[1]
001	Global address [15:0] to identify flash block	
010	Margin level setting	

1. Global Address [23] selects between flash (0) or EEPROM (1) block, that can otherwise eventually share the same address on the MCU global memory map.

Upon clearing NVM_FSTAT[CCIF] to launch the set user margin level command, the memory controller will set the user margin level for the targeted block and then set the NVM_FSTAT[CCIF] flag.

Note

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the Flash block is targeted, the flash user margin levels are applied to both Flash and EEPROM reads. It is not possible to apply user margin levels to the flash block only.

Valid margin level settings for the set user margin level command are defined in the following tables.

Table 4-43. Valid set user margin level settings

CCOB (CCOBIX = 010)	Level description
0x0000	Return to normal level
0x0001	User margin-1 level[1]
0x0002	User margin-0 level[2]

1. Read margin to the erased state
2. Read margin to the programmed state

Table 4-44. Set user margin level command error handling

Register	Error bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command is not available in current mode (see Table 4-9)
		Set if an invalid global address [23:0] is supplied
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

Note

User margin levels can be used to check that NVM memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking NVM memory contents at user margin levels, a potential loss of information has been detected.

4.5.2.9.13 Erase verify EEPROM section command

The erase verify EEPROM section command will verify that a section of code in the EEPROM is erased. The erase verify EEPROM section command defines the starting point of the data to be verified and the number of bytes.

Table 4-45. Erase verify EEPROM section command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x10	Global address [23:16] to identify the EEPROM block
001	Global address [15:0] of the first byte to be verified	
010	Number of bytes to be verified	

Upon clearing NVM_FSTAT[CCIF] to launch the erase verify that EEPROM section command, the memory controller will verify the selected section of EEPROM memory is erased. The NVM_FSTAT[CCIF] flag will set after the erase verify EEPROM section operation has completed. If the section is not erased, which means that blank check failed, both NVM_FSTAT[MGSTAT] bits will be set.

Table 4-46. Erase verify EEPROM section command error handling

Register	Error bit	Error condition
FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 010 at command launch
		Set if command is not available in current mode (see Table 4-9)

Table continues on the next page...

Table 4-46. Erase verify EEPROM section command error handling (continued)

Register	Error bit	Error condition
		Set if an invalid global address [23:0] is supplied
		Set if the requested section breaches the end of the EEPROM block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or it blank check failed.

4.5.2.9.14 Program EEPROM command

The program EEPROM operation programs one to four previously erased bytes in the EEPROM block. The program EEPROM operation will confirm that the targeted location(s) were successfully programmed upon completion.

Note

A EEPROM byte must be in the erased state before being programmed. Cumulative programming of bits within a EEPROM byte is not allowed.

Table 4-47. Program EEPROM command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x11	Global address [23:16] to identify the EEPROM block
001	Global address [15:0] of the first word to be verified	
010		Byte 0 program value
011		Byte 1 program value, if desired
100		Byte 2 program value, if desired
101		Byte 3 program value, if desired

Upon clearing NVM_FSTAT[CCIF] to launch the program EEPROM command, the user-supplied words will be transferred to the memory controller and be programmed if the area is unprotected. The CCOBIX index value at program EEPROM command launch determines how many bytes will be programmed in the EEPROM block. The NVM_FSTAT[CCIF] flag is set when the operation has completed.

Table 4-48. Program EEPROM command error handling

Register	Error Bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] >101 at command launch

Table continues on the next page...

Table 4-48. Program EEPROM command error handling (continued)

Register	Error Bit	Error condition
		Set if command is not available in current mode (see Table 4-9)
		Set if an invalid global address [23:0] is supplied
		Set if the requested group of words breaches the end of the EEPROM block
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

4.5.2.9.15 Erase EEPROM sector command

The erase EEPROM sector operation will erase all addresses in a sector of the EEPROM block.

Table 4-49. Erase EEPROM sector command FCCOB requirements

CCOBIX[2:0]	NVM_FCCOBHI parameters	NVM_FCCOBLO parameters
000	0x12	Global address [23:16] to identify EEPROM block
001	Global address [15:0] anywhere within the sector to be erased. See Overview for EEPROM sector size	

Upon clearing NVM_FSTAT[CCIF] to launch the erase EEPROM sector command, the memory controller will erase the selected EEPROM sector and verify that it is erased. The NVM_FSTAT[CCIF] flag will set after the erase EEPROM sector operation has completed.

Table 4-50. Erase EEPROM sector command error handling

Register	Error bit	Error condition
NVM_FSTAT	ACCERR	Set if CCOBIX[2:0] ≠ 001 at command launch
		Set if command is not available in current mode (see Table 4-9)
		Set if an invalid global address [23:0] is supplied (see Table 4-6)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

4.6 Flash and EEPROM registers descriptions

The flash module contains a set of 16 user control and status registers located between 0x3020 and 0x302F. In the case of the writable registers, the write accesses are forbidden during flash command execution. For more details, see Caution note in Flash and EEPROM memory map. A summary of the flash module registers is given in the following table with detailed descriptions in the following subsections.

NVM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3020	Flash Clock Divider Register (NVM_FCLKDIV)	8	R/W	00h	4.6.1/107
3021	Flash Security Register (NVM_FSEC)	8	R	Undefined	4.6.2/108
3022	Flash CCOB Index Register (NVM_FCCOBIX)	8	R/W	00h	4.6.3/109
3024	Flash Configuration Register (NVM_FCNFG)	8	R/W	00h	4.6.4/109
3025	Flash Error Configuration Register (NVM_FERCNFG)	8	R/W	00h	4.6.5/110
3026	Flash Status Register (NVM_FSTAT)	8	R/W	80h	4.6.6/111
3027	Flash Error Status Register (NVM_FERSTAT)	8	R/W	00h	4.6.7/112
3028	Flash Protection Register (NVM_FPROT)	8	R/W	Undefined	4.6.8/113
3029	EEPROM Protection Register (NVM_EEPROT)	8	R/W	Undefined	4.6.9/114
302A	Flash Common Command Object Register:High (NVM_FCCOBHI)	8	R/W	00h	4.6.10/116
302B	Flash Common Command Object Register: Low (NVM_FCCOBLO)	8	R/W	00h	4.6.11/116
302C	Flash Option Register (NVM_FOPT)	8	R/W	Undefined	4.6.12/116

4.6.1 Flash Clock Divider Register (NVM_FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

NOTE

The FCLKDIV register must not be written while a flash command is executing (NVM_FSTAT[CCIF] = 0)

Address: 3020h base + 0h offset = 3020h

Bit	7	6	5	4	3	2	1	0
Read	FDIVLD	FDIVLCK	FDIV					
Write								
Reset	0	0	0	0	0	0	0	0

NVM_FCLKDIV field descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset. 1 FCLKDIV register has been written since the last reset.
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing. 1 FDIV value is locked and cannot be changed. After the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in user mode.
FDIV	Clock Divider Bits FDIV[5:0] must be set to effectively divide BUSCLK down to 1MHz to control timed events during flash program and erase algorithms. Refer to the table in the Writing the FCLKDIV register for the recommended values of FDIV based on the BUSCLK frequency.

4.6.2 Flash Security Register (NVM_FSEC)

The FSEC register holds all bits associated with the security of the MCU and NVM module. All bits in the FSEC register are readable but not writable. During the reset sequence, the FSEC register is loaded with the contents of the flash security byte in the flash configuration field at global address 0xFF7F located in flash memory.

See Security for security function.

Address: 3020h base + 1h offset = 3021h

Bit	7	6	5	4	3	2	1	0
Read	KEYEN		Reserved				SEC	
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

NVM_FSEC field descriptions

Field	Description
7–6 KEYEN	Backdoor Key Security Enable Bits The KEYEN[1:0] bits define the enabling of backdoor key access to the flash module. **NOTE:** 01 is the preferred KEYEN state to disable backdoor key access. 00 Disabled 01 Disabled 10 Enabled 11 Disabled

Table continues on the next page...

NVM_FSEC field descriptions (continued)

Field	Description
5–2 Reserved	This field is reserved.
SEC	Flash Security Bits The SEC[1:0] bits define the security state of the MCU. If the flash module is unsecured using backdoor key access, the SEC bits are forced to 10. **NOTE:** 00 is the preferred SEC state to set MCU to secured state. 00 Secured 01 Secured 10 Unsecured 11 Secured

4.6.3 Flash CCOB Index Register (NVM_FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for NVM memory operations.

Address: 3020h base + 2h offset = 3022h

Bit	7	6	5	4	3	2	1	0
Read	0					CCOBIX		
Write								
Reset	0	0	0	0	0	0	0	0

NVM_FCCOBIX field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CCOBIX	Common Command Register Index The CCOBIX bits are used to select which word of the FCCOB register array is being read or written to.

4.6.4 Flash Configuration Register (NVM_FCNFG)

The FCNFG register enables the flash command complete interrupt and forces ECC faults on flash array read access from the CPU.

Address: 3020h base + 4h offset = 3024h

Bit	7	6	5	4	3	2	1	0
Read	CCIE	0		IGNSF	0		FDFD	FSFD
Write								
Reset	0	0	0	0	0	0	0	0

NVM_FCNFG field descriptions

Field	Description
7 CCIE	Command Complete Interrupt Enable The CCIE bit controls interrupt generation when a flash command has completed. 0 Command complete interrupt disabled. 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 IGNSF	Ignore Single Bit Fault The IGNSF controls single bit fault reporting in the FERSTAT register. 0 All single bit faults detected during array reads are reported. 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated.
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 FDFD	Force Double Bit Fault Detect The FDFD bit allows the user to simulate a double bit fault during flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. 0 Flash array read operations will set the FERSTAT[DFDIF] flag only if a double bit fault is detected. 1 Any flash array read operation will force the FERSTAT[DFDIF] flag to be set and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set.
0 FSFD	Force Single Bit Fault Detect The FSFD bit allows the user to simulate a single bit fault during flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected. 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set.

4.6.5 Flash Error Configuration Register (NVM_FERCNFG)

The FERCNFG register enables the flash error interrupts for the FERSTAT flags.

Address: 3020h base + 5h offset = 3025h

Bit	7	6	5	4	3	2	1	0
Read	0						DFDIE	SFDIE
Write								
Reset	0	0	0	0	0	0	0	0

NVM_FERCNFG field descriptions

Field	Description
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 DFDIE	Double Bit Fault Detect Interrupt Enable The DFDIE bit controls interrupt generation when a double bit fault is detected during a flash block read operation. 0 DFDIF interrupt disabled. 1 An interrupt will be requested whenever the DFDIF flag is set.
0 SFDIE	Single Bit Fault Detect Interrupt Enable The SFDIE bit controls interrupt generation when a single bit fault is detected during a flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set. 1 An interrupt will be requested whenever the SFDIF flag is set.

4.6.6 Flash Status Register (NVM_FSTAT)

The FSTAT register reports the operational status of the flash and EEPROM module.

Address: 3020h base + 6h offset = 3026h

Bit	7	6	5	4	3	2	1	0
Read	CCIF	0	ACCERR	FPVIOL	MGBUSY	0	MGSTAT	
Write								
Reset	1	0	0	0	0	0	0	0

NVM_FSTAT field descriptions

Field	Description
7 CCIF	Command Complete Interrupt Flag The CCIF flag indicates that a flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress. 1 Flash command has completed.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 ACCERR	Flash Access Error Flag The ACCERR bit indicates an illegal access has occurred to the flash memory caused by either a violation of the command write sequence or issuing an illegal flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR.

Table continues on the next page...

NVM_FSTAT field descriptions (continued)

Field	Description
	0 No access error detected. 1 Access error detected.
4 FPVIOL	Flash Protection Violation Flag The FPVIOL bit indicates an attempt was made to program or erase an address in a protected area of flash or EEPROM memory during a command write sequence. The FPVIOL bit is cleared by writing a 1 to FPVIOL. Writing a 0 to the FPIOL bit has no effect on FPIOL. While FPIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected. 1 Protection violation detected.
3 MGBUSY	Memory Controller Busy Flag The MGBUSY flag reflects the active state of the memory controller. 0 Memory controller is idle. 1 Memory controller is busy executing a flash command (CCIF = 0).
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
MGSTAT	Memory Controller Command Completion Status Flag One or more MGSTAT flag bits are set if an error is detected during execution of a flash command or during the flash reset sequence. **NOTE:** Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence.

4.6.7 Flash Error Status Register (NVM_FERSTAT)

The FERSTAT register reflects the error status of internal flash and EEPROM operations.

Address: 3020h base + 7h offset = 3027h

Bit	7	6	5	4	3	2	1	0
Read	0						DFDIF	SFDIF
Write								
Reset	0	0	0	0	0	0	0	0

NVM_FERSTAT field descriptions

Field	Description
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 DFDIF	Double Bit Fault Detect Interrupt Flag The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a flash array read operation or that a flash array read operation returning invalid data was

Table continues on the next page...

NVM_FERSTAT field descriptions (continued)

Field	Description
	attempted on a flash block that was under a flash command operation. The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF. **NOTE:** The single bit fault and double bit fault flags are mutually exclusive for parity errors, meaning that an ECC fault occurrence can be either single fault or double fault but never both. A simultaneous access collision, when the flash array read operation is returning invalid data attempted while a command is running, is indicated when both SFDIF and DFDIF flags are high. **NOTE:** There is a one cycle delay in storing the ECC DFDIF and SFDIF fault flags in the register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of EEC errors. 0 No double bit fault detected. 1 Double bit fault detected or a flash array read operation returning invalid data was attempted while command running.
0 SFDIF	Single Bit Fault Detect Interrupt Flag With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a flash array read operation or that a flash array read operation returning invalid data was attempted on a flash block that was under a flash command operation. The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SRFDIF. 0 No single bit fault detected. 1 Single bit fault detected and corrected or a flash array read operation returning invalid data was attempted while command running.

4.6.8 Flash Protection Register (NVM_FPROT)

The FPROT register defines which flash sectors are protected against program and erase operations.

The unreserved bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see Protection).

During the reset sequence, the FPROT register is loaded with the contents of the flash protection byte in the flash configuration field at global address 0xFF7C located in flash memory. To change the flash protection that will be loaded during the reset sequence, the upper sector of the flash memory must be unprotected, then the flash protection byte must be reprogrammed.

Trying to alter data in any protected area in the flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a flash block is not possible if any of the flash sectors contained in the same flash block are protected.

Address: 3020h base + 8h offset = 3028h

Bit	7	6	5	4	3	2	1	0
Read	FPOPEN	1	FPHDIS	FPHS		FPLDIS	FPLS	
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

NVM_FPROT field descriptions

Field	Description
7 FPOPEN	Flash Protection Operation Enable The FPOPEN bit determines the protection function for program or erase operations. 0 When FPOPEN is clear, the FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS and FPLS bits. 1 When FPOPEN is set, the FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS and FPLS bits.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 1.
5 FPHDIS	Flash Protection Higher Address Range Disable The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the flash memory ending with global address 0xFFFF. 0 Protection/Unprotection enabled. 1 Protection/Unprotection disabled.
4–3 FPHS	Flash Protection Higher Address Size The FPHS bits determine the size of the protected/unprotected area in flash memory. The FPHS bits can be written to only while the FPHDIS bit is set.
2 FPLDIS	Flash Protection Lower Address Range Disable The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the flash memory beginning with global address 0x8000. 0 Protection/Unprotection enabled. 1 Protection/Unprotection disabled.
FPLS	Flash Protection Lower Address Size The FPLS bits determine the size of the protected/unprotected area in flash memory. The FPLS bits can only be written to while the FPLIDS bit is set.

4.6.9 EEPROM Protection Register (NVM_EEPROT)

The EEPROT register defines which EEPROM sectors are protected against program and erase operations.

The unreserved bits of the EEPROT register are writable with the restriction that protection can be added but not removed. Writes must increase the DPS value and the DPOPEN bit can only be written from 1, protection disabled, to 0, protection enabled. If the DPOPEN bit is set, the state of the DPS bits is irrelevant.

During the reset sequence, fields DPOPEN and DPS of the EEPROT register are loaded with the contents of the EEPROM protection byte in the flash configuration field at global address 0xFF7D located in flash memory. To change the EEPROM protection that will be loaded during the reset sequence, the flash sector containing the EEPROM protection byte must be unprotected. Then the EEPROM protection byte must be programmed.

Trying to alter data in any protected area in the EEPROM memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the EEPROM memory is not possible if any of the EEPROM sectors are protected.

Address: 3020h base + 9h offset = 3029h

Bit	7	6	5	4	3	2	1	0
Read	DPOPEN	0				DPS		
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

NVM_EEPROT field descriptions

Field	Description
7 DPOPEN	EEPROM Protection Control 0 Enables EEPROM memory protection from program and erase with protected address range defined by DPS bits. 1 Disables EEPROM memory protection from program and erase.
6–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DPS	EEPROM Protection Size These bits determine the size of the protected area in the EEPROM memory.

4.6.10 Flash Common Command Object Register:High (NVM_FCCOBHI)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte-wide reads and writes are allowed to the FCCOB register.

Address: 3020h base + Ah offset = 302Ah

Bit	7	6	5	4	3	2	1	0
Read Write	CCOB							
Reset	0	0	0	0	0	0	0	0

NVM_FCCOBHI field descriptions

Field	Description
CCOB	Common Command Object Bit 15:8 High 8 bits of common command object register

4.6.11 Flash Common Command Object Register: Low (NVM_FCCOBLO)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte-wide reads and writes are allowed to the FCCOB register.

Address: 3020h base + Bh offset = 302Bh

Bit	7	6	5	4	3	2	1	0
Read Write	CCOB							
Reset	0	0	0	0	0	0	0	0

NVM_FCCOBLO field descriptions

Field	Description
CCOB	Common Command Object Bit 7:0 Low 8 bits of common command object register

4.6.12 Flash Option Register (NVM_FOPT)

The FOPT register is the flash option register.

During the reset sequence, the FOPT register is loaded from the flash nonvolatile byte in the flash configuration field at global address 0xFF7E located in flash memory as indicated by reset condition.

Address: 3020h base + Ch offset = 302Ch

Bit	7	6	5	4	3	2	1	0
Read Write	NV							
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

NVM_FOPT field descriptions

Field	Description
NV	Nonvolatile Bits The NV[7:0] bits are available as nonvolatile bits. During the reset sequence, the FOPT register is loaded from the flash nonvolatile byte in the flash configuration field at global address 0xFF7E located in flash memory.

Chapter 5
Interrupts

5.1 Interrupts

Interrupts save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so that processing resumes where it left off before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such as an edge on the IRQ pin or a timer-overflow event. The debug module can also generate an SWI under certain circumstances.

If an event occurs in an enabled interrupt source, an associated read-only status flag will be set. The CPU will not respond unless only the local interrupt enable is a logic 1. The I bit in the CCR is 0 to allow interrupts. The global interrupt mask (I bit) in the CCR is initially set after reset that masks (prevents) all maskable interrupt sources. The user program initializes the stack pointer and performs other system setups before clearing the I bit to allow the CPU to respond to interrupts.

When the CPU receives a qualified interrupt request, it completes the current instruction before responding to the interrupt. The interrupt sequence obeys the same cycle-by-cycle sequence as the SWI instruction and consists of:

- Saving the CPU registers on the stack.
- Setting the I bit in the CCR to mask further interrupts.
- Fetching the interrupt vector for the highest-priority interrupt that is currently pending.
- Filling the instruction queue with the first three bytes of program information starting from the address fetched from the interrupt vector locations.

While the CPU is responding to the interrupt, the I bit is automatically set to prevent another interrupt from interrupting the ISR itself, which is called nesting of interrupts. Normally, the I bit is restored to 0 when the CCR is restored from the value stacked on

entry to the ISR. In rare cases, the I bit may be cleared inside an ISR, after clearing the status flag that generated the interrupt, so that other interrupts can be serviced without waiting for the first service routine to finish. This practice is recommended only for the most experienced programmers because it can lead to subtle program errors that are difficult to debug.

The interrupt service routine ends with a return-from-interrupt (RTI) instruction that restores the CCR, A, X, and PC registers to their pre-interrupt values by reading the previously saved information off the stack.

Note

For compatibility with the M68HC08, the H register is not automatically saved and restored. Push H onto the stack at the start of the interrupt service routine (ISR) and restore it immediately before the RTI that is used to return from the ISR.

When two or more interrupts are pending when the I bit is cleared, the highest priority source is serviced first.

5.1.1 Interrupt stack frame

The following figure shows the contents and organization of a stack frame. Before the interrupt, the stack pointer (SP) points at the next available byte location on the stack. The current values of CPU registers are stored on the stack, starting with the low-order byte of the program counter (PC) and ending with the CCR. After stacking, the SP points at the next available location on the stack, which is the address that is one less than the address where the CCR was saved. The PC value that is stacked is the address of the instruction in the main program that would have executed next if the interrupt had not occurred.

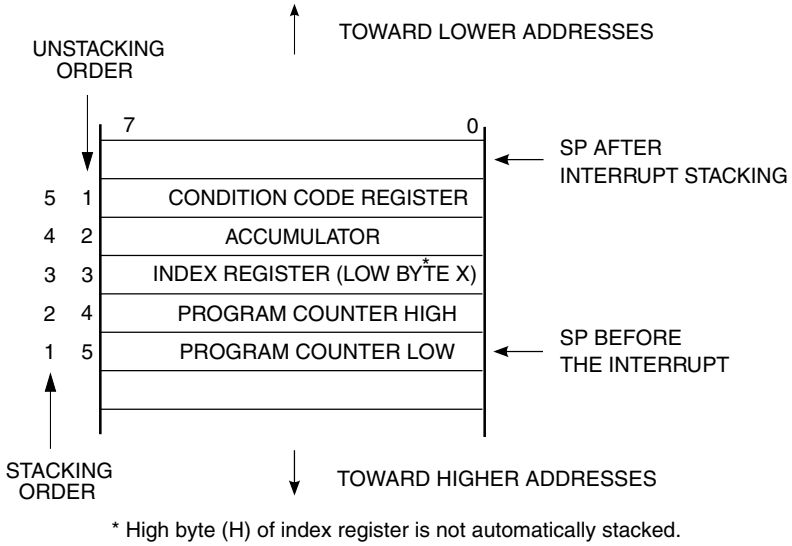


Figure 5-1. Interrupt stack frame

When an RTI instruction executes, these values are recovered from the stack in reverse order. As part of the RTI sequence, the CPU fills the instruction pipeline by reading three bytes of program information, starting from the PC address recovered from the stack.

The status flag causing the interrupt must be acknowledged (cleared) before returning from the ISR. Typically, the flag must be cleared at the beginning of the ISR because if another interrupt is generated by this source it will be registered so that it can be serviced after completion of the current ISR.

5.1.2 Interrupt vectors, sources, and local masks

The following table provides a summary of all interrupt sources. High-priority sources are located toward the bottom of the table. The high-order byte of the address for the interrupt service routine is located at the first address in the vector address column, and the low-order byte of the address for the interrupt service routine is located at the next higher address.

When an interrupt condition occurs, an associated flag bit is set. If the associated local interrupt enable is 1, an interrupt request is sent to the CPU. If the global interrupt mask (I bit in the CCR) is 0, the CPU finishes the current instruction, stacks the PCL, PCH, X, A, and CCR CPU registers, sets the I bit, and then fetches the interrupt vector for the highest priority pending interrupt. Processing then continues in the interrupt service routine.

Table 5-1. Vector summary (from lowest to highest priority)

Vector number	Address (high/ low)	Vector name	Module	Source	Local enable	Description
39	0xFFB0:FFB1	Vnvm	NVM	CCIF DFDIF SFDIF	CCIE	NVM command complete interrupt
38	0xFFB2:FFB3	Vkbi1	KBI1	KBF	KBIE	Keyboard interrupt 1
37	0xFFB4:FFB5	Vkbi0	KBI0	KBF	KBIE	Keyboard interrupt 0
36	0xFFB6:FFB7	Unused	Unused	Unused	Unused	Unused
35	0xFFB8:FFB9	Vrtc	RTC	RTIF	RTIE	RTC overflow
34	0xFFBA:FFBB	Viic	IIC	IICIF	IICIE	IIC
33	0xFFBC:FFBD	Vspi1	SPI1	SPRF MODF SPTEF SPMF	SPIE SPIE SPTIE SPMIE	SPI1 receive SPI1 mode fault SPI1 transmit SPI1 match
32	0xFFBE:FFBF	Vspi0	SPI0	SPRF MODF SPTEF SPMF	SPIE SPIE SPTIE SPMIE	SPI0 receive SPI0 mode fault SPI0 transmit SPI0 match
31	0xFFC0:FFC1	Vsci2tx	SCI2	TRDE TC	TIE TCIE	SCI2 transmit
30	0xFFC2:FFC3	Vsci2rx	SCI2	IDLE RDRF LBKDIF RXEDGIF	ILIE RIE LBKDIE RXEDGIE	SCI2 receive
29	0xFFC4:FFC5	Vsci2err	SCI2	OR NF FE PF	ORIE NEIE FEIE PEIE	SCI2 error
28	0xFFC6:FFC7	Vsci1tx	SCI1	TRDE TC	TIE TCIE	SCI1 transmit
27	0xFFC8:FFC9	Vsci1rx	SCI1	IDLE RDRF LBKDIF RXEDGIF	ILIE RIE LBKDIE RXEDGIE	SCI1 receive
26	0xFFCA:FFCB	Vsci1err	SCI1	OR NF FE PF	ORIE NEIE FEIE PEIE	SCI1 error
25	0xFFCC:FFCD	Vsci0tx	SCI0	TRDE	TIE	SCI0 transmit

Table continues on the next page...

Table 5-1. Vector summary (from lowest to highest priority) (continued)

Vector number	Address (high/ low)	Vector name	Module	Source	Local enable	Description
				TC	TCIE	
24	0xFFCE:FFCF	Vsci0rx	SCI0	IDLE RDRF LBKDIF RXEDGIF	ILIE RIE LBKDIE RXEDGIE	SCI0 receive
23	0xFFD0:FFD1	Vsci0err	SCI0	OR NF FE PF	ORIE NEIE FEIE PEIE	SCI0 error
22	0xFFD2:FFD3	Vadc	ADC	COCO	AIEN	ADC conversion complete interrupt
21	0xFFD4:FFD5	Vacmp	ACMP	ACF	ACIE	Analog comparator interrupt
20	0xFFD6:FFD7	Vmtim1	MTIM1	TOF	TOIE	MTIM1 overflow interrupt
19	0xFFD8:FFD9	Vmtim0	MTIM0	TOF	TOIE	MTIM0 overflow interrupt
18	0xFFDA:FFDB	Vftm0ovf	FTM0	TOF	TOIE	FTM0 overflow
17	0xFFDC:FFDD	Vftm0ch1	FTM0CH1	CH1F	CH1IE	FTM0 channel 1
16	0xFFDE:FFDF	Vftm0ch0	FTM0CH0	CH0F	CH0IE	FTM0 channel 0
15	0xFFE0:FFE1	Vftm1ovf	FTM1	TOF	TOIE	FTM1 overflow
14	0xFFE2:FFE3	Vftm1ch1	FTM1CH1	CH1F	CH1IE	FTM1 channel 1
13	0xFFE4:FFE5	Vftm1ch0	FTM1CH0	CH0F	CH0IE	FTM1 channel 0
12	0xFFE6:FFE7	Vftm2ovf	FTM2	TOF	TOIE	FTM2 overflow
11	0xFFE8:FFE9	Vftm2ch5	FTM2CH5	CH5F	CH5IE	FTM2 channel 5
10	0xFFEA:FFEB	Vftm2ch4	FTM2CH4	CH4F	CH4IE	FTM2 channel 4
9	0xFFEC:FFED	Vftm2ch3	FTM2CH3	CH3F	CH3IE	FTM2 channel 3
8	0xFFEE:FFEF	Vftm2ch2	FTM2CH2	CH2F	CH2IE	FTM2 channel 2
7	0xFFF0:FFF1	Vftm2ch1	FTM2CH1	CH1F	CH1IE	FTM2 channel 1
6	0xFFF2:FFF3	Vftm2ch0	FTM2CH0	CH0F	CH0IE	FTM2 channel 0
5	0xFFF4:FFF5	Vftm2flt	FTM2	FAULTF	FAULTIE	FTM2 fault
4	0xFFF6:FFF7	Vclk	ICS	LOLS	LOLIE	Clock loss of lock
3	0xFFF8:FFF9	Vlvw	System control	LVWF	LVWIE	Low-voltage warning
2	0xFFFA:FFFB	Virq_wdog	WDOG IRQ	WDOGF IRQF	WDOGI IRQIE	WDOG timeout IRQ interrupt
1	0xFFFC:FFFD	Vswi	Core	SWI Instruction	—	Software interrupt
0	0xFFFE:FFFF	Vreset	System control	WDOG LVD RESET pin	WDOGE LVDRE RSTPE	Watchdog timer Low-voltage detect External pin

Table 5-1. Vector summary (from lowest to highest priority)

Vector number	Address (high/ low)	Vector name	Module	Source	Local enable	Description
				Illegal opcode	—	Illegal opcode
				Illegal address	—	Illegal address
				POR	—	Power-on-reset
				ICS	CME	ICS loss of clk reset
				BDFR	—	BDM force reset

5.1.3 Interrupt priority controller (IPC)

This device has interrupt priority controller (IPC) module to provide up to four-level nested interrupt capability. IPC includes the following features:

- Four-level programmable interrupt priority for each interrupt source.
- Support for prioritized preemptive interrupt service routines
  - Low-priority interrupt requests are blocked when high-priority interrupt service routines are being serviced.
  - Higher or equal priority level interrupt requests can preempt lower priority interrupts being serviced.
- Automatic update of interrupt priority mask with being serviced interrupt source priority level when the interrupt vector is being fetched.
- Interrupt priority mask can be modified during main flow or interrupt service execution.
- Previous interrupt mask level is automatically stored when interrupt vector is fetched (four levels of previous values accommodated)

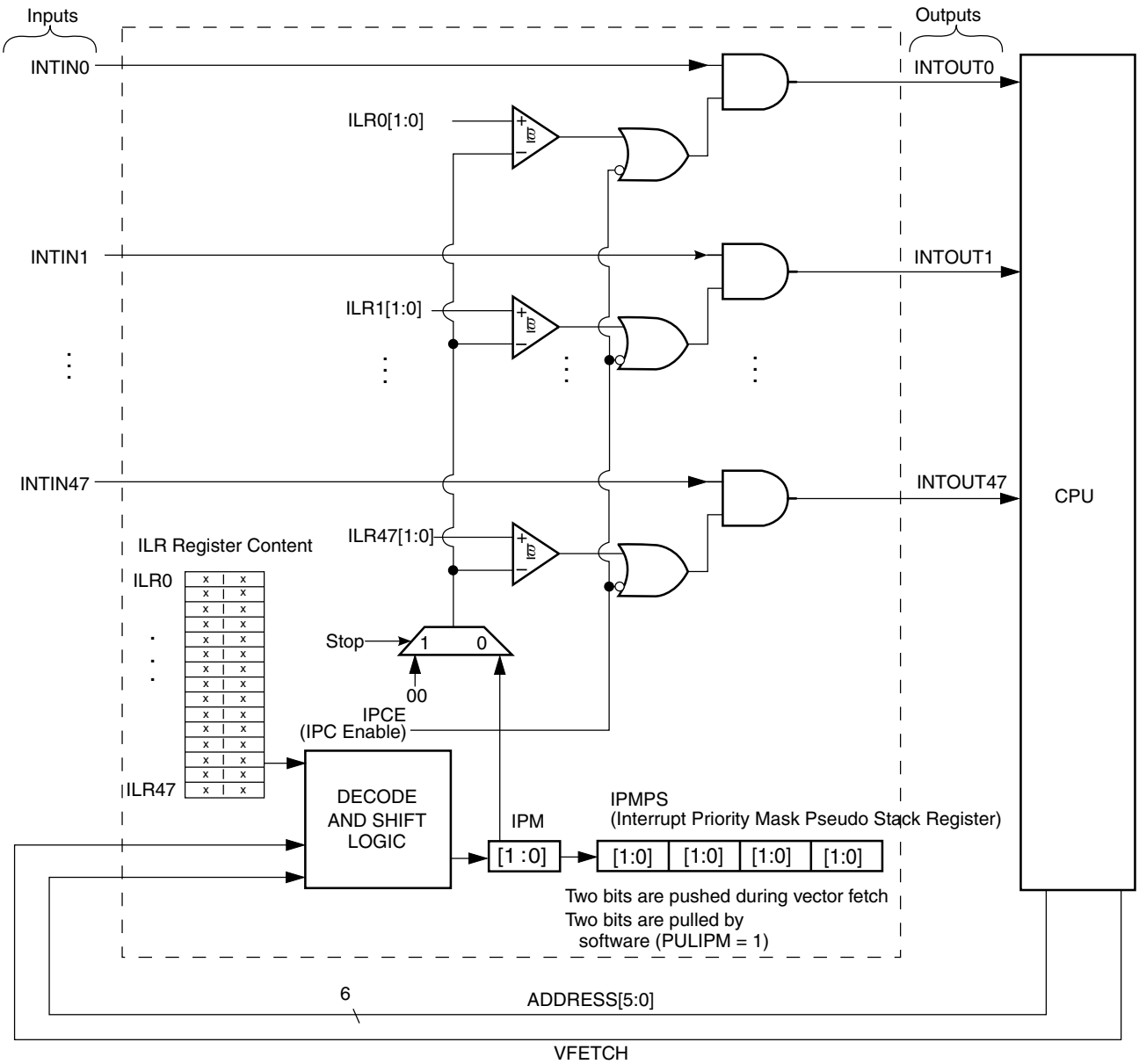


Figure 5-2. Interrupt priority controller block diagram

The IPC works with the existing HCS08 interrupt mechanism to allow nested interrupts with programmable priority levels. This module also allows implementation of preemptive interrupt according to the programmed interrupt priority with minimal software overhead. The IPC consists of three major functional blocks:

- The interrupt priority level registers
- The interrupt priority level comparator set
- The interrupt mask register update and restore mechanism

5.1.3.1 Interrupt priority level register

This set of registers is associated with the interrupt sources to the HCS08 CPU. Each interrupt priority level is a 2-bit value such that a user can program the interrupt priority level of each source to priority 0, 1, 2, or 3. Level 3 has the highest priority while level 0 has the lowest. Software can read or write to these registers at any time. The interrupt priority level comparator set, interrupt mask register update, and restore mechanism use this information.

5.1.3.2 Interrupt priority level comparator set

When the module is enabled, an active interrupt request forces a comparison between the corresponding ILR and the 2-bit interrupt mask IPM[1:0]. In stop3 mode, the IPM[1:0] is substituted by value 00b. If the ILR value is greater than or equal to the value of the interrupt priority mask (IPM bits in IPCSC), the corresponding interrupt out (INTOUT) signal will be asserted and signals an interrupt request to the HCS08 CPU.

When the module is disabled, the interrupt request signal from the source is directly passed to the CPU.

The interrupt priority level programmed in the interrupt priority register will not affect the inherent interrupt priority arbitration as defined by the HCS08 CPU because the IPC is an external module. Therefore, if two (or more) interrupts are present in the HCS08 CPU at the same time, the inherent priority in HCS08 CPU will perform arbitration by the inherent interrupt priority.

5.1.3.3 Interrupt priority mask update and restore mechanism

The interrupt priority mask (IPM) is two bits located in the least significant end of IPCSC register. These two bits control which interrupt is allowed to be presented to the HCS08 CPU. During vector fetch, the interrupt priority mask is updated automatically with the value of the ILR corresponding to that interrupt source. The original value of the IPM will be saved onto IPMPS for restoration after the interrupt service routine completes execution. When the interrupt service routine completes execution, the user restore the original value of IPM by writing 1 to the IPCSC[PULIPM] bit. In both cases, the IPMPS is a shift register functioning as a pseudo stack register for storing the IPM. When the IPM is updated, the original value is shifted into IPMPS. The IPMPS can store four levels of IPM. If the last position of IPMPS is written, the PSF flag indicates that the IPMPS is full. If all the values in the IPMPS were read, the PSE flag indicates that the IPMPS is empty.

5.1.3.4 Integration and application of the IPC

All interrupt inputs that comes from peripheral modules are synchronous signals. None of the asynchronous signals of the interrupts are routed to IPC. The asynchronous signals of the interrupts are routed directly to SIM module to wake system clocks in stop3 mode.

Additional care must be exercised when IRQ is reprioritized by IPC. CPU instructions BIL and BIH need input from IRQ pin. If IRQ interrupt is masked, BIL and BIH still work but the IRQ interrupt will not occur.

- The interrupt priority controller must be enabled to function. While inside an interrupt service routine, some work has to be done to enable other higher priority interrupts. The following is a pseudo code example written in assembly language:

```
INT_SER :
        BCLR        INTFLAG,INTFLAG_R ; clear flag that generate interrupt
        .                             ; do the most critical part
        .                             ; which it cannot be interrupted
        .
        .
        .
        CLI                           ; global interrupt enable and nested interrupt
enabled
        .                             ; continue the less critical
        .
        .
        .
        BSET        PULIPM, PULIPM_R  ; restore the old IPM value before leaving
        RTI                           ; then you can return
```

- A minimum overhead of six bus clock cycles is added inside an interrupt services routine to enable preemptive interrupts.
- As an interrupt of the same priority level is allowed to pass through IPC to HCS08 CPU, the flag generating the interrupt must be cleared before doing CLI to enable preemptive interrupts.
- The IPM is automatically updated to the level the interrupt is servicing and the original level is kept in IPMPS. Watch out for the full (PSF) bit if nesting for more than four levels is expected.
- Before leaving the interrupt service routine, the previous levels must be restored manually by setting PULIPM bit. Watch out for the full (PSF) bit and empty (PSE) bit.

5.2 External interrupt request (IRQ)

The IRQ (external interrupt) module provides a maskable interrupt input.

5.2.1 Features

Features of the IRQ module include:

- A Dedicated External Interrupt Pin
- IRQ Interrupt Control Bits
- Programmable Edge-only or Edge and Level Interrupt Sensitivity
- Automatic Interrupt Acknowledge
- Internal pullup device

A low level applied to the external interrupt request (IRQ) pin can latch a CPU interrupt request. The following figure shows the structure of the IRQ module:

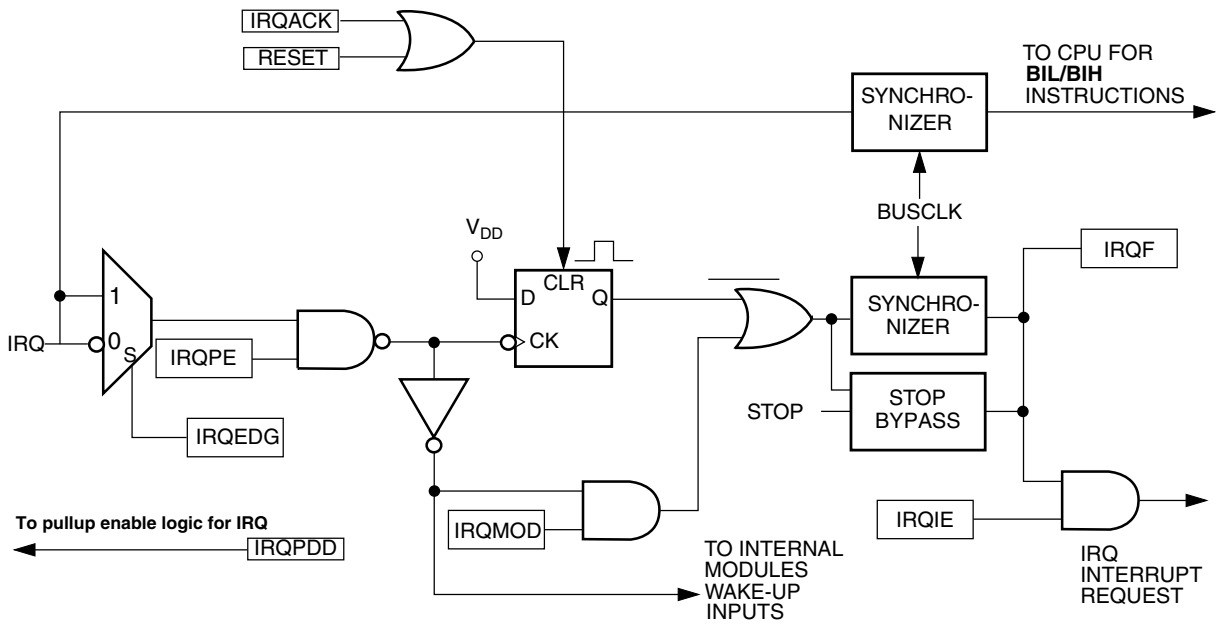


Figure 5-3. IRQ module block diagram

External interrupts are managed by the IRQSC status and control register. When the IRQ function is enabled, synchronous logic monitors the pin for edge-only or edge-and-level events. When the MCU is in stop mode and system clocks are shut down, a separate asynchronous path is used so that the IRQ, if enabled, can wake the MCU.

5.2.1.1 Pin configuration options

The IRQ pin enable control bit (IRQ_SC[IRQPE]) must be 1 for the IRQ pin to act as the IRQ input. The user can choose the polarity of edges or levels detected (IRQEDG), whether the pin detects edges-only or edges and levels (IRQMOD), or whether an event causes an interrupt or only sets the IRQF flag, which can be polled by software.

When enabled, the IRQ pin defaults to use an internal pullup device (IRQ_SC[IRQPDD] = 0). If the user uses an external pullup or pulldown, the IRQ_SC[IRQPDD] can be written to a 1 to turn off the internal device.

BIH and BIL instructions may be used to detect the level on the IRQ pin when it is configured to act as the IRQ input.

5.2.1.2 Edge and level sensitivity

The IRQ_SC[IRQMOD] control bit reconfigures the detection logic so that it can detect edge events and pin levels. In this detection mode, the IRQF status flag is set when an edge is detected, if the IRQ pin changes from the de-asserted to the asserted level, but the flag is continuously set and cannot be cleared as long as the IRQ pin remains at the asserted level.

5.3 IRQ memory map and register definition

IRQ memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3B	Interrupt Pin Request Status and Control Register (IRQ_SC)	8	R/W	00h	5.3.1/129

5.3.1 Interrupt Pin Request Status and Control Register (IRQ_SC)

This direct page register includes status and control bits, which are used to configure the IRQ function, report status, and acknowledge IRQ events.

Address: 3Bh base + 0h offset = 3Bh

Bit	7	6	5	4	3	2	1	0
Read	0	IRQPDD	IRQEDG	IRQPE	IRQF	0	IRQIE	IRQMOD
Write						IRQACK		
Reset	0	0	0	0	0	0	0	0

IRQ_SC field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 IRQPDD	Interrupt Request (IRQ) Pull Device Disable This read/write control bit is used to disable the internal pullup device when the IRQ pin is enabled (IRQPE = 1) allowing for an external device to be used. 0 IRQ pull device enabled if IRQPE = 1. 1 IRQ pull device disabled if IRQPE = 1.
5 IRQEDG	Interrupt Request (IRQ) Edge Select This read/write control bit is used to select the polarity of edges or levels on the IRQ pin that cause IRQF to be set. The IRQMOD control bit determines whether the IRQ pin is sensitive to both edges and levels or only edges. When the IRQ pin is enabled as the IRQ input and is configured to detect rising edges, the optional pullup resistor is disabled. 0 IRQ is falling edge or falling edge/low-level sensitive. 1 IRQ is rising edge or rising edge/high-level sensitive.
4 IRQPE	IRQ Pin Enable This read/write control bit enables the IRQ pin function. When this bit is set the IRQ pin can be used as an interrupt request. 0 IRQ pin function is disabled. 1 IRQ pin function is enabled.
3 IRQF	IRQ Flag This read-only status bit indicates when an interrupt request event has occurred. 0 No IRQ request. 1 IRQ event detected.
2 IRQACK	IRQ Acknowledge This write-only bit is used to acknowledge interrupt request events (write 1 to clear IRQF). Writing 0 has no meaning or effect. Reads always return 0. If edge-and-level detection is selected (IRQMOD = 1), IRQF cannot be cleared while the IRQ pin remains at its asserted level.
1 IRQIE	IRQ Interrupt Enable This read/write control bit determines whether IRQ events generate an interrupt request. 0 Interrupt request when IRQF set is disabled (use polling). 1 Interrupt requested whenever IRQF = 1.
0 IRQMOD	IRQ Detection Mode This read/write control bit selects either edge-only detection or edge-and-level detection. 0 IRQ event on falling/rising edges only. 1 IRQ event on falling/rising edges and low/high levels.

5.4 Interrupt priority controller (IPC) memory map and register definition

IPC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3E	IPC Status and Control Register (IPC_SC)	8	R/W	20h	5.4.1/131
3F	Interrupt Priority Mask Pseudo Stack Register (IPC_IPMPS)	8	R	00h	5.4.2/132
3050	Interrupt Level Setting Registers n (IPC_ILRS0)	8	R/W	00h	5.4.3/133
3051	Interrupt Level Setting Registers n (IPC_ILRS1)	8	R/W	00h	5.4.3/133
3052	Interrupt Level Setting Registers n (IPC_ILRS2)	8	R/W	00h	5.4.3/133
3053	Interrupt Level Setting Registers n (IPC_ILRS3)	8	R/W	00h	5.4.3/133
3054	Interrupt Level Setting Registers n (IPC_ILRS4)	8	R/W	00h	5.4.3/133
3055	Interrupt Level Setting Registers n (IPC_ILRS5)	8	R/W	00h	5.4.3/133
3056	Interrupt Level Setting Registers n (IPC_ILRS6)	8	R/W	00h	5.4.3/133
3057	Interrupt Level Setting Registers n (IPC_ILRS7)	8	R/W	00h	5.4.3/133
3058	Interrupt Level Setting Registers n (IPC_ILRS8)	8	R/W	00h	5.4.3/133
3059	Interrupt Level Setting Registers n (IPC_ILRS9)	8	R/W	00h	5.4.3/133

5.4.1 IPC Status and Control Register (IPC_SC)

This register contains status and control bits for the IPC.

Address: 3Eh base + 0h offset = 3Eh

Bit	7	6	5	4	3	2	1	0
Read	IPCE	0	PSE	PSF	0	0	IPM	
Write					PULIPM			
Reset	0	0	1	0	0	0	0	0

IPC_SC field descriptions

Field	Description
7 IPCE	Interrupt Priority Controller Enable This bit enables/disables the interrupt priority controller module. 0 Disables IPCE. Interrupt generated from the interrupt source is passed directly to CPU without processing (bypass mode). The IPMPS register is not updated when the module is disabled. 1 Enables IPCE and interrupt generated from the interrupt source is processed by IPC before passing to CPU.

Table continues on the next page...

IPC_SC field descriptions (continued)

Field	Description
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 PSE	Pseudo Stack Empty This bit indicates that the pseudo stack has no valid information. This bit is automatically updated after each IPMPS register push or pull operation.
4 PSF	Pseudo Stack Full This bit indicates that the pseudo stack register IPMPS register is full. It is automatically updated after each IPMPS register push or pull operation. If additional interrupt is nested after this bit is set, the earliest interrupt mask value(IPM0[1:0]) stacked in IPMPS will be lost. 0 IPMPS register is not full. 1 IPMPS register is full.
3 PULIPM	Pull IPM from IPMPS This bit pulls stacked IPM value from IPMPS register to IPM bits of IPCSC. Zeros are shifted into bit positions 1 and 0 of IPMPS. 0 No operation. 1 Writing 1 to this bit causes a 2-bit value from the interrupt priority mask pseudo stack register to be pulled to the IPM bits of IPCSC to restore the previous IPM value.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
IPM	Interrupt Priority Mask This field sets the mask for the interrupt priority control. If the interrupt priority controller is enabled, the interrupt source with an interrupt level (ILRxx) value that is greater than or equal to the value of IPM will be presented to the CPU. Writes to this field are allowed, but doing this will not push information to the IPMPS register. Writing IPM with PULIPM setting when IPCE is already set, the IPM will restore the value pulled from the IPMPS register, not the value written to the IPM register.

5.4.2 Interrupt Priority Mask Pseudo Stack Register (IPC_IPMPS)

This register is used to store the previous interrupt priority mask level temporarily when the currently active interrupt is executed.

Address: 3Eh base + 1h offset = 3Fh

Bit	7	6	5	4	3	2	1	0
Read	IPM3		IPM2		IPM1		IPM0	
Write								
Reset	0	0	0	0	0	0	0	0

IPC_IPMPS field descriptions

Field	Description
7–6 IPM3	Interrupt Priority Mask pseudo stack position 3 This field is the pseudo stack register for IPM3. The most recent information is stored in IPM3.
5–4 IPM2	Interrupt Priority Mask pseudo stack position 2 This field is the pseudo stack register for IPM2. The most recent information is stored in IPM2.
3–2 IPM1	Interrupt Priority Mask pseudo stack position 1 This field is the pseudo stack register for IPM1. The most recent information is stored in IPM1.
IPM0	Interrupt Priority Mask pseudo stack position 0 This field is the pseudo stack register for IPM0. The most recent information is stored in IPM0.

5.4.3 Interrupt Level Setting Registers n (IPC_ILRS*n*)

This set of registers (ILRS0-ILRS9) contains the user specified interrupt level for each interrupt source, and indicates the number of the register (ILRSn is ILRS0 through ILRS9).

Address: 3Eh base + 3012h offset + (1d × i), where i=0d to 9d

Bit	7	6	5	4	3	2	1	0
Read Write	ILRn3		ILRn2		ILRn1		ILRn0	
Reset	0	0	0	0	0	0	0	0

IPC_ILRS*n* field descriptions

Field	Description
7–6 ILRn3	Interrupt Level Register for Source n*4+3 This field sets the interrupt level for interrupt source n*4+3.
5–4 ILRn2	Interrupt Level Register for Source n*4+2 This field sets the interrupt level for interrupt source n*4+2.
3–2 ILRn1	Interrupt Level Register for Source n*4+1 This field sets the interrupt level for interrupt source n*4+1.
ILRn0	Interrupt Level Register for Source n*4+0 This field sets the interrupt level for interrupt source n*4+0.

Chapter 6
System control

6.1 System device identification (SDID)

This device is hard coded to the value 0x0040 in SDID registers.

6.2 Universally unique identification (UUID)

This device contains up to 64-bit UUID to identify each device in this family. The intent of UUID is to enable distributed systems to uniquely identify information without significant central coordination.

6.3 Reset and system initialization

Resetting the MCU provides a way to start processing from a set of known initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector (0xFFFE:0xFFFF). On-chip peripheral modules are disabled and I/O pins are initially configured as general-purpose high-impedance inputs with disabled pullup devices. The CCR[I] bit is set to block maskable interrupts so that the user program has a chance to initialize the stack pointer (SP) and system control settings. SP is forced to 0x00FF at reset.

This device has the following sources for reset:

- Power-on reset (POR)
- Low-voltage detect (LVD)
- Watchdog (WDOG) timer
- Illegal opcode detect (ILOP)

- Illegal address detect (ILAD)
- Background debug forced reset
- External reset pin (RESET)
- Internal clock source module reset (CLK)

Each of these sources, with the exception of the background debug forced reset, has an associated bit in the system reset status (SRS) register.

When the MCU is reset by ILAD, the address of illegal address is captured in illegal address register, which is a 16-bit register consisting of ILLAL and ILLAH that contains the LSB and MSB 8-bit of the address, respectively.

6.4 System options

6.4.1 BKGD pin enable

After POR, PTA4/ACMPO/BKGD/MS pin functions as BKGD output. The SYS_SOPT1[BKGDPE] bit must be set to enable the background debug mode pin enable function. When this bit is clear, this pin can function as PTA4 or ACMP output.

6.4.2 $\overline{\text{RESET}}$ pin enable

After POR reset, PTA5/IRQ/TCLK0/$\overline{\text{RESET}}$ functions as $\overline{\text{RESET}}$. The SYS_SOPT1[RSTPE] bit must be set to enable the reset functions. When this bit is clear, this pin can function as PTA5, IRQ, or TCLK0.

6.4.3 SCI0 pin reassignment

After reset, SCI0 module pinouts of RxD and TxD are mapped on PTB0 and PTB1, respectively. SYS_SOPT1[SCI0PS] bit enables to reassign SCI0 pinouts on PTA2 and PTA3.

6.4.4 SPI0 pin reassignment

After reset, SPI0 module pinouts of SPSCK0, MOSI0, MISO0, and $\overline{SS0}$ are mapped on PTB2, PTB3, PTB4, and PTB5. SYS_SOPT1[SPI0PS] bit enables to reassign the SPI0 pinouts on PTE0, PTE1, PTE2, and PTE3, respectively. Please note PTE1/MOSI0 and PTE0/SPSCK0 can provide up to 20 mA sink/source current, which is desirable for high-speed SPI communication.

6.4.5 IIC pins reassignments

After POR reset, IIC module pinouts of SDA and SCL are mapped on PTA2 and PTA3. SYS_SOPT1[IICPS] bit enables to reassign the IIC pinout pair on PTB6 and PTB7 respectively. Please note the PTA2 and PTA3 operate as true open drain, which can support different level IIC communication. When PTB6 and PTB7 act as IIC pins, the remote IIC level is limited to no more than MCU V_{DD}.

6.4.6 FTM2 channels pin reassignment

After POR reset, FTM2 channel pinouts of FTM2CH0, FTM2CH1, FTM2CH2, and FTM2CH3 are default mapped on PTC0, PTC1, PTC2, and PTC3. When set, SYS_SOPT1[FTM2PS] bit enables to reassignment these FTM2 channels on PTH0, PTH1, PTD0, and PTD1, respectively. As PTH0, PTH1, PTD0, PTD1, PTB4, and PTB5 can provide up to 20 mA sink/source current, each FTM2 channel can provide high current with the same time base when this bit is set.

6.4.7 Bus clock output pin enable

The system bus clock can be outputted on PTH2 when the SYS_SOPT3[CLKOE] bits are set by nonzero. Before mapping on the pinout, the output of bus clock can be pre-divided by 1, 2, 4, 8, 16, 32, 64, or 128 by setting SYS_SOPT3[BUSREF].

6.5 System interconnection

This device contains a set of system-level logics for module-to-module interconnection for flexible configuration. These interconnections provide the hardware trigger function between modules with least software configuration, which is ideal for infrared communication, serial communication baudrate detection, low-end motor control, metering clock calibration, and other general-purpose applications.

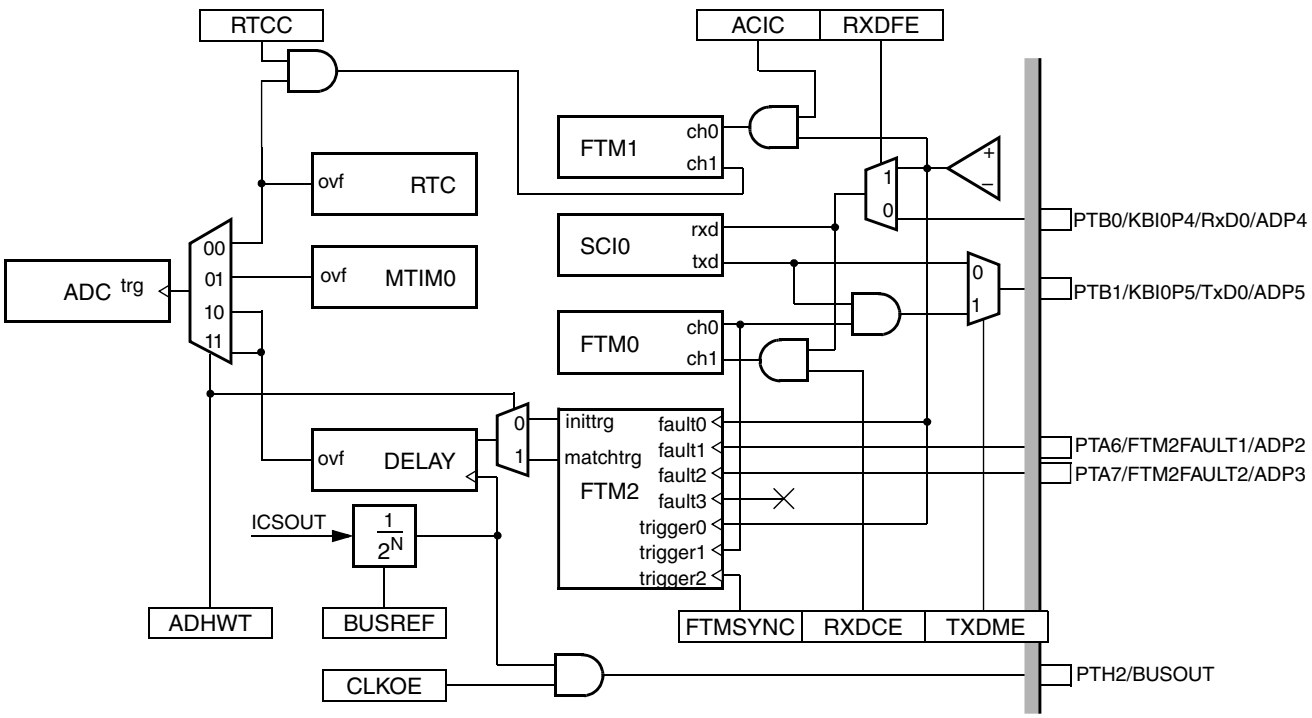


Figure 6-1. System interconnection diagram

6.5.1 ACMP output selection

When set, the SYS_SOPT2[ACIC] bit enables the output of ACMP to connect to the FTM1CH0, the FTM1CH0 pin is released to other shared functions.

6.5.2 SCI0 TxD modulation

SCI0 TXD can be modulated by FTM0 channel 0 output. When SYS_SOPT2[TXDME] bit is set, the TXD output is passed to an AND gate with FTM0 channel 0 output before mapping on TXD0 pinout. When this bit is clear, the TXD is directly mapped on the pinout. To enable IR modulation function, both FTM0CH0 and SCI must be active. The

FTM0 counter modulo register specifies the period of the PWM, and the FTM0 channel 0 value register specifies the duty cycle of the PWM. Then, when TXDME bit is enabled, each data transmitted via TXD0 from SCI0 is modulated by the FTM0 channel 0 output, and the FTM0CH0 pin is released to other shared functions.

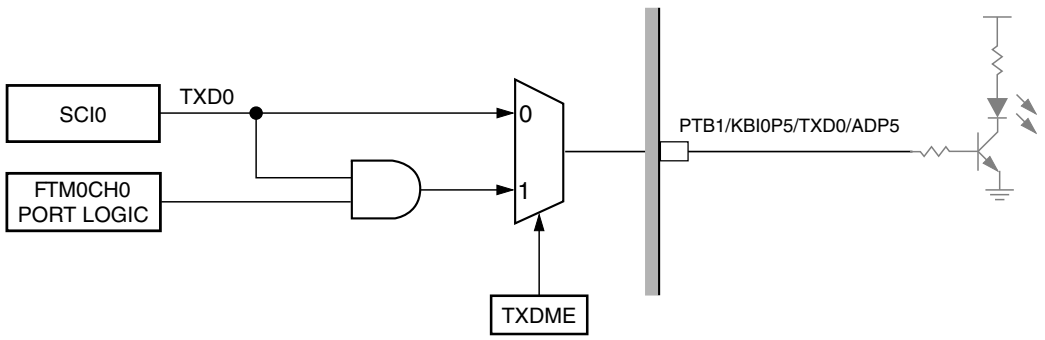


Figure 6-2. IR modulation diagram

6.5.3 SCI0 RxD capture

RxD0 pin is selectable connected to SCI0 module directly or tagged to FTM0 channel 1. When SYS_SOPT2[RXDCE] bit is set, the RxD0 pin is connected to both SCI0 and FTM0 channel 1, and the FTM0CH1 pin is released to other shared functions. When this bit is clear, the RxD0 pin is connected to SCI0 only.

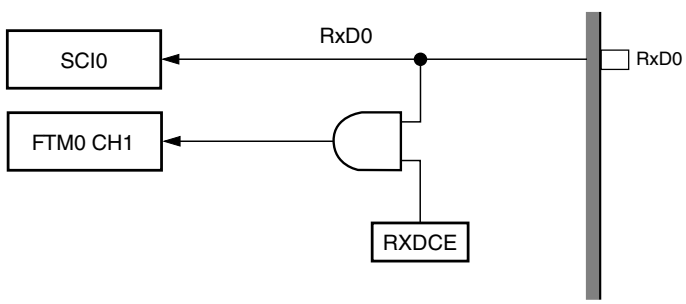


Figure 6-3. RxD0 capture function diagram

6.5.4 SCI0 RxD filter

When SYS_SOPT2[RXDFE] bit is clear, the RxD0 pin is connected to SCI0 module directly. When this bit is set, the ACMP output is connected to the receive channel of SCI0. To enable RxD filter function, both SCI0 and ACMP must be active. If this function is active, the SCI0 external RxD0 pin is released to other shared functions regardless of the configuration of SCI0 pin reassignment. When SCI0 RxD capture function is active, the ACMP output is injected to FTM0CH1 as well.

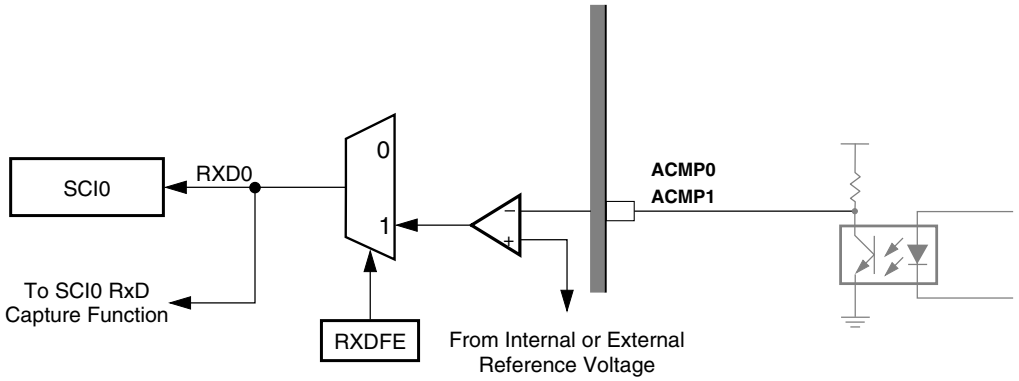


Figure 6-4. IR demodulation diagram

6.5.5 RTC capture

RTC overflow may be captured by FTM1 channel 1 by setting SYS_SOPT2[RTCC] bit. When this bit is set, the RTC overflow is connected to FTM1 channel 1 for capture, the FTM1CH1 pin is released to other shared functions.

6.5.6 FTM2 software synchronization

FTM2 contains three synchronization input trigger, one of which is a software trigger by writing 1 to the SYS_SOPT2[FTMSYNC] bit. Writing 0 to this bit takes no effect. This bit is always read 0.

6.5.7 ADC hardware trigger

ADC module may initiate a conversion via a hardware trigger. MTIM0 overflow, RTC, FTM2 match trigger with 8-bit programmable delay, and FTM2 init trigger with 8-bit programmable delay can be enabled as the hardware trigger for the ADC module by setting the SYS_SOPT2[ADHWT] bits. The following table shows the ADC hardware trigger setting.

Table 6-1. ADC hardware trigger setting

ADHWT	ADC hardware trigger
0:0	RTC overflow
0:1	MTIM0 overflow
1:0	FTM2 init trigger with 8-bit programmable delay
1:1	FTM2 match trigger with 8-bit programmable delay

When ADC hardware trigger selects the output of FTM2 triggers, an 8-bit delay block will be enabled. This logic delays any trigger from FTM2 with an 8-bit counter whose value is specified by SYS_SOPT4[DELAY] bit. The reference clock to this module is the output of ICSOUT with selectable pre-divider specified by SYS_SOPT3[BUSREF].

6.6 System Control Registers

SYS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3000	System Reset Status Register (SYS_SRS)	8	R	82h	6.6.1/141
3001	System Background Debug Force Reset Register (SYS_SBDFR)	8	W (always reads 0)	00h	6.6.2/143
3002	System Device Identification Register: High (SYS_SDIDH)	8	R	00h	6.6.3/144
3003	System Device Identification Register: Low (SYS_SDIDL)	8	R	40h	6.6.4/144
3004	System Options Register 1 (SYS_SOPT1)	8	R/W	0Ch	6.6.5/145
3005	System Options Register 2 (SYS_SOPT2)	8	R/W	00h	6.6.6/146
3006	System Options Register 3 (SYS_SOPT3)	8	R/W	00h	6.6.7/147
3007	System Options Register 4 (SYS_SOPT4)	8	R/W	00h	6.6.8/148
304A	Illegal Address Register: High (SYS_ILLAH)	8	R	Undefined	6.6.9/149
304B	Illegal Address Register: Low (SYS_ILLAL)	8	R	Undefined	6.6.10/149
30F8	Universally Unique Identifier Register 1 (SYS_UUID1)	8	R	Undefined	6.6.11/150
30F9	Universally Unique Identifier Register 2 (SYS_UUID2)	8	R	Undefined	6.6.12/150
30FA	Universally Unique Identifier Register 3 (SYS_UUID3)	8	R	Undefined	6.6.13/151
30FB	Universally Unique Identifier Register 4 (SYS_UUID4)	8	R	Undefined	6.6.14/151
30FC	Universally Unique Identifier Register 5 (SYS_UUID5)	8	R	Undefined	6.6.15/152
30FD	Universally Unique Identifier Register 6 (SYS_UUID6)	8	R	Undefined	6.6.16/152
30FE	Universally Unique Identifier Register 7 (SYS_UUID7)	8	R	Undefined	6.6.17/153
30FF	Universally Unique Identifier Register 8 (SYS_UUID8)	8	R	Undefined	6.6.18/153

6.6.1 System Reset Status Register (SYS_SRS)

This register includes read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to the SYS_SBDFR[BDFR] bit, none of the status bits in SRS will be set. The reset state of these bits depends on what caused the MCU to reset.

NOTE

For PIN, WDOG, and ILOP, any of these reset sources that are active at the time of reset (not including POR or LVR) will

cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset will be cleared.

NOTE

The RESET values in the figure are values for power on reset; for other resets, the values depend on the trigger causes.

Address: 3000h base + 0h offset = 3000h

Bit	7	6	5	4	3	2	1	0
Read	POR	PIN	WDOG	ILOP	ILAD	LOC	LVD	0
Write								
Reset	1	0	0	0	0	0	1	0

SYS_SRS field descriptions

Field	Description
7 POR	Power-On Reset Reset was caused by the power-on detection logic. When the internal supply voltage was ramping up at the time, the low-voltage reset (LVR) status bit is also set to indicate that the reset occurred while the internal supply was below the LVR threshold. **NOTE:** This bit POR to 1, LVR to uncertain value and reset to 0 at any other conditions. 0 Reset not caused by POR. 1 POR caused reset.
6 PIN	External Reset Pin Reset was caused by an active low level on the external reset pin. 0 Reset not caused by external reset pin. 1 Reset came from external reset pin.
5 WDOG	Watchdog (WDOG) Reset was caused by the WDOG timer timing out. This reset source may be blocked by WDOGE = 0. 0 Reset not caused by WDOG timeout. 1 Reset caused by WDOG timeout.
4 ILOP	Illegal Opcode Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register. 0 Reset not caused by an illegal opcode. 1 Reset caused by an illegal opcode.
3 ILAD	Illegal Address Reset was caused by an attempt to access a illegal address. The illegal address is captured in illegal address register (ILLAH:ILLAL). 0 Reset not caused by an illegal address. 1 Reset caused by an illegal address.

Table continues on the next page...

SYS_SRS field descriptions (continued)

Field	Description
2 LOC	Internal Clock Source Module Reset Reset was caused by an ICS module reset. 0 Reset not caused by ICS module. 1 Reset caused by ICS module.
1 LVD	Low Voltage Detect If the LVDRE bit is set in run mode or both LVDRE and LVDSE bits are set in stop mode, and the supply drops below the LVD trip voltage, an LVD reset will occur. This bit is also set by POR. **NOTE:** This bit reset to 1 on POR and LVR and reset to 0 on other reset. 0 Reset not caused by LVD trip or POR. 1 Reset caused by LVD trip or POR.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

6.6.2 System Background Debug Force Reset Register (SYS_SBDFR)

This register contains a single write-only control bit. A serial background command such as WRITE_BYTE must be used to write to SYS_SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

NOTE

This register is the same as the BDC_SBDFR.

Address: 3000h base + 1h offset = 3001h

Bit	7	6	5	4	3	2	1	0
Read	0							0
Write								BDFR
Reset	0	0	0	0	0	0	0	0

SYS_SBDFR field descriptions

Field	Description
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 BDFR	Background Debug Force Reset A serial background command such as WRITE_BYTE may be used to allow an external debug host to force a target system reset. Writing logic 1 to this bit forces an MCU reset. This bit cannot be written from a user program. **NOTE:** BDFR is writable only through serial background debug commands, not from user programs.

6.6.3 System Device Identification Register: High (SYS_SDIDH)

This read-only register, together with SYS_SDIDL, is included so that host development systems can identify the HCS08 derivative and revision number. This allows the development software to recognize where specific memory blocks, registers, and control bits are located in a target MCU.

Address: 3000h base + 2h offset = 3002h

Bit	7	6	5	4	3	2	1	0
Read	Reserved				ID			
Write								
Reset	0	0	0	0	0	0	0	0

SYS_SDIDH field descriptions

Field	Description
7–4 Reserved	This field is reserved.
ID	Part Identification Number These bits, together with the SYS_SDIDL, indicate part identification number. Each derivative in the HCS08 family has a unique identification number. This device is hard coded to the value 0x40.

6.6.4 System Device Identification Register: Low (SYS_SDIDL)

This read-only register, together with SYS_SDIDH, is included so host development systems can identify the HCS08 derivative and revision number. This allows the development software to recognize where specific memory blocks, registers, and control bits are located in a target MCU.

Address: 3000h base + 3h offset = 3003h

Bit	7	6	5	4	3	2	1	0
Read	ID							
Write								
Reset	0	1	0	0	0	0	0	0

SYS_SDIDL field descriptions

Field	Description
ID	Part Identification Number These bits, together with the SYS_SDIDH, indicate part identification number. Each derivative in the HCS08 family has a unique identification number. This device is hard coded to the value 0x40.

6.6.5 System Options Register 1 (SYS_SOPT1)

This register may only be written once after reset. SYS_SOPT1 should be written during the user's reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

Address: 3000h base + 4h offset = 3004h

Bit	7	6	5	4	3	2	1	0
Read Write	SCI0PS	SPI0PS	IICPS	FTM2PS	BKGDPE	RSTPE	FWAKE	STOPE
Reset	0	0	0	0	1	1	0	0

SYS_SOPT1 field descriptions

Field	Description
7 SCI0PS	SCI0 Pin Select This write-once bit selects the SCI0 pinouts. 0 SCI0 RxD and TxD are mapped on PTB0 and PTB1. 1 SCI0 RxD and TxD are mapped on PTA2 and PTA3.
6 SPI0PS	SPI0 Pin Select This write-once bit selects the SPI0 Pinouts. 0 SPI0 SPSCK0, MOSI0, MISO0, and SS0 are mapped on PTB2, PTB3, PTB4, and PTB5. 1 SPI0 SPSCK0, MOSI0, MISO0, and SS0 are mapped on PTE0, PTE1, PTE2, and PTE3.
5 IICPS	IIC Port Pin Select This write-once bit selects the IIC port pins. 0 IIC SCL and SDA are mapped on PTA3 and PTA2, respectively. 1 IIC SCL and SDA are mapped on PTB7 and PTB6, respectively.
4 FTM2PS	FTM2 Port Pin Select This write-once bit selects the FTM2 channels port pins. 0 FTM2 channels mapped on PTC0, PTC1, PTC2, PTC3, PTB4, and PTB5. 1 FTM2 channels mapped on PTH0, PTH1, PTD0, PTD1, PTB4, and PTB5.
3 BKGDPE	Background Debug Mode Pin Enable This write-once bit when set enables the PTA4/ACMPO/BKGD/MS pin to function as BKGD/MS. When clear, the pin functions as output only PTA4. This pin defaults to the BKGD/MS function following any MCU reset. 0 PTA4/ACMPO/BKGD/MS as PTA4 or ACMPO function. 1 PTA4/ACMPO/BKGD/MS as BKGD function.
2 RSTPE	RESET Pin Enable This write-once bit can be written after any reset. When RSTPE is set, the PTA5/IRQ/TCLK0/RESET pin functions as RESET. When clear, the pin functions as one of its alternative functions. This pin defaults to

Table continues on the next page...

SYS_SOPT1 field descriptions (continued)

Field	Description
	RESET following an MCU POR. Other resets will not affect this bit. When RSTPE is set, an internal pullup device on RESET is enabled. 0 PTA5/IRQ/TCLK0/RESET pin functions as PTA5, IRQ, or TCLK0. 1 PTA5/IRQ/TCLK0/RESET pin functions as RESET.
1 FWAKE	Fast Wakeup Enable This write once bit can set CPU wakeup without any interrupt subroutine serviced. This action saved more than 11 cycles(whole interrupt subroutine time). After wake up CPU continue the address before wait or stop. **NOTE:** When FWAKE is set, user should avoid generating interrupt 0~8 bus clock cycles after issuing the stop instruction, or the MCU may stuck at stop3 mode and cannot wake up by interrupts. 0 CPU wakes up as normal. 1 CPU wakes up without any interrupt subroutine serviced.
0 STOPE	Stop Mode Enable This write-once bit defaults to 0 after reset, which disables stop mode. If stop mode is disabled and a user program attempts to execute a STOP instruction, an illegal opcode reset occurs. 0 Stop mode disabled. 1 Stop mode enabled.

6.6.6 System Options Register 2 (SYS_SOPT2)

This register may be read/write at any time. SYS_SOPT2 should be written during the user's reset initialization program to set the desired controls even if the desired settings are the same as the reset settings.

Address: 3000h base + 5h offset = 3005h

Bit	7	6	5	4	3	2	1	0
Read	TXDME	0	RXDFE	RXDCE	ACIC	RTCC	ADHWTS	
Write		FTMSYNC						
Reset	0	0	0	0	0	0	0	0

SYS_SOPT2 field descriptions

Field	Description
7 TXDME	SCI0 TxD Modulation Select This bit enables the SCI0 TxD output modulated by FTM0 channel 0. 0 TxD0 output is connected to pinout directly. 1 TxD0 output is modulated by FTM0 channel 0 before mapped to pinout.
6 FTMSYNC	FTM2 Synchronization Select

Table continues on the next page...

SYS_SOPT2 field descriptions (continued)

Field	Description
	Writing a 1 to this bit generates a PWM synchronization trigger to the FTM modules. 0 No synchronization triggered. 1 Generate a PWM synchronization trigger to the FTM2 modules.
5 RXDFE	SCI0 RxD Filter Select This bit enables the SCI0 RxD input filtered by ACMP. When this function is enabled, any signal tagged with ACMP inputs can be regarded SCI0. 0 RXD0 input signal is connected to SCI0 module directly. 1 RXD0 input signal is filtered by ACMP, then injected to SCI0.
4 RXDCE	SCI0 RxD Capture Select This bit enables the SCI0 RxD is captured by FTM0 channel 1. 0 RXD0 input signal is connected to SCI0 module only. 1 RXD0 input signal is connected to SCI0 module and FTM0 channel 1.
3 ACIC	Analog Comparator to Input Capture Enable This bit connects the output of ACMP to FTM1 input channel 0. 0 ACMP output not connected to FTM1 input channel 0. 1 ACMP output connected to FTM1 input channel 0.
2 RTCC	Real-Time Counter Capture This bit allows the Real-time Counter (RTC) overflow to be captured by FTM1 channel 1. 0 RTC overflow is not connected to FTM1 input channel 1. 1 RTC overflow is connected to FTM1 input channel 1.
ADHWTS	ADC Hardware Trigger Source These bits select the ADC hardware trigger source. All trigger sources start ADC conversion on rising edge. 00 RTC overflow as the ADC hardware trigger. 01 MTIM0 overflow as the ADC hardware trigger. 10 FTM2 init trigger with 8-bit programmable delay. 11 FTM2 match trigger with 8-bit programmable delay.

6.6.7 System Options Register 3 (SYS_SOPT3)

This register may be read and written at any time.

Address: 3000h base + 6h offset = 3006h

Bit	7	6	5	4	3	2	1	0
Read	DLYACT	0			CLKOE	BUSREF		
Write								
Reset	0	0	0	0	0	0	0	0

SYS_SOPT3 field descriptions

Field	Description
7 DLYACT	FTM2 Trigger Delay Active This read-only bit specifies the status if the FTM2 initial or match delay is active. This bit is set when an FTM2 trigger arrives and the delay counter is ticking. Otherwise, this bit will be clear. 0 The delay inactive. 1 The delay active.
6–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 CLKOE	CLK Output Enable This bit enables reference clock output on PTH2 0 ICSOUT output disabled on PTH2. 1 ICSOUT output enabled on PTH2.
BUSREF	BUS Output select This bit enables bus clock output on PTH2 via an optional prescalar. 000 Bus. 001 Bus divided by 2. 010 Bus divided by 4. 011 Bus divided by 8. 100 Bus divided by 16. 101 Bus divided by 32. 110 Bus divided by 64. 111 Bus divided by 128.

6.6.8 System Options Register 4 (SYS_SOPT4)

Address: 3000h base + 7h offset = 3007h

Bit	7	6	5	4	3	2	1	0
Read Write	DELAY							
Reset	0	0	0	0	0	0	0	0

SYS_SOPT4 field descriptions

Field	Description
DELAY	FTM2 Trigger Delay These bits specify the delay from FTM2 initial or match trigger to ADC hardware trigger upon the setting of ADHWT. The 8-bit modulo value allows the delay from 0 to 255 upon the BUSREF clock settings. This is a one-shot counter that starts ticking when the trigger arrives and stop ticking when the counter value reaches the modulo value that is defined.

6.6.9 Illegal Address Register: High (SYS_ILLAH)

The SYS_ILLAH is a read-only register containing the high 8-bit of the illegal address of ILAD reset.

Address: 3000h base + 4Ah offset = 304Ah

Bit	7	6	5	4	3	2	1	0
Read	ADDR[15:8]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_ILLAH field descriptions

Field	Description
ADDR[15:8]	High 8-bit of illegal address **NOTE:** For ILAD, it reset to the high 8-bit of the illegal address; in other cases, the reset to values are undetermined.

6.6.10 Illegal Address Register: Low (SYS_ILLAL)

The SYS_ILLAL is a read-only register containing the low 8-bit of the illegal address of ILAD reset.

Address: 3000h base + 4Bh offset = 304Bh

Bit	7	6	5	4	3	2	1	0
Read	ADDR[7:0]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_ILLAL field descriptions

Field	Description
ADDR[7:0]	Low 8-bit of illegal address **NOTE:** For ILAD, it resets to the low 8-bit of the illegal address; in other cases, the reset to values are undetermined.

6.6.11 Universally Unique Identifier Register 1 (SYS_UUID1)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + F8h offset = 30F8h

Bit	7	6	5	4	3	2	1	0
Read	ID[63:56]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID1 field descriptions

Field	Description
ID[63:56]	Universally Unique Identifier

6.6.12 Universally Unique Identifier Register 2 (SYS_UUID2)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + F9h offset = 30F9h

Bit	7	6	5	4	3	2	1	0
Read	ID[55:48]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

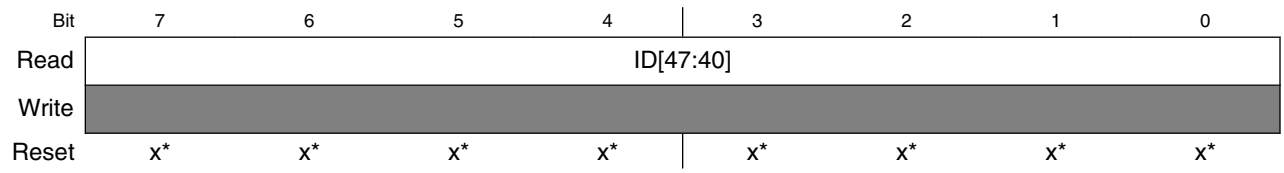
SYS_UUID2 field descriptions

Field	Description
ID[55:48]	Universally Unique Identifier

6.6.13 Universally Unique Identifier Register 3 (SYS_UUID3)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + FAh offset = 30FAh



* Notes:
- x = Undefined at reset.

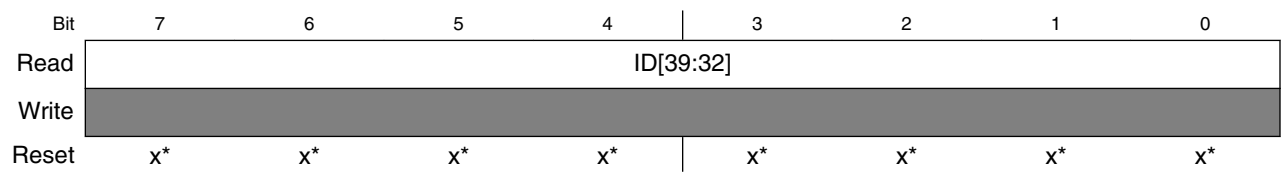
SYS_UUID3 field descriptions

Field	Description
ID[47:40]	Universally Unique Identifier

6.6.14 Universally Unique Identifier Register 4 (SYS_UUID4)

The read-only SYS_UUIDx registers contain a series of 63-bit number to identify the unique device in the family.

Address: 3000h base + FBh offset = 30FBh



* Notes:
- x = Undefined at reset.

SYS_UUID4 field descriptions

Field	Description
ID[39:32]	Universally Unique Identifier

6.6.15 Universally Unique Identifier Register 5 (SYS_UUID5)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FCh offset = 30FCh

Bit	7	6	5	4	3	2	1	0
Read	ID[31:24]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID5 field descriptions

Field	Description
ID[31:24]	Universally Unique Identifier

6.6.16 Universally Unique Identifier Register 6 (SYS_UUID6)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FDh offset = 30FDh

Bit	7	6	5	4	3	2	1	0
Read	ID[23:16]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID6 field descriptions

Field	Description
ID[23:16]	Universally Unique Identifier

6.6.17 Universally Unique Identifier Register 7 (SYS_UUID7)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FEh offset = 30FEh

Bit	7	6	5	4	3	2	1	0
Read	ID[15:8]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID7 field descriptions

Field	Description
ID[15:8]	Universally Unique Identifier

6.6.18 Universally Unique Identifier Register 8 (SYS_UUID8)

The read-only SYS_UUIDx registers contain a series of 64-bit number to identify the unique device in the family.

Address: 3000h base + FFh offset = 30FFh

Bit	7	6	5	4	3	2	1	0
Read	ID[7:0]							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x = Undefined at reset.

SYS_UUID8 field descriptions

Field	Description
ID[7:0]	Universally Unique Identifier

Chapter 7
Parallel input/output

7.1 Introduction

This device has eight sets of I/O ports, which include up to 57 general-purpose I/O pins.

Not all pins are available on all devices. See Table 2-1 to determine which functions are available for a specific device.

Many of the I/O pins are shared with on-chip peripheral functions, as shown in Table 2-1. The peripheral modules have priority over the I/O, so when a peripheral is enabled, the associated I/O functions are disabled.

After reset, the shared peripheral functions are disabled so that the pins are controlled by the parallel I/O except PTA4 and PTA5 that are default to BKGD/MS and $\overline{\text{RESET}}$ function. All of the parallel I/O are configured as high-impedance (Hi-Z). The pin control functions for each pin are configured as follows:

- input disabled (PTxIEn = 0),
- output disabled (PTxOEn = 0), and
- internal pullups disabled (PTxPEn = 0).

Additionally, the parallel I/O that support high drive capability are disabled (HDRVE = 0x00) after reset.

The following figures show the structures of each I/O pin.

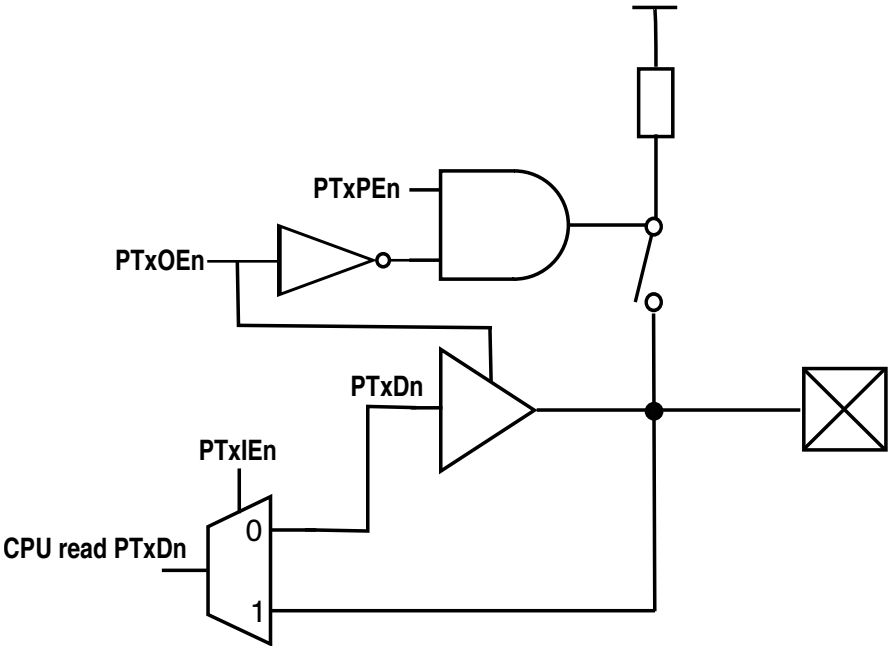


Figure 7-1. Normal I/O structure

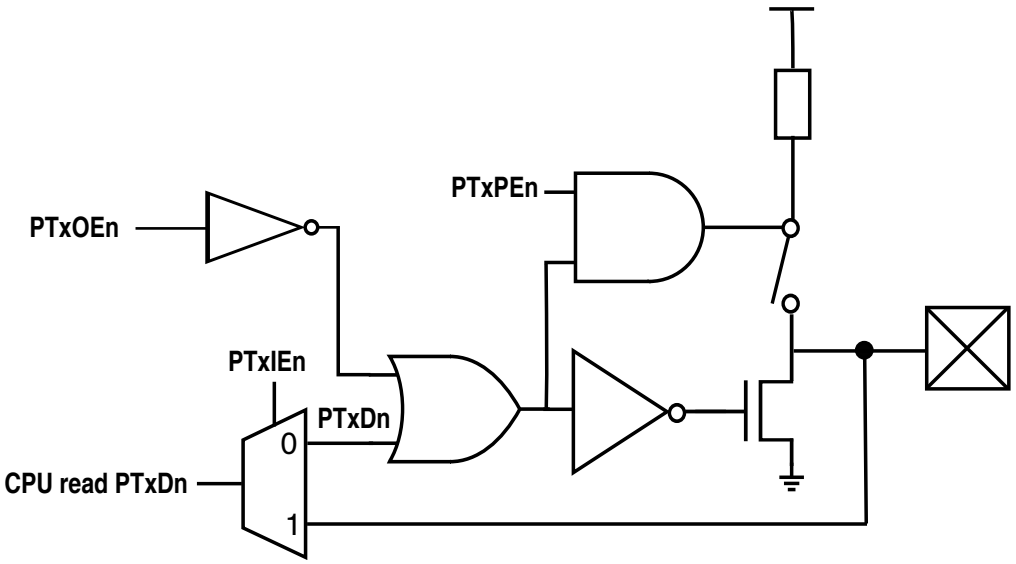


Figure 7-2. SDA(PTA2)/SCL(PTA3) structure

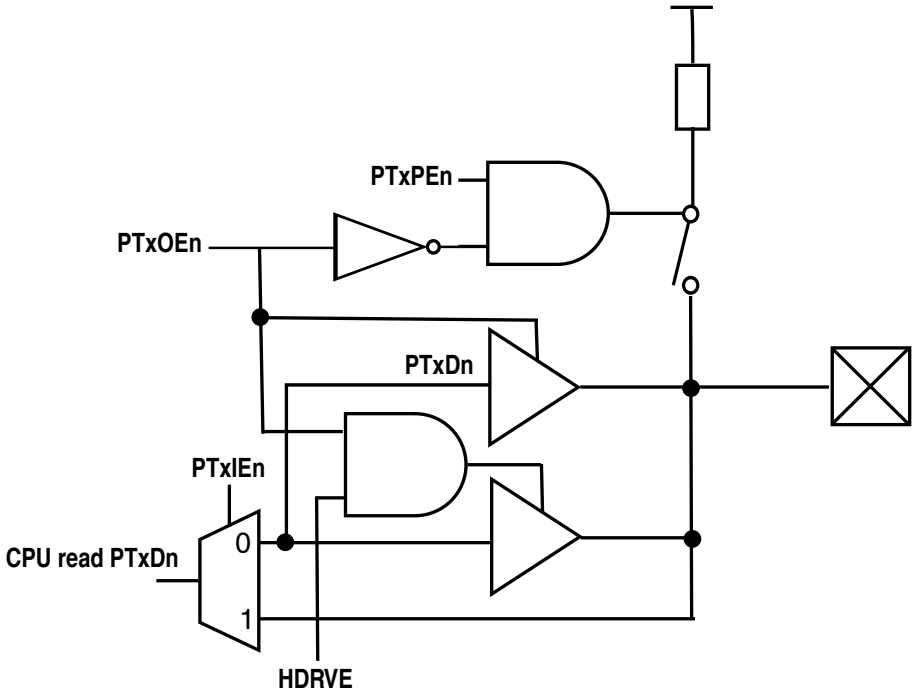


Figure 7-3. High drive I/O structure

7.2 Port data and data direction

Reading and writing of parallel I/O is accomplished through the port data registers (PTxD). The direction, input or output, is controlled through the input enable or output enable registers.

After reset, all parallel I/O default to the Hi-Z state. The corresponding bit in output enable register (PTxOE) or input enable register (PTxIE) must be configured for output or input operation. Each port pin has an input enable bit and an output enable bit. When PTxIEn = 1, a read from PTxDn returns the input value of the associated pin; when PTxIEn = 0, a read from PTxDn returns the last value written to the port data register.

NOTE

The PTxOE must be clear when the corresponding pin is used as input function to avoid contention. If set the corresponding PTxOE and PTxIE bits at same time, read from PTxDn will always return the output data.

When a peripheral module or system function is in control of a port pin, the data direction register bit still controls what is returned for reads of the port data register, even though the peripheral system has overriding control of the actual pin direction.

When a shared analog function is enabled for a pin, all digital pin functions are disabled. A read of the port data register returns a value of 0 for any bits that have shared analog functions enabled. In general, whenever a pin is shared with both an alternate digital function and an analog function, the analog function has priority such that if both of the digital and analog functions are enabled, the analog function controls the pin.

A write of valid data to a port data register must occur before setting the output enable bit of an associated port pin. This ensures that the pin will not be driven with an incorrect data value.

7.3 Internal pullup enable

An internal pullup device can be enabled for each port pin by setting the corresponding bit in one of the pullup enable registers (PTxPEn). The internal pullup device is disabled if the pin is configured as an output by the parallel I/O control logic, or by any shared peripheral function, regardless of the state of the corresponding pullup enable register bit. The internal pullup device is also disabled if the pin is controlled by an analog function.

NOTE

When configuring IIC to use "SDA(PTA2) and SCL(PTA3)" pins, and if an application uses internal pullups instead of external pullups, the internal pullups remain present setting when the pins are configured as outputs, but they are automatically disabled to save power when the output values are low.

7.4 Input glitch filter setting

A filter is implemented for each port pin that is configured as a digital input. It can be used as a simple low-pass filter to filter any glitch that is introduced from the pins of GPIO, IRQ,$\overline{\text{RESET}}$, and KBI. The glitch width threshold can be adjusted easily by setting registers PORT_IOFLTn and PORT_FCLKDIV between 1~4096 BUSCLKs (or 1~128 LPOCLKs). This configurable glitch filter can take the place of an on board external analog filter, and greatly improve the EMC performance.

Setting register PORT_IOFLTn can configure the filter of the whole port, etc. set PORT_IOFLT0[FLTA] will affect all PTAn pins.

7.5 High current drive

Output high sink/source current drive can be enabled by setting the corresponding bit in the HDRVE register for PTH1, PTH0, PTE1, PTE0, PTD1, PTD0, PTB5 and PTB4. Output high sink/source current when they are operated as output. High current drive function is disabled if the pin is configured as an input by the parallel I/O control logic. When configured as any shared peripheral function, high current drive function still works on these pins, but only when they are configured as outputs.

7.6 Pin behavior in stop mode

In stop3 mode, all I/O is maintained because internal logic circuitry stays powered up. Upon recovery, normal I/O function is available to the user.

7.7 Port data registers

PORT memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	Port A Data Register (PORT_PTAD)	8	R/W	00h	7.7.1/160
1	Port B Data Register (PORT_PTBD)	8	R/W	00h	7.7.2/161
2	Port C Data Register (PORT_PTCD)	8	R/W	00h	7.7.3/161
3	Port D Data Register (PORT_PTDD)	8	R/W	00h	7.7.4/162
4	Port E Data Register (PORT_PTED)	8	R/W	00h	7.7.5/162
5	Port F Data Register (PORT_PTFD)	8	R/W	00h	7.7.6/163
6	Port G Data Register (PORT_PTGD)	8	R/W	00h	7.7.7/163
7	Port H Data Register (PORT_PTHD)	8	R/W	00h	7.7.8/164
30AF	Port High Drive Enable Register (PORT_HDRVE)	8	R/W	00h	7.7.9/165
30B0	Port A Output Enable Register (PORT_PTAOE)	8	R/W	00h	7.7.10/166
30B1	Port B Output Enable Register (PORT_PTBOE)	8	R/W	00h	7.7.11/167
30B2	Port C Output Enable Register (PORT_PTCOE)	8	R/W	00h	7.7.12/168
30B3	Port D Output Enable Register (PORT_PTDOE)	8	R/W	00h	7.7.13/170
30B4	Port E Output Enable Register (PORT_PTEOE)	8	R/W	00h	7.7.14/171
30B5	Port F Output Enable Register (PORT_PTFOE)	8	R/W	00h	7.7.15/172
30B6	Port G Output Enable Register (PORT_PTGOE)	8	R/W	00h	7.7.16/173
30B7	Port H Output Enable Register (PORT_PTHOE)	8	R/W	00h	7.7.17/174

Table continues on the next page...

PORT memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
30B8	Port A Input Enable Register (PORT_PTAIE)	8	R/W	00h	7.7.18/175
30B9	Port B Input Enable Register (PORT_PTBIE)	8	R/W	00h	7.7.19/176
30BA	Port C Input Enable Register (PORT_PTCIE)	8	R/W	00h	7.7.20/177
30BB	Port D Input Enable Register (PORT_PTDIE)	8	R/W	00h	7.7.21/179
30BC	Port E Input Enable Register (PORT_PTEIE)	8	R/W	00h	7.7.22/180
30BD	Port F Input Enable Register (PORT_PTFIE)	8	R/W	00h	7.7.23/181
30BE	Port G Input Enable Register (PORT_PTGIE)	8	R/W	00h	7.7.24/182
30BF	Port H Input Enable Register (PORT_PTHIE)	8	R/W	00h	7.7.25/183
30EC	Port Filter Register 0 (PORT_IOFLT0)	8	R/W	00h	7.7.26/184
30ED	Port Filter Register 1 (PORT_IOFLT1)	8	R/W	00h	7.7.27/185
30EE	Port Filter Register 2 (PORT_IOFLT2)	8	R/W	00h	7.7.28/186
30EF	Port Clock Division Register (PORT_FCLKDIV)	8	R/W	00h	7.7.29/187
30F0	Port A Pullup Enable Register (PORT_PTAPE)	8	R/W	00h	7.7.30/188
30F1	Port B Pullup Enable Register (PORT_PTBPE)	8	R/W	00h	7.7.31/189
30F2	Port C Pullup Enable Register (PORT_PTCPE)	8	R/W	00h	7.7.32/190
30F3	Port D Pullup Enable Register (PORT_PTDPE)	8	R/W	00h	7.7.33/192
30F4	Port E Pullup Enable Register (PORT_PTEPE)	8	R/W	00h	7.7.34/193
30F5	Port F Pullup Enable Register (PORT_PTFPE)	8	R/W	00h	7.7.35/194
30F6	Port G Pullup Enable Register (PORT_PTGPE)	8	R/W	00h	7.7.36/196
30F7	Port H Pullup Enable Register (PORT_PTHPE)	8	R/W	00h	7.7.37/197

7.7.1 Port A Data Register (PORT_PTAD)

Address: 0h base + 0h offset = 0h

Bit	7	6	5	4	3	2	1	0
Read Write	PTAD							
Reset	0	0	0	0	0	0	0	0

PORT_PTAD field descriptions

Field	Description
PTAD	Port A Data Register Bits For port A pins that are configured as inputs, a read returns the logic level on the pin. For port A pins that are configured as outputs, a read returns the last value that was written to this register. For port A pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port A pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin.

PORT_PTAD field descriptions (continued)

Field	Description
	Reset forces PTAD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.2 Port B Data Register (PORT_PTBD)

Address: 0h base + 1h offset = 1h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBD							
Reset	0	0	0	0	0	0	0	0

PORT_PTBD field descriptions

Field	Description
PTBD	Port B Data Register Bits For port B pins that are configured as inputs, a read returns the logic level on the pin. For port B pins that are configured as outputs, a read returns the last value that was written to this register. For port B pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port B pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTBD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.3 Port C Data Register (PORT_PTCD)

Address: 0h base + 2h offset = 2h

Bit	7	6	5	4	3	2	1	0
Read Write	PTCD							
Reset	0	0	0	0	0	0	0	0

PORT_PTCD field descriptions

Field	Description
PTCD	Port C Data Register Bits For port C pins that are configured as inputs, a read returns the logic level on the pin. For port C pins that are configured as outputs, a read returns the last value that was written to this register. For port C pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port C pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin.

PORT_PTCD field descriptions (continued)

Field	Description
	Reset forces PTCD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.4 Port D Data Register (PORT_PTDD)

Address: 0h base + 3h offset = 3h

Bit	7	6	5	4	3	2	1	0
Read Write	PTDD							
Reset	0	0	0	0	0	0	0	0

PORT_PTDD field descriptions

Field	Description
PTDD	Port D Data Register Bits For port D pins that are configured as inputs, a read returns the logic level on the pin. For port D pins that are configured as outputs, a read returns the last value that was written to this register. For port D pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port D pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTDD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.5 Port E Data Register (PORT_PTED)

Address: 0h base + 4h offset = 4h

Bit	7	6	5	4	3	2	1	0
Read Write	PTED							
Reset	0	0	0	0	0	0	0	0

PORT_PTED field descriptions

Field	Description
PTED	Port E Data Register Bits For port E pins that are configured as inputs, a read returns the logic level on the pin. For port E pins that are configured as outputs, a read returns the last value that was written to this register. For port E pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port E pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin.

PORT_PTED field descriptions (continued)

Field	Description
	Reset forces PTED to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.6 Port F Data Register (PORT_PTFD)

Address: 0h base + 5h offset = 5h

Bit	7	6	5	4	3	2	1	0
Read Write	PTFD							
Reset	0	0	0	0	0	0	0	0

PORT_PTFD field descriptions

Field	Description
PTFD	Port F Data Register Bits For port F pins that are configured as inputs, a read returns the logic level on the pin. For port F pins that are configured as outputs, a read returns the last value that was written to this register. For port F pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port F pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTFD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.7 Port G Data Register (PORT_PTGD)

Address: 0h base + 6h offset = 6h

Bit	7	6	5	4	3	2	1	0
Read	0				PTGD			
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTGD field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PTGD	Port G Data Register Bits For port G pins that are configured as inputs, a read returns the logic level on the pin. For port G pins that are configured as outputs, a read returns the last value that was written to this register.

Table continues on the next page...

PORT_PTGD field descriptions (continued)

Field	Description
	For port G pins that are configured as Hi-Z, a read returns uncertainty data. Writes are latched into all bits of this register. For port G pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin. Reset forces PTGD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

7.7.8 Port H Data Register (PORT_PTHD)

For port H pins that are configured as inputs, a read returns the logic level on the pin.

For port H pins that are configured as outputs, a read returns the last value that was written to this register.

For port H pins that are configured as Hi-Z, a read returns uncertainty data.

Writes are latched into all bits of this register. For port H pins that are configured as outputs, the logic level is driven out of the corresponding MCU pin.

Reset forces PTHD to all 0s, but these 0s are not driven out of the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.

Address: 0h base + 7h offset = 7h

Bit	7	6	5	4	3	2	1	0
Read	PTHD7	PTHD6	0			PTHD2	PTHD1	PTHD0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTHD field descriptions

Field	Description
7 PTHD7	Port H Data Register Bit 7
6 PTHD6	Port H Data Register Bit 6
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 PTHD2	Port H Data Register Bit 2
1 PTHD1	Port H Data Register Bit 1
0 PTHD0	Port H Data Register Bit 0

7.7.9 Port High Drive Enable Register (PORT_HDRVE)

Address: 0h base + 30AFh offset = 30AFh

Bit	7	6	5	4	3	2	1	0
Read Write	PTH1	PTH0	PTE1	PTE0	PTD1	PTD0	PTB5	PTB4
Reset	0	0	0	0	0	0	0	0

PORT_HDRVE field descriptions

Field	Description
7 PTH1	PTH1 This read/write bit enables the high current drive capability of PTH1 0 PTH1 is disabled to offer high current drive capability. 1 PTH1 is enabled to offer high current drive capability.
6 PTH0	PTH0 This read/write bit enables the high current drive capability of PTH0 0 PTH0 is disabled to offer high current drive capability. 1 PTH0 is enabled to offer high current drive capability.
5 PTE1	PTE1 This read/write bit enables the high current drive capability of PTE1 0 PTE1 is disabled to offer high current drive capability. 1 PTE1 is enabled to offer high current drive capability.
4 PTE0	PTE0 This read/write bit enables the high current drive capability of PTE0 0 PTE0 is disabled to offer high current drive capability. 1 PTE0 is enable to offer high current drive capability.
3 PTD1	PTD1 This read/write bit enables the high current drive capability of PTD1 0 PTD1 is disabled to offer high current drive capability. 1 PTD1 is enable to offer high current drive capability.
2 PTD0	PTD0 This read/write bit enables the high current drive capability of PTD0 0 PTD0 is disabled to offer high current drive capability. 1 PTD0 is enable to offer high current drive capability.
1 PTB5	PTB5 This read/write bit enables the high current drive capability of PTB5

Table continues on the next page...

PORT_HDRVE field descriptions (continued)

Field	Description
	0 PTB5 is disabled to offer high current drive capability. 1 PTB5 is enable to offer high current drive capability.
0 PTB4	PTB4 This read/write bit enables the high current drive capability of PTB4 0 PTB4 is disabled to offer high current drive capability. 1 PTB4 is enable to offer high current drive capability.

7.7.10 Port A Output Enable Register (PORT_PTAOE)

Address: 0h base + 30B0h offset = 30B0h

Bit	7	6	5	4	3	2	1	0
Read Write	PTAOE7	PTAOE6	PTAOE5	PTAOE4	PTAOE3	PTAOE2	PTAOE1	PTAOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTAOE field descriptions

Field	Description
7 PTAOE7	Output Enable for Port A Bit 7 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 7. 1 Output Enabled for port A bit 7.
6 PTAOE6	Output Enable for Port A Bit 6 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 6. 1 Output Enabled for port A bit 6.
5 PTAOE5	Output Enable for Port A Bit 5 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 5. 1 Output Enabled for port A bit 5.
4 PTAOE4	Output Enable for Port A Bit 4 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 4. 1 Output Enabled for port A bit 4.
3 PTAOE3	Output Enable for Port A Bit 3 This read/write bit enables the port A pin as an output.

Table continues on the next page...

PORT_PTAOE field descriptions (continued)

Field	Description
	0 Output Disabled for port A bit 3. 1 Output Enabled for port A bit 3.
2 PTAOE2	Output Enable for Port A Bit 2 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 2. 1 Output Enabled for port A bit 2.
1 PTAOE1	Output Enable for Port A Bit 1 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 1. 1 Output Enabled for port A bit 1.
0 PTAOE0	Output Enable for Port A Bit 0 This read/write bit enables the port A pin as an output. 0 Output Disabled for port A bit 0. 1 Output Enabled for port A bit 0.

7.7.11 Port B Output Enable Register (PORT_PTBOE)

Address: 0h base + 30B1h offset = 30B1h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBOE7	PTBOE6	PTBOE5	PTBOE4	PTBOE3	PTBOE2	PTBOE1	PTBOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTBOE field descriptions

Field	Description
7 PTBOE7	Output Enable for Port B Bit 7 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 7. 1 Output Enabled for port B bit 7.
6 PTBOE6	Output Enable for Port B Bit 6 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 6. 1 Output Enabled for port B bit 6.
5 PTBOE5	Output Enable for Port B Bit 5 This read/write bit enables the port B pin as an output.

Table continues on the next page...

PORT_PTBOE field descriptions (continued)

Field	Description
	0 Output Disabled for port B bit 5. 1 Output Enabled for port B bit 5.
4 PTBOE4	Output Enable for Port B Bit 4 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 4. 1 Output Enabled for port B bit 4.
3 PTBOE3	Output Enable for Port B Bit 3 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 3. 1 Output Enabled for port B bit 3.
2 PTBOE2	Output Enable for Port B Bit 2 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 2. 1 Output Enabled for port B bit 2.
1 PTBOE1	Output Enable for Port B Bit 1 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 1. 1 Output Enabled for port B bit 1.
0 PTBOE0	Output Enable for Port B Bit 0 This read/write bit enables the port B pin as an output. 0 Output Disabled for port B bit 0. 1 Output Enabled for port B bit 0.

7.7.12 Port C Output Enable Register (PORT_PTCOE)

Address: 0h base + 30B2h offset = 30B2h

Bit	7	6	5	4	3	2	1	0
Read Write	PTCOE7	PTCOE6	PTCOE5	PTCOE4	PTCOE3	PTCOE2	PTCOE1	PTCOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTCOE field descriptions

Field	Description
7 PTCOE7	Output Enable for Port C Bit 7 This read/write bit enables the port C pin as an output.

Table continues on the next page...

PORT_PTCOE field descriptions (continued)

Field	Description
	0 Output Disabled for port C bit 7. 1 Output Enabled for port C bit 7.
6 PTCOE6	Output Enable for Port C Bit 6 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 6. 1 Output Enabled for port C bit 6.
5 PTCOE5	Output Enable for Port C Bit 5 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 5. 1 Output Enabled for port C bit 5.
4 PTCOE4	Output Enable for Port C Bit 4 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 4. 1 Output Enabled for port C bit 4.
3 PTCOE3	Output Enable for Port C Bit 3 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 3. 1 Output Enabled for port C bit 3.
2 PTCOE2	Output Enable for Port C Bit 2 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 2. 1 Output Enabled for port C bit 2.
1 PTCOE1	Output Enable for Port C Bit 1 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 1. 1 Output Enabled for port C bit 1.
0 PTCOE0	Output Enable for Port C Bit 0 This read/write bit enables the port C pin as an output. 0 Output Disabled for port C bit 0. 1 Output Enabled for port C bit 0.

7.7.13 Port D Output Enable Register (PORT_PTDOE)

Address: 0h base + 30B3h offset = 30B3h

Bit	7	6	5	4	3	2	1	0
Read Write	PTDOE7	PTDOE6	PTDOE5	PTDOE4	PTDOE3	PTDOE2	PTDOE1	PTDOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTDOE field descriptions

Field	Description
7 PTDOE7	Output Enable for Port D Bit 7 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 7. 1 Output Enabled for port D bit 7.
6 PTDOE6	Output Enable for Port D Bit 6 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 6. 1 Output Enabled for port D bit 6.
5 PTDOE5	Output Enable for Port D Bit 5 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 5. 1 Output Enabled for port D bit 5.
4 PTDOE4	Output Enable for Port D Bit 4 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 4. 1 Output Enabled for port D bit 4.
3 PTDOE3	Output Enable for Port D Bit 3 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 3. 1 Output Enabled for port D bit 3.
2 PTDOE2	Output Enable for Port D Bit 2 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 2. 1 Output Enabled for port D bit 2.
1 PTDOE1	Output Enable for Port D Bit 1 This read/write bit enables the port D pin as an output.

Table continues on the next page...

PORT_PTDOE field descriptions (continued)

Field	Description
	0 Output Disabled for port D bit 1. 1 Output Enabled for port D bit 1.
0 PTDOE0	Output Enable for Port D Bit 0 This read/write bit enables the port D pin as an output. 0 Output Disabled for port D bit 0. 1 Output Enabled for port D bit 0.

7.7.14 Port E Output Enable Register (PORT_PTEOE)

Address: 0h base + 30B4h offset = 30B4h

Bit	7	6	5	4	3	2	1	0
Read Write	PTEOE7	PTEOE6	PTEOE5	PTEOE4	PTEOE3	PTEOE2	PTEOE1	PTEOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTEOE field descriptions

Field	Description
7 PTEOE7	Output Enable for Port E Bit 7 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 7. 1 Output Enabled for port E bit 7.
6 PTEOE6	Output Enable for Port E Bit 6 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 6. 1 Output Enabled for port E bit 6.
5 PTEOE5	Output Enable for Port E Bit 5 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 5. 1 Output Enabled for port E bit 5.
4 PTEOE4	Output Enable for Port E Bit 4 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 4. 1 Output Enabled for port E bit 4.
3 PTEOE3	Output Enable for Port E Bit 3 This read/write bit enables the port E pin as an output.

Table continues on the next page...

PORT_PTEOE field descriptions (continued)

Field	Description
	0 Output Disabled for port E bit 3. 1 Output Enabled for port E bit 3.
2 PTEOE2	Output Enable for Port E Bit 2 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 2. 1 Output Enabled for port E bit 2.
1 PTEOE1	Output Enable for Port E Bit 1 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 1. 1 Output Enabled for port E bit 1.
0 PTEOE0	Output Enable for Port E Bit 0 This read/write bit enables the port E pin as an output. 0 Output Disabled for port E bit 0. 1 Output Enabled for port E bit 0.

7.7.15 Port F Output Enable Register (PORT_PTFOE)

Address: 0h base + 30B5h offset = 30B5h

Bit	7	6	5	4	3	2	1	0
Read Write	PTFOE7	PTFOE6	PTFOE5	PTFOE4	PTFOE3	PTFOE2	PTFOE1	PTFOE0
Reset	0	0	0	0	0	0	0	0

PORT_PTFOE field descriptions

Field	Description
7 PTFOE7	Output Enable for Port F Bit 7 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 7. 1 Output Enabled for port F bit 7.
6 PTFOE6	Output Enable for Port F Bit 6 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 6. 1 Output Enabled for port F bit 6.
5 PTFOE5	Output Enable for Port F Bit 5 This read/write bit enables the port F pin as an output.

Table continues on the next page...

PORT_PTFOE field descriptions (continued)

Field	Description
	0 Output Disabled for port F bit 5. 1 Output Enabled for port F bit 5.
4 PTFOE4	Output Enable for Port F Bit 4 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 4. 1 Output Enabled for port F bit 4.
3 PTFOE3	Output Enable for Port F Bit 3 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 3. 1 Output Enabled for port F bit 3.
2 PTFOE2	Output Enable for Port F Bit 2 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 2. 1 Output Enabled for port F bit 2.
1 PTFOE1	Output Enable for Port F Bit 1 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 1. 1 Output Enabled for port F bit 1.
0 PTFOE0	Output Enable for Port F Bit 0 This read/write bit enables the port F pin as an output. 0 Output Disabled for port F bit 0. 1 Output Enabled for port F bit 0.

7.7.16 Port G Output Enable Register (PORT_PTGOE)

Address: 0h base + 30B6h offset = 30B6h

Bit	7	6	5	4	3	2	1	0
Read	0				PTGOE3	PTGOE2	PTGOE1	PTGOE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTGOE field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

PORT_PTGOE field descriptions (continued)

Field	Description
3 PTGOE3	Output Enable for Port G Bit 3 This read/write bit enables the port G pin as an output. 0 Output Disabled for port G bit 3. 1 Output Enabled for port G bit 3.
2 PTGOE2	Output Enable for Port G Bit 2 This read/write bit enables the port G pin as an output. 0 Output Disabled for port G bit 2. 1 Output Enabled for port G bit 2.
1 PTGOE1	Output Enable for Port G Bit 1 This read/write bit enables the port G pin as an output. 0 Output Disabled for port G bit 1. 1 Output Enabled for port G bit 1.
0 PTGOE0	Output Enable for Port G Bit 0 This read/write bit enables the port G pin as an output. 0 Output Disabled for port G bit 0. 1 Output Enabled for port G bit 0.

7.7.17 Port H Output Enable Register (PORT_PTHOE)

Address: 0h base + 30B7h offset = 30B7h

Bit	7	6	5	4	3	2	1	0
Read	PTHOE7	PTHOE6	0			PTHOE2	PTHOE1	PTHOE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTHOE field descriptions

Field	Description
7 PTHOE7	Output Enable for Port H Bit 7 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 7. 1 Output Enabled for port H bit 7.
6 PTHOE6	Output Enable for Port H Bit 6 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 6. 1 Output Enabled for port H bit 6.

Table continues on the next page...

PORT_PTHOE field descriptions (continued)

Field	Description
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 PTHOE2	Output Enable for Port H Bit 2 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 2. 1 Output Enabled for port H bit 2.
1 PTHOE1	Output Enable for Port H Bit 1 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 1. 1 Output Enabled for port H bit 1.
0 PTHOE0	Output Enable for Port H Bit 0 This read/write bit enables the port H pin as an output. 0 Output Disabled for port H bit 0. 1 Output Enabled for port H bit 0.

7.7.18 Port A Input Enable Register (PORT_PTAIE)

Address: 0h base + 30B8h offset = 30B8h

Bit	7	6	5	4	3	2	1	0
Read	PTAIE7	PTAIE6	PTAIE5	0	PTAIE3	PTAIE2	PTAIE1	PTAIE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAIE field descriptions

Field	Description
7 PTAIE7	Input Enable for Port A Bit 7 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 7. 1 Input enabled for port A bit 7.
6 PTAIE6	Input Enable for Port A Bit 6 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 6. 1 Input enabled for port A bit 6.
5 PTAIE5	Input Enable for Port A Bit 5 This read/write bit enables the port A pin as an input.

Table continues on the next page...

PORT_PTAIE field descriptions (continued)

Field	Description
	0 Input disabled for port A bit 5. 1 Input enabled for port A bit 5.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTAIE3	Input Enable for Port A Bit 3 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 3. 1 Input enabled for port A bit 3.
2 PTAIE2	Input Enable for Port A Bit 2 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 2. 1 Input enabled for port A bit 2.
1 PTAIE1	Input Enable for Port A Bit 1 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 1. 1 Input enabled for port A bit 1.
0 PTAIE0	Input Enable for Port A Bit 0 This read/write bit enables the port A pin as an input. 0 Input disabled for port A bit 0. 1 Input enabled for port A bit 0.

7.7.19 Port B Input Enable Register (PORT_PTBIE)

Address: 0h base + 30B9h offset = 30B9h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBIE7	PTBIE6	PTBIE5	PTBIE4	PTBIE3	PTBIE2	PTBIE1	PTBIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTBIE field descriptions

Field	Description
7 PTBIE7	Input Enable for Port B Bit 7 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 7. 1 Input enabled for port B bit 7.
6 PTBIE6	Input Enable for Port B Bit 6

Table continues on the next page...

PORT_PTBIE field descriptions (continued)

Field	Description
	This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 6. 1 Input enabled for port B bit 6.
5 PTBIE5	Input Enable for Port B Bit 5 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 5. 1 Input enabled for port B bit 5.
4 PTBIE4	Input Enable for Port B Bit 4 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 4. 1 Input enabled for port B bit 4.
3 PTBIE3	Input Enable for Port B Bit 3 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 3. 1 Input enabled for port B bit 3.
2 PTBIE2	Input Enable for Port B Bit 2 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 2. 1 Input enabled for port B bit 2.
1 PTBIE1	Input Enable for Port B Bit 1 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 1. 1 Input enabled for port B bit 1.
0 PTBIE0	Input Enable for Port B Bit 0 This read/write bit enables the port B pin as an input. 0 Input disabled for port B bit 0. 1 Input enabled for port B bit 0.

7.7.20 Port C Input Enable Register (PORT_PTCIE)

Address: 0h base + 30BAh offset = 30BAh

Bit	7	6	5	4	3	2	1	0
Read Write	PTCIE7	PTCIE6	PTCIE5	PTCIE4	PTCIE3	PTCIE2	PTCIE1	PTCIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTCIE field descriptions

Field	Description
7 PTCIE7	Input Enable for Port C Bit 7 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 7. 1 Input enabled for port C bit 7.
6 PTCIE6	Input Enable for Port C Bit 6 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 6. 1 Input enabled for port C bit 6.
5 PTCIE5	Input Enable for Port C Bit 5 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 5. 1 Input enabled for port C bit 5.
4 PTCIE4	Input Enable for Port C Bit 4 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 4. 1 Input enabled for port C bit 4.
3 PTCIE3	Input Enable for Port C Bit 3 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 3. 1 Input enabled for port C bit 3.
2 PTCIE2	Input Enable for Port C Bit 2 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 2. 1 Input enabled for port C bit 2.
1 PTCIE1	Input Enable for Port C Bit 1 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 1. 1 Input enabled for port C bit 1.
0 PTCIE0	Input Enable for Port C Bit 0 This read/write bit enables the port C pin as an input. 0 Input disabled for port C bit 0. 1 Input enabled for port C bit 0.

7.7.21 Port D Input Enable Register (PORT_PTDIE)

Address: 0h base + 30BBh offset = 30BBh

Bit	7	6	5	4	3	2	1	0
Read Write	PTDIE7	PTDIE6	PTDIE5	PTDIE4	PTDIE3	PTDIE2	PTDIE1	PTDIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTDIE field descriptions

Field	Description
7 PTDIE7	Input Enable for Port D Bit 7 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 7. 1 Input enabled for port D bit 7.
6 PTDIE6	Input Enable for Port D Bit 6 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 6. 1 Input enabled for port D bit 6.
5 PTDIE5	Input Enable for Port D Bit 5 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 5. 1 Input enabled for port D bit 5.
4 PTDIE4	Input Enable for Port D Bit 4 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 4. 1 Input enabled for port D bit 4.
3 PTDIE3	Input Enable for Port D Bit 3 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 3. 1 Input enabled for port D bit 3.
2 PTDIE2	Input Enable for Port D Bit 2 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 2. 1 Input enabled for port D bit 2.
1 PTDIE1	Input Enable for Port D Bit 1 This read/write bit enables the port D pin as an input.

Table continues on the next page...

PORT_PTDIE field descriptions (continued)

Field	Description
	0 Input disabled for port D bit 1. 1 Input enabled for port D bit 1.
0 PTDIE0	Input Enable for Port D Bit 0 This read/write bit enables the port D pin as an input. 0 Input disabled for port D bit 0. 1 Input enabled for port D bit 0.

7.7.22 Port E Input Enable Register (PORT_PTEIE)

Address: 0h base + 30BCh offset = 30BCh

Bit	7	6	5	4	3	2	1	0
Read Write	PTEIE7	PTEIE6	PTEIE5	PTEIE4	PTEIE3	PTEIE2	PTEIE1	PTEIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTEIE field descriptions

Field	Description
7 PTEIE7	Input Enable for Port E Bit 7 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 7. 1 Input enabled for port E bit 7.
6 PTEIE6	Input Enable for Port E Bit 6 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 6. 1 Input enabled for port E bit 6.
5 PTEIE5	Input Enable for Port E Bit 5 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 5. 1 Input enabled for port E bit 5.
4 PTEIE4	Input Enable for Port E Bit 4 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 4. 1 Input enabled for port E bit 4.
3 PTEIE3	Input Enable for Port E Bit 3 This read/write bit enables the port E pin as an input.

Table continues on the next page...

PORT_PTEIE field descriptions (continued)

Field	Description
	0 Input disabled for port E bit 3. 1 Input enabled for port E bit 3.
2 PTEIE2	Input Enable for Port E Bit 2 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 2. 1 Input enabled for port E bit 2.
1 PTEIE1	Input Enable for Port E Bit 1 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 1. 1 Input enabled for port E bit 1.
0 PTEIE0	Input Enable for Port E Bit 0 This read/write bit enables the port E pin as an input. 0 Input disabled for port E bit 0. 1 Input enabled for port E bit 0.

7.7.23 Port F Input Enable Register (PORT_PTFIE)

Address: 0h base + 30BDh offset = 30BDh

Bit	7	6	5	4	3	2	1	0
Read Write	PTFIE7	PTFIE6	PTFIE5	PTFIE4	PTFIE3	PTFIE2	PTFIE1	PTFIE0
Reset	0	0	0	0	0	0	0	0

PORT_PTFIE field descriptions

Field	Description
7 PTFIE7	Input Enable for Port F Bit 7 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 7. 1 Input enabled for port F bit 7.
6 PTFIE6	Input Enable for Port F Bit 6 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 6. 1 Input enabled for port F bit 6.
5 PTFIE5	Input Enable for Port F Bit 5 This read/write bit enables the port F pin as an input.

Table continues on the next page...

PORT_PTFIE field descriptions (continued)

Field	Description
	0 Input disabled for port F bit 5. 1 Input enabled for port F bit 5.
4 PTFIE4	Input Enable for Port F Bit 4 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 4. 1 Input enabled for port F bit 4.
3 PTFIE3	Input Enable for Port F Bit 3 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 3. 1 Input enabled for port F bit 3.
2 PTFIE2	Input Enable for Port F Bit 2 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 2. 1 Input enabled for port F bit 2.
1 PTFIE1	Input Enable for Port F Bit 1 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 1. 1 Input enabled for port F bit 1.
0 PTFIE0	Input Enable for Port F Bit 0 This read/write bit enables the port F pin as an input. 0 Input disabled for port F bit 0. 1 Input enabled for port F bit 0.

7.7.24 Port G Input Enable Register (PORT_PTGIE)

Address: 0h base + 30BEh offset = 30BEh

Bit	7	6	5	4	3	2	1	0
Read	0				PTGIE3	PTGIE2	PTGIE1	PTGIE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTGIE field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

PORT_PTGIE field descriptions (continued)

Field	Description
3 PTGIE3	Input Enable for Port G Bit 3 This read/write bit enables the port G pin as an input. 0 Input disabled for port G bit 3. 1 Input enabled for port G bit 3.
2 PTGIE2	Input Enable for Port G Bit 2 This read/write bit enables the port G pin as an input. 0 Input disabled for port G bit 2. 1 Input enabled for port G bit 2.
1 PTGIE1	Input Enable for Port G Bit 1 This read/write bit enables the port G pin as an input. 0 Input disabled for port G bit 1. 1 Input enabled for port G bit 1.
0 PTGIE0	Input Enable for Port G Bit 0 This read/write bit enables the port G pin as an input. 0 Input disabled for port G bit 0. 1 Input enabled for port G bit 0.

7.7.25 Port H Input Enable Register (PORT_PTHIE)

Address: 0h base + 30BFh offset = 30BFh

Bit	7	6	5	4	3	2	1	0
Read	PTHIE7	PTHIE6	0			PTHIE2	PTHIE1	PTHIE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTHIE field descriptions

Field	Description
7 PTHIE7	Input Enable for Port H Bit 7 This read/write bit enables the port H pin as an input. 0 Input disabled for port H bit 7. 1 Input enabled for port H bit 7.
6 PTHIE6	Input Enable for Port H Bit 6 This read/write bit enables the port H pin as an input. 0 Input disabled for port H bit 6. 1 Input enabled for port H bit 6.

Table continues on the next page...

PORT_PTHIE field descriptions (continued)

Field	Description
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 PTHIE2	Input Enable for Port H Bit 2 This read/write bit enables the port H pin as an input. 0 Input disabled for port H bit 2. 1 Input enabled for port H bit 2.
1 PTHIE1	Input Enable for Port H Bit 1 This read/write bit enables the port H pin as an input. 0 Input disabled for port H bit 1. 1 Input enabled for port H bit 1.
0 PTHIE0	Input Enable for Port H Bit 0 This read/write bit enables the port H pin as an input. 0 Input disabled for port H bit 0. 1 Input enabled for port H bit 0.

7.7.26 Port Filter Register 0 (PORT_IOFLT0)

This register sets the filters for input from PTA to PTD.

Address: 0h base + 30ECh offset = 30ECh

Bit	7	6	5	4	3	2	1	0
Read Write	FLTD		FLTC		FLTB		FLTA	
Reset	0	0	0	0	0	0	0	0

PORT_IOFLT0 field descriptions

Field	Description
7–6 FLTD	Filter selection for input from PTD 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
5–4 FLTC	Filter selection for input from PTC 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

Table continues on the next page...

PORT_IOFLT0 field descriptions (continued)

Field	Description
3–2 FLTB	Filter selection for input from PTB 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
FLTA	Filter selection for input from PTA 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

7.7.27 Port Filter Register 1 (PORT_IOFLT1)

This register sets the filters for input from PTE to PTH.

Address: 0h base + 30EDh offset = 30EDh

Bit	7	6	5	4	3	2	1	0
Read Write	FLTH		FLTG		FLTF		FLTE	
Reset	0	0	0	0	0	0	0	0

PORT_IOFLT1 field descriptions

Field	Description
7–6 FLTH	Filter selection for input from PTH 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
5–4 FLTG	Filter selection for input from PTG 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3
3–2 FLTF	Filter selection for input from PTF 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

Table continues on the next page...

PORT_IOFLT1 field descriptions (continued)

Field	Description
FLTE	Filter selection for input from PTE 00 BUSCLK 01 FLTDIV1 10 FLTDIV2 11 FLTDIV3

7.7.28 Port Filter Register 2 (PORT_IOFLT2)

This register sets the filters for input.

Address: 0h base + 30EEh offset = 30EEh

Bit	7	6	5	4	3	2	1	0
Read	0		FLTKBI1		FLTKBI0		FLTRST	
Write								
Reset	0	0	0	0	0	0	0	0

PORT_IOFLT2 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 FLTKBI1	Filter selection for input from KBI1 00 BUSCLK 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3
3–2 FLTKBI0	Filter selection for input from KBI0 00 BUSCLK 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3
FLTRST	Filter selection for input from RESET/IRQ 00 No filter. 01 Select FLTDIV1, and will switch to FLTDIV3 in stop mode automatically. 10 Select FLTDIV2, and will switch to FLTDIV3 in stop mode automatically. 11 FLTDIV3

7.7.29 Port Clock Division Register (PORT_FCLKDIV)

Configure the high/low level glitch width threshold. Glitches that are shorter than the selected clock width will be filtered out; glitches that are more than twice the selected clock width will not be filtered out (they will pass to the internal circuitry).

Address: 0h base + 30EFh offset = 30EFh

Bit	7	6	5	4	3	2	1	0
Read Write	FLTDIV3			FLTDIV2			FLTDIV1	
Reset	0	0	0	0	0	0	0	0

PORT_FCLKDIV field descriptions

Field	Description
7–5 FLTDIV3	Filter Division Set 3 Port Filter Division Set 3 000 LPOCLK. 001 LPOCLK/2. 010 LPOCLK/4. 011 LPOCLK/8. 100 LPOCLK/16. 101 LPOCLK/32. 110 LPOCLK/64. 111 LPOCLK/128.
4–2 FLTDIV2	Filter Division Set 2 Port Filter Division Set 2 000 BUSCLK/32. 001 BUSCLK/64. 010 BUSCLK/128. 011 BUSCLK/256. 100 BUSCLK/512. 101 BUSCLK/1024. 110 BUSCLK/2048. 111 BUSCLK/4096.
FLTDIV1	Filter Division Set 1 Port Filter Division Set 1 00 BUSCLK/2. 01 BUSCLK/4. 10 BUSCLK/8. 11 BUSCLK/16.

7.7.30 Port A Pullup Enable Register (PORT_PTAPE)

Address: 0h base + 30F0h offset = 30F0h

Bit	7	6	5	4	3	2	1	0
Read	PTAPE7	PTAPE6	PTAPE5	0	PTAPE3	PTAPE2	PTAPE1	PTAPE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTAPE field descriptions

Field	Description
7 PTAPE7	Pull Enable for Port A Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 7. 1 Pullup enabled for port A bit 7.
6 PTAPE6	Pull Enable for Port A Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 6. 1 Pullup enabled for port A bit 6.
5 PTAPE5	Pull Enable for Port A Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 5. 1 Pullup enabled for port A bit 5.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTAPE3	Pull Enable for Port A Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. **NOTE:** When configuring to use this pin as output high for IIC, the internal pullup device remains active when PTAPE3 is set. It is automatically disabled to save power when output low. 0 Pullup disabled for port A bit 3. 1 Pullup enabled for port A bit 3.
2 PTAPE2	Pull Enable for Port A Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. **NOTE:** When configuring to use this pin as output high for IIC, the internal pullup device remains active when PTAPE2 is set. It is automatically disabled to save power when output low.

Table continues on the next page...

PORT_PTAPE field descriptions (continued)

Field	Description
	0 Pullup disabled for port A bit 2. 1 Pullup enabled for port A bit 2.
1 PTAPE1	Pull Enable for Port A Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 1. 1 Pullup enabled for port A bit 1.
0 PTAPE0	Pull Enable for Port A Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTA pin. For port A pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port A bit 0. 1 Pullup enabled for port A bit 0.

7.7.31 Port B Pullup Enable Register (PORT_PTBPE)

Address: 0h base + 30F1h offset = 30F1h

Bit	7	6	5	4	3	2	1	0
Read Write	PTBPE7	PTBPE6	PTBPE5	PTBPE4	PTBPE3	PTBPE2	PTBPE1	PTBPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTBPE field descriptions

Field	Description
7 PTBPE7	Pull Enable for Port B Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 7. 1 Pullup enabled for port B bit 7.
6 PTBPE6	Pull Enable for Port B Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 6. 1 Pullup enabled for port B bit 6.
5 PTBPE5	Pull Enable for Port B Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 5. 1 Pullup enabled for port B bit 5.

Table continues on the next page...

PORT_PTBPE field descriptions (continued)

Field	Description
4 PTBPE4	Pull Enable for Port B Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 4. 1 Pullup enabled for port B bit 4.
3 PTBPE3	Pull Enable for Port B Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 3. 1 Pullup enabled for port B bit 3.
2 PTBPE2	Pull Enable for Port B Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 2. 1 Pullup enabled for port B bit 2.
1 PTBPE1	Pull Enable for Port B Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 1. 1 Pullup enabled for port B bit 1.
0 PTBPE0	Pull Enable for Port B Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTB pin. For port B pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port B bit 0. 1 Pullup enabled for port B bit 0.

7.7.32 Port C Pullup Enable Register (PORT_PTCPE)

Address: 0h base + 30F2h offset = 30F2h

Bit	7	6	5	4	3	2	1	0
Read Write	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTCPE field descriptions

Field	Description
7 PTCPE7	Pull Enable for Port C Bit 7

Table continues on the next page...

PORT_PTCPE field descriptions (continued)

Field	Description
	This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 7. 1 Pullup enabled for port C bit 7.
6 PTCPE6	Pull Enable for Port C Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 6. 1 Pullup enabled for port C bit 6.
5 PTCPE5	Pull Enable for Port C Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 5. 1 Pullup enabled for port C bit 5.
4 PTCPE4	Pull Enable for Port C Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 4. 1 Pullup enabled for port C bit 4.
3 PTCPE3	Pull Enable for Port C Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 3. 1 Pullup enabled for port C bit 3.
2 PTCPE2	Pull Enable for Port C Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 2. 1 Pullup enabled for port C bit 2.
1 PTCPE1	Pull Enable for Port C Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port C bit 1. 1 Pullup enabled for port C bit 1.
0 PTCPE0	Pull Enable for Port C Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs or Hi-Z, these bits have no effect.

Table continues on the next page...

PORT_PTCPE field descriptions (continued)

Field	Description
	0 Pullup disabled for port C bit 0. 1 Pullup enabled for port C bit 0.

7.7.33 Port D Pullup Enable Register (PORT_PTDPE)

Address: 0h base + 30F3h offset = 30F3h

Bit	7	6	5	4	3	2	1	0
Read Write	PTDPE7	PTDPE6	PTDPE5	PTDPE4	PTDPE3	PTDPE2	PTDPE1	PTDPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTDPE field descriptions

Field	Description
7 PTDPE7	Pull Enable for Port D Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 7. 1 Pullup enabled for port D bit 7.
6 PTDPE6	Pull Enable for Port D Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 6. 1 Pullup enabled for port D bit 6.
5 PTDPE5	Pull Enable for Port D Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 5. 1 Pullup enabled for port D bit 5.
4 PTDPE4	Pull Enable for Port D Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 4. 1 Pullup enabled for port D bit 4.
3 PTDPE3	Pull Enable for Port D Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 3. 1 Pullup enabled for port D bit 3.

Table continues on the next page...

PORT_PTDPE field descriptions (continued)

Field	Description
2 PTDPE2	Pull Enable for Port D Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 2. 1 Pullup enabled for port D bit 2.
1 PTDPE1	Pull Enable for Port D Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 1. 1 Pullup enabled for port D bit 1.
0 PTDPE0	Pull Enable for Port D Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTD pin. For port D pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port D bit 0. 1 Pullup enabled for port D bit 0.

7.7.34 Port E Pullup Enable Register (PORT_PTEPE)

Address: 0h base + 30F4h offset = 30F4h

Bit	7	6	5	4	3	2	1	0
Read Write	PTEPE7	PTEPE6	PTEPE5	PTEPE4	PTEPE3	PTEPE2	PTEPE1	PTEPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTEPE field descriptions

Field	Description
7 PTEPE7	Pull Enable for Port E Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 7. 1 Pullup enabled for port E bit 7.
6 PTEPE6	Pull Enable for Port E Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 6. 1 Pullup enabled for port E bit 6.
5 PTEPE5	Pull Enable for Port E Bit 5

Table continues on the next page...

PORT_PTEPE field descriptions (continued)

Field	Description
	This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 5. 1 Pullup enabled for port E bit 5.
4 PTEPE4	Pull Enable for Port E Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 4. 1 Pullup enabled for port E bit 4.
3 PTEPE3	Pull Enable for Port E Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 3. 1 Pullup enabled for port E bit 3.
2 PTEPE2	Pull Enable for Port E Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 2. 1 Pullup enabled for port E bit 2.
1 PTEPE1	Pull Enable for Port E Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 1. 1 Pullup enabled for port E bit 1.
0 PTEPE0	Pull Enable for Port E Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTE pin. For port E pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port E bit 0. 1 Pullup enabled for port E bit 0.

7.7.35 Port F Pullup Enable Register (PORT_PTFPE)

Address: 0h base + 30F5h offset = 30F5h

Bit	7	6	5	4	3	2	1	0
Read Write	PTFPE7	PTFPE6	PTFPE5	PTFPE4	PTFPE3	PTFPE2	PTFPE1	PTFPE0
Reset	0	0	0	0	0	0	0	0

PORT_PTFPE field descriptions

Field	Description
7 PTFPE7	Pull Enable for Port F Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 7. 1 Pullup enabled for port F bit 7.
6 PTFPE6	Pull Enable for Port F Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 6. 1 Pullup enabled for port F bit 6.
5 PTFPE5	Pull Enable for Port F Bit 5 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 5. 1 Pullup enabled for port F bit 5.
4 PTFPE4	Pull Enable for Port F Bit 4 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 4. 1 Pullup enabled for port F bit 4.
3 PTFPE3	Pull Enable for Port F Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 3. 1 Pullup enabled for port F bit 3.
2 PTFPE2	Pull Enable for Port F Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 2. 1 Pullup enabled for port F bit 2.
1 PTFPE1	Pull Enable for Port F Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 1. 1 Pullup enabled for port F bit 1.
0 PTFPE0	Pull Enable for Port F Bit 0

Table continues on the next page...

PORT_PTFPE field descriptions (continued)

Field	Description
	This control bit determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port F bit 0. 1 Pullup enabled for port F bit 0.

7.7.36 Port G Pullup Enable Register (PORT_PTGPE)

Address: 0h base + 30F6h offset = 30F6h

Bit	7	6	5	4	3	2	1	0
Read	0				PTGPE3	PTGPE2	PTGPE1	PTGPE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTGPE field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 PTGPE3	Pull Enable for Port G Bit 3 This control bit determines if the internal pullup device is enabled for the associated PTG pin. For port G pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port G bit 3. 1 Pullup enabled for port G bit 3.
2 PTGPE2	Pull Enable for Port G Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTG pin. For port G pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port G bit 2. 1 Pullup enabled for port G bit 2.
1 PTGPE1	Pull Enable for Port G Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTG pin. For port G pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port G bit 1. 1 Pullup enabled for port G bit 1.
0 PTGPE0	Pull Enable for Port G Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTG pin. For port G pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port G bit 0. 1 Pullup enabled for port G bit 0.

7.7.37 Port H Pullup Enable Register (PORT_PTHPE)

Address: 0h base + 30F7h offset = 30F7h

Bit	7	6	5	4	3	2	1	0
Read	PTHPE7	PTHPE6	0			PTHPE2	PTHPE1	PTHPE0
Write								
Reset	0	0	0	0	0	0	0	0

PORT_PTHPE field descriptions

Field	Description
7 PTHPE7	Pull Enable for Port H Bit 7 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 7. 1 Pullup enabled for port H bit 7.
6 PTHPE6	Pull Enable for Port H Bit 6 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 6. 1 Pullup enabled for port H bit 6.
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 PTHPE2	Pull Enable for Port H Bit 2 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 2. 1 Pullup enabled for port H bit 2.
1 PTHPE1	Pull Enable for Port H Bit 1 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 1. 1 Pullup enabled for port H bit 1.
0 PTHPE0	Pull Enable for Port H Bit 0 This control bit determines if the internal pullup device is enabled for the associated PTH pin. For port H pins that are configured as outputs or Hi-Z, these bits have no effect. 0 Pullup disabled for port H bit 0. 1 Pullup enabled for port H bit 0.

Chapter 8
Clock management

8.1 Clock module

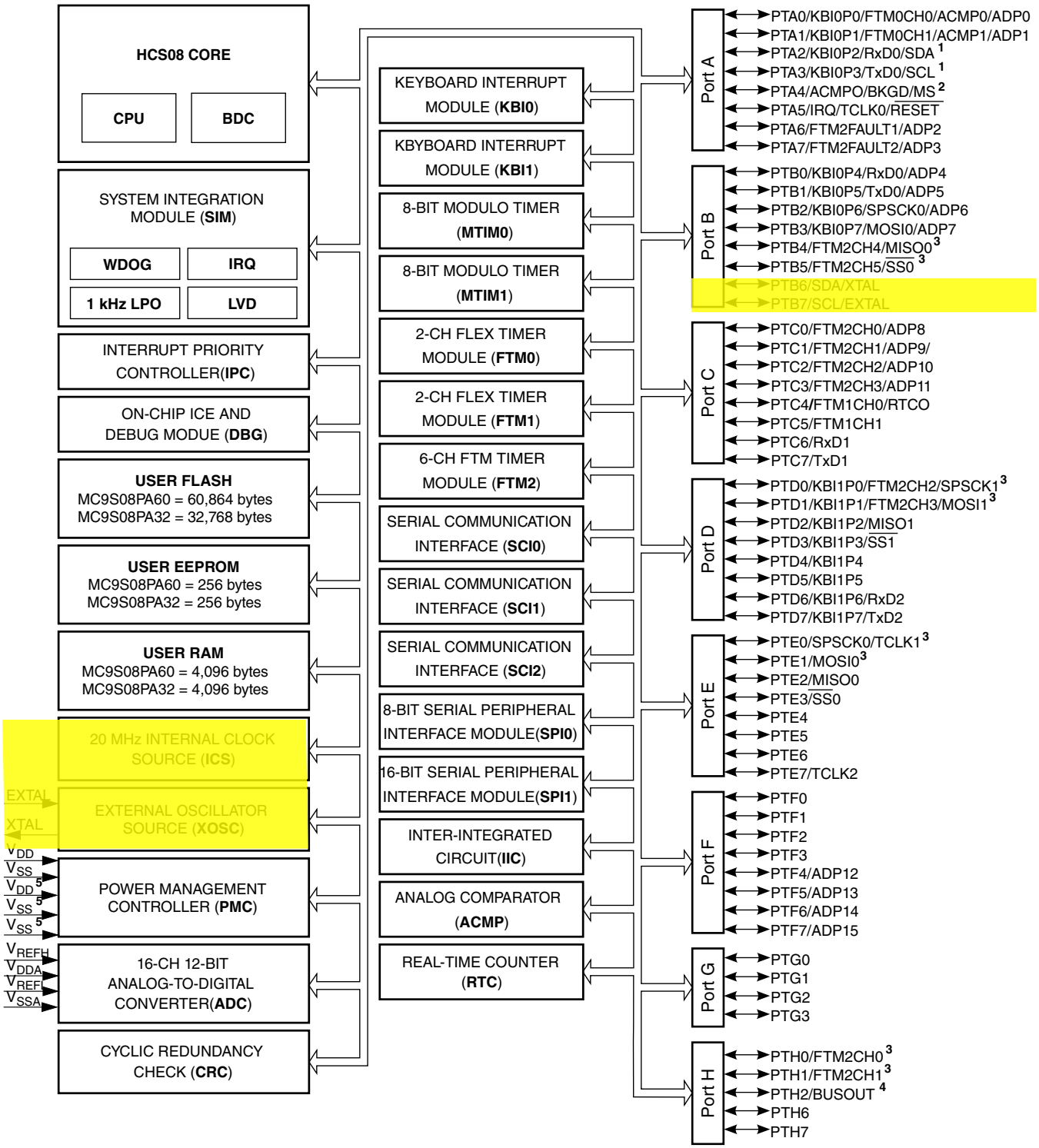
This device has ICS, XOSC, and LPO clock modules.

The internal clock source (ICS) module provides several clock source options for this device. The module contains a frequency-locked loop (FLL) that is controllable by either an internal or external reference clock. The module can select clock from the FLL or bypass the FLL as a source of the MCU system clock. The selected clock source is passed through a reduced bus divider, which allows a lower output clock frequency to be derived.

The external oscillator (XOSC) module allows an external crystal, ceramic resonator, or other external clock source to produce the external reference clock. The output of XOSC module can be used as the reference of ICS to generate system bus clock, and/or clock source of watchdog (WDOG), real-time counter (RTC), and analog-to-digital (ADC) modules.

The low-power oscillator (LPO) module is an on-chip low-power oscillator providing 1 kHz reference clock to RTC and watchdog (WDOG).

The following figures show the block diagram, highlighting the clock modules.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 8-1. Device block diagram highlighting clock modules and pins

8.2 Internal clock source (ICS)

The internal clock source (ICS) module provides clock source options for the MCU. The module contains a frequency-locked loop (FLL) as a clock source that is controllable by an internal or external reference clock. The module can provide this FLL clock or the internal reference clock as a source for the MCU system clock, ICSOUT.

Whichever clock source is chosen, ICSOUT is the output from a bus clock divider (BDIV), which allows a lower clock frequency to be derived.

Key features of the ICS module are:

- Internal reference clock has 9 trim bits for accuracy
- Internal or external reference clocks can be used to control the FLL
- Internal or external reference clocks can be selected as the clock source for the MCU
- Selectable dividers for external reference clock to ensure proper input frequency to FLL
- FLL Engaged Internal mode is automatically selected out of reset
- Digitally-controlled oscillator (DCO) optimized for 16 MHz to 20 MHz frequency range
- FLL lock detector and external clock monitor
    - FLL lock detector with interrupt capability
    - External reference clock monitor with reset capability

8.2.1 Function description

The following figure shows the ICS block diagram.

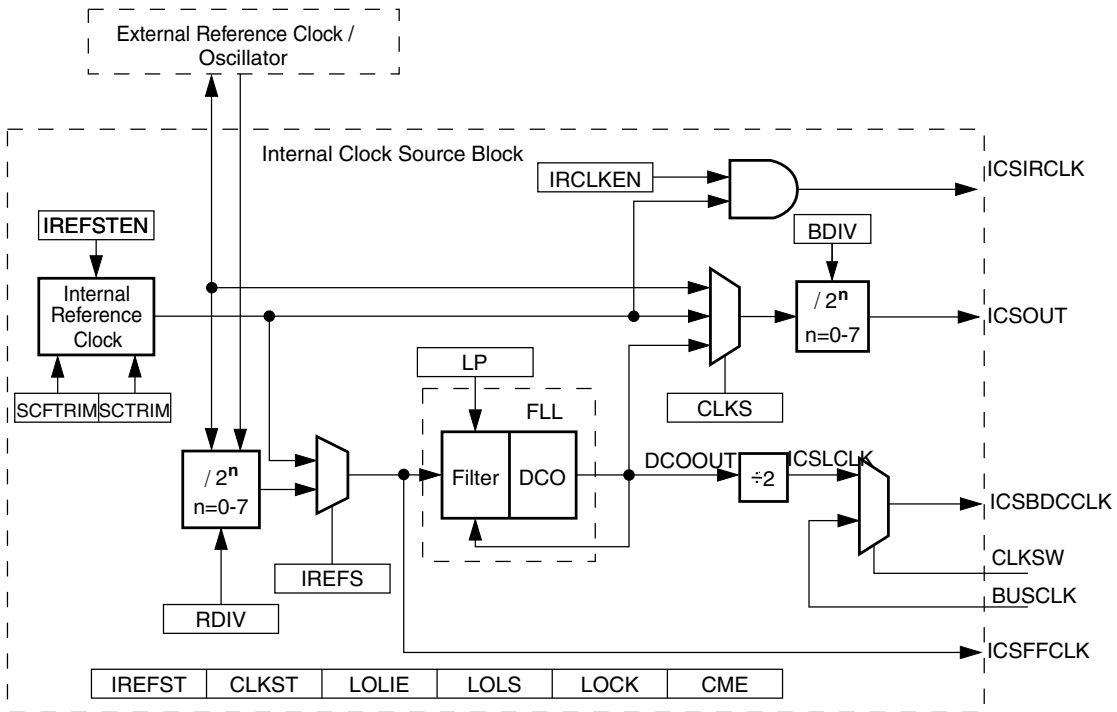


Figure 8-2. Internal clock source (ICS)

8.2.1.1 Bus frequency divider

The ICS_C2[BDIV] bits can be changed at anytime and the actual switch to the new frequency occurs immediately.

8.2.1.2 Low power bit usage

The low power bit (ICS_C2[LP]) is provided to allow the FLL to be disabled and thus conserve power when it is not used.

However, in some applications it may be desirable to allow the FLL to be enabled and to lock for maximum accuracy before switching to an FLL engaged mode. To do this, write the ICS_C2[LP] bit to 0.

8.2.1.3 Internal reference clock (ICSIRCLK)

When ICS_C1[IRCLKEN] is set the internal reference clock signal is presented as ICSIRCLK, which can be used as an additional clock source. To re-target the ICSIRCLK frequency, write a new value to the ICS_C3[SCTRIM] and ICS_C4[SCFTRIM] bits to trim the period of the internal reference clock:

- Writing a larger value slows down the ICSIRCLK frequency.
- Writing a smaller value to the ICSTRM register speeds up the ICSIRCLK frequency.

The trim bits affect the ICSOUT frequency if the ICS is in FLL engaged internal (FEI), FLL bypassed internal (FBI), or FLL bypassed internal low power (FBILP) mode.

Until ICSIRCLK is trimmed, programming low reference divider (BDIV) factors may result in ICSOUT frequencies that exceed the maximum chip-level frequency and violate the chip-level clock timing specifications.

If ICS_C1[IREFSTEN] is set and the ICS_C1[IRCLKEN] bit is written to 1, the internal reference clock keeps running during stop mode in order to provide a fast recovery upon exiting stop.

All MCU devices are factory programmed with trim values in internal memory locations. The SCTRIM and SCFTRIM bits in the ICS_C3 and ICS_C4 registers are normally reset to these factory trim values on any reset. However, any reset that puts the device into BDM (a POR with the BKGD pin held low or a development tool setting BDC_SBDFR[BDFR]) results in the SCTRIM and SCFTRIM bits being set to values of 0x80 and 0. When debugging the MCU, the factory trim value cannot be used, but trim values provided by third party programmers can be copied from the flash locations shown in Table 4-5. Note that third party programmers can trim the internal reference clock to other frequencies within the internal reference clock frequency trim range specified in the data sheet.

NOTE

Some tools like ProcessorExpert or USB Multilink may use flash memory location, such as 0xFF6F and/or 0xFF6E, to store the temporary trim value.

8.2.1.4 Fixed frequency clock (ICSFFCLK)

The ICS presents the divided FLL reference clock as ICSFFCLK for use as an additional clock source. ICSFFCLK frequency must be no more than 1/4 of the ICSOUT frequency to be valid. When ICSFFCLK is valid, ICS output signal (ICSFFE) gets asserted high. Because of this requirement, in bypass modes the ICSFFCLK is valid only in bypass external modes (FBE and FBELP) for the following combinations of BDIV, RDIV, and RANGE values:

- RANGE=1
- BDIV=000 (divide by 1), RDIV ≥ 010

- BDIV=001 (divide by 2), RDIV ≥ 011
- BDIV=010 (divide by 4), RDIV ≥ 100
- BDIV=011 (divide by 8), RDIV ≥ 101
- BDIV=100 (divide by 16), NA
- BDIV=101 (divide by 32), NA
- BDIV=110 (divide by 64), NA
- BDIV=111 (divide by 128), NA

8.2.1.5 BDC clock

The ICS presents the DCO output clock divided by two as ICSLCLK for use as a clock source for BDC communications. ICSLCLK is not available in FLL bypassed internal low power (FBILP) and FLL bypassed external low power (FBELP) modes. The ICSLCLK can be selected as BDC clock.

8.2.2 Modes of operation

There are seven modes of operation for the ICS: FEI, FEE, FBI, FBILP, FBE, FBELP, and stop. The following figure shows the seven states of the ICS as a state diagram. The arrows indicate the allowed movements between the states.

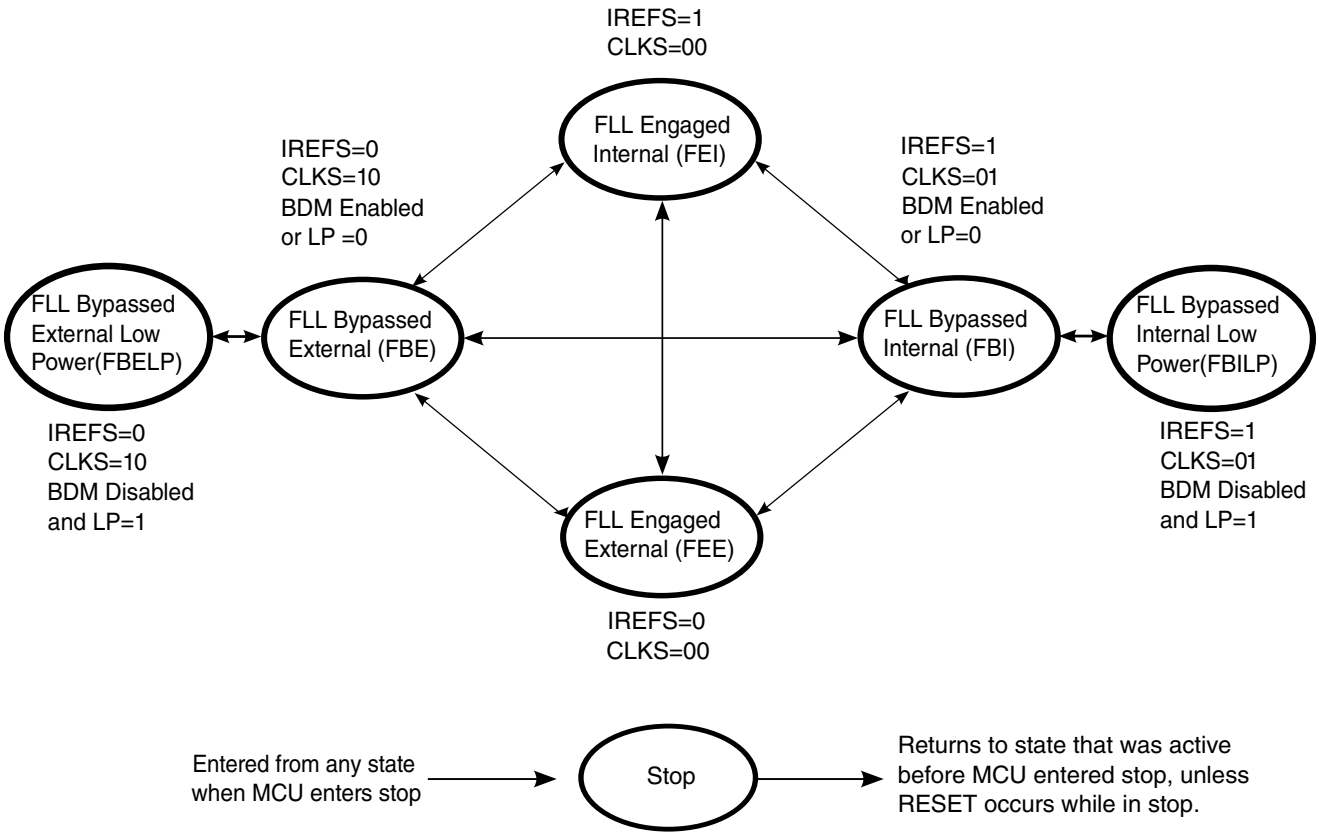


Figure 8-3. ICS clocking switching modes

The ICS_C1[IREFS] bit can be changed at anytime, but the actual switch to the newly selected clock is shown by the ICS_S[IREFST] bit. When switching between FLL engaged internal (FEI) and FLL engaged external (FEE) modes, the FLL will lock again after the switch is completed.

The ICS_C1[CLKS] bits can also be changed at anytime, but the actual switch to the newly selected clock is shown by the ICS_S[CLKST] bits. If the newly selected clock is not available, the previous clock remains selected.

8.2.2.1 FLL engaged internal (FEI)

FLL engaged internal (FEI) is the default mode of operation and is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 0b
- ICS_C1[IREFS] bit is written to 1b

In FLL engaged internal mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the internal reference clock. The FLL loop locks the frequency to the 512 times the internal reference frequency. The ICSLCLK is available for BDC communications, and the internal reference clock is enabled.

8.2.2.2 FLL engaged external (FEE)

The FLL engaged external (FEE) mode is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 00b
- ICS_C1[IREFS] bit written to 0b
- ICS_C1[RDIV] bits are written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz

In FLL engaged external mode, the ICSOUT clock is derived from the FLL clock, which is controlled by the external reference clock source. The FLL loop locks the frequency to the 512 times the external reference frequency, as selected by the ICS_C1[RDIV] bits. The ICSLCLK is available for BDC communications, and the external reference clock is enabled.

8.2.2.3 FLL bypassed internal (FBI)

The FLL bypassed internal (FBI) mode is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 01
- ICS_C1[IREFS] bit is written to 1
- BDM mode is active or ICS_C2[LP] bit is written to 0

In FLL bypassed internal mode, the ICSOUT clock is derived from the internal reference clock. The FLL clock is controlled by the internal reference clock, and the FLL loop locks the FLL frequency to the 512 times the internal reference frequency. The ICSLCLK will be available for BDC communications, and the internal reference clock is enabled.

8.2.2.4 FLL bypassed internal low power (FBILP)

The FLL bypassed internal low power (FBILP) mode is entered when all the following conditions occur:

- ICS_C1[CLKS] bits are written to 01
- ICS_C1[IREFS] bit is written to 1
- BDM mode is not active and ICS_C2[LP] bit is written to 1

In FLL bypassed internal low power mode, the ICSOUT clock is derived from the internal reference clock and the FLL is disabled. The ICSLCLK will be not be available for BDC communications, and the internal reference clock is enabled.

8.2.2.5 FLL bypassed external (FBE)

The FLL bypassed external (FBE) mode is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 10
- ICS_C1[IREFS] bit is written to 0
- ICS_C1[RDIV] bits are written to divide external reference clock to be within the range of 31.25 kHz to 39.0625 kHz
- BDM mode is active or ICS_C2[LP] bit is written to 0

In FLL bypassed external mode, the ICSOUT clock is derived from the external reference clock source. The FLL clock is controlled by the external reference clock, and the FLL loop locks the FLL frequency to the 512 times the external reference frequency, as selected by the ICS_C1[RDIV] bits, so that the ICSLCLK will be available for BDC communications, and the external reference clock is enabled.

8.2.2.6 FLL bypassed external low power (FBELP)

The FLL bypassed external low power (FBELP) mode is entered when all of the following conditions occur:

- ICS_C1[CLKS] bits are written to 10

- ICS_C1[IREFS] bit is written to 0
- BDM mode is not active and ICS_C2[LP] bit is written to 1

In FLL bypassed external low power mode, the ICSOUT clock is derived from the external reference clock source and the FLL is disabled. The ICSLCLK will be not available for BDC communications. The external reference clock source is enabled.

8.2.2.7 Stop (STOP)

In stop mode, the FLL is disabled and the internal clock source can be enabled or disabled. The BDC clock is not available and the ICS does not provide MCU clock source.

Stop mode is entered whenever the MCU enters a stop state. In this mode, all ICS clock signals are static except in the following cases:

- ICSIRCLK will be active in stop mode when all of the following conditions occur:
  - ICS_C1[IRCLKEN] bit is written to 1
  - ICS_C1[IREFSTEN] bit is written to 1
- OSCOUT will be active in stop mode when all of the following conditions occur:
  - ICS_OSCSC[OSCEN] bit is written to 1
  - ICS_OSCSC[OSCSTEN] bit is written to 1

NOTE

The DCO frequency changes from the pre-stop value to its reset value and the FLL need to re-acquire the lock before the frequency is stable. Timing sensitive operations must wait for the FLL acquisition time, t_{Aquire}, before executing.

8.2.3 FLL lock and clock monitor

8.2.3.1 FLL clock lock

In FBE and FEE modes, the clock detector source uses the external reference as the reference. When FLL is detected from lock to unlock, the ICS_S[LOLS] bit is set. An interrupt will be generated if ICS_C4[LOLIE] bit is set. ICS_S[LOLS] bit is cleared by reset or by writing a logic 1 to ICS_S[LOLS] when ICS_S[LOLS] is set. Writing a logic 0 to ICS_S[LOLS] has no effect.

In FBI and FEI modes, the lock detector source uses the internal reference as the reference. When FLL is detected from lock to unlock, the ICS_S[LOLS] bit is set. An interrupt will be generated if ICS_S[LOLS] bit is set. ICS_S[LOLS] bit is cleared by reset or by writing a logic 1 to ICS_S[LOLS] when ICS_S[LOLS] is set. Writing a logic 0 to ICS_S[LOLS] has no effect.

In FBELP and FBILP modes, the FLL is not on, therefore, lock detect function is not applicable.

8.2.3.2 External reference clock monitor

In FBE, FEE, FEI, or FBI modes, if ICS_C4[CME] bit is written to 1, the clock monitor is enabled. If the external reference falls below a certain frequency, such as f_{loc_high} or f_{loc_low} depending on the ICS_OSCSC[RANGE] bit, the MCU will reset. The SYS_SRS[CLK] bit will be set to indicate the error.

In FBELP or FBILP modes, the FLL is not on, so the external reference clock monitor will not function even if ICS_C4[CME] bit is written to 1.

External reference clock monitor uses FLL as the internal reference clock. The FLL must be functional before ICS_C4[CME] bit is set.

8.3 Initialization / application information

This section provides example code to give some basic direction to a user on how to initialize and configure the ICS module. The example software is implemented in C language.

8.3.1 Initializing FEI mode

The following code segment demonstrates setting ICS to FEI mode.

Example: FEI mode initialization routine

```
 /* the following code segment demonstrates setting the ICS to FEI mode using the factory
trim values. The resulting ICSOUT frequency is fint_ft*512/BDIV. */
ICS_C1 = 0x04; // internal reference clock selected as source for FLL
ICS_C2 = 0x00; // BDIV = 0, divide by 1
while (!ICS_S_LOCK); // wait for FLL to lock

/* the following code segment demonstrates setting the ICS to FEI mode using a custom trim
value provided by a programming tool. The resulting ICSOUT frequency is fint_t*512/BDIV. */
ICS_C1 = 0x04; // internal reference clock selected as source for FLL
ICS_C2 = 0x00; // BDIV = 0, divide by 1
ICS_C3 = NV_ICSTRM; // Trim internal reference clock
ICS_C4 = NV_FTRIM; // Fine trim internal reference clock
while (!ICS_S_LOCK); // wait for FLL to lock
```

8.3.2 Initializing FBI mode

The following code segment demonstrates setting ICS to FBI mode.

FBI mode initialization routine

```
/* the following code segment demonstrates setting the ICS to FBI mode using the factory
trim values. The resulting ICSOUT frequency is fint_ft. Note that the FLL will be running at
a frequency of fint_ft*512 even though the FLL is bypassed. */
ICS_C1 = 0x44; // internal reference clock selected
ICS_C2 = 0x00; // BDIV = 0, divide by 1

/* the following code segment demonstrates setting ICS to FBI mode using custom trim values.
The resulting ICSOUT frequency is fint_t. Note that the FLL will be running at a frequency
of fint_t*512 even though the FLL is bypassed. */
ICS_C1 = 0x44; // internal reference clock selected
ICS_C2 = 0x00; // BDIV = 0, divide by 1
ICS_C3 = NV_ICSTRM; // Trim internal reference clock
ICS_C4 = NV_FTRIM; // Fine trim internal reference clock
```

8.3.3 Initializing FEE mode

The following code segment demonstrates setting ICS to FEE mode.

FEE mode initialization routine

```
/* the following code segment demonstrates setting the ICS to FEE mode, generating an 8MHz
bus frequency using an external 4MHz crystal in high gain mode */
ICS_OSCSC = 0x96; // high-range, high-gain, oscillator selected
while (ICS_OSCSC_OSCINIT == 0); // wait until oscillator is ready
ICS_C1 = 0x10; // external reference clock selected as source for FLL, RDIV = 2, divider =
128
                // 4MHz / 128 = 31.25kHz
while (ICS_S_IREFST == 1); // wait for external clock reference active
while (!ICS_S_LOCK); // wait for FLL to lock
```

```
ICS_C2 = 0x20; // BDIV = 1, divide by 2
                // 31.25kHz * 512 / 2 = 8MHz bus
```

8.3.4 Initializing FBE mode

The following code segment demonstrates setting ICS to FBE mode.

FBE mode initialization routine

```
 /* the following code segment demonstrates setting the ICS to FBE mode, generating a 20MHz
bus frequency using an external 20MHz crystal in high gain mode */
ICS_OSCSC = 0x96; // high-range, high-gain, oscillator selected
while (ICS_OSCSC_OSCINIT == 0); // wait until oscillator is ready
ICS_C1 = 0xA0; // external reference clock selected, RDIV = 4, divider = 512
                // 20MHz / 512 = 39.0625kHz
ICS_C2 = 0x00; // BDIV = 0, divider = 1
```

8.3.5 External oscillator (XOSC)

The oscillator module provides the reference clock for internal reference clock module (ICS), the real time counter clock module, and other MCU sub-systems.

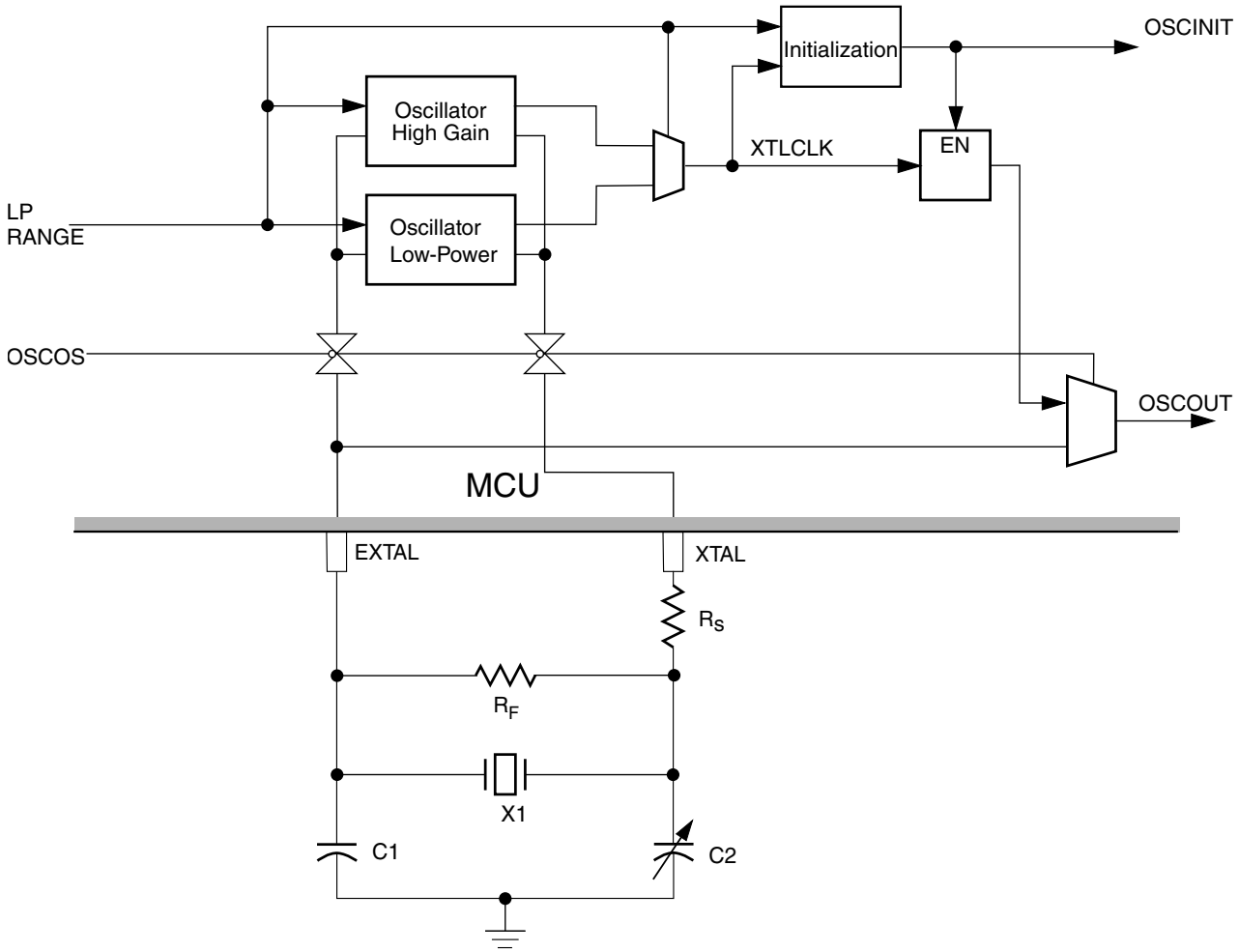


Figure 8-4. Oscillator module block diagram

The external oscillator circuit is designed for use with an external crystal or ceramic resonator to provide an accurate clock source. In its typical configuration, the oscillator is connected in a Pierce oscillator configuration, as shown in the above figure. This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal or ceramic, X1
- Fixed capacitor, C1
- Tuning capacitor, C2, which can also be a fixed capacitor
- Feedback resistor, R_F
- Series resistor, R_S (optional)

8.3.5.1 Bypass mode

In bypass mode (ICS_OSCSC[OSCEN] = 0, ICS_OSCSC[OSCOS] = 0), external clock module is disabled. EXTAL can be used as the input of external clock source. When external clock source is not used in this mode, the EXTAL can be used as GPIO or other function muxed with this pinout. XTAL can be used as GPIO or other function muxed with its pinout even EXTAL is used as external clock source. The following figure shows the typical OSC bypass mode connection.

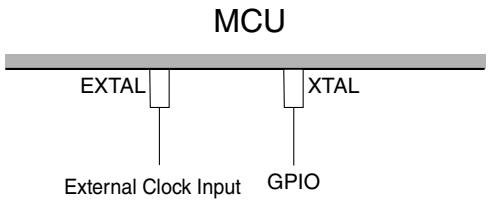


Figure 8-5. OSC bypass mode connection

8.3.5.2 Low-power configuration

In low-power mode, when ICS_OSCSC[OSCEN] = 1, ICS_OSCSC[OSCOS] = 1, and ICS_OSCSC[HGO] = 0, the series resistor R_S is not used. The feedback resistor R_F must be carefully selected to get best performance. The figure below shows the typical OSC low-gain mode connection.

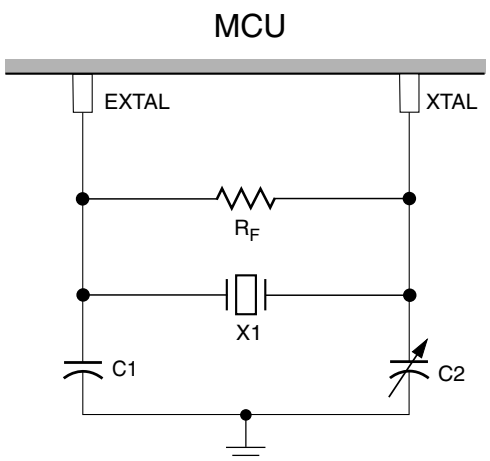


Figure 8-6. OSC low-power mode connection

8.3.5.3 High-gain configuration

In high-gain mode, when ICS_OSCSC[OSCEN] = 1, ICS_OSCSC[OSCOS] = 1, and ICS_OSCSC[HGO] = 1, the series resistor R_S must be used. The series resistor R_S and feedback resistor R_F must be carefully selected to get best performance. The following figure shows the typical OSC high-gain mode connection.

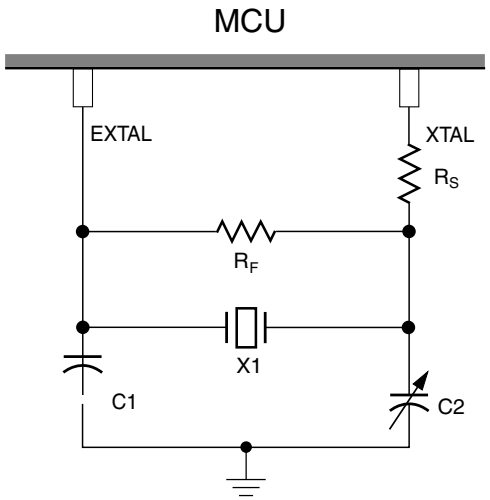


Figure 8-7. OSC high-gain mode connection

8.3.5.4 Initializing external oscillator for peripherals

The following code segment demonstrates initializing external oscillator.

External oscillator initialization routine

```
 /* the following code segment demonstrates initializing the external oscillator using a
32768Hz crystal in low power mode */
ICS_OSCSC = 0xB0; // low-range, low-power, oscillator required, ERCLK enabled in stop mode
while (ICS_OSCSC_OSCINIT == 0); // wait until oscillator is ready
```

8.4 1 kHz low-power oscillator (LPO)

The 1 kHz low-power oscillator acts as a standalone low-frequency clock source in all run, wait, and stop3 modes.

8.5 Peripheral clock gating

This device includes a clock gating system to manage the bus clock sources to the individual peripherals. Using this system, the user can enable or disable the bus clock to each of the peripherals at the clock source, eliminating unnecessary clocks to peripherals that are not in use, thereby reducing the overall run and wait mode currents.

Out of reset, all peripheral clocks will be enabled. For lowest possible run wait currents, user software should disable the clock source to any peripheral not in use. The actual clock will be enabled or disabled immediately following the write to the Clock Gating Control registers (SCG_Cx). Any peripheral with a gated clock cannot be used unless its clock is enabled. Writing to the registers of a peripheral with a disabled clock has no effect.

Note

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

In stop modes, the bus clock is disabled for all gated peripherals, regardless of the setting in SCG_Cx registers.

8.6 ICS control registers

ICS memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3038	ICS Control Register 1 (ICS_C1)	8	R/W	04h	8.6.1/216
3039	ICS Control Register 2 (ICS_C2)	8	R/W	20h	8.6.2/217
303A	ICS Control Register 3 (ICS_C3)	8	R/W	See section	8.6.3/218
303B	ICS Control Register 4 (ICS_C4)	8	R/W	See section	8.6.4/218
303C	ICS Status Register (ICS_S)	8	R/W	10h	8.6.5/219
303E	OSC Status and Control Register (ICS_OSCSC)	8	R/W	00h	8.6.6/220

8.6.1 ICS Control Register 1 (ICS_C1)

Address: 3038h base + 0h offset = 3038h

Bit	7	6	5	4	3	2	1	0
Read Write	CLKS		RDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

ICS_C1 field descriptions

Field	Description
7–6 CLKS	Clock Source Select Selects the clock source that controls the bus frequency. The actual bus frequency depends on the value of the BDIV bits. 00 Output of FLL is selected. 01 Internal reference clock is selected. 10 External reference clock is selected. 11 Reserved.
5–3 RDIV	Reference Divider Selects the amount to divide down the FLL reference clock selected by the IREFS bits. Resulting frequency must be in the range 31.25 kHz to 39.0625 kHz.

RDIV	ICS_OSCSC[RANGE]= 0	ICS_OSCSC[RANGE]= 1
000	1[1]	32
001	2	64
010	4	128
011	8	256
100	16	512
101	32	1024
110	64	Reserved
111	128	Reserved

1. Reset default

2 IREFS	Internal Reference Select The IREFS bit selects the reference clock source for the FLL. 0 External reference clock selected. 1 Internal reference clock selected.
1 IRCLKEN	Internal Reference Clock Enable The IRCLKEN bit enables the internal reference clock for use as ICSIRCLK. 0 ICSIRCLK inactive. 1 ICSIRCLK active.

Table continues on the next page...

ICS_C1 field descriptions (continued)

Field	Description
0 IREFSTEN	Internal Reference Stop Enable The IREFSTEN bit controls whether or not the internal reference clock remains enabled when the ICS enters stop mode. 0 Internal reference clock is disabled in stop. 1 Internal reference clock stays enabled in stop if IRCLKEN is set or if ICS is in FEI, FBI, or FBILP mode before entering stop.

1. Reset default

8.6.2 ICS Control Register 2 (ICS_C2)

Address: 3038h base + 1h offset = 3039h

Bit	7	6	5	4	3	2	1	0
Read	BDIV			LP	0			
Write								
Reset	0	0	1	0	0	0	0	0

ICS_C2 field descriptions

Field	Description
7–5 BDIV	Bus Frequency Divider Selects the amount to divide down the clock source selected by the CLKS bits. This controls the bus frequency. 000 Encoding 0 - Divides selected clock by 1. 001 Encoding 1 - Divides selected clock by 2. 010 Encoding 2 - Divides selected clock by 4. 011 Encoding 3 - Divides selected clock by 8. 100 Encoding 4 - Divides selected clock by 16. 101 Encoding 5 - Divides selected clock by 32. 110 Encoding 6 - Divides selected clock by 64. 111 Encoding 7 - Divides selected clock by 128.
4 LP	Low Power Select The LP bit controls whether the FLL is disabled in FLL bypassed modes. 0 FLL is not disabled in bypass mode. 1 FLL is disabled in bypass modes unless BDM is active.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

8.6.3 ICS Control Register 3 (ICS_C3)

Address: 3038h base + 2h offset = 303Ah

Bit	7	6	5	4	3	2	1	0
Read Write	SCTRIM							
Reset	*	*	*	*	*	*	*	*

* Notes:
- SCTRIM is loaded during reset from a factory programmed location when not in BDM mode. If in a BDM mode, SCTRIM gets loaded with a value of 0x80.

ICS_C3 field descriptions

Field	Description
SCTRIM	Slow Internal Reference Clock Trim Setting The SCTRIM bits control the slow internal reference clock frequency by controlling the internal reference clock period. The bits are binary weighted. In other words, bit 1 adjusts twice as much as bit 0. Increasing the binary value in SCTRIM will increase the period, and decreasing the value will decrease the period. An additional fine trim bit is available in ICS_C4 as the SCFTRIM bit.

8.6.4 ICS Control Register 4 (ICS_C4)

Address: 3038h base + 3h offset = 303Bh

Bit	7	6	5	4	3	2	1	0
Read	LOLIE	0	CME	0				SCFTRIM
Write								
Reset	0	0	0	0	0	0	0	*

* Notes:
- SCFTRIM field: SCFTRIM is loaded during reset from a factory programmed location when not in any BDM mode. If in a BDM mode, SCFTRIM is 0.

ICS_C4 field descriptions

Field	Description
7 LOLIE	Loss of Lock Interrupt Determines if an interrupt request is made following a loss of lock indication. The LOLIE bit has an effect only when LOLS is set. 0 No request on loss of lock. 1 Generate an interrupt request on loss of lock.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

ICS_C4 field descriptions (continued)

Field	Description
5 CME	Clock Monitor Enable Determines if a reset request is made following a loss of external clock indication. The CME bit should be set to a logic 1 only when the ICS is in an operational mode that uses the external clock (FEE or FBE). 0 Clock monitor is disabled. 1 Generate a reset request on loss of external clock.
4–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 SCFTRIM	Slow Internal Reference Clock Fine Trim The SCFTRIM bit controls the smallest adjustment of the internal reference clock frequency. Setting SCFTRIM will increase the period and clearing SCFTRIM will decrease the period by the smallest amount possible.

8.6.5 ICS Status Register (ICS_S)

Address: 3038h base + 4h offset = 303Ch

Bit	7	6	5	4	3	2	1	0
Read	LOLS	LOCK	0	IREFST	CLKST		0	
Write	w1c							
Reset	0	0	0	1	0	0	0	0

ICS_S field descriptions

Field	Description
7 LOLS	Loss of Lock Status This bit is a sticky indication of lock status for the FLL. LOLS is set when lock detection is enabled and after acquiring lock, the FLL output frequency has fallen outside the lock exit frequency tolerance, D_{unl}. LOLIE determines whether an interrupt request is made when set. LOLS is cleared by reset or by writing a logic 1 to LOLS when LOLS is set. Writing a logic 0 to LOLS has no effect. 0 FLL has not lost lock since LOLS was last cleared. 1 FLL has lost lock since LOLS was last cleared.
6 LOCK	Lock Status Indicates whether the FLL has acquired lock. Lock detection is disabled when FLL is disabled. If the lock status bit is set then changing the value of any of the following bits IREFS, RDIV[2:0], or, if in FEI or FBI modes, TRIM[7:0] will cause the lock status bit to clear and stay cleared until the FLL has reacquired lock. Stop mode entry will also cause the lock status bit to clear and stay cleared until the FLL has reacquired lock. **NOTE:** Wait at least for $t_{Acquire}$ after wake from stop mode to start timing critical tasks like serial communication. Do not need to wait for LOCK bit to set after wake from stop mode. 0 FLL is currently unlocked. 1 FLL is currently locked.

Table continues on the next page...

ICS_S field descriptions (continued)

Field	Description
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 IREFST	Internal Reference Status The IREFST bit indicates the current source for the reference clock. The IREFST bit does not update immediately after a write to the IREFS bit due to internal synchronization between clock domains. 0 Source of reference clock is external clock. 1 Source of reference clock is internal clock.
3–2 CLKST	Clock Mode Status The CLKST bits indicate the current clock mode. The CLKST bits don't update immediately after a write to the CLKS bits due to internal synchronization between clock domains. 00 Output of FLL is selected. 01 FLL Bypassed, internal reference clock is selected. 10 FLL Bypassed, external reference clock is selected. 11 Reserved.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

8.6.6 OSC Status and Control Register (ICS_OSCSC)

Address: 3038h base + 6h offset = 303Eh

Bit	7	6	5	4	3	2	1	0
Read	OSCEN	0	OSCSTEN	OSCOS	0	RANGE	HGO	OSCINIT
Write								
Reset	0	0	0	0	0	0	0	0

ICS_OSCSC field descriptions

Field	Description
7 OSCEN	OSC Enable The OSCEN bit enables the external oscillator module. 0 OSC module disabled. 1 OSC module enabled.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 OSCSTEN	OSC Enable in Stop mode Controls whether or not the OSC clock remains enabled when MCU enters Stop mode and OSCEN is set. OSCSTEN has no effect if ICS requests OSC enable.

Table continues on the next page...

ICS_OSCSC field descriptions (continued)

Field	Description
	0 OSC clock is disabled in Stop mode. 1 OSC clock stays enabled in Stop mode.
4 OSCOS	OSC Output Select This bit is used to select the output clock of OSC module. 0 External clock source from EXTAL pin is selected. 1 Oscillator clock source is selected.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 RANGE	Frequency Range Select Selects the frequency range for the OSC module. 0 Low frequency range of 31.25kHz - 39.0625kHz. 1 High frequency range of 4 - 20MHz.
1 HGO	High Gain Oscillator Select The HGO bit controls the OSC mode of operation. 0 Low gain mode. 1 High gain mode.
0 OSCINIT	OSC Initialization This bit set after the initialization cycles of oscillator completes. 0 Oscillator initialization not completes. 1 Oscillator initialization completed.

8.7 System clock gating control registers

SCG memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
300C	System Clock Gating Control 1 Register (SCG_C1)	8	R/W	E7h	8.7.1/222
300D	System Clock Gating Control 2 Register (SCG_C2)	8	R/W	3Ch	8.7.2/223
300E	System Clock Gating Control 3 Register (SCG_C3)	8	R/W	7Eh	8.7.3/224
300F	System Clock Gating Control 4 Register (SCG_C4)	8	R/W	ABh	8.7.4/225

8.7.1 System Clock Gating Control 1 Register (SCG_C1)

This high page register contains control bits to enable or disable the bus clock to the FTMs, MTIMs, and RTC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 300Ch base + 0h offset = 300Ch

Bit	7	6	5	4	3	2	1	0
Read	FTM2	FTM1	FTM0	0		MTIM1	MTIM0	RTC
Write								
Reset	1	1	1	0	0	1	1	1

SCG_C1 field descriptions

Field	Description
7 FTM2	FTM2 Clock Gate Control This bit controls the clock gate to the FTM2 module. 0 Bus clock to the FTM2 module is disabled. 1 Bus clock to the FTM2 module is enabled.
6 FTM1	FTM1 Clock Gate Control This bit controls the clock gate to the FTM1 module. 0 Bus clock to the FTM1 module is disabled. 1 Bus clock to the FTM1 module is enabled.
5 FTM0	FTM0 Clock Gate Control This bit controls the clock gate to the FTM0 module. 0 Bus clock to the FTM0 module is disabled. 1 Bus clock to the FTM0 module is enabled.
4–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 MTIM1	MTIM1 Clock Gate Control This bit controls the clock gate to the MTIM1 module. 0 Bus clock to the MTIM1 module is disabled. 1 Bus clock to the MTIM1 module is enabled.
1 MTIM0	MTIM0 Clock Gate Control

Table continues on the next page...

SCG_C1 field descriptions (continued)

Field	Description
	This bit controls the clock gate to the MTIM0 module. 0 Bus clock to the MTIM0 module is disabled. 1 Bus clock to the MTIM0 module is enabled.
0 RTC	RTC Clock Gate Control This bit controls the clock gate to the RTC module. 0 Bus clock to the MTRTCIM1 module is disabled. 1 Bus clock to the RTC module is enabled.

8.7.2 System Clock Gating Control 2 Register (SCG_C2)

This high-page register contains control bits to enable or disable the bus clock to the DBG, NVM, CRC, and IPC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 300Ch base + 1h offset = 300Dh

Bit	7	6	5	4	3	2	1	0
Read	0		DBG	NVM	IPC	CRC	0	
Write								
Reset	0	0	1	1	1	1	0	0

SCG_C2 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 DBG	DBG Clock Gate Control This bit controls the clock gate to the DBG module. 0 Bus clock to the DBG module is disabled. 1 Bus clock to the DBG module is enabled.
4 NVM	NVM Clock Gate Control This bit controls the clock gate to the NVM module.

Table continues on the next page...

SCG_C2 field descriptions (continued)

Field	Description
	0 Bus clock to the NVM module is disabled. 1 Bus clock to the NVM module is enabled.
3 IPC	IPC Clock Gate Control This bit controls the clock gate to the IPC module. 0 Bus clock to the IPC module is disabled. 1 Bus clock to the IPC module is enabled.
2 CRC	CRC Clock Gate Control This bit controls the clock gate to the CRC module. 0 Bus clock to the CRC module is disabled. 1 Bus clock to the CRC module is enabled.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

8.7.3 System Clock Gating Control 3 Register (SCG_C3)

This high page register contains control bits to enable or disable the bus clock to the SCI, SPI, IIC modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

Address: 300Ch base + 2h offset = 300Eh

Bit	7	6	5	4	3	2	1	0
Read	0	SCI2	SCI1	SCI0	SPI1	SPI0	IIC	0
Write								
Reset	0	1	1	1	1	1	1	0

SCG_C3 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 SCI2	SCI2 Clock Gate Control This bit controls the clock gate to the SCI2 module.

Table continues on the next page...

SCG_C3 field descriptions (continued)

Field	Description
	0 Bus clock to the SCI2 module is disabled. 1 Bus clock to the SCI2 module is enabled.
5 SCI1	SCI1 Clock Gate Control This bit controls the clock gate to the SCI1 module. 0 Bus clock to the SCI1 module is disabled. 1 Bus clock to the SCI1 module is enabled.
4 SCI0	SCI0 Clock Gate Control This bit controls the clock gate to the SCI0 module. 0 Bus clock to the SCI0 module is disabled. 1 Bus clock to the SCI0 module is enabled.
3 SPI1	SPI1 Clock Gate Control This bit controls the clock gate to the SPI1 module. 0 Bus clock to the SPI1 module is disabled. 1 Bus clock to the SPI1 module is enabled.
2 SPI0	SPI0 Clock Gate Control This bit controls the clock gate to the SPI0 module. 0 Bus clock to the SPI0 module is disabled. 1 Bus clock to the SPI0 module is enabled.
1 IIC	IIC Clock Gate Control This bit controls the clock gate to the IIC module. 0 Bus clock to the IIC module is disabled. 1 Bus clock to the IIC module is enabled.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

8.7.4 System Clock Gating Control 4 Register (SCG_C4)

This high page register contains control bits to enable or disable the bus clock to the ACMP, ADC, IRQ, and KBI modules. Gating off the clocks to unused peripherals is used to reduce the MCU's run and wait currents.

NOTE

User software should disable the peripheral before disabling the clocks to the peripheral. When clocks are re-enabled to a peripheral, the peripheral registers need to be re-initialized by user software.

System clock gating control registers

Address: 300Ch base + 3h offset = 300Fh

Bit	7	6	5	4	3	2	1	0
Read	ACMP	0	ADC	0	IRQ	0	KBI1	KBI0
Write								
Reset	1	0	1	0	1	0	1	1

SCG_C4 field descriptions

Field	Description
7 ACMP	ACMP Clock Gate Control This bit controls the clock gate to the ACMP module. 0 Bus clock to the ACMP module is disabled. 1 Bus clock to the ACMP module is enabled.
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 ADC	ADC Clock Gate Control This bit controls the clock gate to the ADC module. 0 Bus clock to the ADC module is disabled. 1 Bus clock to the ADC module is enabled.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 IRQ	IRQ Clock Gate Control This bit controls the clock gate to the IRQ module. 0 Bus clock to the IRQ module is disabled. 1 Bus clock to the IRQ module is enabled.
2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 KBI1	KBI1 Clock Gate Control This bit controls the clock gate to the KBI1 module. 0 Bus clock to the KBI1 module is disabled. 1 Bus clock to the KBI1 module is enabled.
0 KBI0	KBI0 Clock Gate Control This bit controls the clock gate to the KBI0 module. 0 Bus clock to the KBI0 module is disabled. 1 Bus clock to the KBI0 module is enabled.

Chapter 9
Chip configurations

9.1 Introduction

This chapter provides details on the individual modules of the device. It includes:

- device block diagrams highlighting the specific modules and pin-outs
- specific module-to-module interactions not necessarily discussed in the individual module chapters, and
- links for more information

9.2 Core modules

9.2.1 Central processor unit (CPU)

The HCS08 CPU is fully source- and object-code-compatible with the M68HC08 CPU. Several instructions and enhanced addressing modes were added to improve C compiler efficiency and to support a new background debug system which replaces the monitor mode of earlier M68HC08 microcontrollers.

9.2.2 Debug module (DBG)

The DBG module implements an on-chip ICE (in-circuit emulation) system and allows non-intrusive debug of application software by providing an on-chip trace buffer with flexible triggering capability. The trigger can also provide extended breakpoint capacity. The on-chip ICE system is optimized for the HCS08 8-bit architecture and supports 64 KB of memory space.

9.3 System modules

9.3.1 Watchdog (WDOG)

The watchdog timer (WDOG) module triggers a system reset if it is allowed to time out. The program is expected to periodically reload the watchdog timer, thereby preventing it from timing out. However, if a fault occurs that causes the program to stop working, the timer will not be reloaded and it will time out. The resulting trigger of a system reset brings the system back from an unresponsive state into a normal state.

9.4 Clock module

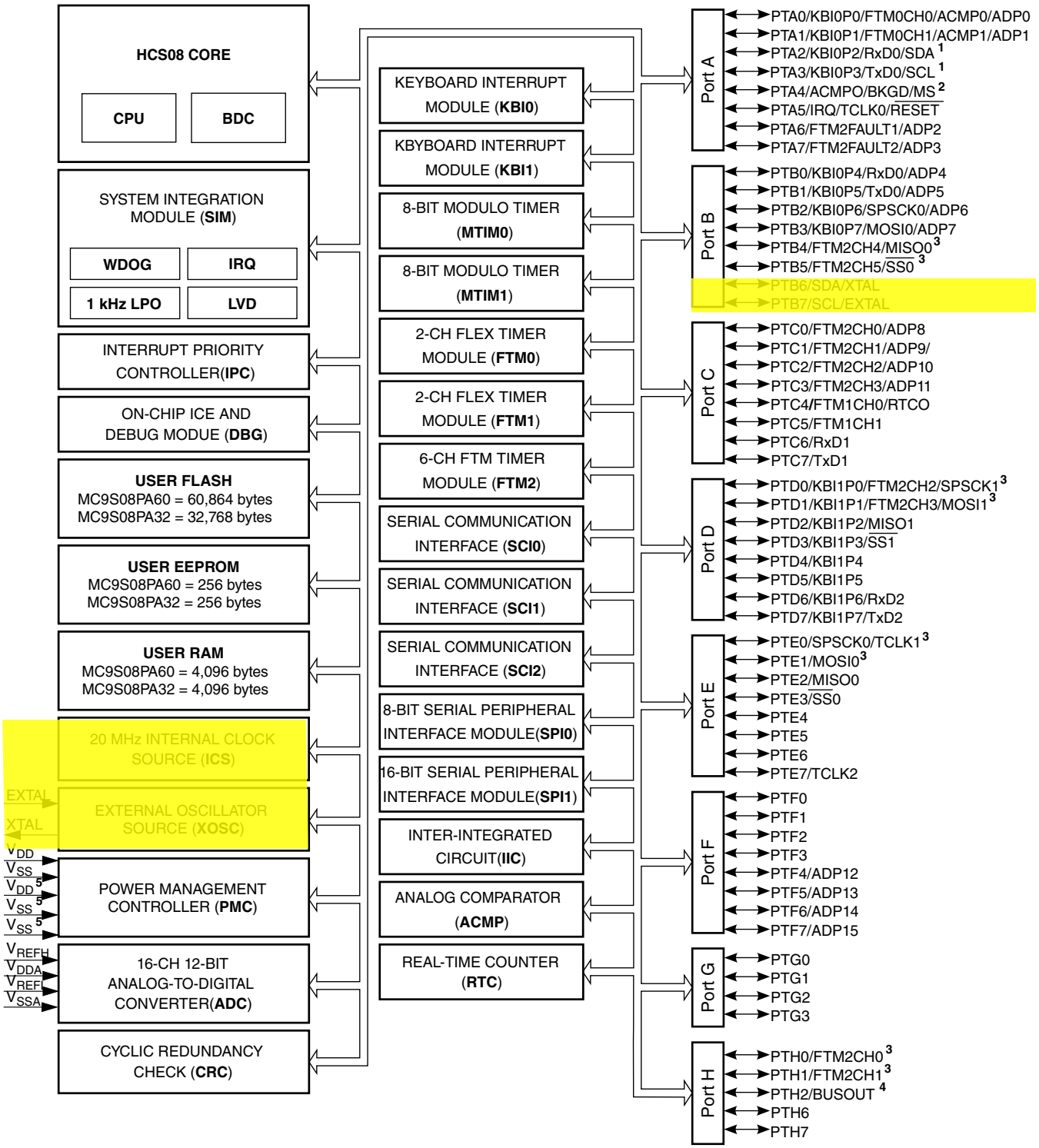
This device has ICS, XOSC, and LPO clock modules.

The internal clock source (ICS) module provides several clock source options for this device. The module contains a frequency-locked loop (FLL) that is controllable by either an internal or external reference clock. The module can select clock from the FLL or bypass the FLL as a source of the MCU system clock. The selected clock source is passed through a reduced bus divider, which allows a lower output clock frequency to be derived.

The external oscillator (XOSC) module allows an external crystal, ceramic resonator, or other external clock source to produce the external reference clock. The output of XOSC module can be used as the reference of ICS to generate system bus clock, and/or clock source of watchdog (WDOG), real-time counter (RTC), and analog-to-digital (ADC) modules.

The low-power oscillator (LPO) module is an on-chip low-power oscillator providing 1 kHz reference clock to RTC and watchdog (WDOG).

The following figures show the block diagram, highlighting the clock modules.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-1. Device block diagram highlighting clock modules and pins

9.5 Memory

9.5.1 Random-access-memory (RAM)

This device contains 4,096 byte static RAM and addresses 0x0040 through 0x103F. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64 KB memory space.

9.5.2 Non-volatile memory (NVM)

The NVM is ideal for single-supply applications allowing for field programming without requiring external high voltage sources from program or erase operations. The NVM module includes a memory controller that executes commands to modify NVM contents.

This device contains two types of non-volatile memory: Flash memory and EEPROM. The Flash is mostly used for the storage of program and constant. The EEPROM is used for storing frequently modified non-volatile data.

Non-volatile memory (NVM) includes:

- Flash memory
  - MC9S08PA60—60,864 bytes: 119 sectors of 512 bytes[1]
  - MC9S08PA32—32,768 bytes: 64 sectors of 512 bytes
- EEPROM memory
  - MC9S08PA60—256 bytes: 128 sectors of 2 bytes
  - MC9S08PA32—256 bytes: 128 sectors of 2 bytes

9.6 Power modules

This device contains on-chip regulator for various operational power modes of run, wait, and stop3 modes. The low voltage detect (LVD) system allows the system to protect against low voltage conditions in order to protect memory contents and control MCU system states during supply voltage variations. The on-chip bandgap reference (≈1.2V), which is internally connected to ADC channel, provides independent accuracy reference which will not drop over the full operating voltage even when the operating voltage is falling.

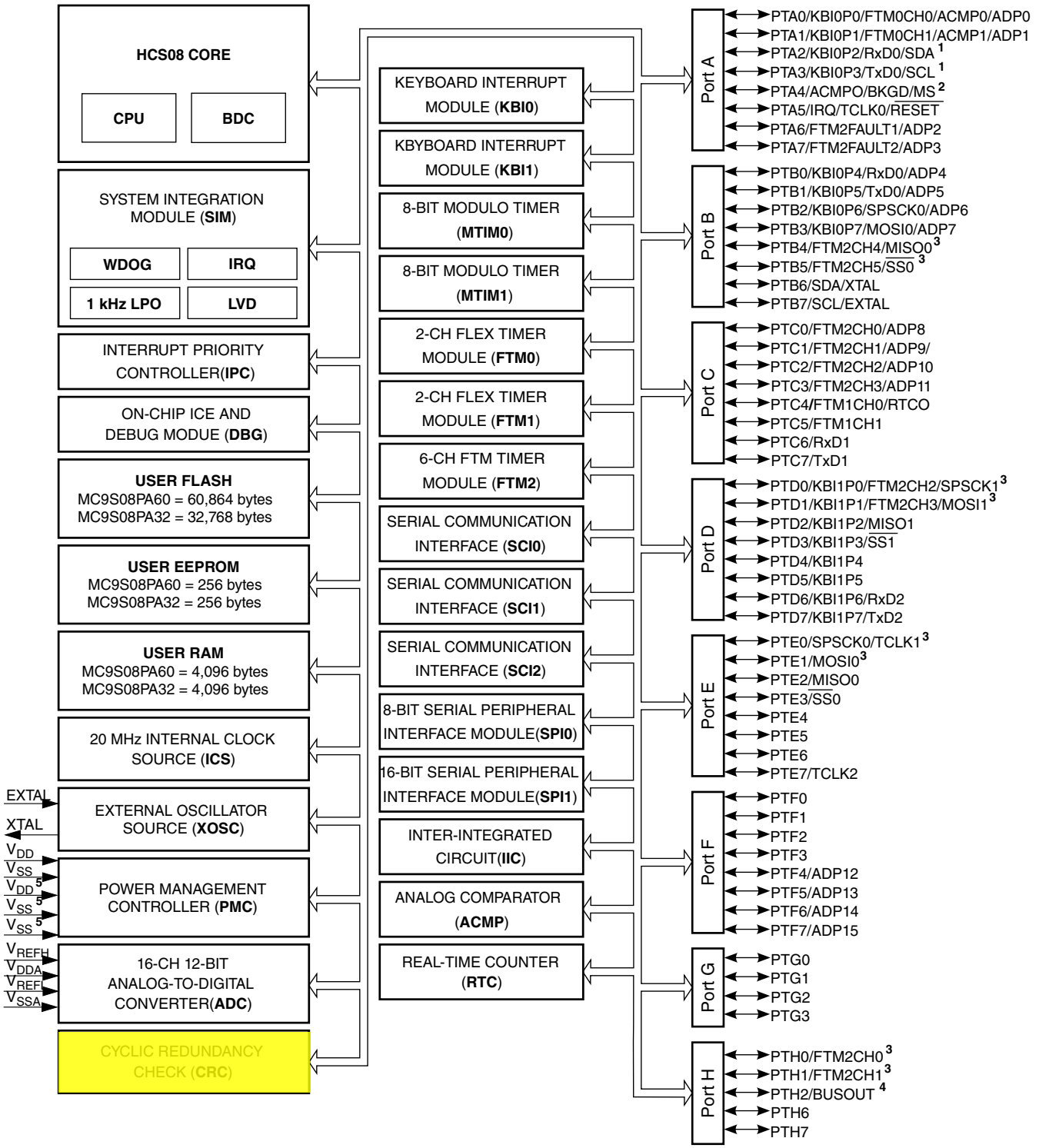
1. One of the sectors contains 448 bytes.

9.7 Security

9.7.1 Cyclic redundancy check (CRC)

The CRC generator module uses a programmable polynomial to generate CRC code for error detection. The 16-bit code is calculated for 8-bit of data at a time, and provides a simple check for all accessible memory locations in flash and RAM.

The following figure shows the device block diagram highlighting the CRC module.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-2. Device block diagram highlighting CRC module

9.8 Timers

9.8.1 FlexTimer module (FTM)

The FlexTimer module is an up to six-channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

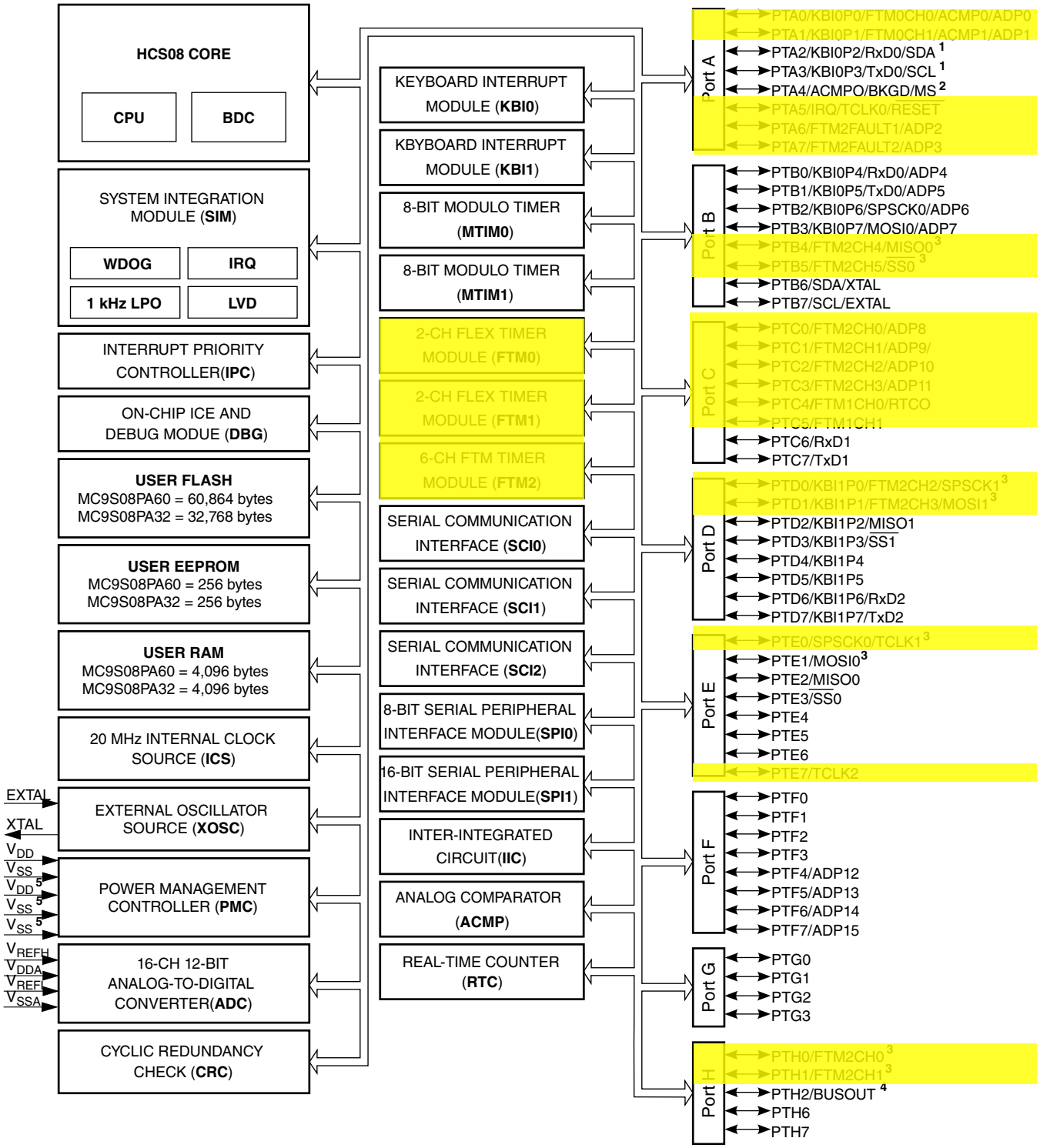
This MCU contains up to three FTM modules with one 6-channel FTM and two 2-channel FTMs. FTM0 and FTM1, each of which has two independent channels, are fully compatible to the TPM. FTM2, which has six channels, is backward compatible to the TPM for simple configuration and operation, and features hardware deadtime insertion, pairs with complementary outputs, generation of triggers, and fault inputs.

Each FTM module has independent external clock input. The following table summarizes the external signals of FTM modules.

Table 9-1. FTM module external signals

FTM	Functions	Default	Alternate
FTM0	channel 0	PTA0/FTM0CH0	
	channel 1	PTA1/FTM0CH1	
	alternate clock	PTA5/TCLK0	
FTM1	channel 0	PTC4/FTM1CH0	
	channel 1	PTC5/FTM1CH1	
	alternate clock	PTE0/TCLK1	
FTM2	channel 0	PTC0/FTM2CH0	PTH0/FTM2CH0
	channel 1	PTC1/FTM2CH1	PTH1/FTM2CH1
	channel 2	PTC2/FTM2CH2	PTD0/FTM2CH2
	channel 3	PTC3/FTM2CH3	PTD1/FTM2CH3
	channel 4	PTB4/FTM2CH4	
	channel 5	PTB5/FTM2CH5	
	fault 1	PTA6/FTM2FAULT1	
	fault 2	PTA7/FTM2FAULT2	
	alternate clock	PTE7/TCLK2	

The following figure shows the device block diagram highlighting FTM modules and pins.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-3. Device block diagram highlighting FTM modules and pins

9.8.1.1 FTM0 interconnection

SCI0 TxD signal can be modulated by FTM0 channel 0 PWM output. Please refer to SCI0 TxD modulation.

SCI0 RxD signal can be tagged by FTM0 channel 1 input capture function. Please refer to SCI0 RxD filter.

9.8.1.2 FTM1 interconnection

ACMP output can be internally connected to FTM1 channel 0 capture input. See ACMP output selection for details.

9.8.1.3 FTM2 interconnection

FTM2 supports three PWM synchronization sources:

- Trigger0 is connected to the output of ACMP.
- Trigger1 is connected to FTM0 channel 0 output.
- Trigger2 is a software trigger by writing 1 to the SYS_SOPT2[FTMSYNC] bit. Please refer to System interconnection.

FTM2 supports four FTM fault sources:

- Fault 0 is connected to ACMP output.
- Fault1 is connected to PTA6.
- Fault 2 is connected to PTA7.
- Fault 3 is not used. Please refer to System interconnection.

FTM2 supports seven FTM triggers including an initialization trigger and six channel triggers to other modules. The initialization trigger and match trigger are optionally connected to ADC hardware trigger via an 8-bit delay counter. All other triggers are not used in this device. Please refer to System interconnection.

9.8.1.4 FTM registers

The following table lists all the FTM registers this device has.

Table 9-2. FTM registers

Registers (x=0, 1, 2)	FTM0	FTM1	FTM2
FTMx_SC	Y	Y	Y
FTM2_CNTH	Y	Y	Y
FTMx_CNTL	Y	Y	Y
FTMx_MODH	Y	Y	Y
FTMx_MODL	Y	Y	Y
FTMx_C0SC	Y	Y	Y
FTMx_C0VH	Y	Y	Y
FTMx_C0VL	Y	Y	Y
FTMx_C1SC	Y	Y	Y
FTMx_C1VH	Y	Y	Y
FTMx_C1VL	Y	Y	Y
FTMx_C2SC	N	N	Y
FTMx_C2VH	N	N	Y
FTMx_C2VL	N	N	Y
FTMx_C3SC	N	N	Y
FTMx_C3VH	N	N	Y
FTMx_C3VL	N	N	Y
FTMx_C4SC	N	N	Y
FTMx_C4VH	N	N	Y
FTMx_C4VL	N	N	Y
FTMx_C5SC	N	N	Y
FTMx_C5VH	N	N	Y
FTMx_C5VL	N	N	Y
FTMx_CNTINH	N	N	Y
FTMx_CNTINL	N	N	Y
FTMx_STATUS	N	N	Y
FTMx_MODE	N	N	Y
FTMx_SYNC	N	N	Y
FTMx_OUTINIT	N	N	Y
FTMx_OUTMASK	N	N	Y
FTMx_COMBINE0	N	N	Y
FTMx_COMBINE1	N	N	Y
FTMx_COMBINE2	N	N	Y
FTMx_DEADTIME	N	N	Y
FTMx_EXTTRIG	N	N	Y
FTMx_POL	N	N	Y
FTMx_FMS	N	N	Y
FTMx_FILTER0	N	N	Y
FTMx_FILTER1	N	N	Y

Table continues on the next page...

Table 9-2. FTM registers (continued)

Registers (x=0, 1, 2)	FTM0	FTM1	FTM2
FTMx_FLTFILTER	N	N	Y
FTMx_FLTCTRL	N	N	Y

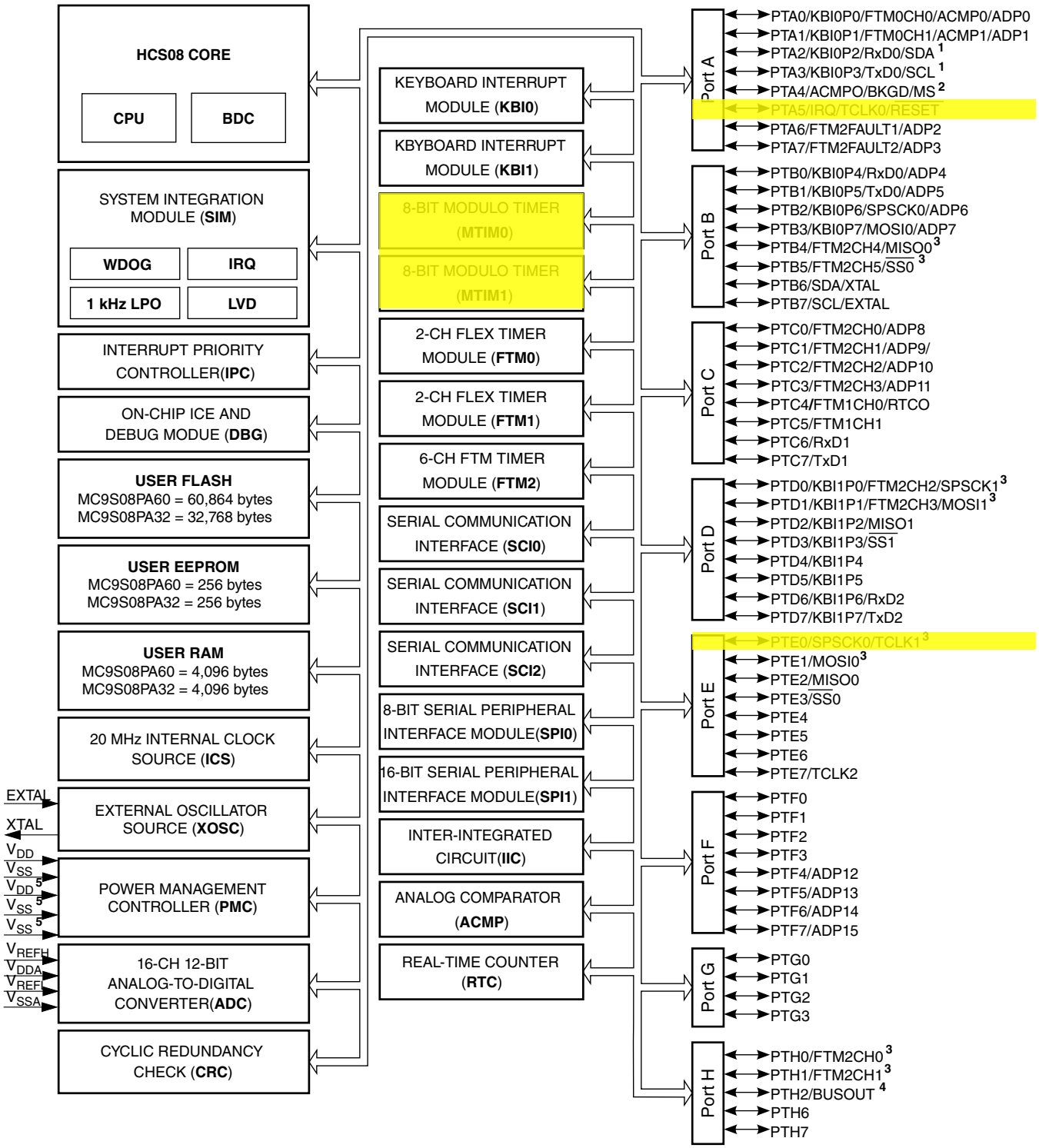
9.8.2 8-bit modulo timer (MTIM)

MTIM0 8-bit modulo timer module that provide a circuit of selectable clock sources and a programmable interrupt. The MTIM module contain an 8-bit modulo counter, which can operate as a free-running counter or a modulo counter. A timer overflow interrupt can be enabled to generate periodic interrupts for time-based software events. MTIM module may also use external clock source.

NOTE

The TCLK in the chapter of 8-bit modulo timer (MTIM) is the FFCLK in the System clock distribution.

The following figure shows the device block diagram highlighting the MTIM module and pins.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-4. Block diagram highlighting the MTIM module and pins

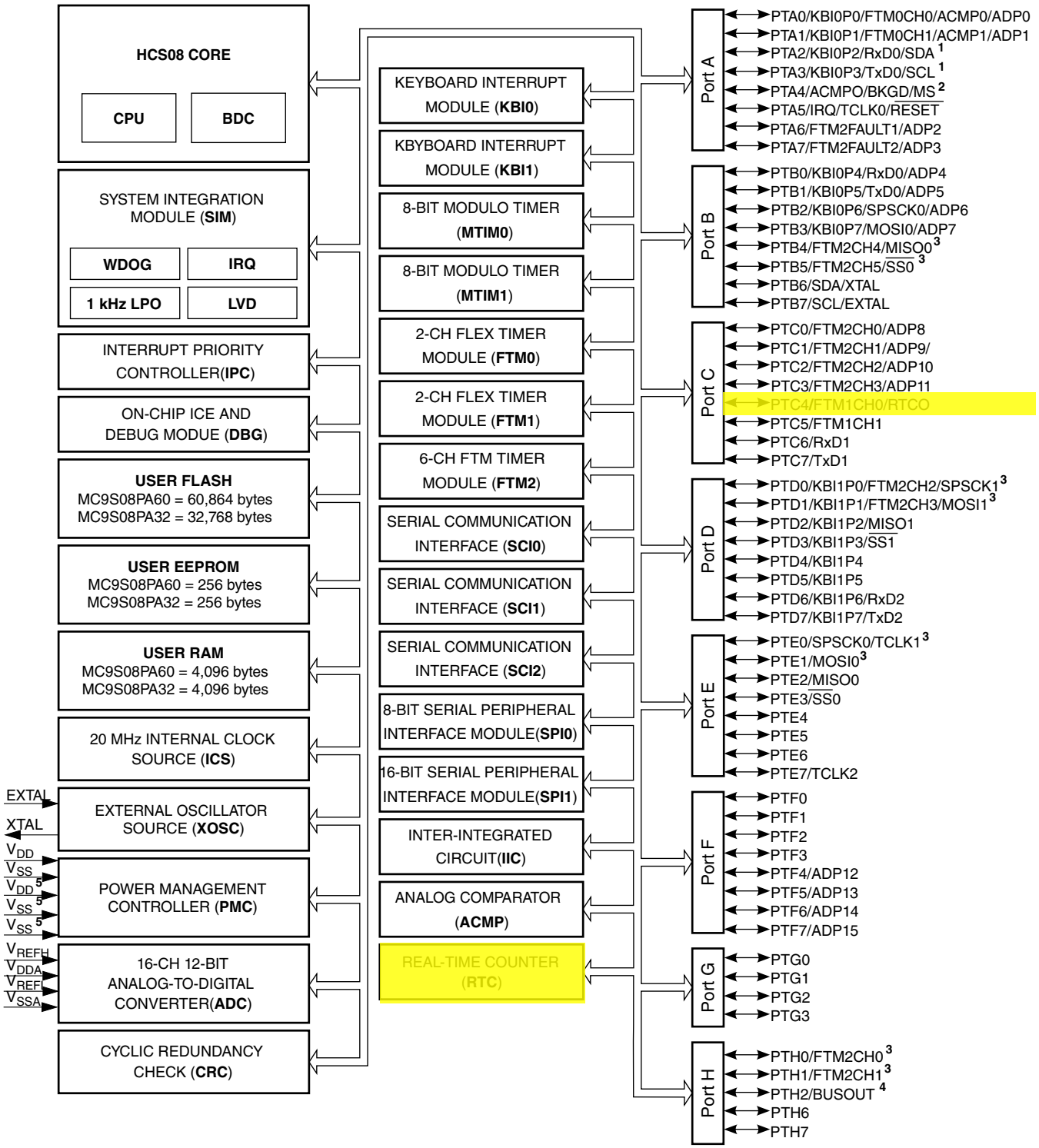
9.8.2.1 MTIM0 as ADC hardware trigger

MTIM0 overflow can be used as ADC hardware trigger. See ADC hardware trigger for details.

9.8.3 Real-time counter (RTC)

The real-time counter (RTC) consists of one 16-bit counter, one 16-bit comparator, several binary-based and decimal-based prescaler dividers, two clock sources, and one programmable periodic interrupt. This module can be used for time-of-day, calendar or any task scheduling functions. It can also serve as a cyclic wakeup from low power modes without external components. RTC overflow trigger can be used as hardware trigger for ADC module. Furthermore, when the trigger is enabled, RTC can toggle external pin function if the counter overflows.

The following figure shows the device block diagram highlighting RTC module and pin.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-5. Device block diagram highlighting RTC module and pin

9.9 Communication interfaces

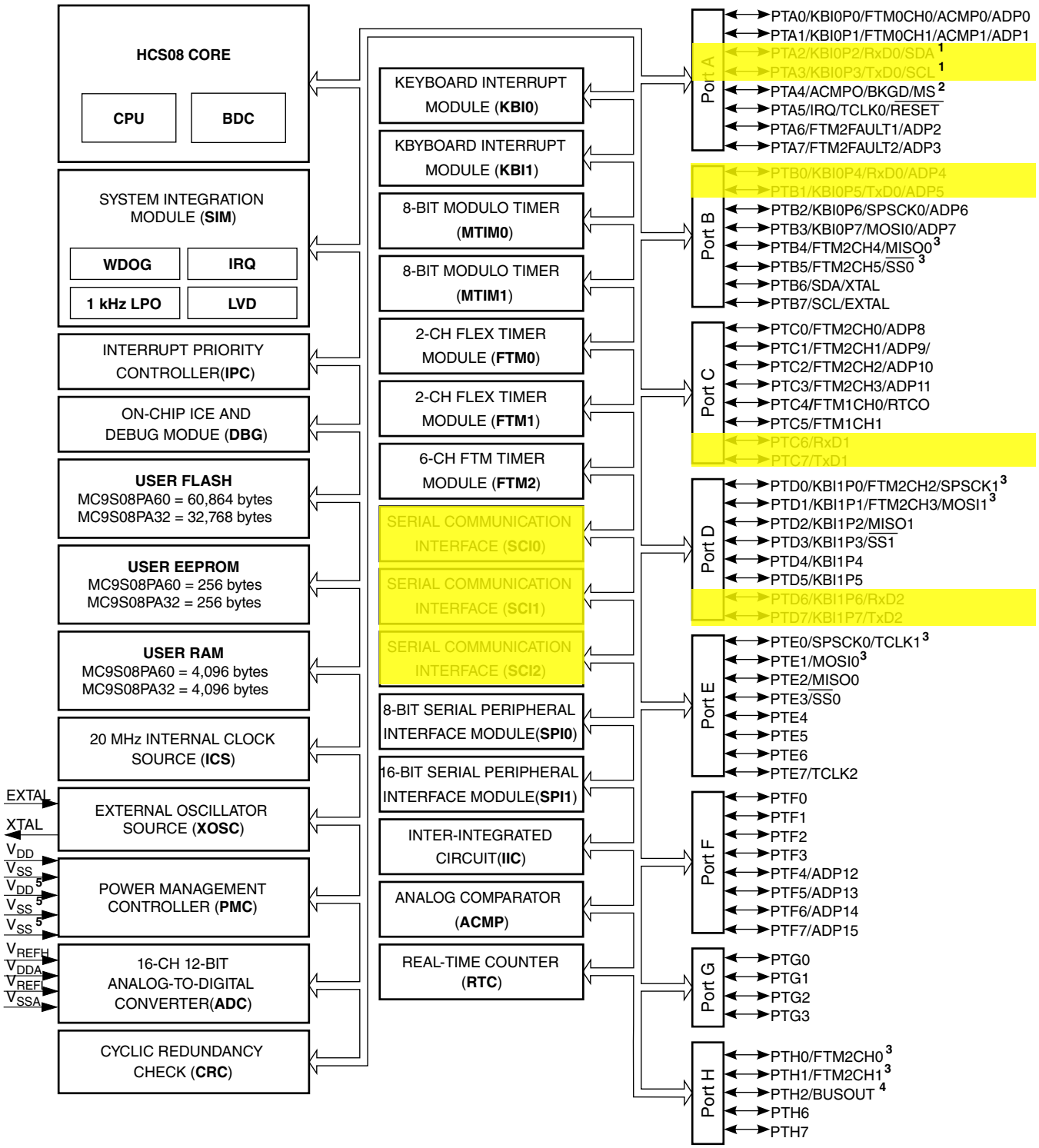
9.9.1 Serial communications interface (SCI)

This device includes three independent serial communications interface (SCI) modules. Typically, these systems are used to connect to the RS232 serial input/output port of a personal computer or workstation. They can also be used to communicate with other embedded controllers.

A flexible, 13-bit, modulo-based baud rate generator supports a broad range of standard baud rates beyond 115.2 kBd. Transmit and receive within the same SCI use a common baud rate, and each SCI module has a separate baud rate generator.

This SCI system offers many advanced features not commonly found on other asynchronous serial I/O peripherals of the embedded controllers. The receiver employs an advanced data sampling technique that ensures reliable communication and noise detection. Hardware parity, receiver wakeup, and double buffering on transmit and receive are also included.

The following figure shows the device block diagram highlighting SCI modules and pins.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-6. Device block diagram highlighting SCI modules and pins

9.9.1.1 SCI0 infrared functions

9.9.1.1.1 SCI0 TxD modulation

SCI0 TxD output can be modulated by FTM0 channel 0 PWM output. Please refer to SCI0 TxD modulation.

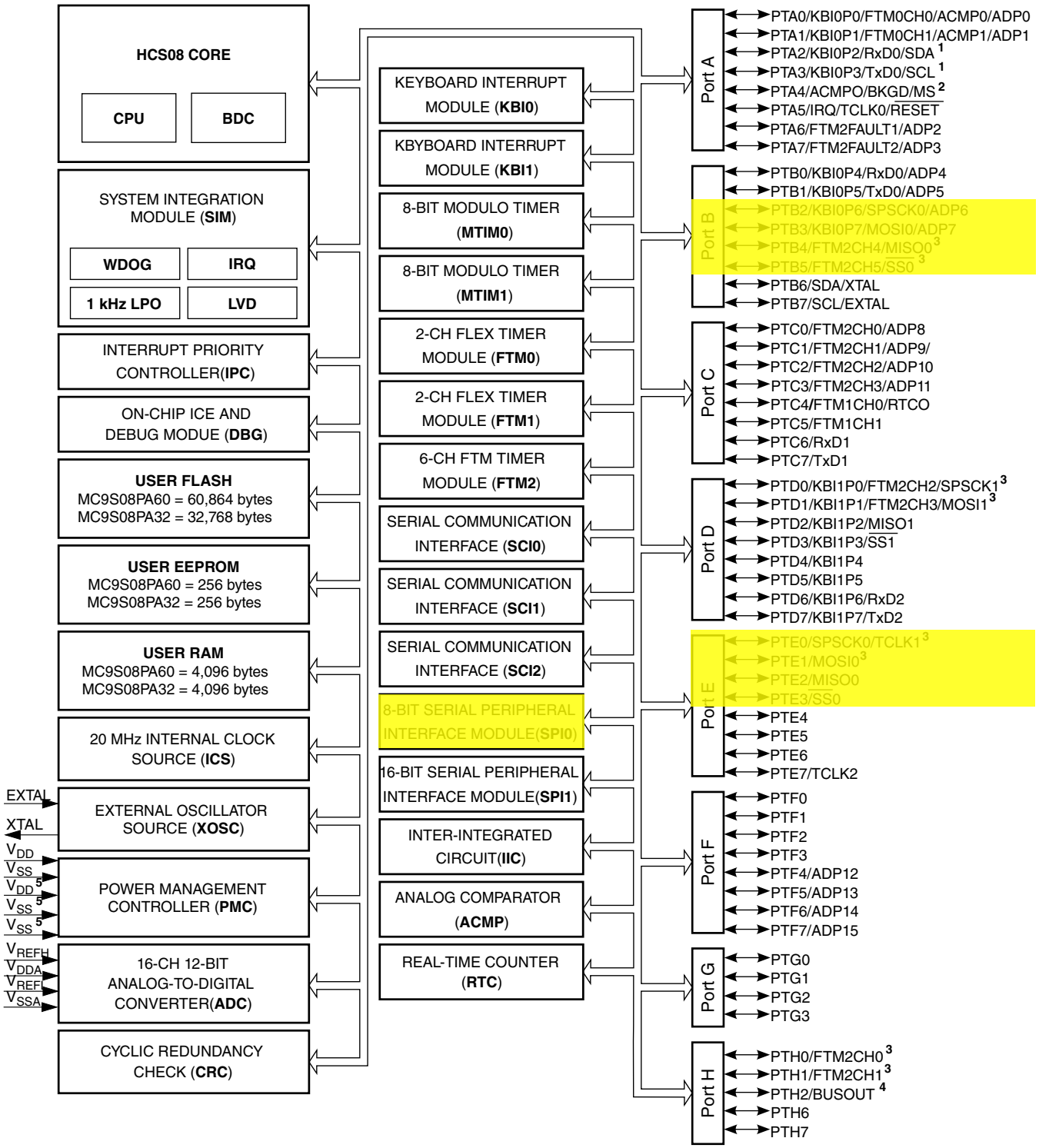
9.9.1.1.2 SCI0 RxD tag

ACMP module output can be directly ejected to SCI0 RxD. In this mode, SCI0 external RxD pinout does not work. Any external signal tagged to ACMP inputs can be set as SCI input. Please refer to SCI0 RxD filter.

9.9.2 8-Bit Serial Peripheral Interface (8-bit SPI)

This MCU contains an 8-bit serial peripheral interface (SPI0) module which provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, memories, etc.

The following figure shows the device block diagram highlighting 8-bit SPI module and pins.



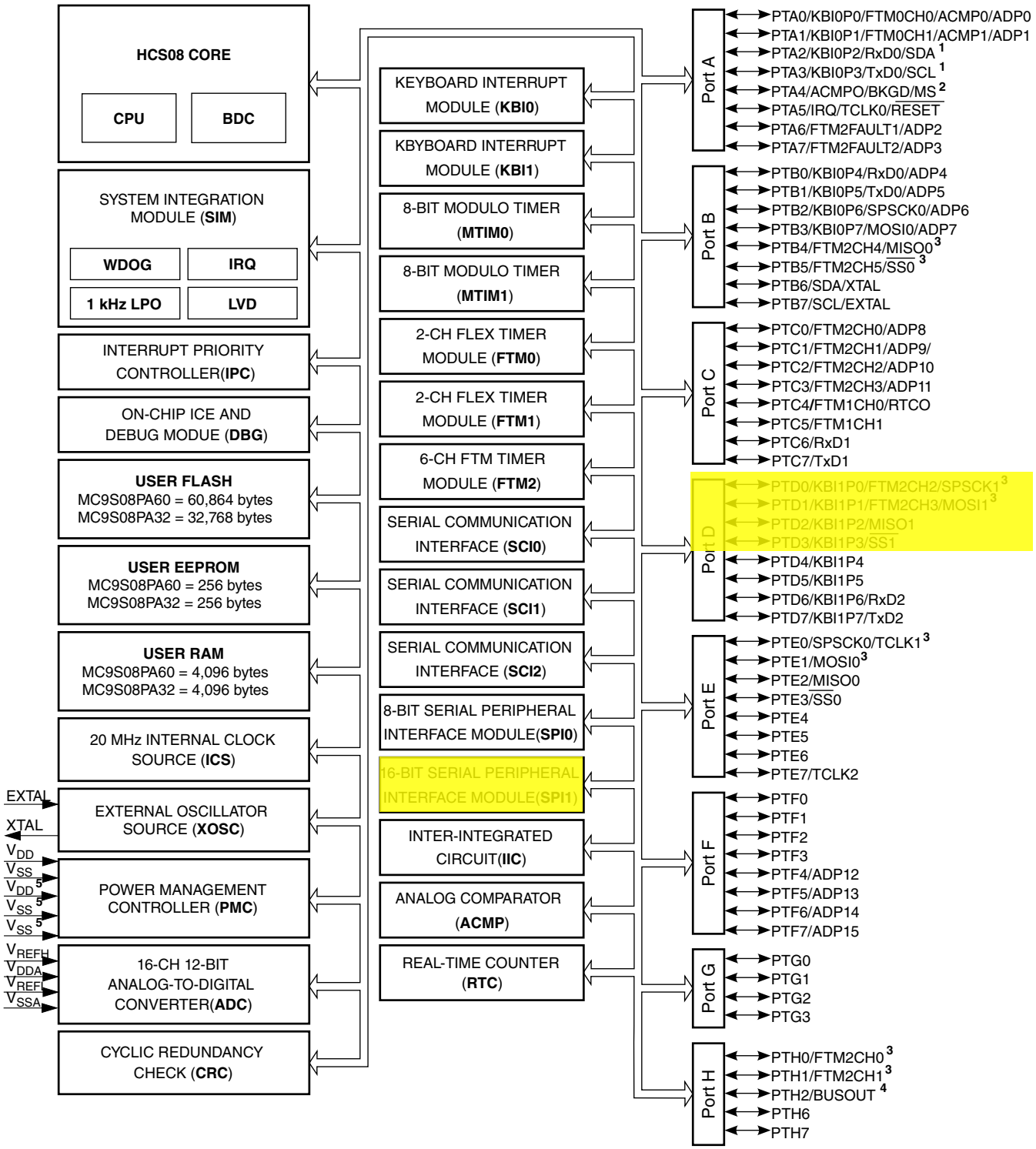
1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-7. Device block diagram highlighting 8-bit SPI module and pins

9.9.3 16-bit serial peripheral interface (16-bit SPI)

This device contains a 16-bit serial peripheral interface (SPI1) module which provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, memories, etc.

The following figure shows device block diagram highlighting 16-bit SPI module and pins.



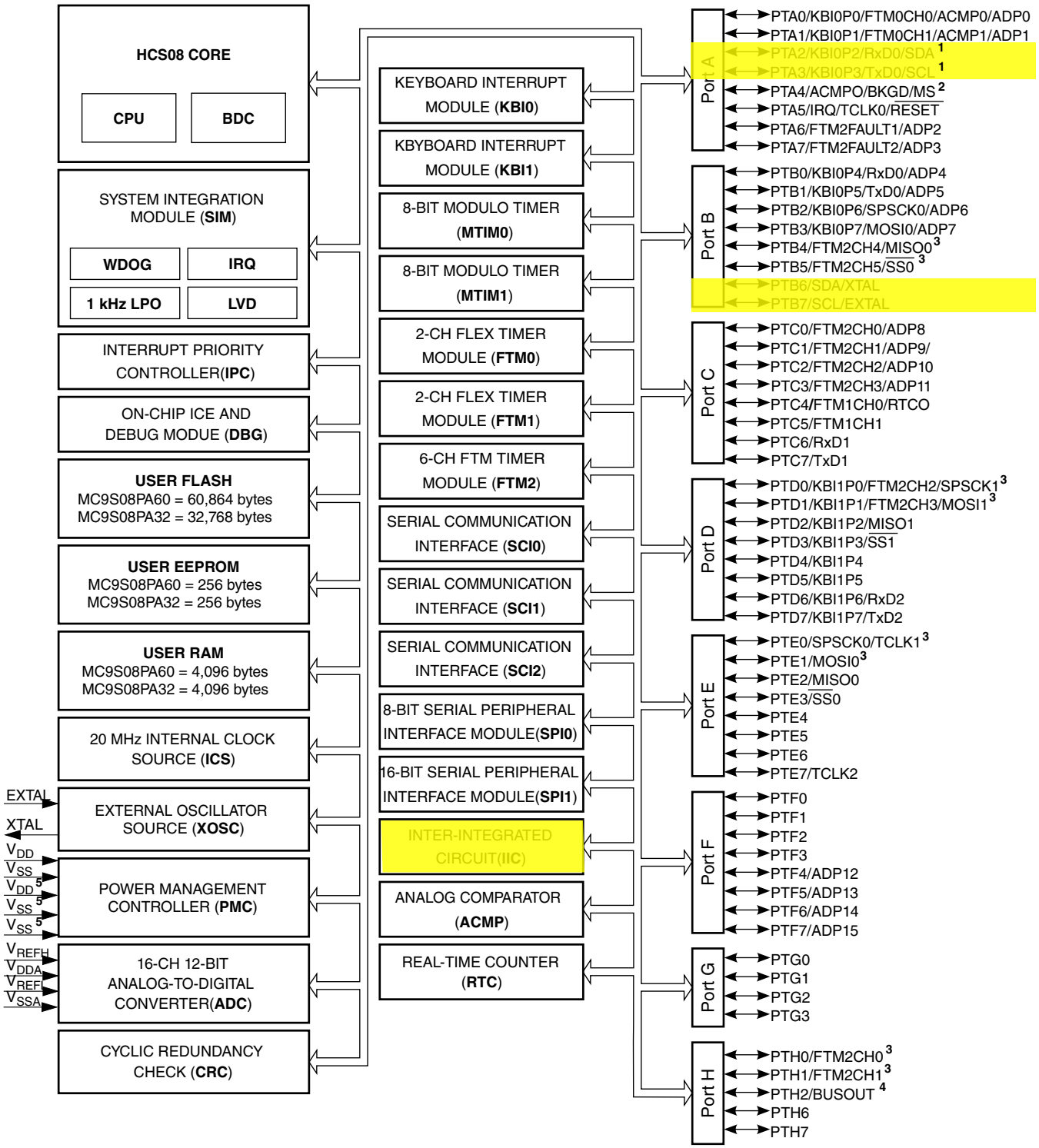
1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-8. Device block diagram highlighting 16-bit SPI module and pins

9.9.4 Inter-Integrated Circuit (I2C)

This device contains an inter-integrated circuit (I2C) module for communication with other integrated circuits.

The following figure shows the device block diagram highlighting I2C module and pins.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

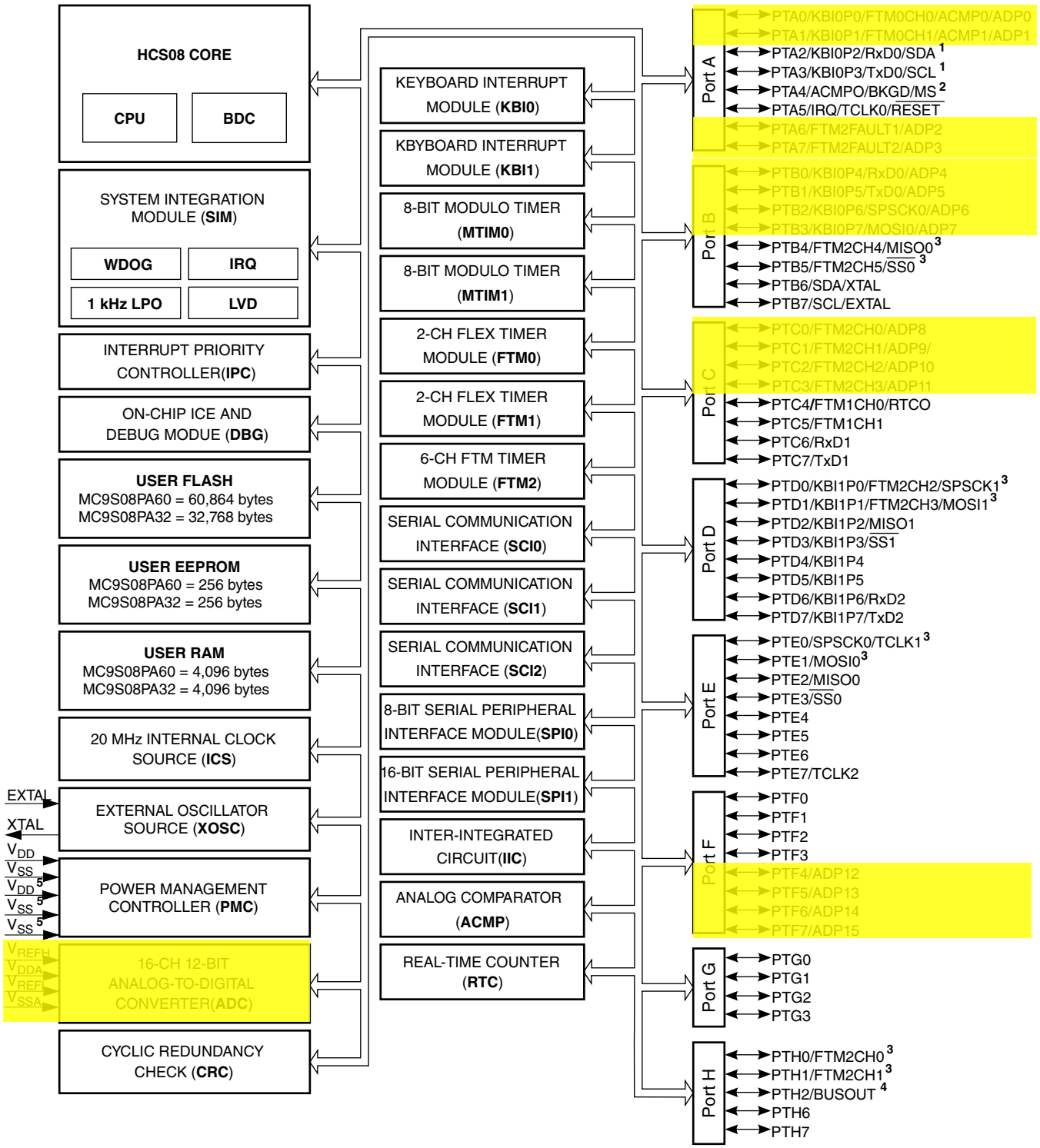
Figure 9-9. Device block diagram highlighting I2C module and pins

9.10 Analog

9.10.1 Analog-to-digital converter (ADC)

This device contains an analog-to-digital converter (ADC) of 12-bit, a successive approximation ADC for operation within an integrated microcontroller system-on-chip. The ADC channel assignments, alternate clock function, and hardware trigger function are configured as described following sections.

The following figure shows device block diagram highlighting ADC module and pins.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-10. Device block diagram highlighting ADC module and pins

9.10.1.1 ADC channel assignments

The ADC channel assignments for the device are shown in the following table. Reserved channels convert to an unknown value.

Table 9-3. ADC channel assignments

ADCH	Channel	Input
00000	AD0	PTA0/ADP0
00001	AD1	PTA1/ADP1
00010	AD2	PTA6/ADP2
00011	AD3	PTA7/ADP3
00100	AD4	PTB0/ADP4
00101	AD5	PTB1/ADP5
00110	AD6	PTB2/ADP6
00111	AD7	PTB3/ADP7
01000	AD8	PTC0/ADP8
01001	AD9	PTC1/ADP9
01010	AD10	PTC2/ADP10
01011	AD11	PTC3/ADP11
01100	AD12	PTF4/ADP12
01101	AD13	PTF5/ADP13
01110	AD14	PTF6/ADP14
01111	AD15	PTF7/ADP15
10000	AD16	V_{SS}
10001	AD17	V_{SS}
10010	AD18	V_{SS}
10011	AD19	Reserved
10100	AD20	Reserved
10101	AD21	Reserved
10110	AD22	Temperature sensor
10111	AD23	Bandgap
11000	AD24	Reserved
11001	AD25	Reserved
11010	AD26	Reserved
11011	AD27	Reserved
11100	AD28	Reserved
11101	AD29	V_{REFH}
11110	AD30	V_{REFL}
11111	Module disabled	None

9.10.1.2 Alternate clock

The ADC module is capable of performing conversions using the MCU bus clock, the bus clock divided by two, the local asynchronous clock (ADACK) within the module, or the alternate clock, ALTCLK. The alternate clock for the devices is the external oscillator output (OSCOUT).

The selected clock source must run at a frequency such that the ADC conversion clock (ADCK) runs at a frequency within its specified range (f_{ADCK}) after being divided down from the ALTCLK input as determined by the ADIV bits.

ALTCLK is active while the MCU is in wait mode provided the conditions described above are met. This allows ALTCLK to be used as the conversion clock source for the ADC while the MCU is in wait mode.

ALTCLK cannot be used as the ADC conversion clock source while the MCU is in stop3 mode.

9.10.1.3 Hardware trigger

The ADC hardware trigger is selectable from MTIM0 overflow, RTC overflow, FTM2 match trigger with 8-bit programmable delay, or FTM2 init trigger with 8-bit programmable delay. The MCU can be configured to use any of those hardware trigger sources in run and wait modes. The RTC overflow can be used as ADC hardware trigger in STOP3 mode. Please refer to ADC hardware trigger.

9.10.1.4 Temperature sensor

The ADC module integrates an on-chip temperature sensor. Following actions must be performed to use this temperature sensor.

- Configure ADC for long sample with a maximum of 1 MHz clock
- Convert the bandgap voltage reference channel (AD23)
  - By converting the digital value of the bandgap voltage reference channel using the value of V_{BG} the user can determine V_{DD}.
- Convert the temperature sensor channel (AD22)
  - By using the calculated value of V_{DD}, convert the digital value of AD22 into a voltage, V_{TEMP}

The following equation provides an approximate transfer function of the on-chip temperature sensor for V_{DD} = 5.0V, Temp = 25°C, using the ADC at f_{ADCK} = 1.0 MHz and configured for long sample.

$$\text{Temp} = 25 - ((V_{TEMP} - V_{TEMP25}) \div m)$$

where:

- V_{TEMP} is the voltage of the temperature sensor channel at the ambient temperature
- V_{TEMP25} is the voltage of the temperature sensor channel at 25 °C
- m is the hot or cold voltage versus temperature slope in V/°C

For temperature calculations, use the V_{TEMP25} and m values in the data sheet.

In application code, you read the temperature sensor channel, calculate V_{TEMP}, and compare it to V_{TEMP25}. If V_{TEMP} is greater than V_{TEMP25}, the cold slope value is applied in the above equation. If V_{TEMP} is less than V_{TEMP25} the hot slope value is applied.

Calibrating at 25°C will improve accuracy to ±4.5°C.

Calibration at three points -40°C, 25°C, and 105°C will improve accuracy to ±2.5°C. After calibration has been completed, you will need to calculate the slope for both hot and cold. In application code, you can calculate the temperature as detailed above and determine if it is above or below 25°C. After you have determined whether the temperature is above or below 25 °C. you can recalculate the temperature using the hot or cold slope value obtained during calibration.

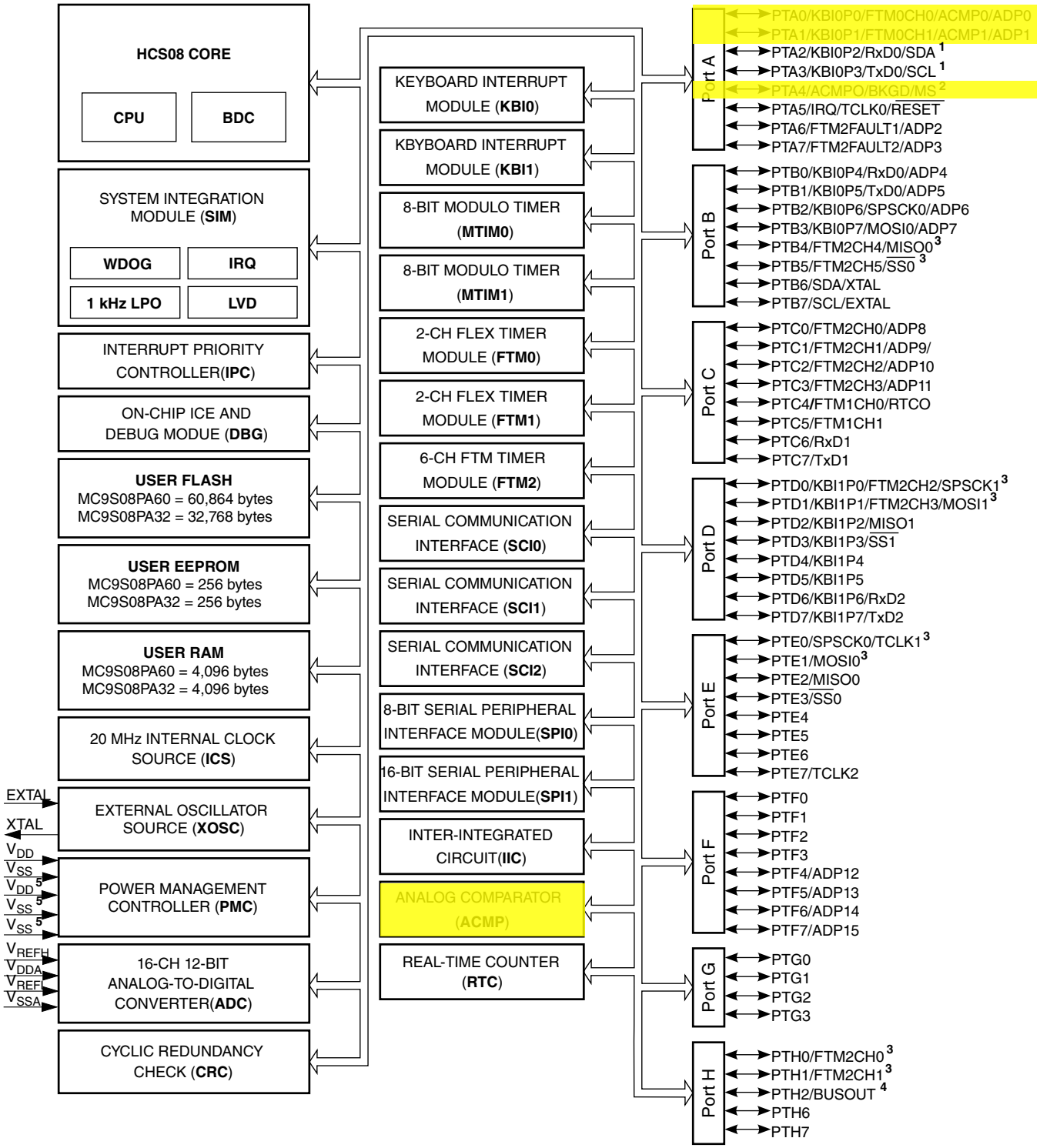
9.10.2 Analog comparator (ACMP)

The analog comparator module (ACMP) provides a circuit for comparing two analog input voltages or for comparing one analog input voltage to an internal reference voltage. The comparator circuit is used to operate across the full range of the supply voltage (rail-to-rail operation).

The ACMP features four different inputs muxed with both positive and negative inputs to the ACMP. One is fixed connected to built-in DAC output. ACMP0 and ACMP1 are externally mapped on pinouts. ACMP2 is reserved.

When using the bandgap reference voltage as the reference voltage to the built-in DAC, the user must enable the bandgap buffer by setting BGBE =1 in SPMSC1. For value of bandgap voltage reference see Bandgap reference.

The following figure shows the device block diagram highlighting ACMP modules and pins.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-11. Device block diagram highlighting ACMP modules and pins

9.10.2.1 ACMP configuration information

The ACMP features four different inputs muxed with both positive and negative inputs to the ACMP. One is fixed connected to built-in DAC output. ACMP0 and ACMP1 are externally mapped on pinouts. ACMP2 is reserved. The following table shows the connection of ACMP input assignments.

Table 9-4. ACMP module external signals

ACMP Channel	Connection
0	PTA0/KBI0P0/FTM0CH0/ACMP0/ADP0
1	PTA1/KBI0P1/FTM0CH1/ACMP1/ADP1
2	Reserved
3	DAC output

When using the bandgap reference voltage as the reference voltage to the built-in DAC, the user must enable the bandgap buffer by setting BGBE =1 in SPMSC1. For value of bandgap voltage reference see Bandgap reference.

9.10.2.2 ACMP in stop3 mode

ACMP continues to operate in stop3 mode if enabled. If ACMP_SC[ACOPE] is enabled, comparator output will operate as in the normal operating mode and will control ACMPO pin. The MCU is brought out of stop when a compare event occurs and ACMP_SC[ACIE] is enabled; ACF flag sets accordingly.

9.10.2.3 ACMP to FTM configuration information

The ACMP module can be configured to connect the output of the analog comparator to FTM1 input capture channel 0 by setting ACIC in SOPT2. With ACIC set, the FTM1CH0 pin is not available externally regardless of the configuration of the FTM1 module for channel 0.

9.10.2.4 ACMP for SCI0 RXD filter

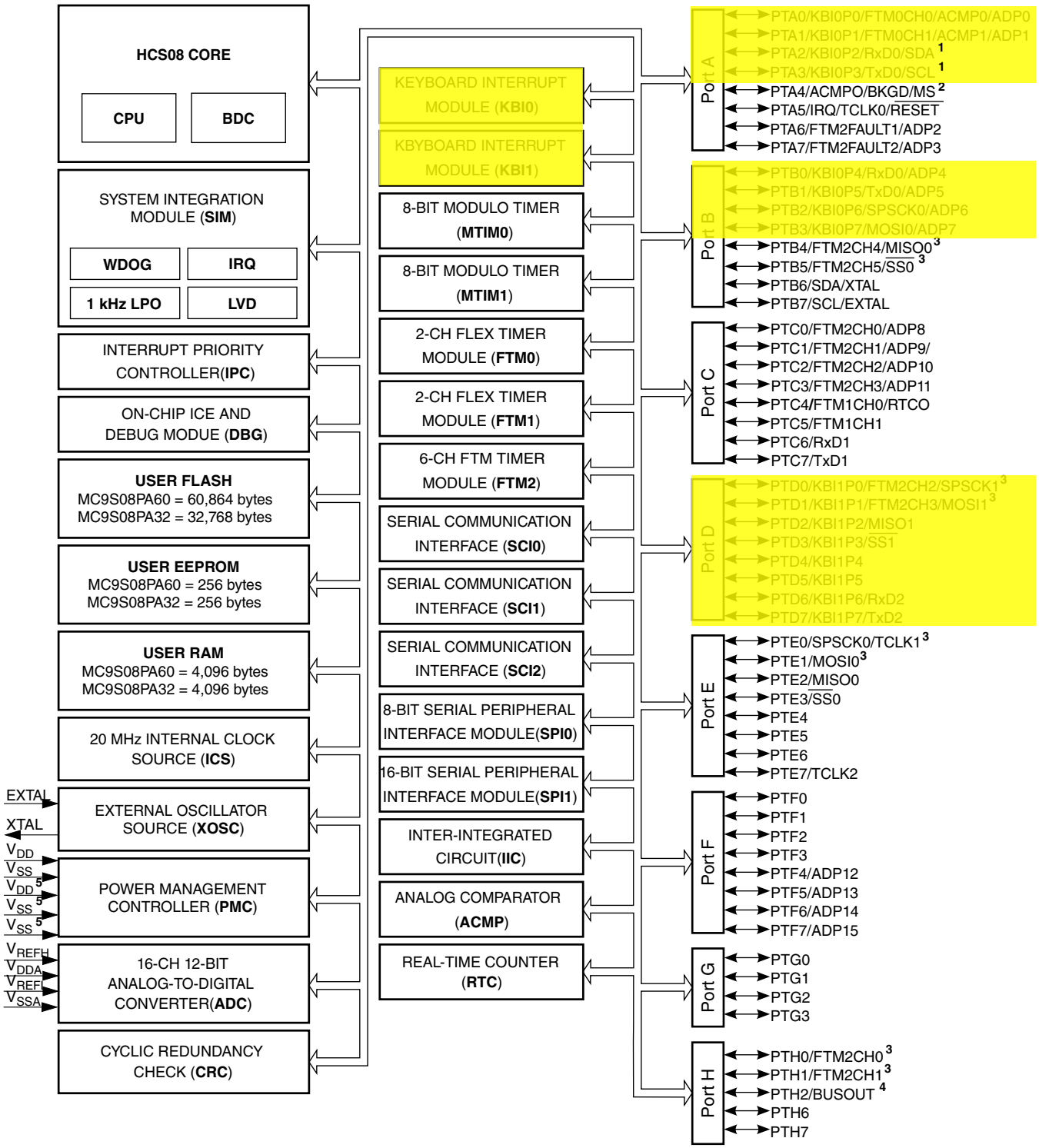
ACMP module output can be directly ejected to SCI0 RxD. In this mode, SCI0 external RxD pinout does not work. Any external signal tagged to ACMP inputs can be regarded as input pins. Please refer SCI0 RxD filter.

9.11 Human-machine interfaces HMI

9.11.1 Keyboard interrupts (KBI)

This device has two KBI modules with up to 16 keyboard interrupt inputs grouped in two KBI modules available depending on packages.

The following figure shows the device block diagram with the KBI modules and pins highlighted.



1. PTA2 and PTA3 operate as true open drain when working as output .
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 and PTH1 can provide high sink/source current drive.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 9-12. Block diagram highlighting KBI modules and pins

Chapter 10
Central processor unit

10.1 Introduction

This section provides summary information about the registers, addressing modes, special operations, instructions and exceptions processing of the HCS08 V6 CPU.

The HCS08 V6 CPU is fully source- and object-code-compatible with the HCS08 CPU.

10.1.1 Features

Features of the HCS08 V6 CPU include:

- Object code fully upward-compatible with M68HC05 and M68HC08 families
- 16-bit stack pointer (any size stack anywhere in 64 KB CPU address space)
- 16-bit index register (H:X) with powerful indexed addressing modes
- 8-bit accumulator (A)
- Many instructions treat X as a second general-purpose 8-bit register
- Seven addressing modes:
  - Inherent — Operands in internal registers
  - Relative — 8-bit signed offset to branch destination
  - Immediate — Operand in next object code byte(s)
  - Direct — Operand in memory at 0x0000–0x00FF
  - Extended — Operand anywhere in 64-Kbyte address space

- Indexed relative to H:X — Five submodes including auto increment
- Indexed relative to SP — Improves C efficiency dramatically

- Memory-to-memory data move instructions with four address mode combinations
- Overflow, half-carry, negative, zero, and carry condition codes support conditional branching on the results of signed, unsigned, and binary-coded decimal (BCD) operations
- Efficient bit manipulation instructions
- STOP and WAIT instructions to invoke low-power operating modes

10.2 Programmer's Model and CPU Registers

Figure 10-1 shows the five CPU registers. CPU registers are not part of the memory map.

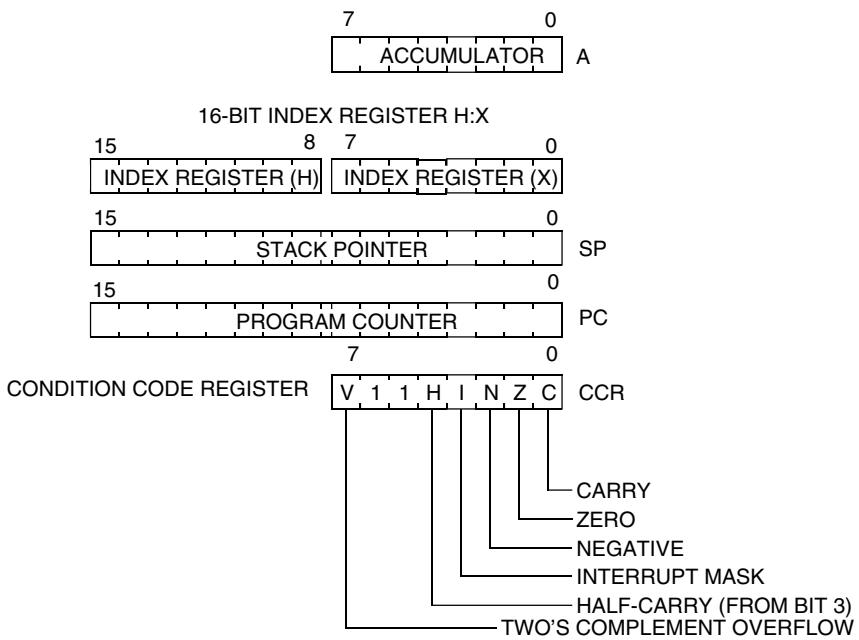


Figure 10-1. CPU Registers

10.2.1 Accumulator (A)

The A accumulator is a general-purpose 8-bit register. One input operand from the arithmetic logic unit (ALU) is connected to the accumulator, and the ALU results are often stored into the A accumulator after arithmetic and logical operations. The

accumulator can be loaded from memory using various addressing modes to specify the address where the loaded data comes from, or the contents of A can be stored to memory using various addressing modes to specify the address where data from A will be stored.

Reset has no effect on the contents of the A accumulator.

10.2.2 Index Register (H:X)

This 16-bit register is actually two separate 8-bit registers (H and X), which often work together as a 16-bit address pointer where H holds the upper byte of an address and X holds the lower byte of the address. All indexed addressing mode instructions use the full 16-bit value in H:X as an index reference pointer; however, for compatibility with the earlier M68HC05 family, some instructions operate only on the low-order 8-bit half (X).

Many instructions treat X as a second general-purpose 8-bit register that can be used to hold 8-bit data values. X can be cleared, incremented, decremented, complemented, negated, shifted, or rotated. Transfer instructions allow data to be transferred from A or transferred to A where arithmetic and logical operations can then be performed.

For compatibility with the earlier M68HC05 family, H is forced to 0x00 during reset. Reset has no effect on the contents of X.

10.2.3 Stack Pointer (SP)

This 16-bit address pointer register points at the next available location on the automatic last-in-first-out (LIFO) stack. The stack may be located anywhere in the 64 KB address space that has RAM, and can be any size up to the amount of available RAM. The stack is used to automatically save the return address for subroutine calls, the return address and CPU registers during interrupts, and for local variables. The AIS (add immediate to stack pointer) instruction adds an 8-bit signed immediate value to SP. This is most often used to allocate or deallocate space for local variables on the stack.

SP is forced to 0x00FF at reset for compatibility with the earlier M68HC05 family. HCS08 V6 programs normally change the value in SP to the address of the last location (highest address) in on-chip RAM during reset initialization to free up direct page RAM (from the end of the on-chip registers to 0x00FF).

The RSP (reset stack pointer) instruction was included for compatibility with the M68HC05 family and is seldom used in new HCS08 V6 programs because it affects only the low-order half of the stack pointer.

10.2.4 Program Counter (PC)

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

During normal program execution, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, interrupt, and return operations load the program counter with an address other than that of the next sequential location. This is called a change-of-flow.

During reset, the program counter is loaded with the reset vector that is located at 0xFFFE and 0xFFFF. The vector stored there is the address of the first instruction that will be executed after exiting the reset state.

10.2.5 Condition Code Register (CCR)

The 8-bit condition code register contains the interrupt mask (I) and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code bits in general terms.

Table 10-1. CCR Register Field Descriptions

Field	Description
7 V	**Two's Complement Overflow Flag** — The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag. 0 No overflow 1 Overflow
4 H	**Half-Carry Flag** — The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C condition code bits to automatically add a correction value to the result from a previous ADD or ADC on BCD operands to correct the result to a valid BCD value. 0 No carry between bits 3 and 4 1 Carry between bits 3 and 4
3 I	**Interrupt Mask Bit** — When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the first instruction of the interrupt service routine is executed. Interrupts are not recognized at the instruction boundary after any instruction that clears I (CLI or TAP). This ensures that the next instruction after a CLI or TAP will always be executed without the possibility of an intervening interrupt, provided I was set. 0 Interrupts enabled

Table continues on the next page...

Table 10-1. CCR Register Field Descriptions (continued)

Field	Description
	1 Interrupts disabled
2 N	**Negative Flag** — The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result. Simply loading or storing an 8-bit or 16-bit value causes N to be set if the most significant bit of the loaded or stored value was 1. 0 Non-negative result 1 Negative result
1 Z	**Zero Flag** — The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of 0x00 or 0x0000. Simply loading or storing an 8-bit or 16-bit value causes Z to be set if the loaded or stored value was all 0s. 0 Non-zero result 1 Zero result
0 C	**Carry/Borrow Flag** — The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag. 0 No carry out of bit 7 1 Carry out of bit 7

10.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08 V6, memory, status and control registers, and input/output (I/O) ports share a single 64 KB CPU address space. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

Every addressing mode, except inherent, generates a 16-bit effective address. The effective address is the address of the memory location that the instruction acts on. Effective address computations do not require extra execution cycles. The HCS08 V6 CPU uses the 16 addressing modes described in the following sections.

10.3.1 Inherent Addressing Mode (INH)

In this addressing mode, instructions either have no operands or all operands are in internal CPU registers. In either case, the CPU does not need to access any memory locations to complete the instruction. Examples:

```
NOP          ;this instruction has no operands
CLRA         ;operand is a CPU register
```

10.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed two's complement byte offset value is located in the memory location immediately following the opcode. The offset gives a branching range of -128 to +127 bytes. In most assemblers, the programmer does not need to calculate the offset, because the assembler determines the proper offset and verifies that it is within the span of the branch.

During program execution, if a branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address. If a branch condition is false, the CPU executes the next instruction.

10.3.3 Immediate Addressing Mode (IMM)

The operand for instructions with the immediate addressing mode is contained in the byte(s) immediately following the opcode. The byte or bytes that follow the opcode are the value of the statement rather than the address of the value. The pound symbol (#) is used to indicate an immediate addressing mode operand. One very common programming error is to accidentally omit the # symbol. This causes the assembler to misinterpret the following expression as an address rather than explicitly provided data. For example LDA #$55 means to load the immediate value $55 into the accumulator, while LDA $55 means to load the value from address $0055 into the accumulator. Without the # symbol, the instruction is erroneously interpreted as a direct addressing instruction.

Example:

```
LDA       #$55
CPHX      #$FFFF
LDHX      #$67
```

The size of the immediate operand is implied by the instruction context. In the third example, the instruction implies a 16-bit immediate value, but only an 8-bit value is supplied. In this case the assembler generates the 16-bit value $0067 because the CPU expects a 16-bit value in the instruction stream.

10.3.4 Direct Addressing Mode (DIR)

This addressing mode is sometimes called zero-page addressing because it accesses operands in the address range $0000 through $00FF. Since these addresses always begin with $00, only the low byte of the address needs to be included in the instruction, which saves program space and execution time. A system can be optimized by placing the most commonly accessed data in this area of memory. The low byte of the operand address is supplied with the instruction and the high byte of the address is assumed to be zero.

Examples:

```
LDA       $55
```

The value $55 is taken to be the low byte of an address in the range $0000 through $00FF. The high byte of the address is assumed to be zero. During execution, the CPU combines the value $55 from the instruction with the assumed value of $00 to form the address $0055, which is then used to access the data to be loaded into accumulator.

```
LDHX      $20
```

In this example, the value $20 is combined with the assumed value of $00 to form the address $0020. Since the LDHX instruction requires a 16-bit value, a 16-bit word of data is read from addresses $0020 and $0021. After execution, the H:X index register has the value from address $0020 in its high byte and the value from address $0021 in its low byte. The same happens for CPHX and STHX.

```
BRSET     0,$80,foo
```

In this example, direct addressing is used to access the operand and relative addressing is used to identify the destination address of a branch, in case the branch-taken conditions are met. This is also the case for BRCLR.

10.3.5 Extended Addressing Mode (EXT)

In extended addressing, the full 16-bit address of the memory location to be operated on is provided in the instruction. Extended addressing can access any location in the 64 KB memory map.

Example:

```
LDA     $F03B
```

This instruction uses extended addressing because $F03B is above the zero page. In most assemblers, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

10.3.6 Indexed Addressing Mode

Indexed addressing mode has seven variations, including five that use the 16-bit H:X index register pair and two that use the stack pointer as the base reference.

10.3.6.1 Indexed, No Offset (IX)

Instructions using the indexed, no offset addressing mode are one-byte instructions that can access data with variable addresses. The X (Index register low byte) register contains the low byte of the conditional address of the operand and the H (Index register high byte) register contains the high byte of the address.

Indexed, no offset instructions can move a pointer through a table or hold the address of a frequently used RAM or input/output (I/O) location.

10.3.6.2 Indexed, No Offset with Post Increment (IX+)

Instructions using the indexed, no offset with post increment addressing mode are two-byte instructions that address the operands and then increment the Index register (H:X). The X (Index register low byte) register contains the low byte of the conditional address of the operand and the H (Index register high byte) register contains the high byte of the address. This addressing mode is usually used for table searches. MOV and CBEQ instructions use this addressing mode as well.

10.3.6.3 Indexed, 8-Bit Offset (IX1)

Indexed with 8-bit offset instructions are two-byte instructions that can access data with a variable address. The CPU adds the unsigned bytes in the H:X register to the unsigned byte immediately following the opcode. The sum is the effective address.

Indexed, 8-bit offset instructions are useful in selecting the k-th element in an n-element table. The table can begin anywhere and can extend as far as the address map allows. The k value would typically be in H:X, and the address of the beginning of the table would be

in the byte following the opcode. Using H:X in this way, this addressing mode is limited to the first 256 addresses in memory. Tables can be located anywhere in the address map when H:X is used as the base address, and the byte following the opcode is the offset.

10.3.6.4 Indexed, 8-Bit Offset with Post Increment (IX1+)

Indexed, 8-bit offset with post-increment instructions are three-byte instructions that access the operands with variable addresses, then increment H:X. The CPU adds the unsigned bytes in the H:X register to the byte immediately following the opcode. The sum is the effective address. This addressing mode is generally used for table searches. This addressing mode is used for CBEQ instruction.

10.3.6.5 Indexed, 16-Bit Offset (IX2)

Indexed, 16-bit offset instructions are three-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned contents of H:X to the 16-bit unsigned word formed by the two bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the most significant byte of the 16-bit offset; the second byte is the least significant byte of the 16-bit offset. As with direct and extended addressing, most assemblers determine the shortest form of indexed addressing.

Indexed, 16-bit offset instructions are useful in selecting the k-th element in an n-element table. The table can begin anywhere and can extend as far as the address map allows. The k value would typically be in H:X, and the address of the beginning of the table would be in the bytes following the opcode.

10.3.6.6 SP-Relative, 8-Bit Offset (SP1)

Stack pointer, 8-bit offset instructions are three-byte instructions that address operands in much the same way as indexed 8-bit offset instructions, except that the 8-bit offset is added to the value of the stack pointer instead of the index register.

The stack pointer, 8-bit offset addressing mode permits easy addressing of data on the stack. The CPU adds the unsigned byte in the 16-bit stack pointer (SP) register to the unsigned byte following the opcode. The sum is the effective address of the operand. If interrupts are disabled, this addressing mode allows the stack pointer to be used as a second "index" register.

Stack pointer relative instructions require a pre-byte for access. Consequently, all SP relative instructions take one cycle longer than their index relative counterparts.

10.3.6.7 SP-Relative, 16-Bit Offset (SP2)

Stack pointer, 16-bit offset instructions are four-byte instructions used to access data relative to the stack pointer with variable addresses at any location in memory. The CPU adds the unsigned contents of the 16-bit stack pointer to the 16-bit unsigned word formed by the two bytes following the opcode. The sum is the effective address of the operand.

As with direct and extended addressing, most assemblers determine the shortest form of stack pointer addressing. Due to the pre-byte, stack pointer relative instructions take one cycle longer than their index relative counterparts.

Stack pointer, 16-bit offset instructions are useful in selecting the k-th element a an n-element table. The table can begin anywhere and can extend anywhere in memory. The k value would typically be in the stack pointer register, and the address of the beginning of the table is located in the two bytes following the two-byte opcode.

10.3.7 Memory to memory Addressing Mode

Memory to memory addressing mode has the following four variations.

10.3.7.1 Direct to Direct

This addressing mode is used to move data within the direct page of memory. Both the source operand and the destination operand are in the direct page. The source data is addressed by the first byte immediately following the opcode, and the destination location is addressed by the second byte following the opcode.

10.3.7.2 Immediate to Direct

This addressing mode is used to move an 8-bit constant to any location in the direct page memory. The source data is the byte immediately following the opcode, and the destination is addressed by the second byte following the opcode.

10.3.7.3 Indexed to Direct, Post Increment

Used only by the MOV instruction, this addressing mode accesses a source operand addressed by the H:X register, and a destination location within the direct page addressed by the byte following the opcode. H:X is incremented after the source operand is accessed.

10.3.7.4 Direct to Indexed, Post-Increment

Used only with the MOV instruction, this addressing mode accesses a source operand addressed by the byte following the opcode, and a destination location addressed by the H:X register. H:X is incremented after the destination operand is written.

10.4 Operation modes

The CPU can be placed into the following operation modes: stop, wait, background and security.

10.4.1 Stop mode

Usually, all system clocks, including the crystal oscillator (when used), are halted during stop mode to minimize power consumption. In such systems, external circuitry is needed to control the time spent in stop mode and to issue a signal to wake up the target MCU when it is time to resume processing. Unlike the earlier M68HC05 and M68HC08 MCUs, the HCS08 V6 can be configured to keep a minimum set of clocks running in stop mode. This optionally allows an internal periodic signal to wake the target MCU from stop mode.

When a host debug system is connected to the background debug pin (BKGD) and the ENBDM control bit has been set by a serial command through the background interface (or because the MCU was reset into active background mode), the oscillator is forced to remain active when the MCU enters stop mode. In this case, if a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in stop mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in stop mode.

10.4.2 Wait mode

The WAIT instruction enables interrupts by clearing the I bit in the CCR. It then halts the clocks to the CPU to reduce overall power consumption while the CPU is waiting for the interrupt or reset event that will wake the CPU from wait mode. When an interrupt or reset event occurs, the CPU clocks will resume and the interrupt or reset event will be processed normally.

If a serial BACKGROUND command is issued to the MCU through the background debug interface while the CPU is in wait mode, CPU clocks will resume and the CPU will enter active background mode where other serial background commands can be processed. This ensures that a host development system can still gain access to a target MCU even if it is in wait mode.

While in wait mode, there are some restrictions on which background debug commands can be used. Only the BACKGROUND command and memory-access-with-status commands are available while in wait mode. The memory-access-with-status commands do not allow memory access, but they report an error indicating that the CPU is in either stop or wait mode. The BACKGROUND command can be used to wake the CPU from wait mode and enter active background mode.

10.4.3 Background mode

Background instruction (BGND) is not used in normal user programs because it forces the CPU to stop processing user instructions and enter the active background mode waiting for serial background commands. The only way to resume execution of the user program is through reset or by a host debug system issuing a GO, TRACE1, or TAGGO serial command through the background debug interface.

Software-based breakpoints can be set by replacing an opcode at the desired breakpoint address with the BGND opcode. When the program reaches this breakpoint address, the CPU is forced to active background mode rather than continuing the user program.

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 V6 core. The BDC provides the means for analyzing MCU operation during software development. Active background mode is entered in any of the following ways:

- When the BKGD/MS pin is low at the time the MCU exits reset.
- When a BACKGROUND command is received through the BKGD pin.

- When a BGND instruction is executed.
- When encountering a BDC breakpoint.

Background commands are of two types:

- Non-intrusive commands, defined as commands that can be issued while the user program is running. Non-intrusive commands can be issued through the BKGD pin while the MCU is in run mode; non-intrusive commands can also be executed when the MCU is in the active background mode. Non-intrusive commands include:
  - Memory access commands
  - Memory-access-with-status commands
  - BDC register access commands
  - The BACKGROUND command
- Active background commands, which can be executed only while the MCU is in active background mode. Active background commands include commands to:
  - Read or write CPU registers
  - Trace one user program instruction at a time
  - Leave active background mode to return to the user's application program (GO)

The active background mode is used to program a bootloader or user application program into the flash program memory before the MCU is operated in run mode for the first time. The active background mode can also be used to erase and reprogram the flash memory after it has been previously programmed.

10.4.4 Security mode

Usually HCS08 V6 MCUs are implemented with a secure operating mode. When in secure mode, external access to internal memory is restricted, so that only instructions fetched from secure memory can access secure memory.

The method by which the MCU is put into secure mode is not defined by the HCS08 V6 Core. The core receives an external input signal that, when asserted, informs to the core that the MCU is in secure mode.

While in secure mode, the core controls the following set of conditions:

1. The RAM, flash, and EEPROM arrays are considered secure memory. All registers in Direct Page or High Page are considered non-secure memory.
2. Read data is tagged as either secure or non-secure during a program read, depending on whether the read is from secure or non-secure memory.
3. A data read of secure memory returns a value of $00 when the current instruction is tagged as non-secure or the access is a BDC access.
4. A data write to secure memory is blocked and data at the target address does not change state when the current instruction is tagged as non-secure or the access is through BDC.
5. A data write to secure memory is never blocked during the stacking cycles of interrupt service routines.
6. Data accesses to either secure or non-secure memory are allowed when the current instruction is tagged as secure.
7. BDC accesses to non-secure memory are allowed.

When the device is in the non-secure mode, secure memory is treated the same as non-secure memory, and all accesses are allowed.

Table 10-2 details the security conditions for allowing or disabling a read access.

Table 10-2. Security conditions for read access

Inputs conditions					Read control
Security enabled	Ram, flash or EEPROM access	Program or vector read	Current CPU instruction from secure memory	Current access is via BDC	Read access allowed
0	x	x	x	x	1
1	0	x	x	x	1
1	1	1	x	x	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0

10.5 HCS08 V6 Opcodes

The HCS08 V6 Core has 254 one-byte opcodes and 47 two-byte opcodes, totaling 301 opcodes. For a more detailed description of the HCS08 V6 instructions please refer to the Instruction Set Summary section.

10.6 Special Operations

The CPU performs a few special operations that are similar to instructions but do not have opcodes like other CPU instructions. This section provides additional information about these operations.

10.6.1 Reset Sequence

Reset can be caused by a power-on-reset (POR) event, internal conditions such as the COP (computer operating properly) watchdog, or by assertion of an external active-low reset pin. When a reset event occurs, the CPU immediately stops whatever it is doing (the MCU does not wait for an instruction boundary before responding to a reset event).

The reset event is considered concluded when the sequence to determine whether the reset came from an internal source is done and when the reset pin is no longer asserted. At the conclusion of a reset event, the CPU performs a 6-cycle sequence to fetch the reset vector from $FFFE and $FFFF and to fill the instruction queue in preparation for execution of the first program instruction.

10.6.2 Interrupt Sequence

When an interrupt is requested, the CPU completes the current instruction before responding to the interrupt. At this point, the program counter is pointing at the start of the next instruction, which is where the CPU should return after servicing the interrupt. The CPU responds to an interrupt by performing the same sequence of operations as for a software interrupt (SWI) instruction, except the address used for the vector fetch is determined by the highest priority interrupt that is pending when the interrupt sequence started.

The CPU sequence for an interrupt is:

1. Store the contents of PCL, PCH, X, A, and CCR on the stack, in that order.
2. Set the I bit in the CCR.
3. Fetch the high-order half of the interrupt vector.
4. Fetch the low-order half of the interrupt vector.
5. Delay for one free bus cycle.

Fetch three bytes of program information starting at the address indicated by the interrupt vector to fill the instruction queue in preparation for execution of the first instruction in the interrupt service routine.

After the CCR contents are pushed onto the stack, the I bit in the CCR is set to prevent other interrupts while in the interrupt service routine. Although it is possible to clear the I bit with an instruction in the interrupt service routine, this would allow nesting of interrupts (which is not recommended because it leads to programs that are difficult to debug and maintain).

For compatibility with the earlier M68HC05 MCUs, the high-order half of the H:X index register pair (H) is not saved on the stack as part of the interrupt sequence. The user must use a PSHH instruction at the beginning of the service routine to save H and then use a PULH instruction just before the RTI that ends the interrupt service routine. It is not necessary to save H if you are certain that the interrupt service routine does not use any instructions or auto-increment addressing modes that might change the value of H.

The software interrupt (SWI) instruction is like a hardware interrupt except that it is not masked by the global I bit in the CCR and it is associated with an instruction opcode within the program so it is not asynchronous to program execution.

10.7 Instruction Set Summary

Table 10-3. Instruction Set Summary

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
ADC #opr8i	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM	A9	ii	2
ADC opr8a			↕	↕	–	↕	↕	↕	DIR	B9	dd	3
ADC opr16a			↕	↕	–	↕	↕	↕	EXT	C9	hh ll	4
ADC oprx16,X			↕	↕	–	↕	↕	↕	IX2	D9	ee ff	4
ADC oprx8,X			↕	↕	–	↕	↕	↕	IX1	E9	ff	3
ADC ,X			↕	↕	–	↕	↕	↕	IX	F9		3
ADC oprx16,SP			↕	↕	–	↕	↕	↕	SP2	9ED9	ee ff	5
ADC oprx8,SP			↕	↕	–	↕	↕	↕	SP1	9EE9	ff	4

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
ADD #opr8i	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM	AB	ii	2
ADD opr8a			↕	↕	–	↕	↕	↕	DIR	BB	dd	3
ADD opr16a			↕	↕	–	↕	↕	↕	EXT	CB	hh ll	4
ADD oprx16,X			↕	↕	–	↕	↕	↕	IX2	DB	ee ff	4
ADD oprx8,X			↕	↕	–	↕	↕	↕	IX1	EB	ff	3
ADD ,X			↕	↕	–	↕	↕	↕	IX	FB		3
ADD oprx16,SP			↕	↕	–	↕	↕	↕	SP2	9EDB	ee ff	5
ADD oprx8,SP			↕	↕	–	↕	↕	↕	SP1	9EEB	ff	4
AIS #opr8i	Add Immediate Value (Signed) to Stack Pointer	SP ← (SP) + (M) where M is sign extended to a 16-bit value	–	–	–	–	–	–	IMM	A7	ii	2
AIX #opr8i	Add Immediate Value (Signed) to Index Register (H:X)	H:X ← (H:X) + (M) where M is sign extended to a 16-bit value	–	–	–	–	–	–	IMM	AF	ii	2
AND #opr8i	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM	A4	ii	2
AND opr8a			0	–	–	↕	↕	–	DIR	B4	dd	3
AND opr16a			0	–	–	↕	↕	–	EXT	C4	hh ll	4
AND oprx16,X			0	–	–	↕	↕	–	IX2	D4	ee ff	4
AND oprx8,X			0	–	–	↕	↕	–	IX1	E4	ff	3
AND ,X			0	–	–	↕	↕	–	IX	F4		3
AND oprx16,SP			0	–	–	↕	↕	–	SP2	9ED4	ee ff	5
AND oprx8,SP			0	–	–	↕	↕	–	SP1	9EE4	ff	4
ASL opr8a	Arithmetic Shift Left (same as LSL)	C ← MSB, LSB ← 0	↕	–	–	↕	↕	↕	DIR	38	dd	5
ASLA			↕	–	–	↕	↕	↕	INH	48		1
ASLX			↕	–	–	↕	↕	↕	INH	58		1
ASL oprx8,X			↕	–	–	↕	↕	↕	IX1	68	ff	5
ASL ,X			↕	–	–	↕	↕	↕	IX	78		4
ASL oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E68	ff	6
ASR opr8a	Arithmetic Shift Right	MSB → MSB, LSB → C	↕	–	–	↕	↕	↕	DIR	37	dd	5
ASRA			↕	–	–	↕	↕	↕	INH	47		1
ASRX			↕	–	–	↕	↕	↕	INH	57		1
ASR oprx8,X			↕	–	–	↕	↕	↕	IX1	67	ff	5
ASR ,X			↕	–	–	↕	↕	↕	IX	77		4
ASR oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E67	ff	6
BCC rel	Branch if Carry Bit Clear	Branch if (C) = 0	–	–	–	–	–	–	REL	24	rr	3
			–	–	–	–	–	–	DIR (b0)	11	dd	5

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BCLR n,opr8a	Clear Bit n in Memory	Mn ← 0	–	–	–	–	–	–	DIR (b1)	13	dd	5
			–	–	–	–	–	–	DIR (b2)	15	dd	5
			–	–	–	–	–	–	DIR (b3)	17	dd	5
			–	–	–	–	–	–	DIR (b4)	19	dd	
			–	–	–	–	–	–	DIR (b5)	1B	dd	5
			–	–	–	–	–	–	DIR (b6)	1D	dd	5
			–	–	–	–	–	–	DIR (b7)	1F	dd	5
BCS rel	Branch if Carry Bit Set (same as BLO)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ rel	Branch if Equal	Branch if (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE rel	Branch if Greater Than or Equal To (Signed Operands)	Branch if (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGND	Enter Active Background if ENBDM = 1	Waits For and Processes BDM Commands Until GO, TRACE1, or TAGGO	–	–	–	–	–	–	INH	82		5+
BGT rel	Branch if Greater Than (Signed Operands)	Branch if (Z) ǀ (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC rel	Branch if Half Carry Bit Clear	Branch if (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS rel	Branch if Half Carry Bit Set	Branch if (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI rel	Branch if Higher	Branch if (C) ǀ (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS rel	Branch if Higher or Same (same as BCC)	Branch if (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH rel	Branch if IRQ Pin High	Branch if IRQ pin = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL rel	Branch if IRQ Pin Low	Branch if IRQ pin = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #opr8i	Bit Test	(A) & (M), (CCR Updated but Operands Not Changed)	0	–	–	↕	↕	–	IMM	A5	ii	2
BIT opr8a			0	–	–	↕	↕	–	DIR	B5	dd	3
BIT opr16a			0	–	–	↕	↕	–	EXT	C5	hh ll	4
BIT oprx16,X			0	–	–	↕	↕	–	IX2	D5	ee ff	4
BIT oprx8,X			0	–	–	↕	↕	–	IX1	E5	ff	3
BIT ,X			0	–	–	↕	↕	–	IX	F5		3
BIT oprx16,SP			0	–	–	↕	↕	–	SP2	9ED5	ee ff	5
BIT oprx8,SP			0	–	–	↕	↕	–	SP1	9EE5	ff	4

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BLE rel	Branch if Less Than or Equal To (Signed Operands)	Branch if (Z) | (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO rel	Branch if Lower (Same as BCS)	Branch if (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS rel	Branch if Lower or Same	Branch if (C) | (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT rel	Branch if Less Than (Signed Operands)	Branch if (N ⊕ V) = 1	–	–	–	–	–	–	REL	91	rr	3
BMC rel	Branch if Interrupt Mask Clear	Branch if (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI rel	Branch if Minus	Branch if (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS rel	Branch if Interrupt Mask Set	Branch if (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE rel	Branch if Not Equal	Branch if (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL rel	Branch if Plus	Branch if (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA rel	Branch Always	No Test	–	–	–	–	–	–	REL	20	rr	3
BRCLR n,opr8a,rel	Branch if Bit n in Memory Clear	Branch if (Mn) = 0	–	–	–	–	–	↕	DIR (b0)	01	dd rr	5
			–	–	–	–	–	↕	DIR (b1)	03	dd rr	5
			–	–	–	–	–	↕	DIR (b2)	05	dd rr	5
			–	–	–	–	–	↕	DIR (b3)	07	dd rr	5
			–	–	–	–	–	↕	DIR (b4)	09	dd rr	5
			–	–	–	–	–	↕	DIR (b5)	0B	dd rr	5
			–	–	–	–	–	↕	DIR (b6)	0D	dd rr	5
			–	–	–	–	–	↕	DIR (b7)	0F	dd rr	5
BRN rel	Branch Never	Uses 3 Bus Cycles	–	–	–	–	–	–	REL	21	rr	3
BRSET n,opr8a,rel	Branch if Bit n in Memory Set	Branch if (Mn) = 1	–	–	–	–	–	↕	DIR (b0)	00	dd rr	5
			–	–	–	–	–	↕	DIR (b1)	02	dd rr	5
			–	–	–	–	–	↕	DIR (b2)	04	dd rr	5
			–	–	–	–	–	↕	DIR (b3)	06	dd rr	5
			–	–	–	–	–	↕	DIR (b4)	08	dd rr	5
			–	–	–	–	–	↕	DIR (b5)	0A	dd rr	5
			–	–	–	–	–	↕	DIR (b6)	0C	dd rr	5
			–	–	–	–	–	↕	DIR (b7)	0E	dd rr	5
			–	–	–	–	–	–	DIR (b0)	10	dd	5
			–	–	–	–	–	–	DIR (b1)	12	dd	5
			–	–	–	–	–	–	DIR (b2)	14	dd	5

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
BSET n,opr8a	Set Bit n in Memory	Mn ← 1	–	–	–	–	–	–	DIR (b3)	16	dd	5
			–	–	–	–	–	–	DIR (b4)	18	dd	5
			–	–	–	–	–	–	DIR (b5)	1A	dd	5
			–	–	–	–	–	–	DIR (b6)	1C	dd	5
			–	–	–	–	–	–	DIR (b7)	1E	dd	5
BSR rel	Branch to Subroutine	PC ← (PC) + 0x0002 push (PCL) SP ← (SP) – 0x0001 push (PCH) SP ← (SP) – 0x0001 PC ← (PC) + rel	–	–	–	–	–	–	REL	AD	rr	5
CBEQ opr8a,rel	Compare and Branch if Equal	Branch if (A) = (M)	–	–	–	–	–	–	DIR	31	dd rr	5
CBEQA #opr8i,rel		Branch if (A) = (M)	–	–	–	–	–	–	IMM	41	ii rr	4
CBEQX #opr8i,rel		Branch if (X) = (M)	–	–	–	–	–	–	IMM	51	ii rr	4
CBEQ oprx8,X+,rel		Branch if (A) = (M)	–	–	–	–	–	–	IX1+	61	ff rr	5
CBEQ ,X+,rel		Branch if (A) = (M)	–	–	–	–	–	–	IX+	71	rr	5
CBEQ oprx8,SP,rel		Branch if (A) = (M)	–	–	–	–	–	–	SP1	9E61	ff rr	6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask Bit	I ← 0	–	–	0	–	–	–	INH	9A		1
CLR opr8a	Clear	M ← 0x00	0	–	–	0	1	–	DIR	3F	dd	5
CLRA		A ← 0x00	0	–	–	0	1	–	INH	4F		1
CLRX		X ← 0x00	0	–	–	0	1	–	INH	5F		1
CLRH		H ← 0x00	0	–	–	0	1	–	INH	8C		1
CLR oprx8,X		M ← 0x00	0	–	–	0	1	–	IX1	6F	ff	5
CLR ,X		M ← 0x00	0	–	–	0	1	–	IX	7F		4
CLR oprx8,SP		M ← 0x00	0	–	–	0	1	–	SP1	9E6F	ff	6
CMP #opr8i	Compare Accumulator with Memory	(A) – (M); (CCR Updated But Operands Not Changed)	↕	–	–	↕	↕	↕	IMM	A1	ii	2
CMP opr8a			↕	–	–	↕	↕	↕	DIR	B1	dd	3
CMP opr16a			↕	–	–	↕	↕	↕	EXT	C1	hh ll	4
CMP oprx16,X			↕	–	–	↕	↕	↕	IX2	D1	ee ff	4
CMP oprx8,X			↕	–	–	↕	↕	↕	IX1	E1	ff	3
CMP ,X			↕	–	–	↕	↕	↕	IX	F1		3
CMP oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED1	ee ff	5

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
CMP oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE1	ff	4
COM opr8a	One's Complement	M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	DIR	33	dd	5
COMA		A ← (A) = 0xFF – (A)	0	–	–	↕	↕	1	INH	43		1
COMX		X ← (X) = 0xFF – (X)	0	–	–	↕	↕	1	INH	53		1
COM oprx8,X		M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	IX1	63	ff	5
COM ,X		M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	IX	73		4
COM oprx8,SP		M ← (M) = 0xFF – (M)	0	–	–	↕	↕	1	SP1	9E63	ff	6
CPHX opr16a	Compare Index Register (H:X) with Memory	(H:X) – (M:M + 0x0001); (CCR Updated But Operands Not Changed)	↕	–	–	↕	↕	↕	EXT	3E	hh ll	6
CPHX #opr16i			↕	–	–	↕	↕	↕	IMM	65	jj kk	3
CPHX opr8a			↕	–	–	↕	↕	↕	DIR	75	dd	5
CPHX oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EF3	ff	6
CPX #opr8i	Compare X (Index Register Low) with Memory	(X) – (M); (CCR Updated But Operands Not Changed)	↕	–	–	↕	↕	↕	IMM	A3	ii	2
CPX opr8a			↕	–	–	↕	↕	↕	DIR	B3	dd	3
CPX opr16a			↕	–	–	↕	↕	↕	EXT	C3	hh ll	4
CPX oprx16,X			↕	–	–	↕	↕	↕	IX2	D3	ee ff	4
CPX oprx8,X			↕	–	–	↕	↕	↕	IX1	E3	ff	3
CPX ,X			↕	–	–	↕	↕	↕	IX	F3		3
CPX oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED3	ee ff	5
CPX oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE3	ff	4
DAA	Decimal Adjust Accumulator After ADD or ADC of BCD Values	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		1
DBNZ opr8a,rel	Decrement and Branch if Not Zero	Decrement A, X, or M Branch if (result) ≠ 0 Affects X, Not H	–	–	–	–	–	–	DIR	3B	dd rr	7
DBNZA rel			–	–	–	–	–	–	INH	4B	rr	4
DBNZX rel			–	–	–	–	–	–	INH	5B	rr	4
DBNZ oprx8,X,rel			–	–	–	–	–	–	IX1	6B	ff rr	7
DBNZ ,X,rel			–	–	–	–	–	–	IX	7B	rr	6
DBNZ oprx8,SP,rel			–	–	–	–	–	–	SP1	9E6B	ff rr	8
DEC opr8a		M ← (M) – 0x01	↕	–	–	↕	↕	–	DIR	3A	dd	5
DECA		A ← (A) – 0x01	↕	–	–	↕	↕	–	INH	4A		1
DECX		X ← (X) – 0x01	↕	–	–	↕	↕	–	INH	5A		1

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
DEC oprx8,X	Decrement	M ← (M) – 0x01	↕	–	–	↕	↕	–	IX1	6A	ff	5
DEC ,X		M ← (M) – 0x01	↕	–	–	↕	↕	–	IX	7A		4
DEC oprx8,SP		M ← (M) – 0x01	↕	–	–	↕	↕	–	SP1	9E6A	ff	6
DIV	Divide	A ← (H:A)÷(X), H ← Remainder	–	–	–	–	↕	↕	INH	52		6
EOR #opr8i	Exclusive OR Memory with Accumulator	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM	A8	ii	2
EOR opr8a			0	–	–	↕	↕	–	DIR	B8	dd	3
EOR opr16a			0	–	–	↕	↕	–	EXT	C8	hh ll	4
EOR oprx16,X			0	–	–	↕	↕	–	IX2	D8	ee ff	4
EOR oprx8,X			0	–	–	↕	↕	–	IX1	E8	ff	3
EOR ,X			0	–	–	↕	↕	–	IX	F8		3
EOR oprx16,SP			0	–	–	↕	↕	–	SP2	9ED8	ee ff	5
EOR oprx8,SP			0	–	–	↕	↕	–	SP1	9EE8	ff	4
INC opr8a	Increment	M ← (M) + 0x01	↕	–	–	↕	↕	–	DIR	3C	dd	5
INCA		A ← (A) + 0x01	↕	–	–	↕	↕	–	INH	4C		1
INCX		X ← (X) + 0x01	↕	–	–	↕	↕	–	INH	5C		1
INC oprx8,X		M ← (M) + 0x01	↕	–	–	↕	↕	–	IX1	6C	ff	5
INC ,X		M ← (M) + 0x01	↕	–	–	↕	↕	–	IX	7C		4
INC oprx8,SP		M ← (M) + 0x01	↕	–	–	↕	↕	–	SP1	9E6C	ff	6
JMP opr8a	Jump	PC ← Jump Address							DIR	BC	dd	3
JMP opr16a									EXT	CC	hh ll	4
JMP oprx16,X			–	–	–	–	–	–	IX2	DC	ee ff	4
JMP oprx8,X									IX1	EC	ff	3
JMP ,X									IX	FC		3
JSR opr8a	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL) SP ← (SP) – 0x0001 Push (PCH) SP ← (SP) – 0x0001 PC ← Unconditional Address	–	–	–	–	–	–	DIR	BD	dd	5
JSR opr16a			–	–	–	–	–	–	EXT	CD	hh ll	6
JSR oprx16,X			–	–	–	–	–	–	IX2	DD	ee ff	6
JSR oprx8,X			–	–	–	–	–	–	IX1	ED	ff	5
JSR ,X			–	–	–	–	–	–	IX	FD		5
LDA #opr8i	Load Accumulator from Memory	A ← (M)	0	–	–	↕	↕	–	IMM	A6	ii	2
LDA opr8a									DIR	B6	dd	3
LDA opr16a									EXT	C6	hh ll	4
LDA oprx16,X									IX2	D6	ee ff	4
LDA oprx8,X									IX1	E6	ff	3

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
LDA ,X									IX	F6		3
LDA oprx16,SP									SP2	9ED6	ee ff	5
LDA oprx8,SP									SP1	9EE6	ff	4
LDHX #opr16i	Load Index Register (H:X) from Memory	H:X ← (M:M + 0x0001)	0	–	–	↕	↕	–	IMM	45	jj kk	3
LDHX opr8a			0	–	–	↕	↕	–	DIR	55	dd	4
LDHX opr16a			0	–	–	↕	↕	–	EXT	32	hh ll	5
LDHX ,X			0	–	–	↕	↕	–	IX	9EAE		5
LDHX oprx16,X			0	–	–	↕	↕	–	IX2	9EBE	ee ff	6
LDHX oprx8,X			0	–	–	↕	↕	–	IX1	9ECE	ff	5
LDHX oprx8,SP			0	–	–	↕	↕	–	SP1	9EFE	ff	5
LDX #opr8i	Load X (Index Register Low) from Memory	X ← (M)	0	–	–	↕	↕	–	IMM	AE	ii	2
LDX opr8a			0	–	–	↕	↕	–	DIR	BE	dd	3
LDX opr16a			0	–	–	↕	↕	–	EXT	CE	hh ll	4
LDX oprx16,X			0	–	–	↕	↕	–	IX2	DE	ee ff	4
LDX oprx8,X			0	–	–	↕	↕	–	IX1	EE	ff	3
LDX ,X			0	–	–	↕	↕	–	IX	FE		3
LDX oprx16,SP			0	–	–	↕	↕	–	SP2	9EDE	ee ff	5
LDX oprx8,SP			0	–	–	↕	↕	–	SP1	9EEE	ff	4
LSL opr8a	Logical Shift Left (Same as ASL)	C ← MSB, LSB ← 0	↕	–	–	↕	↕	↕	DIR	38	dd	5
LSLA			↕	–	–	↕	↕	↕	INH	48		1
LSLX			↕	–	–	↕	↕	↕	INH	58		1
LSL oprx8,X			↕	–	–	↕	↕	↕	IX1	68	ff	5
LSL ,X			↕	–	–	↕	↕	↕	IX	78		4
LSL oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E68	ff	6
LSR opr8a	Logical Shift Right	0 → MSB, LSB → C	↕	–	–	0	↕	↕	DIR	34	dd	5
LSRA			↕	–	–	0	↕	↕	INH	44		1
LSRX			↕	–	–	0	↕	↕	INH	54		1
LSR oprx8,X			↕	–	–	0	↕	↕	IX1	64	ff	5
LSR ,X			↕	–	–	0	↕	↕	IX	74		4
LSR oprx8,SP			↕	–	–	0	↕	↕	SP1	9E64	ff	6
MOV oprx8,opr8a	Move	$(M)_{destination} \leftarrow (M)_{source}$	0	–	–	↕	↕	–	DIR/DIR	4E	dd	5
MOV opr8a,X+			0	–	–	↕	↕	–	DIR/IX+	5E	dd	5

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
MOV #opr8i,opr8a		H:X ← (H:X) + 0x0001 in IX+/DIR and DIR/IX+ Modes	0	–	–	↕	↕	–	IMM/DIR	6E	ii	4
MOV ,X+,opr8a			0	–	–	↕	↕	–	IX+/DIR	7E	dd	5
MUL	Unsigned multiply	X:A ← (X) × (A)	–	0	–	–	–	0	INH	42		5
NEG opr8a	Negate (Two's Complement)	M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	DIR	30	dd	5
NEGA		A ← – (A) = 0x00 – (A)	↕	–	–	↕	↕	↕	INH	40		1
NEGX		X ← – (X) = 0x00 – (X)	↕	–	–	↕	↕	↕	INH	50		1
NEG oprx8,X		M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	IX1	60	ff	5
NEG ,X		M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	IX	70		4
NEG oprx8,SP		M ← – (M) = 0x00 – (M)	↕	–	–	↕	↕	↕	SP1	9E60	ff	6
NOP	No Operation	Uses 1 Bus Cycle	–	–	–	–	–	–	INH	9D		1
NSA	Nibble Swap Accumulator	A ← (A[3:0]:A[7:4])	–	–	–	–	–	–	INH	62		1
ORA #opr8i	Inclusive OR Accumulator and Memory	A ← (A) | (M)	0	–	–	↕	↕	–	IMM	AA	ii	2
ORA opr8a			0	–	–	↕	↕	–	DIR	BA	dd	3
ORA opr16a			0	–	–	↕	↕	–	EXT	CA	hh ll	4
ORA oprx16,X			0	–	–	↕	↕	–	IX2	DA	ee ff	4
ORA oprx8,X			0	–	–	↕	↕	–	IX1	EA	ff	3
ORA ,X			0	–	–	↕	↕	–	IX	FA		3
ORA oprx16,SP			0	–	–	↕	↕	–	SP2	9EDA	ee ff	5
ORA oprx8,SP			0	–	–	↕	↕	–	SP1	9EEA	ff	4
PSHA	Push Accumulator onto Stack	Push (A); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	87		2
PSHH	Push H (Index Register High) onto Stack	Push (H); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	8B		2
PSHX	Push X (Index Register Low) onto Stack	Push (X); SP ← (SP) – 0x0001	–	–	–	–	–	–	INH	89		2
PULA	Pull Accumulator from Stack	SP ← (SP + 0x0001); Pull (A)	–	–	–	–	–	–	INH	86		3
PULH	Pull H (Index Register High) from Stack	SP ← (SP + 0x0001); Pull (H)	–	–	–	–	–	–	INH	8A		3
PULX	Pull X (Index Register Low) from Stack	SP ← (SP + 0x0001); Pull (X)	–	–	–	–	–	–	INH	88		3
ROL opr8a			↕	–	–	↕	↕	↕	DIR	39	dd	5
ROLA			↕	–	–	↕	↕	↕	INH	49		1

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
ROLX	Rotate Left through Carry	C ← MSB, LSB ← C	↕	–	–	↕	↕	↕	INH	59		1
ROL oprx8,X			↕	–	–	↕	↕	↕	IX1	69	ff	5
ROL ,X			↕	–	–	↕	↕	↕	IX	79		4
ROL oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E69	ff	6
ROR opr8a	Rotate Right through Carry	LSB → C, C → MSB	↕	–	–	↕	↕	↕	DIR	36	dd	5
RORA			↕	–	–	↕	↕	↕	INH	46		1
RORX			↕	–	–	↕	↕	↕	INH	56		1
ROR oprx8,X			↕	–	–	↕	↕	↕	IX1	66	ff	5
ROR ,X			↕	–	–	↕	↕	↕	IX	76		4
ROR oprx8,SP			↕	–	–	↕	↕	↕	SP1	9E66	ff	6
RSP	Reset Stack Pointer	SP ← 0xFF (High Byte Not Affected)	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 0x0001, Pull (CCR) SP ← (SP) + 0x0001, Pull (A) SP ← (SP) + 0x0001, Pull (X) SP ← (SP) + 0x0001, Pull (PCH) SP ← (SP) + 0x0001, Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← SP + 0x0001, Pull (PCH) SP ← SP + 0x0001, Pull (PCL)	–	–	–	–	–	–	INH	81		6
SBC #opr8i	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM	A2	ii	2
SBC opr8a			↕	–	–	↕	↕	↕	DIR	B2	dd	3
SBC opr16a			↕	–	–	↕	↕	↕	EXT	C2	hh ll	4
SBC oprx16,X			↕	–	–	↕	↕	↕	IX2	D2	ee ff	4
SBC oprx8,X			↕	–	–	↕	↕	↕	IX1	E2	ff	3
SBC ,X			↕	–	–	↕	↕	↕	IX	F2		3
SBC oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED2	ee ff	5
SBC oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE2	ff	4
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask Bit	I ← 1	–	–	1	–	–	–	INH	9B		1

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
STA opr8a	Store Accumulator in Memory	M ← (A)	0	–	–	↕	↕	–	DIR	B7	dd	3
STA opr16a			0	–	–	↕	↕	–	EXT	C7	hh ll	4
STA oprx16,X			0	–	–	↕	↕	–	IX2	D7	ee ff	4
STA oprx8,X			0	–	–	↕	↕	–	IX1	E7	ff	3
STA ,X			0	–	–	↕	↕	–	IX	F7		2
STA oprx16,SP			0	–	–	↕	↕	–	SP2	9ED7	ee ff	5
STA oprx8,SP			0	–	–	↕	↕	–	SP1	9EE7	ff	4
STHX opr8a	Store H:X (Index Reg.)	(M:M + 0x0001) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STHX opr16a			0	–	–	↕	↕	–	EXT	96	hh ll	5
STHX oprx8,SP			0	–	–	↕	↕	–	SP1	9EFF	ff	5
STOP	Enable Interrupts: Stop Processing. Refer to MCU Documentation.	I bit ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		3+
STX opr8a	Store X (Low 8 Bits of Index Register) in Memory	M ← (X)	0	–	–	↕	↕	–	DIR	BF	dd	3
STX opr16a			0	–	–	↕	↕	–	EXT	CF	hh ll	4
STX oprx16,X			0	–	–	↕	↕	–	IX2	DF	ee ff	4
STX oprx8,X			0	–	–	↕	↕	–	IX1	EF	ff	3
STX ,X			0	–	–	↕	↕	–	IX	FF		2
STX oprx16,SP			0	–	–	↕	↕	–	SP2	9EDF	ee ff	5
STX oprx8,SP			0	–	–	↕	↕	–	SP1	9EEF	ff	4
SUB #opr8i	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM	A0	ii	2
SUB opr8a			↕	–	–	↕	↕	↕	DIR	B0	dd	3
SUB opr16a			↕	–	–	↕	↕	↕	EXT	C0	hh ll	4
SUB oprx16,X			↕	–	–	↕	↕	↕	IX2	D0	ee ff	4
SUB oprx8,X			↕	–	–	↕	↕	↕	IX1	E0	ff	3
SUB ,X			↕	–	–	↕	↕	↕	IX	F0		3
SUB oprx16,SP			↕	–	–	↕	↕	↕	SP2	9ED0	ee ff	5
SUB oprx8,SP			↕	–	–	↕	↕	↕	SP1	9EE0	ff	4
		PC ← (PC) + 0x0001 Push (PCL) SP ← (SP) – 0x0001 Push (PCH) SP ← (SP) – 0x0001, Push (X) SP ← (SP) – 0x0001 Push (A)										

Table continues on the next page...

Table 10-3. Instruction Set Summary (continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles
			V	H	I	N	Z	C				
SWI	Software Interrupt	SP ← (SP) – 0x0001 Push (CCR) SP ← (SP) – 0x0001 I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	–	–	1	–	–	–	INH	83		11
TAP	Transfer Accumulator to CCR	CCR ← (A)	↕	↕	↕	↕	↕	↕	INH	84		1
TAX	Transfer Accumulator to X (Index Register Low)	X ← (A)	–	–	–	–	–	–	INH	97		1
TPA	Transfer CCR to Accumulator	A ← (CCR)	–	–	–	–	–	–	INH	85		1
TST opr8a	Test for Negative or Zero	(M) – 0x00	0	–	–	↕	↕	–	DIR	3D	dd	4
TSTA		(A) – 0x00	0	–	–	↕	↕	–	INH	4D		1
TSTX		(X) – 0x00	0	–	–	↕	↕	–	INH	5D		1
TST oprx8,X		(M) – 0x00	0	–	–	↕	↕	–	IX1	6D	ff	4
TST ,X		(M) – 0x00	0	–	–	↕	↕	–	IX	7D		3
TST oprx8,SP		(M) – 0x00	0	–	–	↕	↕	–	SP1	9E6D	ff	5
TSX	Transfer SP to Index Register	H:X ← (SP) + 0x0001	–	–	–	–	–	–	INH	95		2
TXA	Transfer X (Index Reg. Low) to Accumulator	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer Index Register to SP	SP ← (H:X) – 0x0001	–	–	–	–	–	–	INH	94		2
WAIT	Enable Interrupts Wait for Interrupt	I bit ← 0, Halt CPU	–	–	0	–	–	–	INH	8F		3+

Chapter 11
Keyboard Interrupts (KBI)

11.1 Introduction

11.1.1 Features

The KBI features include:

- Up to eight keyboard interrupt pins with individual pin enable bits
- Each keyboard interrupt pin is programmable as:
  - falling-edge sensitivity only
  - rising-edge sensitivity only
  - both falling-edge and low-level sensitivity
  - both rising-edge and high-level sensitivity
- One software-enabled keyboard interrupt
- Exit from low-power modes

11.1.2 Modes of Operation

This section defines the KBI operation in:

- Wait mode
- Stop mode
- Background debug mode

11.1.2.1 KBI in Wait mode

Executing the Wait instruction places the MCU into Wait mode. The KBI interrupt should be enabled (KBI_SC[KBIE] = 1), if desired, before executing the Wait instruction, allowing the KBI to continue to operate while the MCU is in Wait mode. An enabled KBI pin (KBI_PE[KBIPEn] = 1) can be used to bring the MCU out of Wait mode if the KBI interrupt is enabled (KBI_SC[KBIE] = 1).

11.1.2.2 KBI in Stop modes

Executing the Stop instruction places the MCU into Stop3 mode (when Stop3 is selected), where the KBI can operate asynchronously. If this is the desired behavior, the KBI interrupt must be enabled (KBI_SC[KBIE] = 1) before executing the Stop instruction, allowing the KBI to continue to operate while the MCU is in Stop3 mode. An enabled KBI pin (KBI_PE[KBIPEn] = 1) can be used to bring the MCU out of Stop3 mode if the KBI interrupt is enabled (KBI_SC[KBIE] = 1).

11.1.2.3 KBI in Active Background mode

When the MCU is in Active Background mode, the KBI will continue to operate normally.

11.1.3 Block Diagram

The block diagram for the keyboard interrupt module is shown below..

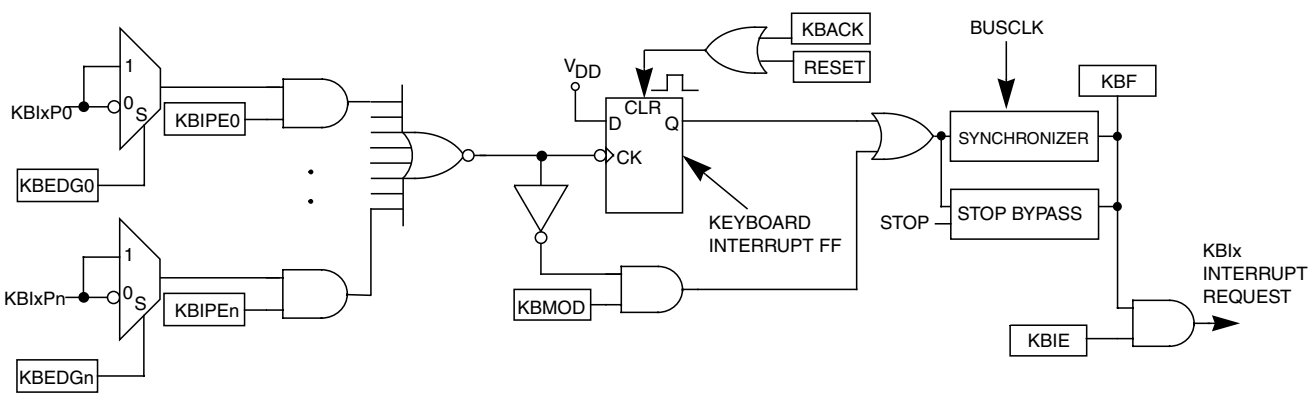


Figure 11-1. KBI block diagram

11.2 External signals description

The KBI input pins can be used to detect either falling edges, or both falling edge and low-level interrupt requests. The KBI input pins can also be used to detect either rising edges, or both rising edge and high-level interrupt requests.

The signal properties of KBI are shown in the following table:

Table 11-1. External signals description

Signal	Function	I/O
KBIxPn	Keyboard interrupt pins	I

11.3 Register definition

The KBI includes following registers:

- A pin status and control register, KBIx_SC
- A pin enable register, KBIx_PE
- An edge select register, KBIx_ES

See the direct-page register summary in the Memory chapter for the absolute address assignments for all KBIx registers. This section refers to registers and control bits only by their names.

Some MCUs may have more than one KBI, so register names include placeholder characters to identify which KBI is being referenced.

11.4 Memory Map and Registers

KBI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3C	KBI Status and Control Register (KBI0_SC)	8	R/W	00h	11.4.1/290
307C	KBI Pin Enable Register (KBI0_PE)	8	R/W	00h	11.4.2/291
307D	KBI Edge Select Register (KBI0_ES)	8	R/W	00h	11.4.3/291
3D	KBI Status and Control Register (KBI1_SC)	8	R/W	00h	11.4.1/290
307E	KBI Pin Enable Register (KBI1_PE)	8	R/W	00h	11.4.2/291
307F	KBI Edge Select Register (KBI1_ES)	8	R/W	00h	11.4.3/291

11.4.1 KBI Status and Control Register (KBIx_SC)

KBIx_SC contains the status flag and control bits, which are used to configure the KBI.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	0				KBF		KBIE	KBMOD
Write						KBACK		
Reset	0	0	0	0	0	0	0	0

KBIx_SC field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 KBF	KBI Interrupt Flag KBF indicates when a KBIx interrupt request is detected. Writes have no effect on KBF. 0 KBI interrupt request not detected. 1 KBI interrupt request detected.
2 KBACK	KBI Acknowledge Writing a 1 to KBACK is part of the flag clearing mechanism.
1 KBIE	KBI Interrupt Enable KBIE determines whether a KBI interrupt is enabled or not. 0 KBI interrupt not enabled. 1 KBI interrupt enabled.
0 KBMOD	KBI Detection Mode KBMOD (along with the KBEDG bits) controls the detection mode of the KBI interrupt pins. 0 Keyboard detects edges only. 1 Keyboard detects both edges and levels.

11.4.2 KBI Pin Enable Register (KBIx_PE)

KBIx_PE contains the pin enable control bits.

Address: Base address + 3040h offset

Bit	7	6	5	4	3	2	1	0
Read Write	KBIPE							
Reset	0	0	0	0	0	0	0	0

KBIx_PE field descriptions

Field	Description
KBIPE	KBI Pin Enables Each of the KBIPEn bits enable the corresponding KBI interrupt pin. 0 Pin is not enabled as KBI interrupt. 1 Pin is enabled as KBI interrupt.

11.4.3 KBI Edge Select Register (KBIx_ES)

KBIx_ES contains the edge select control bits.

Address: Base address + 3041h offset

Bit	7	6	5	4	3	2	1	0
Read Write	KBEDG							
Reset	0	0	0	0	0	0	0	0

KBIx_ES field descriptions

Field	Description
KBEDG	KBI Edge Selects Each of the KBEDGn bits selects the falling edge/low-level or rising edge/high-level function of the corresponding pin. 0 Falling edge/low level. 1 Rising edge/high level.

11.5 Functional Description

This on-chip peripheral module is called a keyboard interrupt module because originally it was designed to simplify the connection and use of row-column matrices of keyboard switches. However, these inputs are also useful as extra external interrupt inputs and as an external means of waking the MCU from stop or wait low-power modes.

The KBI module allows up to eight pins to act as additional interrupt sources. Writing to the KBIx_PE[KBIPEn] bits independently enables or disables each KBI pin. Each KBI pin can be configured as edge sensitive or edge and level sensitive based on the KBIx_SC[KBMOD] bit. Edge sensitive can be software programmed to be either falling or rising; the level can be either low or high. The polarity of the edge or edge and level sensitivity is selected using the KBIx_ES[KBEDGn] bits.

11.5.1 Edge-only sensitivity

Synchronous logic is used to detect edges. A falling edge is detected when an enabled keyboard interrupt (KBIx_PE[KBIPEn]=1) input signal is seen as a logic 1 (the deasserted level) during one bus cycle and then a logic 0 (the asserted level) during the next cycle. A rising edge is detected when the input signal is seen as a logic 0 (the deasserted level) during one bus cycle and then a logic 1 (the asserted level) during the next cycle.

Before the first edge is detected, all enabled keyboard interrupt input signals must be at the deasserted logic levels. After any edge is detected, all enabled keyboard interrupt input signals must return to the deasserted level before any new edge can be detected.

A valid edge on an enabled KBI pin will set KBIx_SC[KBF]. If KBIx_SC[KBIE] is set, an interrupt request will be presented to the MPU. Clearing of KBIx_SC[KBF] is accomplished by writing a 1 to KBIx_SC[KBACK].

11.5.2 Edge and level sensitivity

A valid edge or level on an enabled KBI pin will set KBIx_SC[KBF]. If KBIx_SC[KBIE] is set, an interrupt request will be presented to the MCU. Clearing of KBIx_SC[KBF] is accomplished by writing a 1 to KBIx_SC[KBACK], provided all enabled keyboard inputs are at their deasserted levels. KBIx_SC[KBF] will remain set if any enabled KBI pin is asserted while attempting to clear KBIx_SC[KBF] by writing a 1 to KBIx_SC[KBACK].

11.5.3 KBI Pullup Resistor

Each KBI pin, if enabled by KBIx_PE, can be configured via the associated I/O port pull enable register, see chapter, to use:

- an internal pullup resistor, or
- no resistor

If an internal pullup resistor is enabled for an enabled KBI pin, the associated I/O port pull select register (see I/O Port chapter) can be used to select an internal pullup resistor.

11.5.4 KBI initialization

When a keyboard interrupt pin is first enabled, it is possible to get a false keyboard interrupt flag. To prevent a false interrupt request during keyboard initialization, the user should do the following:

1. Mask keyboard interrupts by clearing KBIx_SC[KBIE].
2. Enable the KBI polarity by setting the appropriate KBIx_ES[KBEDGn] bits.
3. Before using internal pullup resistors, configure the associated bits in PORT_.
4. Enable the KBI pins by setting the appropriate KBIx_PE[KBIPEn] bits.
5. Write to KBIx_SC[KBACK] to clear any false interrupts.
6. Set KBIx_SC[KBIE] to enable interrupts.

Chapter 12
FlexTimer Module (FTM)

12.1 Introduction

NOTE

For the chip-specific implementation details of this module's instances, see the chip configuration information.

The FlexTimer module is a two to eight channel timer which supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

12.1.1 FlexTimer philosophy

The FlexTimer is built upon a very simple timer used for many years on NXP's 8-bit microcontrollers, the HCS08 Timer PWM Module – TPM. The FlexTimer extends the functionality to meet the demands of motor control, digital lighting solutions, and power conversion, while providing low cost and backwards compatibility with the TPM module.

Several key enhancements are made: signed up-counter, dead time insertion hardware, fault control inputs, enhanced triggering functionality and initialization, and polarity control.

All of the features common with the TPM module have fully backwards compatible register assignments and the FlexTimer can use code on the same core platform without change to perform the same functions. A small exception to this is when the FlexTimer clock frequency is twice bus clock frequency to provide extra resolution for high speed PWM applications.

Motor control and power conversion features have been added through a dedicated set of registers. The new features, such as hardware dead time insertion, polarity, fault control, and masking, greatly reduce loading on the execution software and are usually each controlled by a group of registers. All of the new features are disabled after reset by default.

Flextimer input triggers can come directly from other modules integrated on the chip, such as comparators or ADCs, to automatically initiate timer functions. These triggers can be linked in a variety of ways during integration of the modules so please note carefully the options available for used FlexTimer configuration.

All main user access registers are buffered to ease the load on the executing software. A number of trigger options exist to determine which registers are updated with this user defined data.

12.1.2 Features

The FTM features include:

- Selectable FTM source clock:
  - Source clock can be the system clock, the fixed frequency clock, or an external clock
  - Fixed frequency clock is an additional clock input to allow the selection of an on chip clock source other than the system clock
  - Selecting external clock connects FTM clock to a chip level input pin therefore allowing to synchronize the FTM counter with an off chip clock source
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- FTM has a 16-bit counter
  - It can be a free-running counter or a counter with initial and final value
  - The counting can be up or up-down
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode
- In input capture mode:
  - The capture can occur on rising edges, falling edges or both edges
  - An input filter can be selected for some channels

- In output compare mode the output signal can be set, cleared, or toggled on match
- All channels can be configured for center-aligned PWM mode
- Each pair of channels can be combined to generate a PWM signal with independent control of both edges of PWM signal
- The FTM channels can operate as pairs with equal outputs, pairs with complementary outputs, or independent channels with independent outputs
- The deadtime insertion is available for each complementary pair
- Generation of triggers (match trigger)
- Software control of PWM outputs
- Up to four fault inputs for global fault control
- The polarity of each channel is configurable
- The generation of an interrupt per channel
- The generation of an interrupt when the counter overflows
- The generation of an interrupt when the fault condition is detected
- Synchronized loading of write buffered FTM registers
- Write protection for critical registers
- Backwards compatible with TPM
- Testing of input captures for a stuck at zero and one conditions
- Dual edge capture for pulse and period width measurement

12.1.3 Modes of operation

When the MCU is in active BDM background or BDM foreground mode, the FTM temporarily suspends all counting until the MCU returns to normal user operating mode. During stop mode, all FTM input clocks are stopped, so the FTM is effectively disabled until clocks resume. During wait mode, the FTM continues to operate normally. If the FTM does not need to produce a real time reference or provide the interrupt sources needed to wake the MCU from wait mode, the power can then be saved by disabling FTM functions before entering wait mode.

12.1.4 Block diagram

The FTM uses one input/output (I/O) pin per channel, CHn (FTM channel (n)) where n is the channel number (0–7).

The following figure shows the FTM structure. The central component of the FTM is the 16-bit counter with programmable initial and final values and its counting can be up or up-down.

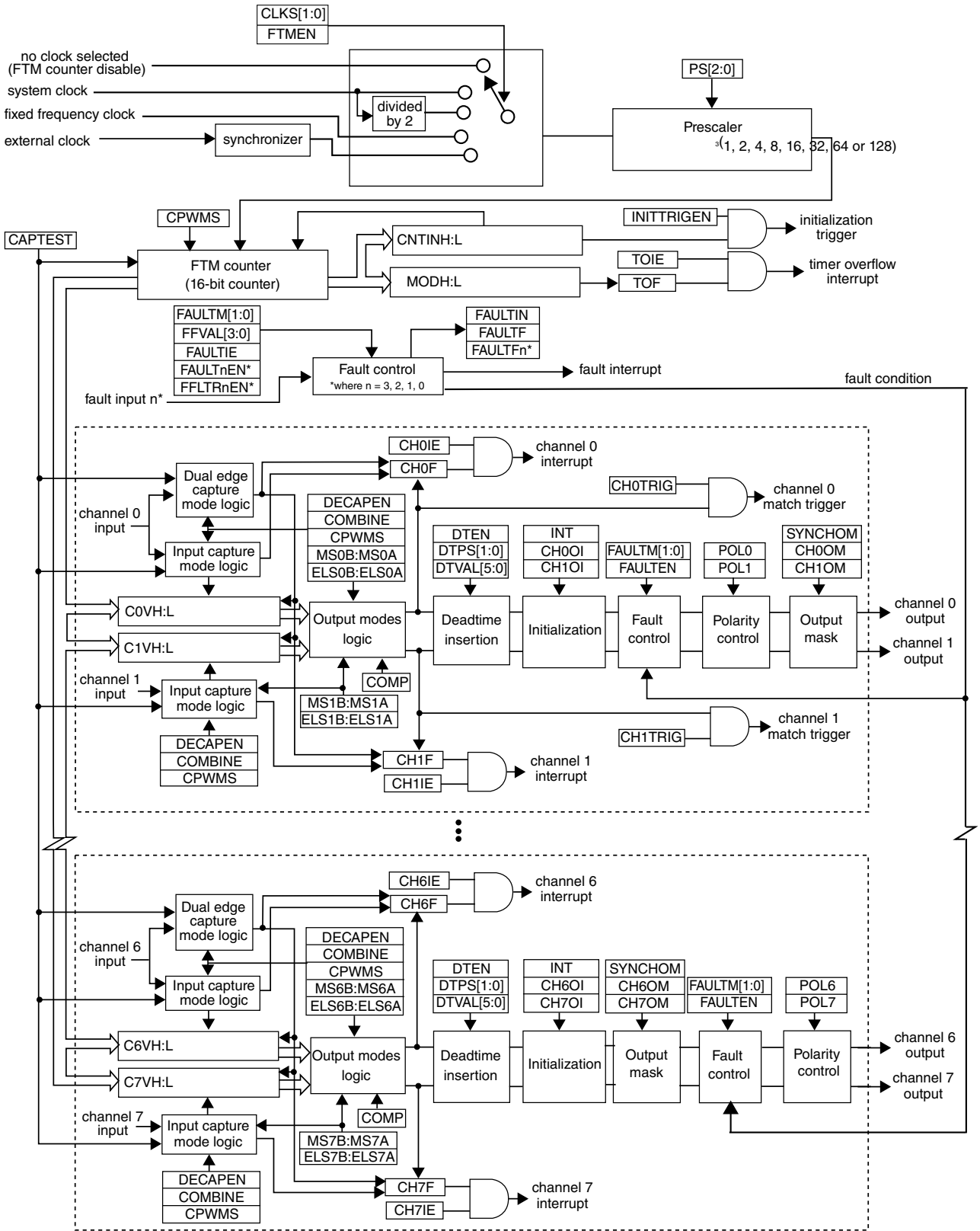


Figure 12-1. FTM block diagram

12.2 Signal description

The following table shows the user-accessible signals for the FTM.

Table 12-1. Signal properties

Name	Function
EXTCLK	External clock – FTM external clock can be selected to drive the FTM counter.
CHn[1]	Channel (n) – I/O pin associated with FTM channel (n).
FAULTj[2]	Fault input (j) – input pin associated with fault input (j).

1. n = channel number (0 to 7)
2. j = fault input (0 to 3)

12.2.1 EXTCLK — FTM external clock

The external clock input signal is used as the FTM counter clock if selected by CLKS[1:0] bits in the SC register. This clock signal must not exceed 1/4 of system clock frequency. The FTM counter prescaler selection and settings are also used when an external clock is selected.

12.2.2 CHn — FTM channel (n) I/O pin

Each FTM channel can be configured to operate either as input or output. The direction associated with each channel, input or output, is selected according to the mode assigned for that channel.

12.2.3 FAULTj — FTM fault input

The fault input signals are used to control the CHn channel output state. If a fault is detected, the FAULTj signal is asserted and the channel output is put in a safe state. The behavior of the fault logic is defined by the FAULTM[1:0] control bits in the MODE register and FAULTEN bit in the COMBINEm register. Note that each FAULTj input may affect all channels selectively since FAULTM[1:0] and FAULTEN control bits are defined for each pair of channels. Each FAULTj input is activated by its corresponding FAULTjEN bit in the FLTCTRL register.

12.3 Memory map and register definition

This section provides a detailed description of all FTM registers.

12.3.1 Module memory map

This section presents a high-level summary of the FTM registers and how they are mapped.

The FTM memory map can be split into two sets of registers. The first set has the original TPM registers.

Starting with Counter Initial Value High (CNTINH), the second set has the FTM specific registers. Any second set registers, or bits within these registers, that are used by an unavailable function in the FTM configuration remain in the memory map and in the reset value even though they have no active function.

Note

Do not write to the FTM specific registers (second set registers) when FTMEN = 0.

12.3.2 Register descriptions

This section consists of register descriptions in address order.

NOTE

Not all the registers in the following memory map are available for this device, see FTM registers for details.

FTM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
20	Status and Control (FTM0_SC)	8	R/W	00h	12.3.3/305
21	Counter High (FTM0_CNTH)	8	R/W	00h	12.3.4/306
22	Counter Low (FTM0_CNTL)	8	R/W	00h	12.3.5/307
23	Modulo High (FTM0_MODH)	8	R/W	00h	12.3.6/307
24	Modulo Low (FTM0_MODL)	8	R/W	00h	12.3.7/308
25	Channel Status and Control (FTM0_C0SC)	8	R/W	00h	12.3.8/308

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
26	Channel Value High (FTM0_C0VH)	8	R/W	00h	12.3.9/311
27	Channel Value Low (FTM0_C0VL)	8	R/W	00h	12.3.10/312
28	Channel Status and Control (FTM0_C1SC)	8	R/W	00h	12.3.8/308
29	Channel Value High (FTM0_C1VH)	8	R/W	00h	12.3.9/311
2A	Channel Value Low (FTM0_C1VL)	8	R/W	00h	12.3.10/312
2B	Channel Status and Control (FTM0_C2SC)	8	R/W	00h	12.3.8/308
2C	Channel Value High (FTM0_C2VH)	8	R/W	00h	12.3.9/311
2D	Channel Value Low (FTM0_C2VL)	8	R/W	00h	12.3.10/312
2E	Channel Status and Control (FTM0_C3SC)	8	R/W	00h	12.3.8/308
2F	Channel Value High (FTM0_C3VH)	8	R/W	00h	12.3.9/311
30	Channel Value Low (FTM0_C3VL)	8	R/W	00h	12.3.10/312
31	Channel Status and Control (FTM0_C4SC)	8	R/W	00h	12.3.8/308
32	Channel Value High (FTM0_C4VH)	8	R/W	00h	12.3.9/311
33	Channel Value Low (FTM0_C4VL)	8	R/W	00h	12.3.10/312
34	Channel Status and Control (FTM0_C5SC)	8	R/W	00h	12.3.8/308
35	Channel Value High (FTM0_C5VH)	8	R/W	00h	12.3.9/311
36	Channel Value Low (FTM0_C5VL)	8	R/W	00h	12.3.10/312
37	Counter Initial Value High (FTM0_CNTINH)	8	R/W	00h	12.3.11/312
38	Counter Initial Value Low (FTM0_CNTINL)	8	R/W	00h	12.3.12/313
39	Capture and Compare Status (FTM0_STATUS)	8	R/W	00h	12.3.13/313
3A	Features Mode Selection (FTM0_MODE)	8	R/W	04h	12.3.14/315
3B	Synchronization (FTM0_SYNC)	8	R/W	00h	12.3.15/316
3C	Initial State for Channel Output (FTM0_OUTINIT)	8	R/W	00h	12.3.16/318
3D	Output Mask (FTM0_OUTMASK)	8	R/W	00h	12.3.17/320
3E	Function for Linked Channels (FTM0_COMBINE0)	8	R/W	00h	12.3.18/321
3F	Function for Linked Channels (FTM0_COMBINE1)	8	R/W	00h	12.3.18/321
40	Function for Linked Channels (FTM0_COMBINE2)	8	R/W	00h	12.3.18/321
42	Deadtime Insertion Control (FTM0_DEADTIME)	8	R/W	00h	12.3.19/323
43	External Trigger (FTM0_EXTTRIG)	8	R/W	00h	12.3.20/324
44	Channels Polarity (FTM0_POL)	8	R/W	00h	12.3.21/325
45	Fault Mode Status (FTM0_FMS)	8	R/W	00h	12.3.22/327
46	Input Capture Filter Control (FTM0_FILTER0)	8	R/W	00h	12.3.23/328
47	Input Capture Filter Control (FTM0_FILTER1)	8	R/W	00h	12.3.23/328
48	Fault Input Filter Control (FTM0_FLTFILTER)	8	R/W	00h	12.3.24/329
49	Fault Input Control (FTM0_FLTCTRL)	8	R/W	00h	12.3.25/330
30	Status and Control (FTM1_SC)	8	R/W	00h	12.3.3/305
31	Counter High (FTM1_CNTH)	8	R/W	00h	12.3.4/306
32	Counter Low (FTM1_CNTL)	8	R/W	00h	12.3.5/307

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
33	Modulo High (FTM1_MODH)	8	R/W	00h	12.3.6/307
34	Modulo Low (FTM1_MODL)	8	R/W	00h	12.3.7/308
35	Channel Status and Control (FTM1_C0SC)	8	R/W	00h	12.3.8/308
36	Channel Value High (FTM1_C0VH)	8	R/W	00h	12.3.9/311
37	Channel Value Low (FTM1_C0VL)	8	R/W	00h	12.3.10/312
38	Channel Status and Control (FTM1_C1SC)	8	R/W	00h	12.3.8/308
39	Channel Value High (FTM1_C1VH)	8	R/W	00h	12.3.9/311
3A	Channel Value Low (FTM1_C1VL)	8	R/W	00h	12.3.10/312
3B	Channel Status and Control (FTM1_C2SC)	8	R/W	00h	12.3.8/308
3C	Channel Value High (FTM1_C2VH)	8	R/W	00h	12.3.9/311
3D	Channel Value Low (FTM1_C2VL)	8	R/W	00h	12.3.10/312
3E	Channel Status and Control (FTM1_C3SC)	8	R/W	00h	12.3.8/308
3F	Channel Value High (FTM1_C3VH)	8	R/W	00h	12.3.9/311
40	Channel Value Low (FTM1_C3VL)	8	R/W	00h	12.3.10/312
41	Channel Status and Control (FTM1_C4SC)	8	R/W	00h	12.3.8/308
42	Channel Value High (FTM1_C4VH)	8	R/W	00h	12.3.9/311
43	Channel Value Low (FTM1_C4VL)	8	R/W	00h	12.3.10/312
44	Channel Status and Control (FTM1_C5SC)	8	R/W	00h	12.3.8/308
45	Channel Value High (FTM1_C5VH)	8	R/W	00h	12.3.9/311
46	Channel Value Low (FTM1_C5VL)	8	R/W	00h	12.3.10/312
47	Counter Initial Value High (FTM1_CNTINH)	8	R/W	00h	12.3.11/312
48	Counter Initial Value Low (FTM1_CNTINL)	8	R/W	00h	12.3.12/313
49	Capture and Compare Status (FTM1_STATUS)	8	R/W	00h	12.3.13/313
4A	Features Mode Selection (FTM1_MODE)	8	R/W	04h	12.3.14/315
4B	Synchronization (FTM1_SYNC)	8	R/W	00h	12.3.15/316
4C	Initial State for Channel Output (FTM1_OUTINIT)	8	R/W	00h	12.3.16/318
4D	Output Mask (FTM1_OUTMASK)	8	R/W	00h	12.3.17/320
4E	Function for Linked Channels (FTM1_COMBINE0)	8	R/W	00h	12.3.18/321
4F	Function for Linked Channels (FTM1_COMBINE1)	8	R/W	00h	12.3.18/321
50	Function for Linked Channels (FTM1_COMBINE2)	8	R/W	00h	12.3.18/321
52	Deadtime Insertion Control (FTM1_DEADTIME)	8	R/W	00h	12.3.19/323
53	External Trigger (FTM1_EXTTRIG)	8	R/W	00h	12.3.20/324
54	Channels Polarity (FTM1_POL)	8	R/W	00h	12.3.21/325
55	Fault Mode Status (FTM1_FMS)	8	R/W	00h	12.3.22/327
56	Input Capture Filter Control (FTM1_FILTER0)	8	R/W	00h	12.3.23/328
57	Input Capture Filter Control (FTM1_FILTER1)	8	R/W	00h	12.3.23/328
58	Fault Input Filter Control (FTM1_FLTFILTER)	8	R/W	00h	12.3.24/329
59	Fault Input Control (FTM1_FLTCTRL)	8	R/W	00h	12.3.25/330

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
30C0	Status and Control (FTM2_SC)	8	R/W	00h	12.3.3/305
30C1	Counter High (FTM2_CNTH)	8	R/W	00h	12.3.4/306
30C2	Counter Low (FTM2_CNTL)	8	R/W	00h	12.3.5/307
30C3	Modulo High (FTM2_MODH)	8	R/W	00h	12.3.6/307
30C4	Modulo Low (FTM2_MODL)	8	R/W	00h	12.3.7/308
30C5	Channel Status and Control (FTM2_C0SC)	8	R/W	00h	12.3.8/308
30C6	Channel Value High (FTM2_C0VH)	8	R/W	00h	12.3.9/311
30C7	Channel Value Low (FTM2_C0VL)	8	R/W	00h	12.3.10/312
30C8	Channel Status and Control (FTM2_C1SC)	8	R/W	00h	12.3.8/308
30C9	Channel Value High (FTM2_C1VH)	8	R/W	00h	12.3.9/311
30CA	Channel Value Low (FTM2_C1VL)	8	R/W	00h	12.3.10/312
30CB	Channel Status and Control (FTM2_C2SC)	8	R/W	00h	12.3.8/308
30CC	Channel Value High (FTM2_C2VH)	8	R/W	00h	12.3.9/311
30CD	Channel Value Low (FTM2_C2VL)	8	R/W	00h	12.3.10/312
30CE	Channel Status and Control (FTM2_C3SC)	8	R/W	00h	12.3.8/308
30CF	Channel Value High (FTM2_C3VH)	8	R/W	00h	12.3.9/311
30D0	Channel Value Low (FTM2_C3VL)	8	R/W	00h	12.3.10/312
30D1	Channel Status and Control (FTM2_C4SC)	8	R/W	00h	12.3.8/308
30D2	Channel Value High (FTM2_C4VH)	8	R/W	00h	12.3.9/311
30D3	Channel Value Low (FTM2_C4VL)	8	R/W	00h	12.3.10/312
30D4	Channel Status and Control (FTM2_C5SC)	8	R/W	00h	12.3.8/308
30D5	Channel Value High (FTM2_C5VH)	8	R/W	00h	12.3.9/311
30D6	Channel Value Low (FTM2_C5VL)	8	R/W	00h	12.3.10/312
30D7	Counter Initial Value High (FTM2_CNTINH)	8	R/W	00h	12.3.11/312
30D8	Counter Initial Value Low (FTM2_CNTINL)	8	R/W	00h	12.3.12/313
30D9	Capture and Compare Status (FTM2_STATUS)	8	R/W	00h	12.3.13/313
30DA	Features Mode Selection (FTM2_MODE)	8	R/W	04h	12.3.14/315
30DB	Synchronization (FTM2_SYNC)	8	R/W	00h	12.3.15/316
30DC	Initial State for Channel Output (FTM2_OUTINIT)	8	R/W	00h	12.3.16/318
30DD	Output Mask (FTM2_OUTMASK)	8	R/W	00h	12.3.17/320
30DE	Function for Linked Channels (FTM2_COMBINE0)	8	R/W	00h	12.3.18/321
30DF	Function for Linked Channels (FTM2_COMBINE1)	8	R/W	00h	12.3.18/321
30E0	Function for Linked Channels (FTM2_COMBINE2)	8	R/W	00h	12.3.18/321
30E2	Deadtime Insertion Control (FTM2_DEADTIME)	8	R/W	00h	12.3.19/323
30E3	External Trigger (FTM2_EXTTRIG)	8	R/W	00h	12.3.20/324
30E4	Channels Polarity (FTM2_POL)	8	R/W	00h	12.3.21/325
30E5	Fault Mode Status (FTM2_FMS)	8	R/W	00h	12.3.22/327
30E6	Input Capture Filter Control (FTM2_FILTER0)	8	R/W	00h	12.3.23/328

Table continues on the next page...

FTM memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
30E7	Input Capture Filter Control (FTM2_FILTER1)	8	R/W	00h	12.3.23/328
30E8	Fault Input Filter Control (FTM2_FLTFILTER)	8	R/W	00h	12.3.24/329
30E9	Fault Input Control (FTM2_FLTCTRL)	8	R/W	00h	12.3.25/330

12.3.3 Status and Control (FTMx_SC)

SC contains the overflow status flag and control bits used to configure the interrupt enable, FTM configuration, clock source, and prescaler factor. These controls relate to all channels within this module.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	TOF	TOIE	CPWMS	CLKS		PS		
Write	0							
Reset	0	0	0	0	0	0	0	0

FTMx_SC field descriptions

Field	Description
7 TOF	Timer Overflow Flag Set by hardware when the FTM counter passes the value in the Counter Modulo registers. The TOF bit is cleared by reading the SC register while TOF is set and then writing a 0 to TOF bit. Writing a 1 to TOF has no effect. If another FTM overflow occurs between the read and write operations, the write operation has no effect; therefore, TOF remains set indicating an overflow has occurred. In this case a TOF interrupt request is not lost due to the clearing sequence for a previous TOF. 0 FTM counter has not overflowed. 1 FTM counter has overflowed.
6 TOIE	Timer Overflow Interrupt Enable Enables FTM overflow interrupts. 0 Disable TOF interrupts. Use software polling. 1 Enable TOF interrupts. An interrupt is generated when TOF equals one.
5 CPWMS	Center-aligned PWM Select Selects CPWM mode. This mode configures the FTM to operate in up-down counting mode. CPWMS is write protected. It can be written only when MODE[WPDIS] = 1. 0 FTM counter operates in up counting mode. 1 FTM counter operates in up-down counting mode.

Table continues on the next page...

FTMx_SC field descriptions (continued)

Field	Description
4–3 CLKS	Clock Source Selection Selects one of the three FTM counter clock sources. CLKS is write protected. It can be written only when MODE[WPDIS] = 1. 00 No clock selected (this in effect disables the FTM counter). 01 If MODE[FTMEN] = 0, the System clock divided by 2 is selected for FTM2. If MODE[FTMEN] = 1, the System clock is selected for FTM2. System clock is selected for FTM0 and FTM1 10 Fixed frequency clock 11 External clock
PS	Prescale Factor Selection Selects one of 8 division factors for the clock source selected by CLKS. The new prescaler factor affects the clock source on the next system clock cycle after the new value is updated into the register bits. PS is write protected. It can be written only when MODE[WPDIS] = 1. 000 Divide by 1 001 Divide by 2 010 Divide by 4 011 Divide by 8 100 Divide by 16 101 Divide by 32 110 Divide by 64 111 Divide by 128

12.3.4 Counter High (FTMx_CNTH)

The Counter registers contain the high and low bytes of the counter value. Reading either byte latches the contents of both bytes into a buffer where they remain latched until the other half is read. This allows coherent 16-bit reads in either big-endian or little-endian order which makes this more friendly to various compiler implementations. The coherency mechanism is automatically restarted by an MCU reset or any write to the Status and Control register.

Writing any value to COUNT_H or COUNT_L updates the FTM counter with its initial 16-bit value (contained in the Counter Initial Value registers) and resets the read coherency mechanism, regardless of the data involved in the write.

When BDM is active, the FTM counter is frozen (this is the value that you may read); the read coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both counter bytes are read while BDM is active. This assures that if you were in the middle of reading a 16-bit register when BDM became active, it reads the appropriate value from the other half of the 16-bit value after returning to normal execution.

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read Write	COUNT_H							
Reset	0	0	0	0	0	0	0	0

FTMx_CNTH field descriptions

Field	Description
COUNT_H	Counter value high byte

12.3.5 Counter Low (FTMx_CNTL)

See the description for the Counter High register.

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read Write	COUNT_L							
Reset	0	0	0	0	0	0	0	0

FTMx_CNTL field descriptions

Field	Description
COUNT_L	Counter value low byte

12.3.6 Modulo High (FTMx_MODH)

The Modulo registers contain the high and low bytes of the modulo value for the FTM counter. After the FTM counter reaches the modulo value, the overflow flag (TOF) becomes set at the next clock, and the next value of FTM counter depends on the selected counting method (Counter).

Writing to either byte latches the value into a buffer. The register is updated with the value of their write buffer according to Update of the registers with write buffers.

If MODE[FTMEN] = 0, this write coherency mechanism may be manually reset by writing to the SC register whether BDM is active or not.

When BDM is active, this write coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both bytes of the modulo register are written while BDM is active. Any write to the modulo register bypasses the buffer latches and directly writes to the modulo register while BDM is active.

It is recommended to initialize the FTM counter, by writing to CNTH or CNTL, before writing to the FTM modulo register to avoid confusion about when the first counter overflow will occur.

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MOD_H							
Reset	0	0	0	0	0	0	0	0

FTMx_MODH field descriptions

Field	Description
MOD_H	High byte of the modulo value

12.3.7 Modulo Low (FTMx_MODL)

See the description for the Modulo High register.

Address: Base address + 4h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MOD_L							
Reset	0	0	0	0	0	0	0	0

FTMx_MODL field descriptions

Field	Description
MOD_L	Low byte of the modulo value

12.3.8 Channel Status and Control (FTMx_C*n*SC)

CnSC contains the channel-interrupt-status flag and control bits used to configure the interrupt enable, channel configuration, and pin function.

Table 12-2. Mode, edge, and level selection

DECAPEN	COMBINE	CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	X	X	XX	00	None	Pin not used for FTM
0	0	0	00	01	Input capture	Capture on Rising Edge Only

Table continues on the next page...

Table 12-2. Mode, edge, and level selection (continued)

DECAPEN	COMBINE	CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
				10		Capture on Falling Edge Only
				11		Capture on Rising or Falling Edge
			01	01	Output compare	Toggle Output on match
				10		Clear Output on match
				11		Set Output on match
			1X	10	Edge-aligned PWM	High-true pulses (clear Output on match)
				X1		Low-true pulses (set Output on match)
		1	XX	10	Center-aligned PWM	High-true pulses (clear Output on match-up)
				X1		Low-true pulses (set Output on match-up)
	1	0	XX	10	Combine PWM	High-true pulses (set on channel (n) match, and clear on channel (n+1) match)
				X1		Low-true pulses (clear on channel (n) match, and set on channel (n +1) match)
1	0	0	X0	See the following table.	Dual Edge Capture Mode	One-shot capture mode
			X1			Continuous capture mode

Table 12-3. Dual edge capture mode — edge polarity selection

ELSnB	ELSnA	Channel Port Enable	Detected Edges
0	0	Disabled	No edge
0	1	Enabled	Rising edge
1	0	Enabled	Falling edge
1	1	Enabled	Rising and falling edges

Address: Base address + 5h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read	CHF	CHIE	MSB	MSA	ELSB	ELSA	0	0
Write	0							
Reset	0	0	0	0	0	0	0	0

FTMx_C*n*SC field descriptions

Field	Description
7 CHF	Channel Flag Set by hardware when an event occurs on the channel. CHF is cleared by reading the CnSC register while CHnF is set and then writing a 0 to the CHF bit. Writing a 1 to CHF has no effect. If another event occurs between the read and write operations, the write operation has no effect; therefore, CHF remains set indicating an event has occurred. In this case a CHF interrupt request is not lost due to the clearing sequence for a previous CHF. 0 No channel event has occurred. 1 A channel event has occurred.
6 CHIE	Channel Interrupt Enable Enables channel interrupts. 0 Disable channel interrupts. Use software polling. 1 Enable channel interrupts.
5 MSB	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See the table in the register description. MSB is write protected. It can be written only when MODE[WPDIS] = 1.
4 MSA	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See the table in the register description. MSA is write protected. It can be written only when MODE[WPDIS] = 1.
3 ELSB	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See the table in the register description. ELSB is write protected. It can be written only when MODE[WPDIS] = 1.
2 ELSA	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See the table in the register description. ELSA is write protected. It can be written only when MODE[WPDIS] = 1.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

12.3.9 Channel Value High (FTMx_C*n*VH)

These registers contain the captured FTM counter value of the input capture function or the match value for the output modes.

In input capture, capture test, and dual edge capture modes, reading a single byte in CnV latches the contents into a buffer where they remain latched until the other byte is read. This latching mechanism also resets, or becomes unlatched, when the CnSC register is written whether BDM mode is active or not. Any write to the channel registers is ignored during these input modes.

When BDM is active, the read coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both bytes of the channel value register are read while BDM is active. This ensures that if you were in the middle of reading a 16-bit register when BDM became active, it reads the appropriate value from the other half of the 16-bit value after returning to normal execution. Any read of the CnV registers in BDM mode bypasses the buffer latches and returns the value of these registers and not the value of their read buffer.

In output modes, writing to CnV latches the value into a buffer. The registers are updated with the value of their write buffer according to Update of the registers with write buffers.

If MODE[FTMEN] = 0, this write coherency mechanism may be manually reset by writing to the CnSC register whether BDM mode is active or not. This latching mechanism allows coherent 16-bit writes in either big-endian or little-endian order, which is friendly to various compiler implementations.

When BDM is active, the write coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active even if one or both bytes of the channel value register are written while BDM is active. Any write to the CnV registers bypasses the buffer latches and writes directly to the register while BDM is active. The values written to the channel value registers while BDM is active are used in output modes operation after normal execution resumes. Writes to the channel value registers while BDM is active do not interfere with the partial completion of a coherency sequence. After the write coherency mechanism has been fully exercised, the channel value registers are updated using the buffered values while BDM was not active.

Address: Base address + 6h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read Write	VAL_H							
Reset	0	0	0	0	0	0	0	0

FTMx_C*n*VH field descriptions

Field	Description
VAL_H	Channel Value High Byte Captured FTM counter value of the input capture function or the match value for the output modes

12.3.10 Channel Value Low (FTMx_C*n*VL)

See the description for the Channel Value High register.

Address: Base address + 7h offset + (3d × i), where i=0d to 5d

Bit	7	6	5	4	3	2	1	0
Read Write	VAL_L							
Reset	0	0	0	0	0	0	0	0

FTMx_C*n*VL field descriptions

Field	Description
VAL_L	Channel Value Low Byte Captured FTM counter value of the input capture function or the match value for the output modes

12.3.11 Counter Initial Value High (FTMx_CNTINH)

The Counter Initial Value registers contain the high and low bytes of the initial value for the FTM counter.

Writing to either byte latches the value into a buffer. The registers are updated with the value of their write buffer.

When BDM is active, the write coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both bytes of the counter initial value register are written while BDM is active. Any write to the counter initial value registers bypasses the buffer latches and writes directly to the counter initial value register while BDM is active.

The first time that the FTM clock is selected (first write to change the CLKS bits to a non-zero value), FTM counter starts with the value 0x0000. To avoid this behavior, before the first write to select the FTM clock, write the new value to the Counter Initial Value registers and then initialize the FTM counter by writing any value to CNT).

Address: Base address + 17h offset

Bit	7	6	5	4	3	2	1	0
Read Write	INIT_H							
Reset	0	0	0	0	0	0	0	0

FTMx_CNTINH field descriptions

Field	Description
INIT_H	Counter Initial Value High Byte

12.3.12 Counter Initial Value Low (FTMx_CNTINL)

See the description for the Counter Initial Value High register.

Address: Base address + 18h offset

Bit	7	6	5	4	3	2	1	0
Read Write	INIT_L							
Reset	0	0	0	0	0	0	0	0

FTMx_CNTINL field descriptions

Field	Description
INIT_L	Counter Initial Value Low Byte

12.3.13 Capture and Compare Status (FTMx_STATUS)

STATUS contains a copy of the status flag CHnF bit, in CnSC, for each FTM channel for software convenience.

Each CHnF bit in STATUS is a mirror of CHnF bit in CnSC. All CHnF bits can be checked using only one read of STATUS. All CHnF bits can be cleared by reading STATUS followed by writing 0x00 to STATUS.

Hardware sets the individual channel flags when an event occurs on the channel. CHF is cleared by reading STATUS while CHnF is set and then writing a 0 to the CHF bit. Writing a 1 to CHF has no effect.

If another event occurs between the read and write operations, the write operation has no effect; therefore, CHF remains set indicating an event has occurred. In this case, a CHF interrupt request is not lost due to the clearing sequence for a previous CHF.

NOTE

The use of STATUS register is available only when (MODE[FTMEN] = 1), (COMBINE = 1), and (CPWMS = 0). The use of this register with (MODE[FTMEN] = 0), (COMBINE = 0), or (CPWMS = 1) is not recommended and its results are not guaranteed.

Address: Base address + 19h offset

Bit	7	6	5	4	3	2	1	0
Read	CH7F	CH6F	CH5F	CH4F	CH3F	CH2F	CH1F	CH0F
Write	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

FTMx_STATUS field descriptions

Field	Description
7 CH7F	Channel 7 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
6 CH6F	Channel 6 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
5 CH5F	Channel 5 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
4 CH4F	Channel 4 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
3 CH3F	Channel 3 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
2 CH2F	Channel 2 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.

Table continues on the next page...

FTMx_STATUS field descriptions (continued)

Field	Description
1 CH1F	Channel 1 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.
0 CH0F	Channel 0 Flag See the register description. 0 No channel event has occurred. 1 A channel event has occurred.

12.3.14 Features Mode Selection (FTMx_MODE)

This register contains the control bits used to configure the fault interrupt and fault control, capture test mode, PWM synchronization, write protection, channel output initialization, and enable the enhanced features of the FTM. These controls relate to all channels within this module.

Address: Base address + 1Ah offset

Bit	7	6	5	4	3	2	1	0
Read Write	FAULTIE	FAULTM		CAPTEST	PWMSYNC	WPDIS	INIT	FTMEN
Reset	0	0	0	0	0	1	0	0

FTMx_MODE field descriptions

Field	Description
7 FAULTIE	Fault Interrupt Enable Enables the generation of an interrupt when a fault is detected by FTM and the FTM fault control is enabled. 0 Fault control interrupt is disabled. 1 Fault control interrupt is enabled.
6–5 FAULTM	Fault Control Mode Defines the FTM fault control mode. FAULTM is write protected. These bits can be written only if MODE[WPDIS] = 1. 00 Fault control is disabled for all channels. 01 Fault control is enabled for even channels only (channels 0, 2, 4, and 6), and the selected mode is the manual fault clearing. 10 Fault control is enabled for all channels, and the selected mode is the manual fault clearing. 11 Fault control is enabled for all channels, and the selected mode is the automatic fault clearing.

Table continues on the next page...

FTMx_MODE field descriptions (continued)

Field	Description
4 CAPTEST	Capture Test Mode Enable Enables the capture test mode. CAPTEST bit is write protected. This bit can be written only if WPDIS = 1. 0 Capture test mode is disabled. 1 Capture test mode is enabled.
3 PWMSYNC	PWM Synchronization Mode Selects which triggers can be used by MOD, CV, CHnOM, and FTM counter synchronization (PWM synchronization). 0 No restrictions. Software and hardware triggers can be used by MOD, CV, CHnOM, and FTM counter synchronization. 1 Software trigger can be used only by MOD and CV synchronization, and hardware triggers can be used only by CHnOM and FTM counter synchronization.
2 WPDIS	Write Protection Disable When write protection is enabled (MODE[WPDIS] = 0), write protected bits can not be written. When write protection is disabled (MODE[WPDIS] = 1), write protected bits can be written. The WPDIS bit is the negation of the WPEN bit. WPDIS is cleared when 1 is written to WPEN. WPDIS is set when WPEN bit is read as a 1 and then 1 is written to WPDIS. Writing 0 to WPDIS has no effect. 0 Write protection is enabled. 1 Write protection is disabled.
1 INIT	Initialize the Output Channels When a 1 is written to INIT bit the output channels are initialized according to the state of their corresponding bit in the OUTINIT register. Writing a 0 to INIT bit has no effect. The INIT bit is always read as 0.
0 FTMEN	FTM Enable This bit is write protected, and can be written only if WPDIS = 1. 0 Only the TPM-compatible registers (first set of registers) can be used without any restriction. Do not use the FTM-specific registers. 1 All registers including the FTM-specific registers (second set of registers) are available for use with no restrictions.

12.3.15 Synchronization (FTMx_SYNC)

This register configures the PWM synchronization.

A synchronization event can perform the synchronized update of MOD, CV, and OUTMASK registers with the value of their write buffer and the FTM counter initialization.

NOTE

The software trigger (SWSYNC bit) and hardware triggers (TRIG0, TRIG1, and TRIG2 bits) have a potential conflict if used together. Use only hardware or software triggers but not both at the same time, otherwise unpredictable behavior is likely to happen.

The selection of the boundary cycle (CNTMAX and CNTMIN bits) is intended to provide the update of MOD, CNTIN, and CV across all enabled channels simultaneously. The use of the boundary cycle selection together with TRIG0, TRIG1, or TRIG2 bits is likely to result in unpredictable behavior.

The MODE[PWMSYNC] bit determines which type of trigger event controls the functions enabled by the SYNC register.

Address: Base address + 1Bh offset

Bit	7	6	5	4	3	2	1	0
Read Write	SWSYNC	TRIG2	TRIG1	TRIG0	SYNCHOM	REINIT	CNTMAX	CNTMIN
Reset	0	0	0	0	0	0	0	0

FTMx_SYNC field descriptions

Field	Description
7 SWSYNC	PWM Synchronization Software Trigger Selects the software trigger as the PWM synchronization trigger. The software trigger occurs when a 1 is written to SWSYNC bit. 0 Software trigger is not selected. 1 Software trigger is selected.
6 TRIG2	PWM Synchronization External Trigger 2 Selects external trigger 2 as the PWM synchronization trigger. External trigger 2 occurs when the FTM detects a rising edge in the trigger 2 input signal. 0 External trigger 2 is not selected. 1 External trigger 2 is selected.
5 TRIG1	PWM Synchronization External Trigger 1 Selects external trigger 1 as the PWM synchronization trigger. External trigger 1 occurs when the FTM detects a rising edge in the trigger 1 input signal. 0 External trigger 1 is not selected. 1 External trigger 1 is selected.
4 TRIG0	PWM Synchronization External Trigger 0 Selects external trigger 0 as the PWM synchronization trigger. External trigger 0 occurs when the FTM detects a rising edge in the trigger 0 input signal.

Table continues on the next page...

FTMx_SYNC field descriptions (continued)

Field	Description
	0 External trigger 0 is not selected. 1 External trigger 0 is selected.
3 SYNCHOM	Output Mask Synchronization Selects when the CHnOM bits in register OUTMASK are updated with the value of their write buffer. 0 CHnOM bits are updated with the value of the OUTMASK write buffer in all rising edges of the system clock. 1 CHnOM bits are updated with the value of the OUTMASK write buffer only by the PWM synchronization.
2 REINIT	FTM Counter Reinitialization by Synchronization (See “FTM Counter Synchronization”) Determines if the FTM counter is reinitialized when the selected trigger for the synchronization is detected. 0 FTM counter continues to count normally. 1 FTM counter is updated with its initial value when the selected trigger is detected.
1 CNTMAX	Maximum Boundary Cycle Enable Determines when the MOD, CNTIN, and CV registers are updated with their write buffer contents following a PWM synchronization event. If CNTMAX is enabled, the registers are updated when the FTM counter reaches its maximum value MOD. 0 The maximum boundary cycle is disabled. 1 The maximum boundary cycle is enabled.
0 CNTMIN	Minimum Boundary Cycle Enable Determines when the MOD and CV registers are updated with their write buffer contents after a PWM synchronization event. If CNTMIN is enabled, the registers are updated when the FTM counter reaches its minimum value CNTIN. 0 The minimum boundary cycle is disabled. 1 The minimum boundary cycle is enabled.

12.3.16 Initial State for Channel Output (FTMx_OUTINIT)

Address: Base address + 1Ch offset

Bit	7	6	5	4	3	2	1	0
Read Write	CH7OI	CH6OI	CH5OI	CH4OI	CH3OI	CH2OI	CH1OI	CH0OI
Reset	0	0	0	0	0	0	0	0

FTMx_OUTINIT field descriptions

Field	Description
7 CH7OI	Channel 7 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs.

Table continues on the next page...

FTMx_OUTINIT field descriptions (continued)

Field	Description
	0 The initialization value is 0. 1 The initialization value is 1.
6 CH6OI	Channel 6 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
5 CH5OI	Channel 5 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
4 CH4OI	Channel 4 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
3 CH3OI	Channel 3 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
2 CH2OI	Channel 2 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
1 CH1OI	Channel 1 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.
0 CH0OI	Channel 0 Output Initialization Value Selects the value that is forced into the channel output when the initialization occurs. 0 The initialization value is 0. 1 The initialization value is 1.

12.3.17 Output Mask (FTMx_OUTMASK)

This register provides a mask for each FTM channel. The mask of a channel determines if its output responds, that is, it is masked or not, when a match occurs. This feature is used for BLDC control applications where the PWM signal is presented to an electric motor at specific times to provide electronic commutation.

Any write to the OUTMASK register stores the value into a write buffer. The register is updated with the value of its write buffer according to PWM synchronization.

Address: Base address + 1Dh offset

Bit	7	6	5	4	3	2	1	0
Read Write	CH7OM	CH6OM	CH5OM	CH4OM	CH3OM	CH2OM	CH1OM	CH0OM
Reset	0	0	0	0	0	0	0	0

FTMx_OUTMASK field descriptions

Field	Description
7 CH7OM	Channel 7 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
6 CH6OM	Channel 6 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
5 CH5OM	Channel 5 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
4 CH4OM	Channel 4 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
3 CH3OM	Channel 3 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally).

Table continues on the next page...

FTMx_OUTMASK field descriptions (continued)

Field	Description
	0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
2 CH2OM	Channel 2 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
1 CH1OM	Channel 1 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.
0 CH0OM	Channel 0 Output Mask Defines if the channel output is masked (forced to its inactive state) or unmasked (it continues to operate normally). 0 Channel output is not masked. It continues to operate normally. 1 Channel output is masked. It is forced to its inactive state.

12.3.18 Function for Linked Channels (FTMx_COMBINE*n*)

This register contains the control bits used to configure the fault control, synchronization, deadtime, dual edge capture mode, complementary, and combine features of channels (n) and (n+1).

- COMBINE0 supports channels 0 and 1.
- COMBINE1 supports channels 2 and 3.
- COMBINE2 supports channels 4 and 5.

NOTE

The channel (n) is the even channel and the channel (n+1) is the odd channel of a pair of channels.

Address: Base address + 1Eh offset + (1d × i), where i=0d to 2d

Bit	7	6	5	4	3	2	1	0
Read	0	FAULTEN	SYNCEN	DTEN	DECAP	DECAPEN	COMP	COMBINE
Write								
Reset	0	0	0	0	0	0	0	0

FTMx_COMBINE*n* field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 FAULTEN	Fault Control Enable Enables the fault control in channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The fault control in this pair of channels is disabled. 1 The fault control in this pair of channels is enabled.
5 SYNCEN	Synchronization Enable Enables PWM synchronization of registers C(n)V and C(n+1)V. 0 The PWM synchronization in this pair of channels is disabled. 1 The PWM synchronization in this pair of channels is enabled.
4 DTEN	Deadtime Enable Enables the deadtime insertion in the channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The deadtime insertion in this pair of channels is disabled. 1 The deadtime insertion in this pair of channels is enabled.
3 DECAP	Dual Edge Capture Mode Captures Enables the capture of the FTM counter value according to the channel (n) input event and the configuration of the dual edge capture bits. This field applies only when MODE[FTMEN] = 1 and DECAPEN = 1. DECAP bit is cleared automatically by hardware if dual edge capture one-shot mode is selected and when the capture of channel (n+1) event is made. 0 The dual edge captures are inactive. 1 The dual edge captures are active.
2 DECAPEN	Dual Edge Capture Mode Enable Enables the dual edge capture mode in the channels (n) and (n+1). This bit reconfigures the function of MSnA, ELSnB:ELSnA, and ELS(n+1)B:ELS(n+1)A bits in dual edge capture mode according to the table Mode, Edge, and Level Selection in the description of the CnSC register. This field applies only when MODE[FTMEN] = 1. DECAPEN is write protected, this bit can be written only if MODE[WPDIS] = 1. 0 The dual edge capture mode in this pair of channels is disabled. 1 The dual edge capture mode in this pair of channels is enabled.
1 COMP	Complement of Channel (n) Enables complementary mode for the combined channels. In complementary mode the channel (n+1) output is the inverse of the channel (n) output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel (n+1) output is the same as the channel (n) output. 1 The channel (n+1) output is the complement of the channel (n) output.

Table continues on the next page...

FTMx_COMBINE*n* field descriptions (continued)

Field	Description
0 COMBINE	Combine Channels Enables the combine feature for channels (n) and (n+1). This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Channels (n) and (n+1) are independent. 1 Channels (n) and (n+1) are combined.

12.3.19 Deadtime Insertion Control (FTMx_DEADTIME)

This register selects the deadtime prescaler factor and deadtime value. All FTM channels use this clock prescaler and this deadtime value for the deadtime insertion.

Address: Base address + 22h offset

Bit	7	6	5	4	3	2	1	0
Read Write	DTPS		DTVAL					
Reset	0	0	0	0	0	0	0	0

FTMx_DEADTIME field descriptions

Field	Description
7–6 DTPS	Deadtime Prescaler Value Selects the division factor of the system clock. This prescaled clock is used by the deadtime counter. DTPS is write protected. It can be written only when MODE[WPDIS] = 1. 0x Divide the system clock by 1. 10 Divide the system clock by 4. 11 Divide the system clock by 16.
DTVAL	Deadtime Value Selects the deadtime insertion value for the deadtime counter. The deadtime counter is clocked by a scaled version of the system clock. See the description of DTPS. Deadtime insert value = (DTPS × DTVAL). DTVAL selects the number of deadtime counts inserted as follows: • When DTVAL is 0, no counts are inserted. • When DTVAL is 1, 1 count is inserted. • When DTVAL is 2, 2 counts are inserted. This pattern continues up to a possible 63 counts. DTVAL is write protected. It can be written only when MODE[WPDIS] = 1.

12.3.20 External Trigger (FTMx_EXTTRIG)

This register indicates when a channel trigger was generated, enables the generation of a trigger when the FTM counter is equal to its initial value, and selects which channels are used in the generation of the channel triggers. Several FTM channels can be selected to generate multiple triggers in one PWM period.

Channels 6 and 7 are not used to generate channel triggers.

Address: Base address + 23h offset

Bit	7	6	5	4	3	2	1	0
Read Write	TRIGF	INITTRIGEN	CH1TRIG	CH0TRIG	CH5TRIG	CH4TRIG	CH3TRIG	CH2TRIG
Reset	0	0	0	0	0	0	0	0

FTMx_EXTTRIG field descriptions

Field	Description
7 TRIGF	Channel Trigger Flag Set by hardware when a channel trigger is generated. Clear TRIGF by reading EXTTRIG while TRIGF is set and then writing a 0 to TRIGF. Writing a 1 to TRIGF has no effect. If another channel trigger is generated before the clearing sequence is completed, the sequence is reset so TRIGF remains set after the clear sequence is completed for the earlier TRIGF. 0 No channel trigger was generated. 1 A channel trigger was generated.
6 INITTRIGEN	Initialization Trigger Enable Enables the generation of the trigger when the FTM counter is equal to its initial value. 0 The generation of initialization trigger is disabled. 1 The generation of initialization trigger is enabled.
5 CH1TRIG	Channel 1 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
4 CH0TRIG	Channel 0 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
3 CH5TRIG	Channel 5 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.

Table continues on the next page...

FTMx_EXTTRIG field descriptions (continued)

Field	Description
2 CH4TRIG	Channel 4 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
1 CH3TRIG	Channel 3 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.
0 CH2TRIG	Channel 2 Trigger Enable Enables the generation of the channel trigger when the FTM counter is equal to the CV register. 0 The generation of the channel trigger is disabled. 1 The generation of the channel trigger is enabled.

12.3.21 Channels Polarity (FTMx_POL)

This register defines the output polarity of the FTM channels.

NOTE

The safe value that is driven in a channel output when the fault control is enabled and a fault condition is detected is the inactive state of the channel. That is, the safe value of a channel is the value of its POL bit.

Address: Base address + 24h offset

Bit	7	6	5	4	3	2	1	0
Read Write	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
Reset	0	0	0	0	0	0	0	0

FTMx_POL field descriptions

Field	Description
7 POL7	Channel 7 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
6 POL6	Channel 6 Polarity

Table continues on the next page...

FTMx_POL field descriptions (continued)

Field	Description
	Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
5 POL5	Channel 5 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
4 POL4	Channel 4 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
3 POL3	Channel 3 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
2 POL2	Channel 2 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
1 POL1	Channel 1 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.
0 POL0	Channel 0 Polarity Defines the polarity of the channel output. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 The channel polarity is active high. 1 The channel polarity is active low.

12.3.22 Fault Mode Status (FTMx_FMS)

This register contains the fault detection flags, write protection enable bit, and the logic OR of the enable fault inputs.

Address: Base address + 25h offset

Bit	7	6	5	4	3	2	1	0
Read	FAULTF	WPEN	FAULTIN	0	FAULTF3	FAULTF2	FAULTF1	FAULTF0
Write	0				0	0	0	0
Reset	0	0	0	0	0	0	0	0

FTMx_FMS field descriptions

Field	Description
7 FAULTF	Fault Detection Flag Represents the logic OR of the individual FAULTFn bits. Clear FAULTF by reading the FMS register while FAULTF is set and then writing a 0 to FAULTF while there is no existing fault condition at the enabled fault inputs. Writing a 1 to FAULTF has no effect. If another fault condition is detected in an enabled fault input before the clearing sequence is completed, the sequence is reset so FAULTF remains set after the clearing sequence is completed for the earlier fault condition. FAULTF is also cleared when FAULTFn bits are cleared individually. 0 No fault condition was detected. 1 A fault condition was detected.
6 WPEN	Write Protection Enable The WPEN bit is the negation of the WPDIS bit. WPEN is set when 1 is written to it. WPEN is cleared when WPEN bit is read as a 1 and then 1 is written to WPDIS. Writing 0 to WPEN has no effect. 0 Write protection is disabled. Write protected bits can be written. 1 Write protection is enabled. Write protected bits cannot be written.
5 FAULTIN	Fault Inputs Represents the logic OR of the enabled fault input after its filter, if its filter is enabled, when fault control is enabled. 0 The value of the fault input is 0. 1 The value of the fault input is 1.
4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3 FAULTF3	Fault Detection Flag 3 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected in the fault input. Clear FAULTF by reading the FMS register while FAULTFn is set and then writing a 0 to FAULTFn FAULTF while there is no existing fault condition at the fault input n. Writing a 1 to FAULTFn has no effect. FAULTFn bit is also cleared when FAULTF bit is cleared.

Table continues on the next page...

FTMx_FMS field descriptions (continued)

Field	Description
	If another fault condition is detected at fault input n before the clearing sequence is completed, the sequence is reset so FAULTFn remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected in the fault input. 1 A fault condition was detected in the fault input.
2 FAULTF2	Fault Detection Flag 2 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected in the fault input. Clear FAULTF by reading the FMS register while FAULTFn is set and then writing a 0 to FAULTFn FAULTF while there is no existing fault condition at the fault input n. Writing a 1 to FAULTFn has no effect. FAULTFn bit is also cleared when FAULTF bit is cleared. If another fault condition is detected at fault input n before the clearing sequence is completed, the sequence is reset so FAULTFn remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected in the fault input. 1 A fault condition was detected in the fault input.
1 FAULTF1	Fault Detection Flag 1 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected in the fault input. Clear FAULTF by reading the FMS register while FAULTFn is set and then writing a 0 to FAULTFn FAULTF while there is no existing fault condition at the fault input n. Writing a 1 to FAULTFn has no effect. FAULTFn bit is also cleared when FAULTF bit is cleared. If another fault condition is detected at fault input n before the clearing sequence is completed, the sequence is reset so FAULTFn remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected in the fault input. 1 A fault condition was detected in the fault input.
0 FAULTF0	Fault Detection Flag 0 Set by hardware when fault control is enabled, the corresponding fault input is enabled and a fault condition is detected in the fault input. Clear FAULTF by reading the FMS register while FAULTFn is set and then writing a 0 to FAULTFn FAULTF while there is no existing fault condition at the fault input n. Writing a 1 to FAULTFn has no effect. FAULTFn bit is also cleared when FAULTF bit is cleared. If another fault condition is detected at fault input n before the clearing sequence is completed, the sequence is reset so FAULTFn remains set after the clearing sequence is completed for the earlier fault condition. 0 No fault condition was detected in the fault input. 1 A fault condition was detected in the fault input.

12.3.23 Input Capture Filter Control (FTMx_FILTER*n*)

This register selects the filter value for the inputs of channels.

- FILTER0 supports Channels 0 and 1.
- FILTER1 supports Channels 2 and 3.
- Channels 4 and 5 do not have an input filter.

NOTE

Writing to this register has immediate effect and must be done only when the input capture modes of the affected channels are disabled. Failure to do this could result in a missing valid signal.

Address: Base address + 26h offset + (1d × i), where i=0d to 1d

Bit	7	6	5	4	3	2	1	0
Read Write	CHoddFVAL				CHevenFVAL			
Reset	0	0	0	0	0	0	0	0

FTMx_FILTERn field descriptions

Field	Description
7–4 CHoddFVAL	Input Filter for Odd Channel Selects the filter value for the odd-numbered channel input. The filter is disabled when the value is zero.
CHevenFVAL	Input Filter for Even Channel Selects the filter value for the even-numbered channel input. The filter is disabled when the value is zero.

12.3.24 Fault Input Filter Control (FTMx_FLTFILTER)

This register selects the fault inputs and enables the fault input filter.

Address: Base address + 28h offset

Bit	7	6	5	4	3	2	1	0
Read	0				FFVAL			
Write								
Reset	0	0	0	0	0	0	0	0

FTMx_FLTFILTER field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
FFVAL	Fault Input Filter Selects the filter value for the fault inputs.

Table continues on the next page...

FTMx_FLTFILTER field descriptions (continued)

Field	Description
	The fault filter is disabled when the value is zero. **NOTE:** Writing to this field has immediate effect and must be done only when the fault control or the fault input is disabled. Failure to do so could result in a missing fault detection.

12.3.25 Fault Input Control (FTMx_FLTCTRL)

This register selects the fault inputs and enables the fault input filter.

Address: Base address + 29h offset

Bit	7	6	5	4	3	2	1	0
Read Write	FFLTR3EN	FFLTR2EN	FFLTR1EN	FFLTR0EN	FAULT3EN	FAULT2EN	FAULT1EN	FAULT0EN
Reset	0	0	0	0	0	0	0	0

FTMx_FLTCTRL field descriptions

Field	Description
7 FFLTR3EN	Fault Input 3 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
6 FFLTR2EN	Fault Input 2 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
5 FFLTR1EN	Fault Input 1 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.
4 FFLTR0EN	Fault Input 0 Filter Enable Enables the filter for the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input filter is disabled. 1 Fault input filter is enabled.

Table continues on the next page...

FTMx_FLTCTRL field descriptions (continued)

Field	Description
3 FAULT3EN	Fault Input 3 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.
2 FAULT2EN	Fault Input 2 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.
1 FAULT1EN	Fault Input 1 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.
0 FAULT0EN	Fault Input 0 Enable Enables the fault input. This field is write protected. It can be written only when MODE[WPDIS] = 1. 0 Fault input is disabled. 1 Fault input is enabled.

12.4 Functional Description

The following sections describe the FTM features.

The notation used in this document to represent the counters and the generation of the signals is shown in the following figure.

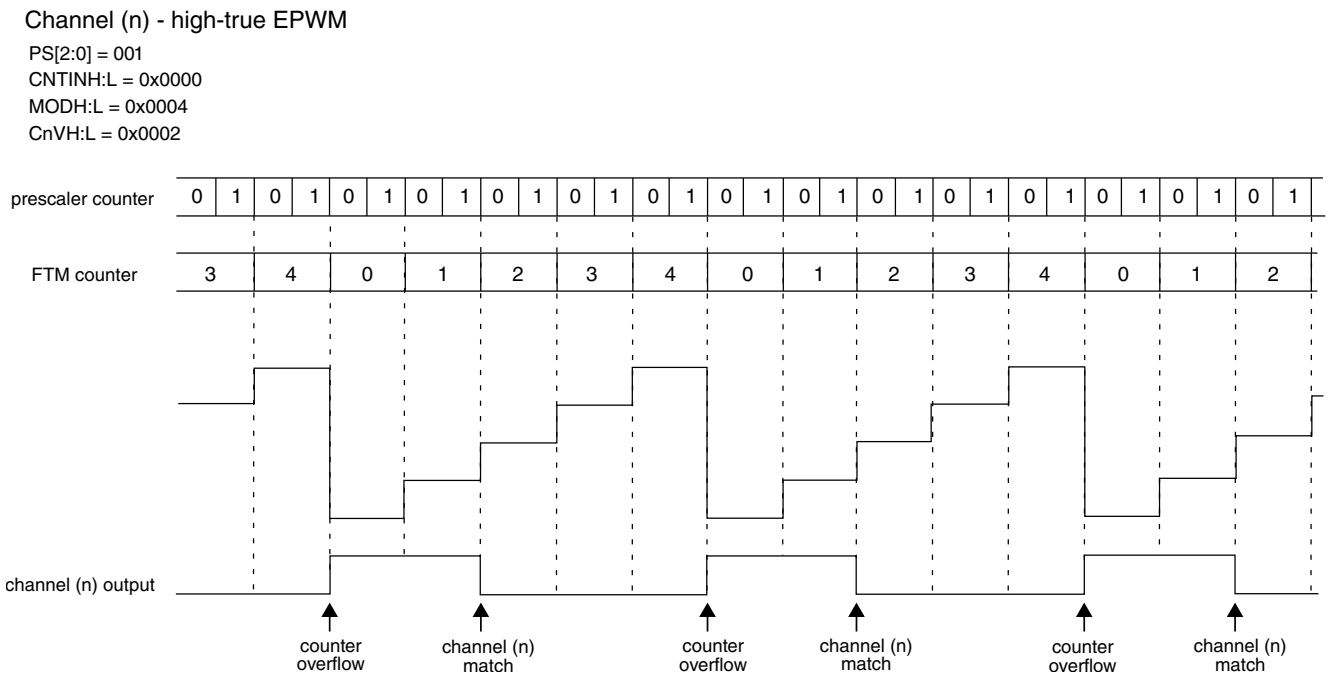


Figure 12-2. Notation used

12.4.1 Clock Source

FTM module has only one clock domain that is the system clock.

12.4.1.1 Counter Clock Source

The CLKS[1:0] bits in the SC register select one of three possible clock sources for the FTM counter or disable the FTM counter. After any MCU reset, CLKS[1:0] = 0:0 so no clock source is selected.

The CLKS[1:0] bits may be read or written at any time. Disabling the FTM counter by writing 0:0 to the CLKS[1:0] bits does not affect the FTM counter value or other registers.

The fixed frequency clock is an alternative clock source for the FTM counter that allows the selection of a clock other than the system clock or an external clock. This clock input is defined by chip integration. Refer to chip specific documentation for further information. Due to FTM hardware implementation limitations, the frequency of the fixed frequency clock must not exceed the system clock frequency.

The external clock passes through a synchronizer clocked by the system clock to ensure that counter transitions are properly aligned to system clock transitions. Therefore, to meet the Nyquist criteria and account for jitter, the frequency of the external clock source must not exceed 1/4 of the system clock frequency.

12.4.2 Prescaler

The selected counter clock source passes through a prescaler that is a 7-bit counter. The value of the prescaler is selected by the PS[2:0] bits. The following figure shows an example of the prescaler counter and FTM counter.

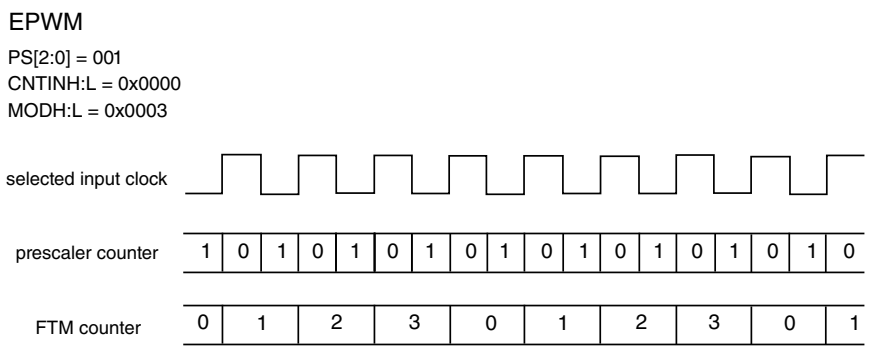


Figure 12-3. Example of the prescaler counter

12.4.3 Counter

The FTM has a 16-bit counter that is used by the channels either for input or output modes. The FTM counter clock is the selected clock divided by the prescaler (see Prescaler).

The FTM counter has these modes of operation:

- up counting (see Up counting)
- up-down counting (see Up-down counting)

12.4.3.1 Up counting

Up counting is selected when (CPWMS = 0).

CNTINH:L defines the starting value of the count and MODH:L defines the final value of the count; see the following figure. The value of CNTINH:L is loaded into the FTM counter, and the counter increments until the value of MODH:L is reached, at which point the counter is reloaded with CNTINH:L.

The FTM period when using up counting is (MODH:L – CNTINH:L + 0x0001) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MODH:L to CNTINH:L.

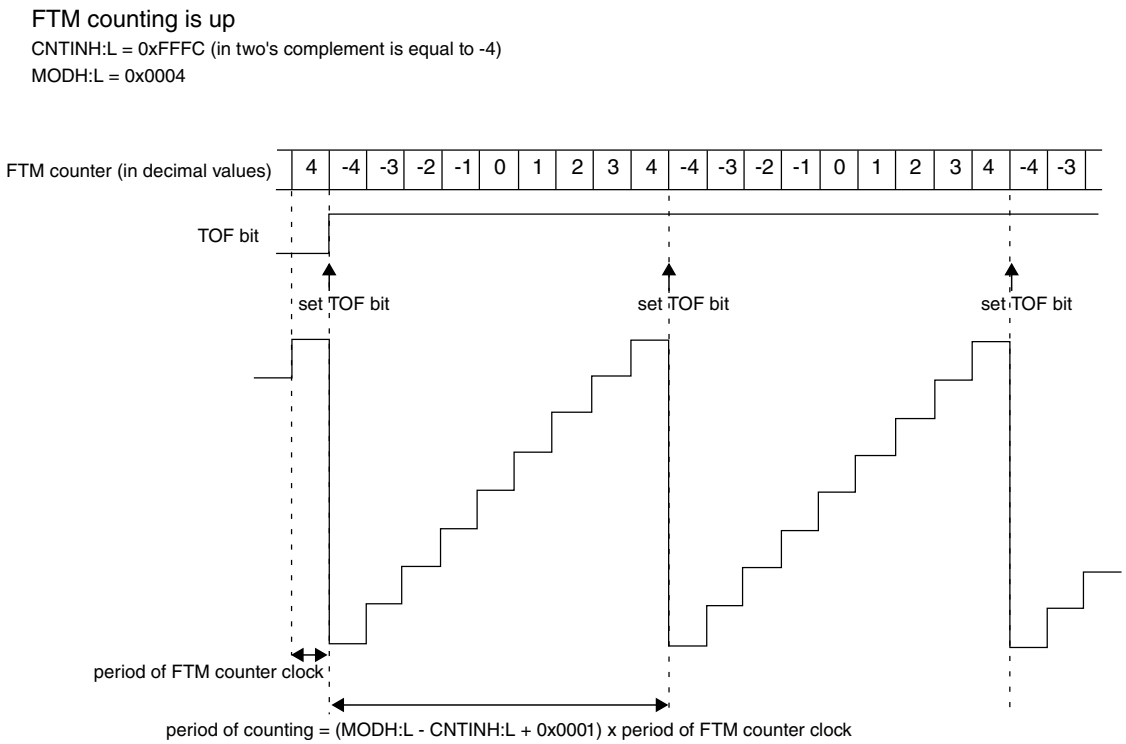


Figure 12-4. Example of FTM up and signed counting

If (CNTINH:L = 0x0000), the FTM counting is equivalent to TPM up counting; that is, up and unsigned counting. See the following figure. If (CNTINH[7] = 1), then the initial value of the FTM counter is a negative number in two's complement format, so the FTM counting is up and signed. Conversely, if (CNTINH[7] = 0 and CNTINH:L ≠ 0x0000), then the initial value of the FTM counter is a positive number, therefore the FTM counting is up and unsigned.

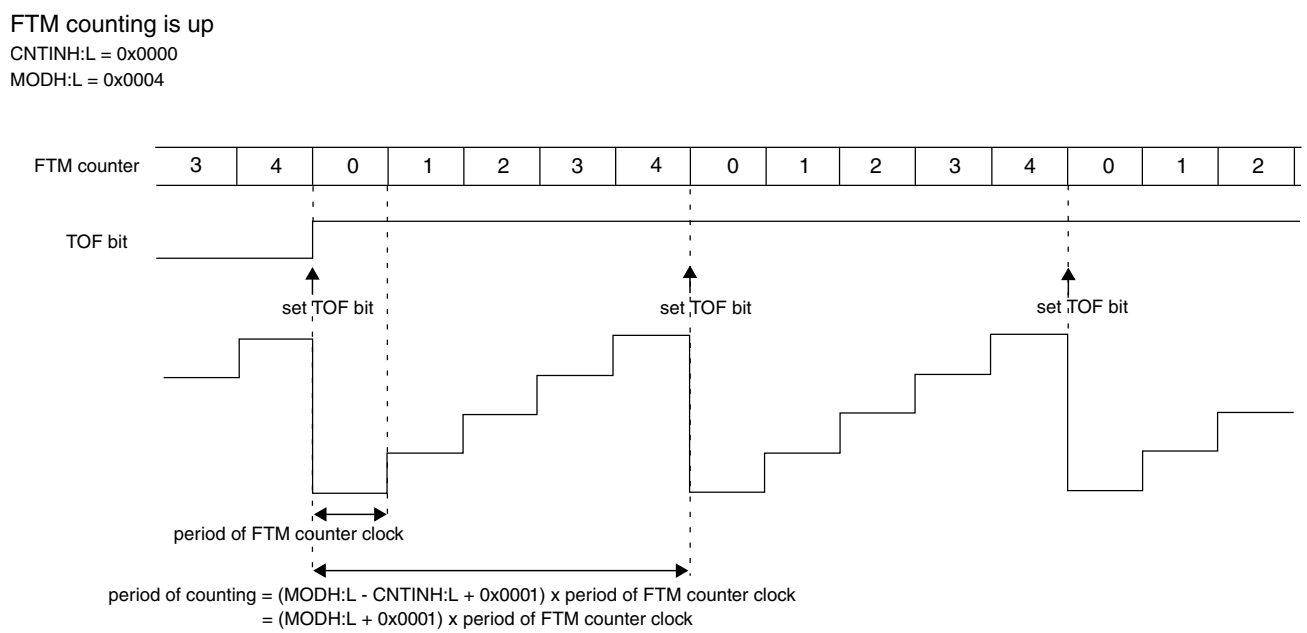


Figure 12-5. Example of FTM up counting with CNTIN = 0x0000

Note

- FTM operation is valid only when the value of the CNTINH:L registers is less than the value of the MODH:L registers, either in the unsigned counting or signed counting.. Software must ensure that the values in the CNTINH:L and MODH:L registers meet this requirement. Any values of CNTINH:L and MODH:L that do not satisfy this criteria can result in unpredictable behavior.
- MODH:L = CNTINH:L is a redundant condition. In this case, the FTM counter is always equal to MODH:L and the TOF bit is set in each rising edge of the FTM counter clock.
- When MODH:L = 0x0000, CNTINH:L = 0x0000 (for example after reset), and FTMEN = 1, the FTM counter remains stopped at 0x0000 until a non-zero value is written into the MODH:L or CNTINH:L registers.
- Setting CNTINH:L to be greater than the value of MODH:L is not recommended as this unusual setting may make the FTM operation difficult to comprehend. However, there is no restriction on this configuration, and an example is shown in the following figure.

FTM counting is up
MODH:L = 0x0005
CNTINH:L = 0x0015

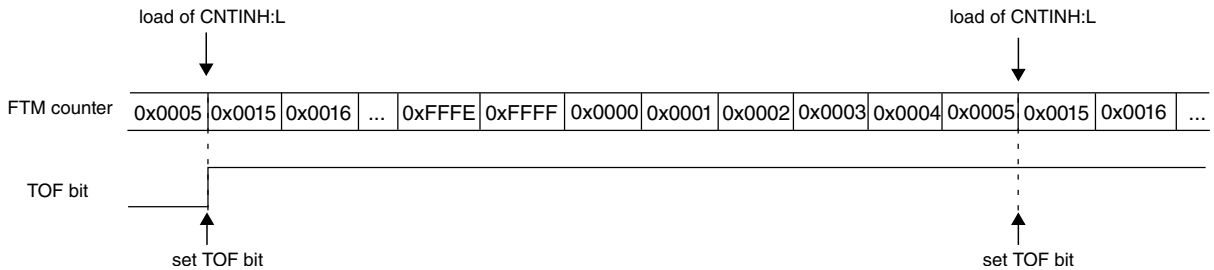


Figure 12-6. Example of up counting when the value of CNTIN registers is greater than the value of MOD registers

12.4.3.2 Up-down counting

Up-down counting is selected when (CPWMS = 1).

CNTINH:L defines the starting value of the count and MODH:L defines the final value of the count. The value of CNTINH:L is loaded into the FTM counter, and the counter increments until the value of MODH:L is reached, at which point the counter is decremented until it returns to the value of CNTINH:L and the up-down counting restarts.

The FTM period when using up-down counting is 2 × (MODH:L – CNTINH:L) × period of the FTM counter clock.

The TOF bit is set when the FTM counter changes from MODH:L to (MODH:L – 1).

If (CNTINH:L = 0x0000), the FTM counting is equivalent to TPM up-down counting; that is, up-down and unsigned counting. See the following figure.

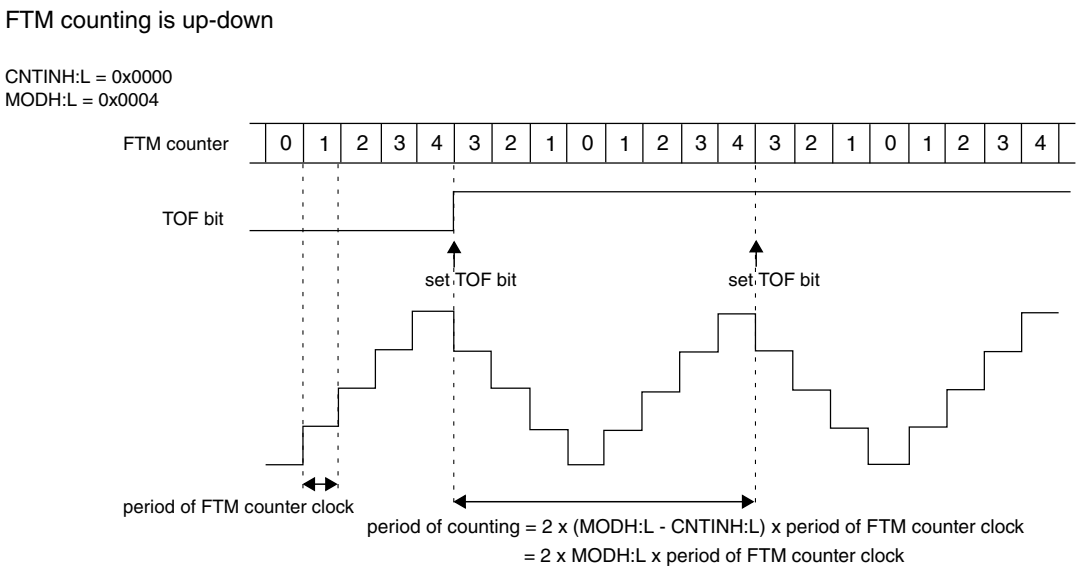


Figure 12-7. Example of up-down counting when CNTIN = 0x0000

Note

- The up-down counting is available only when (CNTINH:L = 0x0000).
- The configuration with (CNTINH:L ≠ 0x0000) when (CPWMS = 1) is not recommended and its results are not guaranteed.

12.4.3.3 Free running counter

If (FTMEN = 0) and (MODH:L = 0x0000 or MODH:L = 0xFFFF), the FTM counter is a free running counter. In this case, the FTM counter runs free from 0x0000 through 0xFFFF and the TOF bit is set when the FTM counter changes from 0xFFFF to 0x0000 See the following figure.

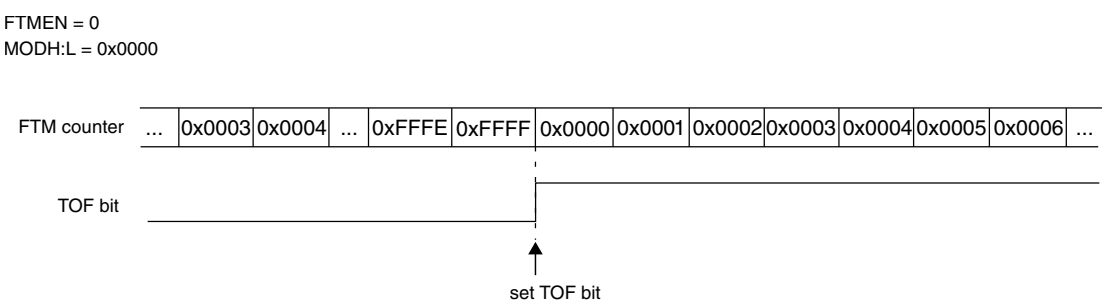


Figure 12-8. Example when the FTM counter is a free running

The FTM counter is also a free running counter when all of the following apply:

- (FTMEN = 1)

- (CPWMS = 0)
- (CNTINH:L = 0x0000)
- (MODH:L = 0xFFFF)

In this case, the FTM counter runs free from 0x0000 through 0xFFFF and the TOF bit is set when the FTM counter changes from 0xFFFF to 0x0000.

12.4.3.4 Counter reset

Any write to CNTH or CNTL register resets the FTM counter to the value of CNTINH:L and the channels output to its initial value, except for channels in output compare mode.

The FTM counter synchronization can also be used to force the value of CNTINH:L into the FTM counter and the channels output to its initial value, except for channels in output compare mode.

12.4.4 Input capture mode

The input capture mode is selected when (DECAPEN = 0), (COMBINE = 0), (CPWMS = 0), (MSnB:MSnA = 0:0), and (ELSnB:ELSnA ≠ 0:0).

When a selected edge occurs on the channel input, the current value of the FTM counter is captured into the CnVH:L registers. At the same time, the CHnF bit is set and the channel interrupt is generated if enabled by CHnIE = 1. See the following figure.

When a channel is configured for input capture, the CHn pin is an edge-sensitive input. ELSnB:ELSnA control bits determine which edge, falling or rising, triggers input-capture event. Note that the maximum frequency for the channel input signal to be detected correctly is system clock divided by four, which is required to meet Nyquist criteria for signal sampling.

When either half of the 16-bit capture register (CnVH:L) is read, the other half is latched into a buffer to support coherent 16-bit access in big-endian or little-endian order. This read coherency mechanism can be manually reset by writing to CnSC register.

Writes to the CnVH:L registers are ignored in input capture mode.

While in BDM, the input capture function works as configured. When a selected edge event occurs, the FTM counter value, which is frozen because of BDM, is captured into the CnVH:L registers and the CHnF bit is set.

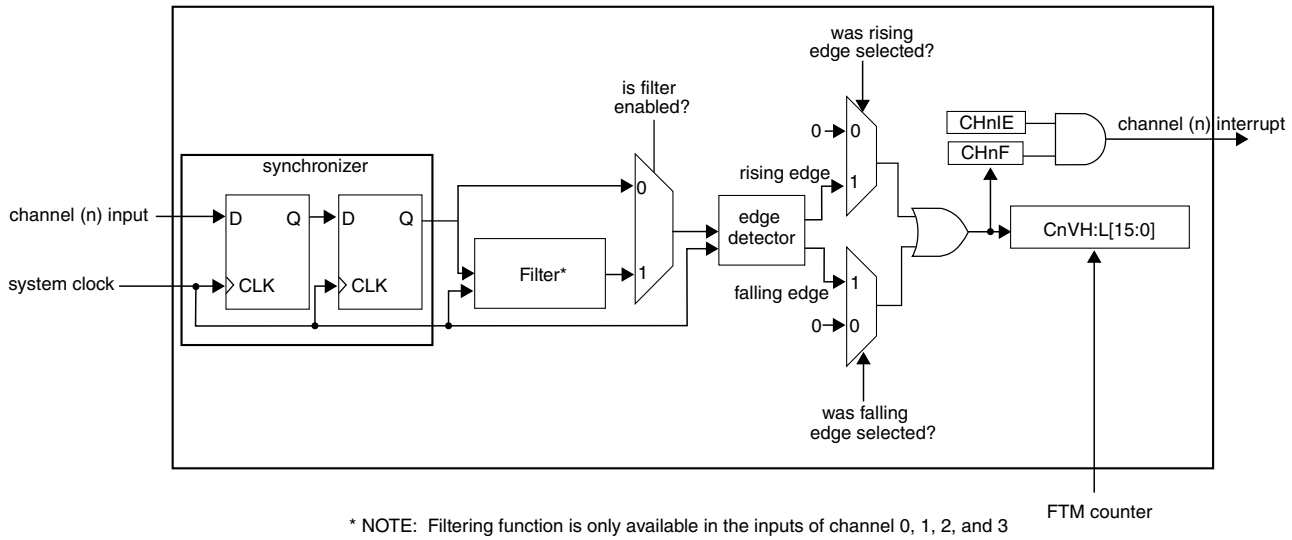


Figure 12-9. Input capture mode

If the channel input does not have a filter enabled, then the input signal is always delayed three rising edges of the system clock; that is, two rising edges to the synchronizer plus one more rising edge to the edge detector. In other words, the CHnF bit is set on the third rising edge of the system clock after a valid edge occurs on the channel input.

Note

- Input capture mode is available only with (CNTINH:L = 0x0000).
- Input capture mode with (CNTINH:L ≠ 0x0000) is not recommended and its results are not guaranteed.

12.4.4.1 Filter for input capture mode

The filter function is available only on channels 0, 1, 2, and 3.

Firstly, the input signal is synchronized by the system clock. Following synchronization, the input signal enters the filter block; see the following figure. When there is a state change in the input signal, the 5-bit counter is reset and starts counting up. As long as the new state is stable on the input, the counter continues to increment. If the 5-bit counter overflows (the counter exceeds the value of the CHnFVAL[3:0] bits), the state change of the input signal is validated. It is then transmitted as a pulse edge to the edge detector.

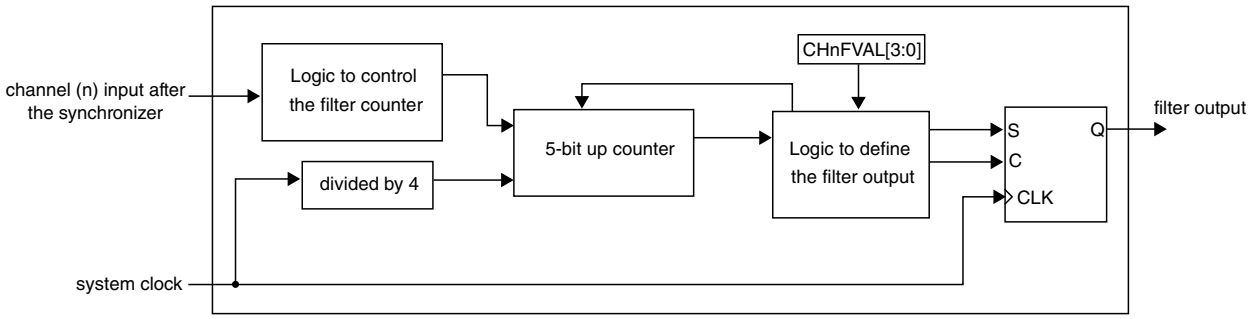


Figure 12-10. Channel input filter

If the opposite edge appears on the input signal before validation, the counter is reset. At the next input transition, the counter starts counting again. Any pulse shorter than the minimum valid width (CHnFVAL[3:0] bits × 4 system clocks) is regarded as a glitch and is not passed on to the edge detector. A timing diagram of the input filter is shown in the following figure.

The filter function is disabled when CHnFVAL[3:0] bits are zero. In this case, the input signal is delayed three rising edges of the system clock. If (CHnFVAL[3:0] ≠ 0000), then the input signal is delayed by the minimum pulse width (CHnFVAL[3:0] × 4 system clocks) plus a further four rising edges of the system clock (two rising edges to the synchronizer, one rising edge to the filter output plus one more to the edge detector). In other words, CHnF is set (4 + 4 × CHnFVAL[3:0]) system clock periods after a valid edge occurs on the channel input.

The clock for the 5-bit counter in the channel input filter is the system clock divided by 4.

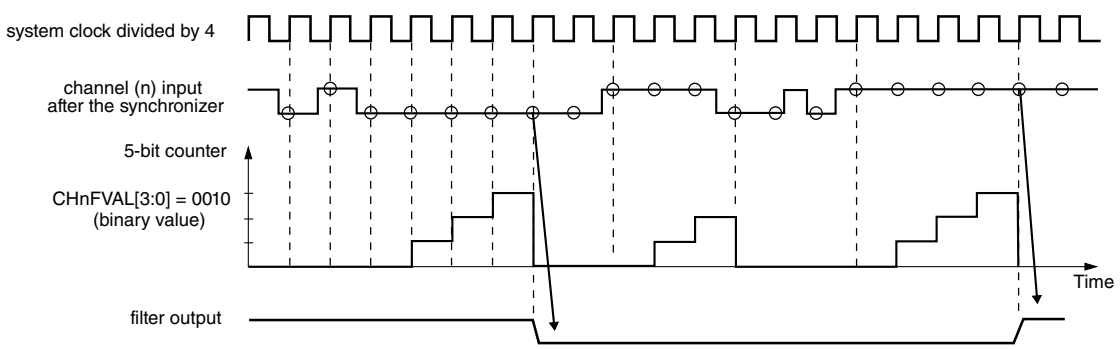


Figure 12-11. Channel input filter example

12.4.5 Output compare mode

The output compare mode is selected when (DECAPEN = 0), (COMBINE = 0), (CPWMS = 0) and (MSnB:MSnA = 0:1).

In output compare mode, the FTM can generate timed pulses with programmable position, polarity, duration, and frequency. When the counter matches the value in the CnVH:CnVL registers of an output compare channel, the channel (n) output can be set, cleared, or toggled.

When a channel is initially configured to toggle mode, the previous value of the channel output is held until the first output compare event occurs.

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:CnVL).

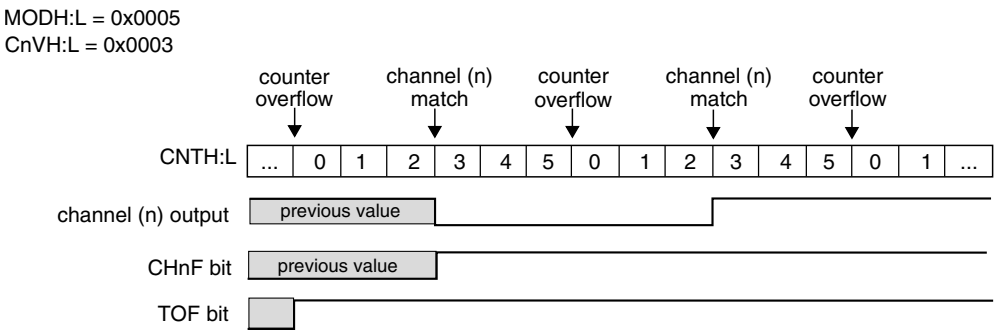


Figure 12-12. Example of the output compare mode when the match toggles the channel output

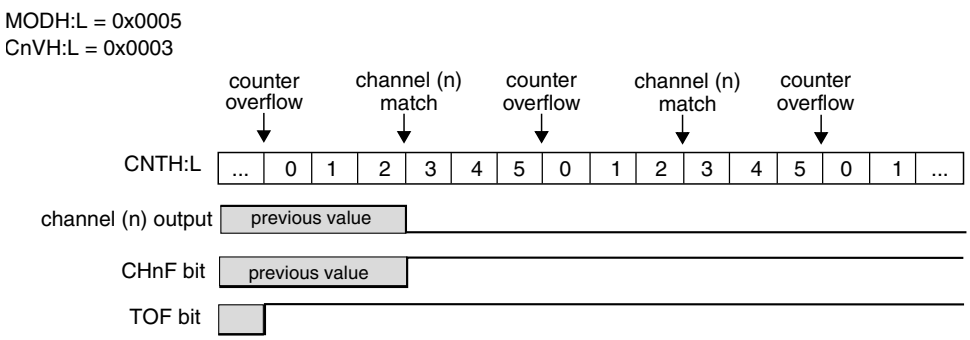


Figure 12-13. Example of the output compare mode when the match clears the channel output

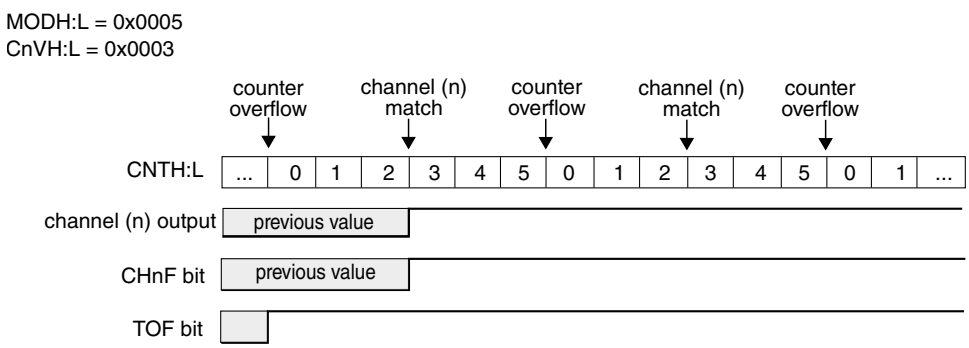


Figure 12-14. Example of the output compare mode when the match sets the channel output

It is possible to use the output compare mode with (ELSnB:ELSnA = 0:0). In this case, when the counter reaches the value in the CnVH:CnVL registers, the CHnF bit is set and the channel (n) interrupt is generated, if CHnIE = 1. However, the channel (n) output is not modified and controlled by FTM.

Note

- Output compare mode is available only with (CNTINH:CNTINL = 0x0000).
- Output compare mode with (CNTINH:CNTINL ≠ 0x0000) is not recommended and its results are not guaranteed.

12.4.6 Edge-aligned PWM (EPWM) mode

The edge-aligned mode is selected when all of the following apply:

- (DECAPEN = 0)
- (COMBINE = 0)
- (CPWMS = 0)
- (MSnB = 1)

The EPWM period is determined by (MODH:L – CNTINH:L + 0x0001) and the pulse width (duty cycle) is determined by (CnVH:L – CNTINH:L).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:L), that is, at the end of the pulse width.

This type of PWM signal is called edge-aligned because the leading edges of all PWM signals are aligned with the beginning of the period, which is the same for all channels within an FTM.

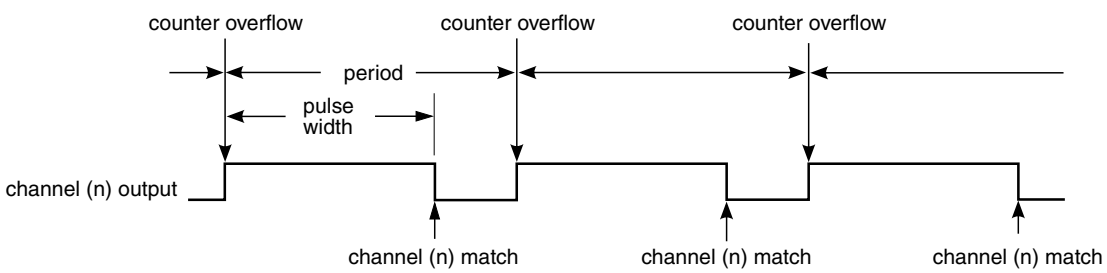


Figure 12-15. EPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnVH:L registers, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however, the channel (n) output is not controlled by FTM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the counter overflow, when the value of CNTINH:L is loaded into the FTM counter. Additionally, it is forced low at the channel (n) match, when the FTM counter = CnVH:L. See the following figure.

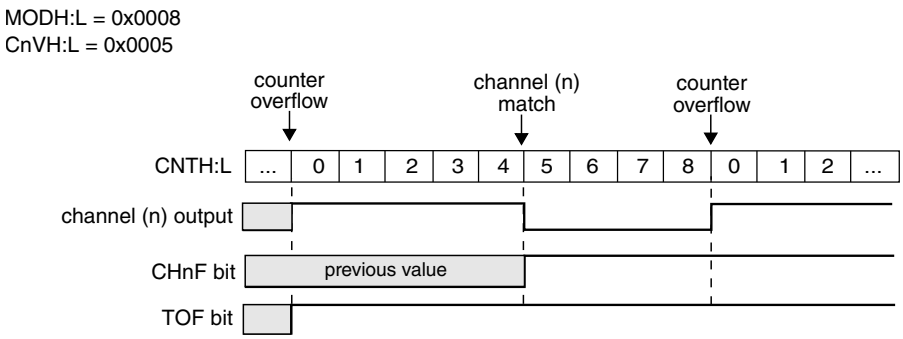


Figure 12-16. EPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the counter overflow, when the value of CNTINH:L is loaded into the FTM counter. Additionally, it is forced high at the channel (n) match, when the FTM counter = CnVH:L. See the following figure.

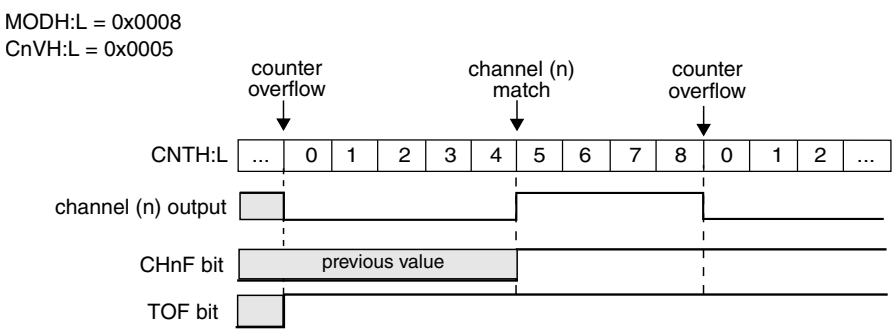


Figure 12-17. EPWM signal with ELSnB:ELSnA = X:1

If (CnVH:L = 0x0000), then the channel (n) output is a 0% duty cycle EPWM signal and CHnF bit is not set, even when there is the channel (n) match. If (CnVH:L > MODH:L), then the channel (n) output is a 100% duty cycle EPWM signal and CHnF bit is not set, even when there is the channel (n) match. Therefore, MODH:MODL must be less than 0xFFFF in order to get a 100% duty cycle EPWM signal.

Note

- EPWM mode is available only with (CNTINH:L = 0x0000).
- EPWM mode with (CNTINH:L ≠ 0x0000) is not recommended and its results are not guaranteed.

12.4.7 Center-aligned PWM (CPWM) mode

The center-aligned mode is selected when all of the following apply:

- (DECAPEN = 0)
- (COMBINE = 0)
- (CPWMS = 1)

The CPWM pulse width (duty cycle) is determined by 2 × (CnVH:L – CNTINH:L). The period is determined by 2 × (MODH:L – CNTINH:L). See the following figure. MODH:L must be kept in the range of 0x0001 to 0x7FFF because values outside this range can produce ambiguous results.

In the CPWM mode, the FTM counter counts up until it reaches MODH:L and then counts down until it reaches the value of CNTINH:L.

The CHnF bit is set and channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = CnVH:L) when the FTM counting is down, at the begin of the pulse width, and when the FTM counting is up, at the end of the pulse width.

This type of PWM signal is called center-aligned because the pulse width centers for all channels are aligned with the value of CNTINH:L.

The other channel modes are not compatible with the up-down counter (CPWMS = 1). Therefore, all FTM channels must be used in CPWM mode when (CPWMS = 1).

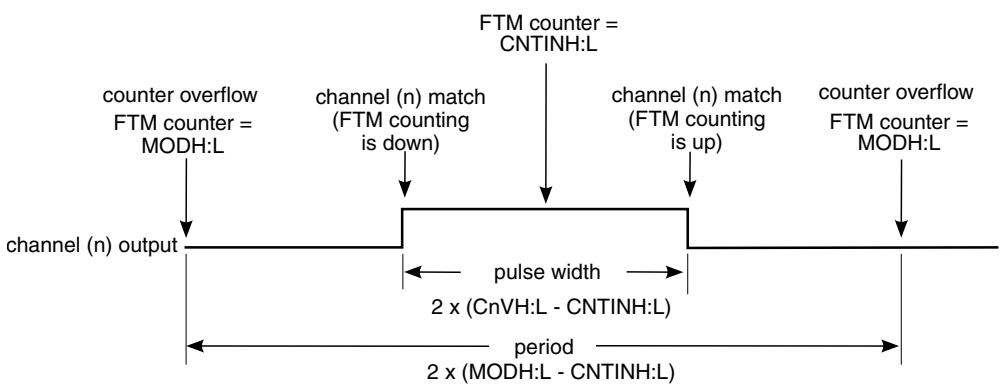


Figure 12-18. CPWM period and pulse width with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = 0:0) when the counter reaches the value in the CnVH:L registers, the CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1), however the channel (n) output is not controlled by FTM.

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced high at the channel (n) match (FTM counter = CnVH:L) when counting down, and it is forced low at the channel (n) match when counting up; see the following figure.

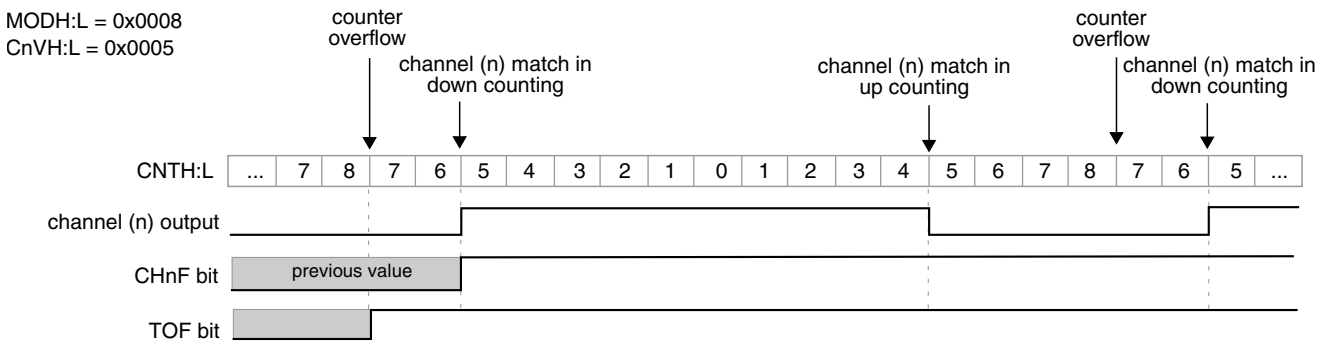


Figure 12-19. CPWM signal with ELSnB:ELSnA = 1:0

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced low at the channel (n) match (FTM counter = CnVH:L) when counting down, and it is forced high at the channel (n) match when counting up; see the following figure.

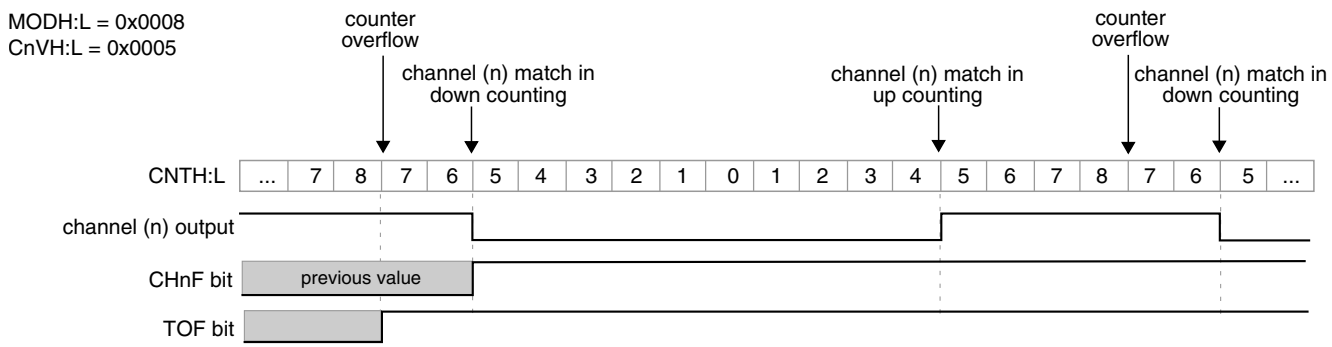


Figure 12-20. CPWM signal with ELSnB:ELSnA = X:1

If (CnVH:L = 0x0000) or (CnVH:L is a negative value, that is, CnVH[7] = 1) then the channel (n) output is a 0% duty cycle CPWM signal and CHnF bit is not set even when there is the channel (n) match.

If (CnVH:L is a positive value, that is, CnVH[7] = 0), (CnVH:L ≥ MODH:L), and (MODH:L ≠ 0x0000), then the channel (n) output is a 100% duty cycle CPWM signal and CHnF bit is not set even when there is the channel (n) match. This implies that the usable range of periods set by MODH:L is 0x0001 through 0x7FFE, or 0x7FFF if you do not need to generate a 100% duty cycle CPWM signal. This is not a significant limitation because the resulting period is much longer than required for normal applications.

The CPWM mode must not be used when the FTM counter is a free running counter.

Note

- CPWM mode is available only with (CNTINH:L = 0x0000).
- CPWM mode with (CNTINH:L ≠ 0x0000) is not recommended and its results are not guaranteed.

12.4.8 Combine mode

The combine mode is selected when all of the following apply:

- (FTMEN = 1)
- (DECAPEN = 0)
- (COMBINE = 1)
- (CPWMS = 0)

In combine mode, the even channel (n) and adjacent odd channel (n+1) are combined to generate a PWM signal in the channel (n) output.

In the combine mode, the PWM period is determined by (MODH:L – CNTINH:L + 0x0001) and the PWM pulse width (duty cycle) is determined by (|C(n+1)VH:L – C(n)VH:L|).

The CHnF bit is set and the channel (n) interrupt is generated (if CHnIE = 1) at the channel (n) match (FTM counter = C(n)VH:L). The CH(n+1)F bit is set and the channel (n+1) interrupt is generated (if CH(n+1)IE = 1) at the channel (n+1) match (FTM counter = C(n+1)VH:C(n+1)VL).

If (ELSnB:ELSnA = 1:0), then the channel (n) output is forced low at the beginning of the period (FTM counter = CNTINH:L) and at the channel (n+1) match (FTM counter = C(n+1)VH:L). It is forced high at the channel (n) match (FTM counter = C(n)VH:L). See the following figure.

If (ELSnB:ELSnA = X:1), then the channel (n) output is forced high at the beginning of the period (FTM counter = CNTINH:L) and at the channel (n+1) match (FTM counter = C(n+1)VH:L). It is forced low at the channel (n) match (FTM counter = C(n)VH:L). See the following figure.

In combine mode, the ELS(n+1)B and ELS(n+1)A bits are not used in the generation of the channels (n) and (n+1) output.

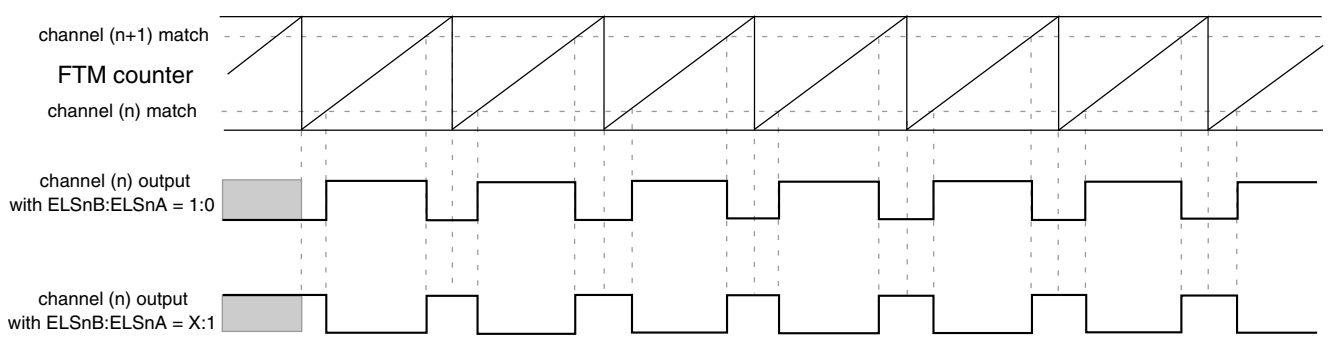


Figure 12-21. Combine mode

The following figures illustrate the generation of PWM signals using combine mode.

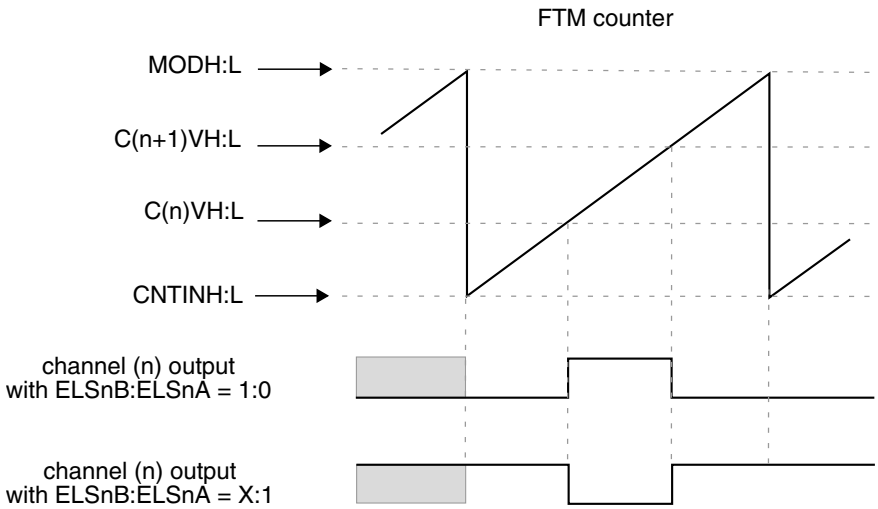


Figure 12-22. Channel (n) output if (CNTIN < C(n)V < MOD) and (CNTIN < C(n+1)V < MOD) and (C(n)V < C(n+1)V)

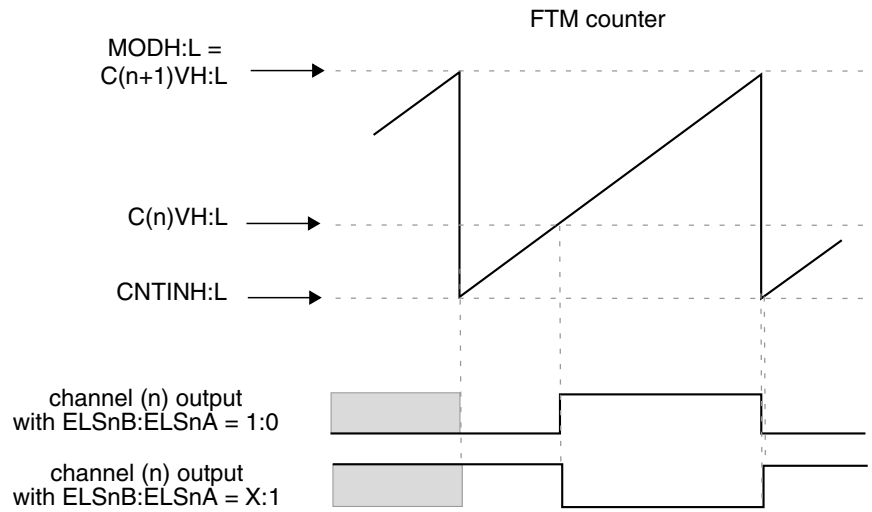


Figure 12-23. Channel (n) output if (CNTIN < C(n)V < MOD) and (C(n+1)V = MOD)

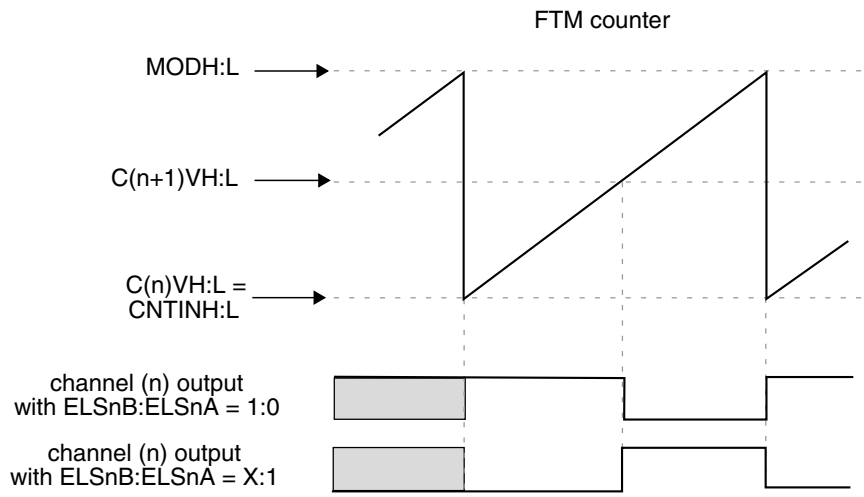


Figure 12-24. Channel (n) output if (C(n)V = CNTIN) and (CNTIN < C(n+1)V < MOD)

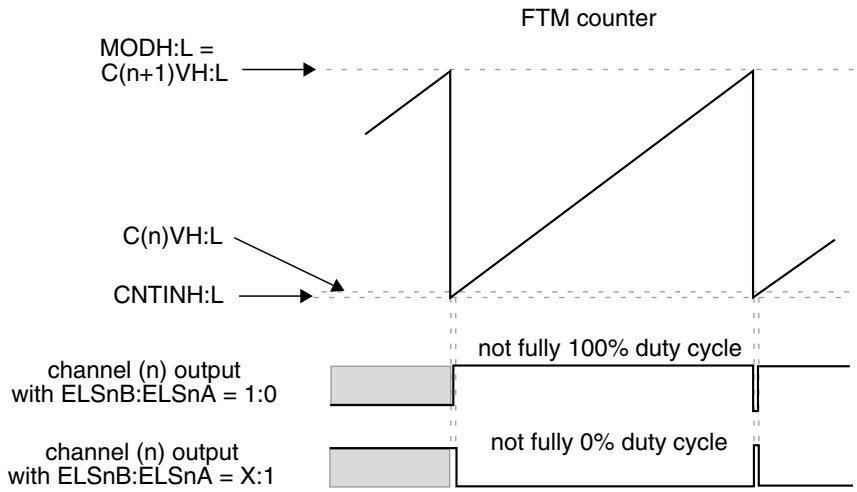


Figure 12-25. Channel (n) output if (CNTIN < C(n)V < MOD) and (C(n)V is almost equal to CNTIN) and (C(n+1)V = MOD)

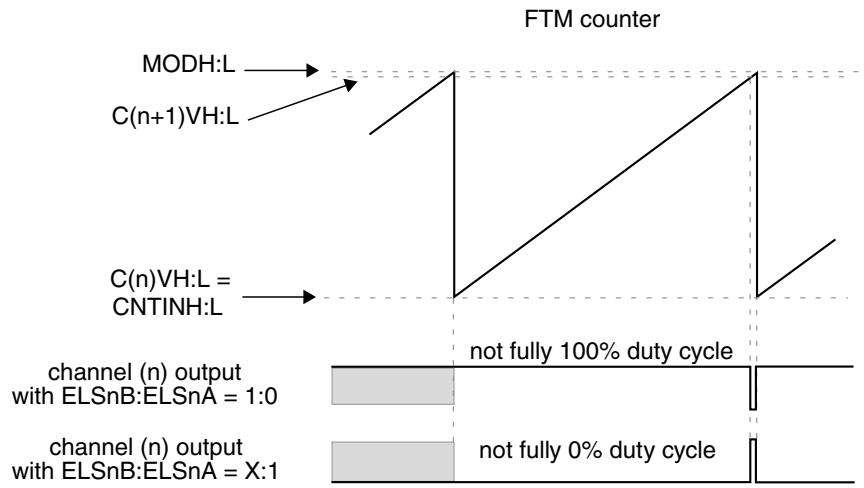


Figure 12-26. Channel (n) output if (C(n)V = CNTIN) and (CNTIN < C(n+1)V < MOD) and (C(n+1)V is almost equal to MOD)

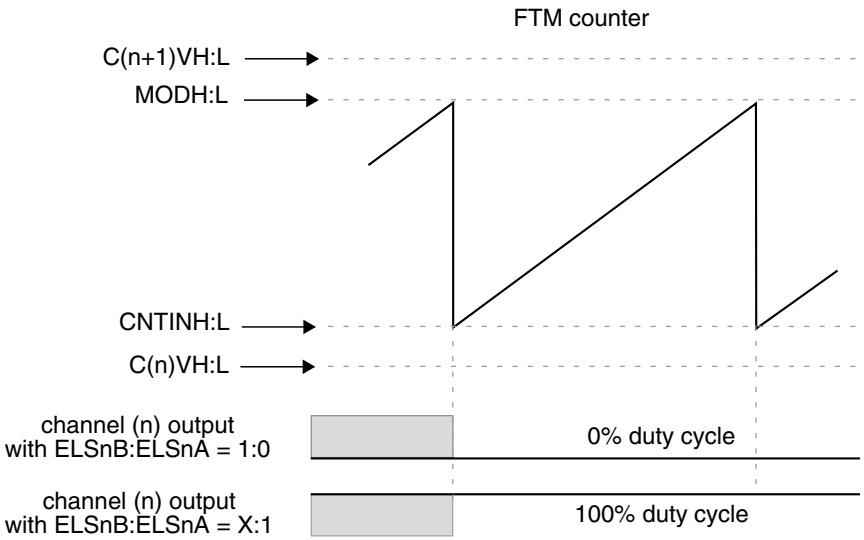


Figure 12-27. Channel (n) output if C(n)V and C(n+1)V are not between CNTIN and MOD

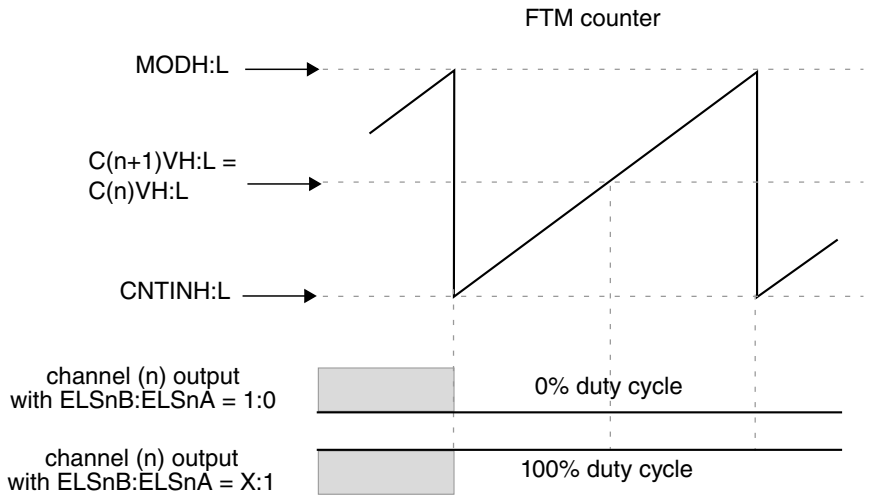


Figure 12-28. Channel (n) output if (CNTIN < C(n)V < MOD) and (CNTIN < C(n+1)V < MOD) and (CnV = C(n+1)V)

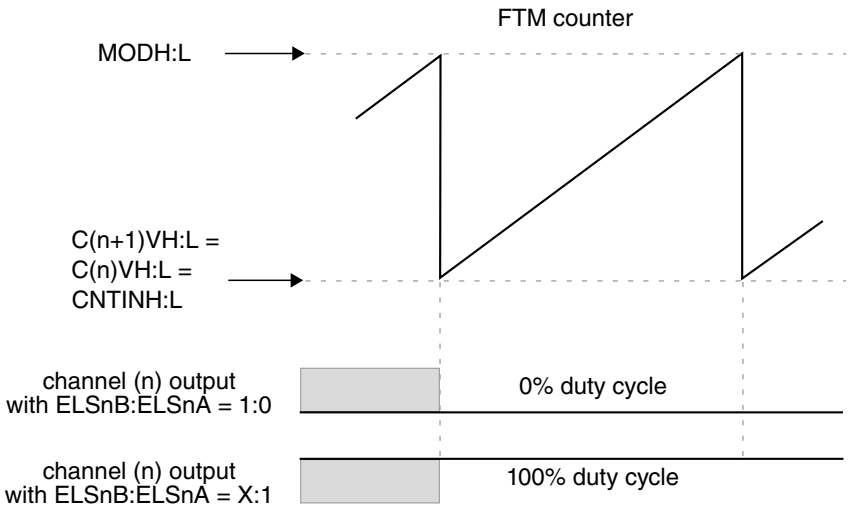


Figure 12-29. Channel (n) output if (C(n)V = C(n+1)V = CNTIN)

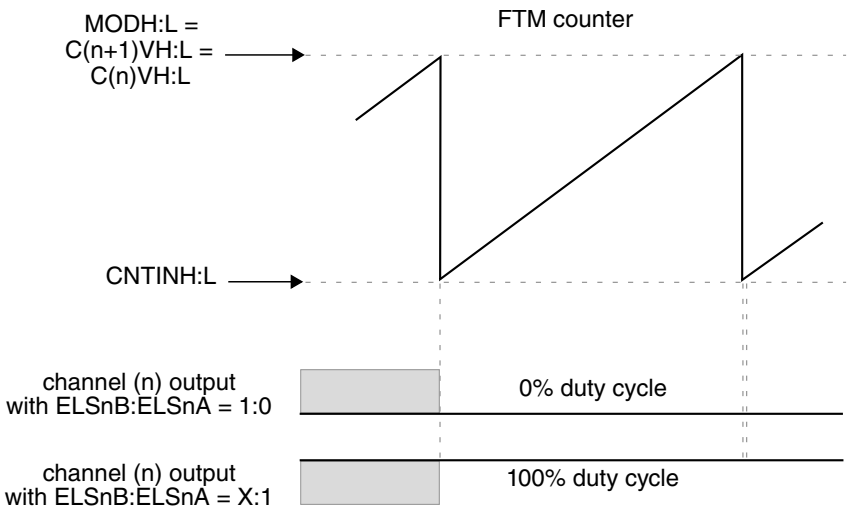


Figure 12-30. Channel (n) output if (C(n)V = C(n+1)V = MOD)

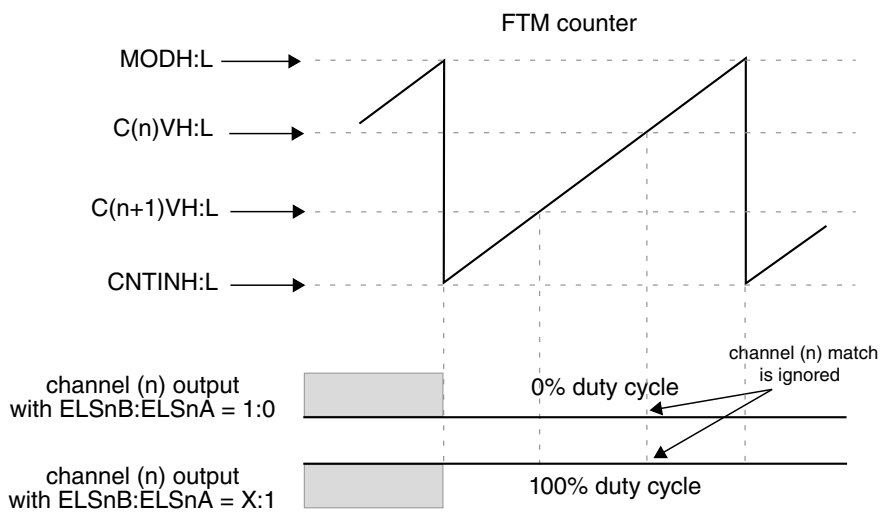


Figure 12-31. Channel (n) output if (CNTIN < C(n)V < MOD) and (CNTIN < C(n+1)V < MOD) and (C(n)V > C(n+1)V)

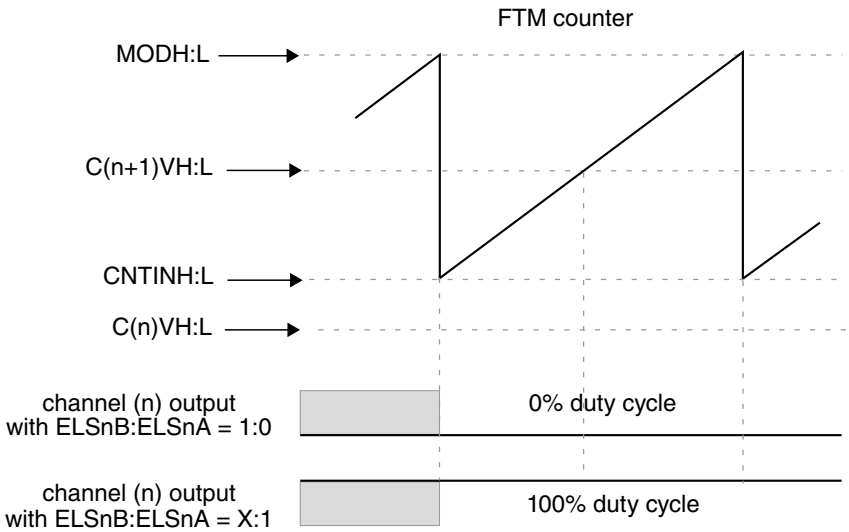


Figure 12-32. Channel (n) output if (C(n)V < CNTIN) and (CNTIN < C(n+1)V < MOD)

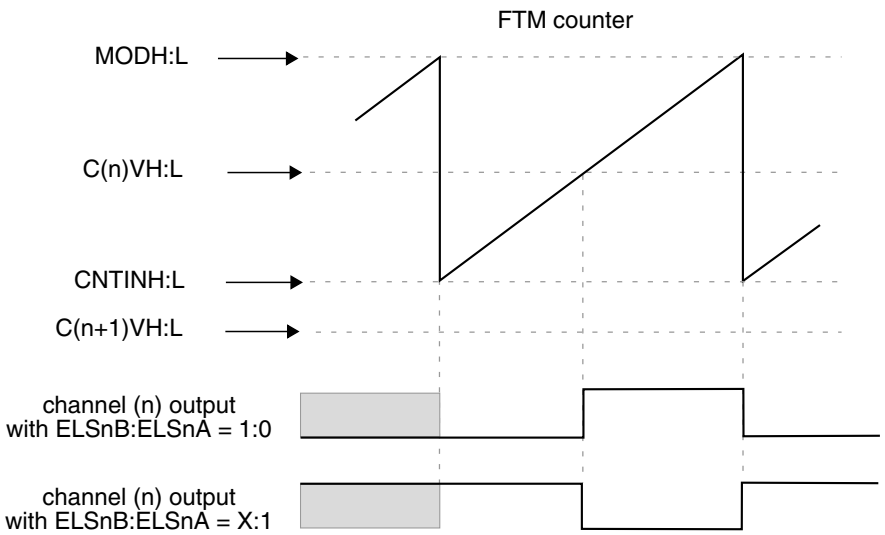


Figure 12-33. Channel (n) output if (C(n+1)V < CNTIN) and (CNTIN < C(n)V < MOD)

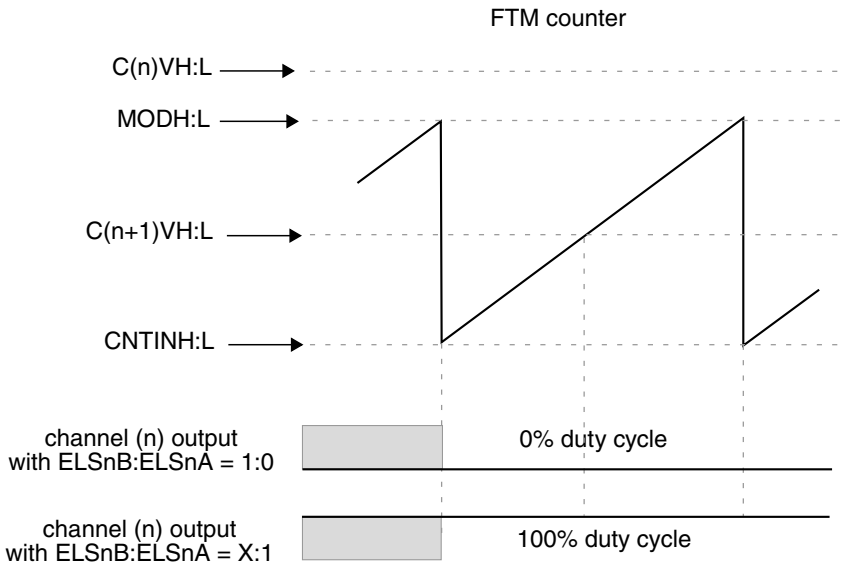


Figure 12-34. Channel (n) output if (C(n)V > MOD) and (CNTIN < C(n+1)V < MOD)

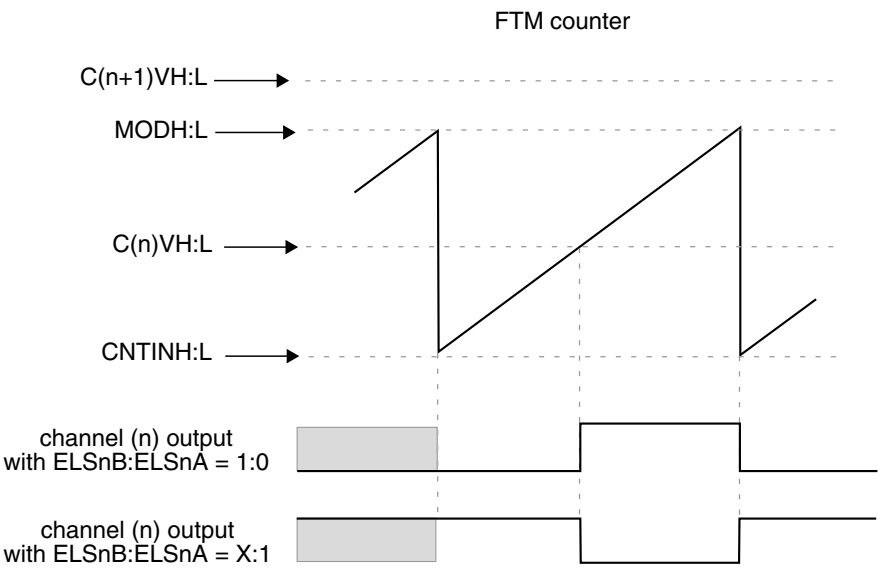


Figure 12-35. Channel (n) output if (C(n+1)V > MOD) and (CNTIN < C(n)V < MOD)

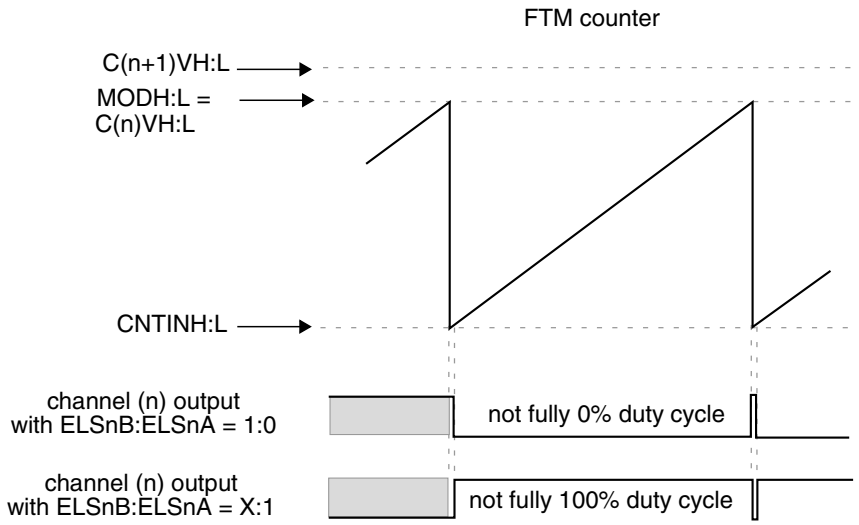


Figure 12-36. Channel (n) output if (C(n+1)V > MOD) and (CNTIN < C(n)V = MOD)

12.4.8.1 Asymmetrical PWM

In the combine mode, the control of the PWM signal first edge (when the channel (n) match occurs, that is, FTM counter = C(n)VH:L) is independent of the control of the PWM signal second edge (when the channel (n+1) match occurs, that is, FTM counter = C(n+1)VH:L). So, the combine mode allows to generate asymmetrical PWM signals.

12.4.9 Complementary mode

The complementary mode is selected when all of the following apply:

- (FTMEN = 1)
- (DECAPEN = 0)
- (COMBINE = 1)
- (CPWMS = 0)
- (COMP = 1)

In complementary mode the channel (n+1) output is the inverse of the channel (n) output.

The channel (n+1) output is the same as the channel (n) output if all of the following apply:

- (FTMEN = 1)
- (DECAPEN = 0)
- (COMBINE = 1)
- (CPWMS = 0)
- (COMP = 0)

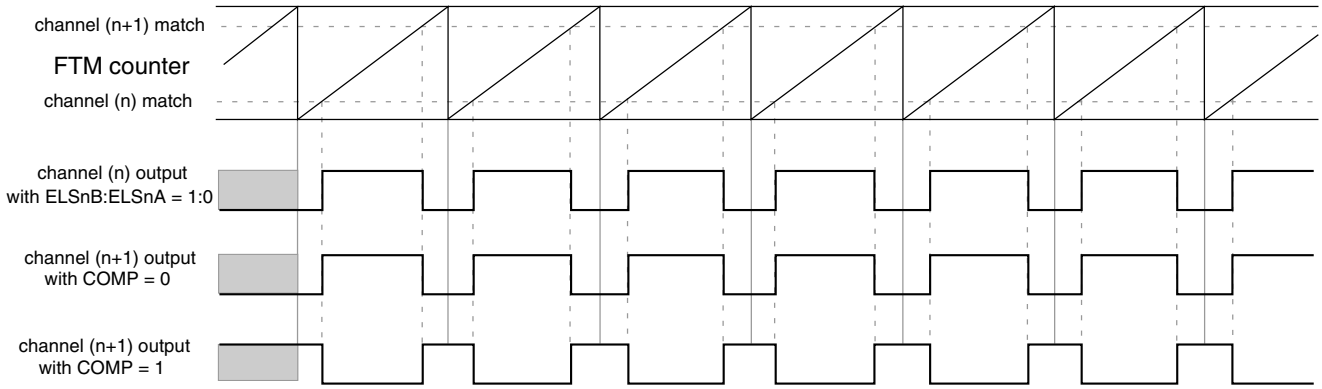


Figure 12-37. Channel (n+1) output in complementary mode with (ELSnB:ELSnA = 1:0)

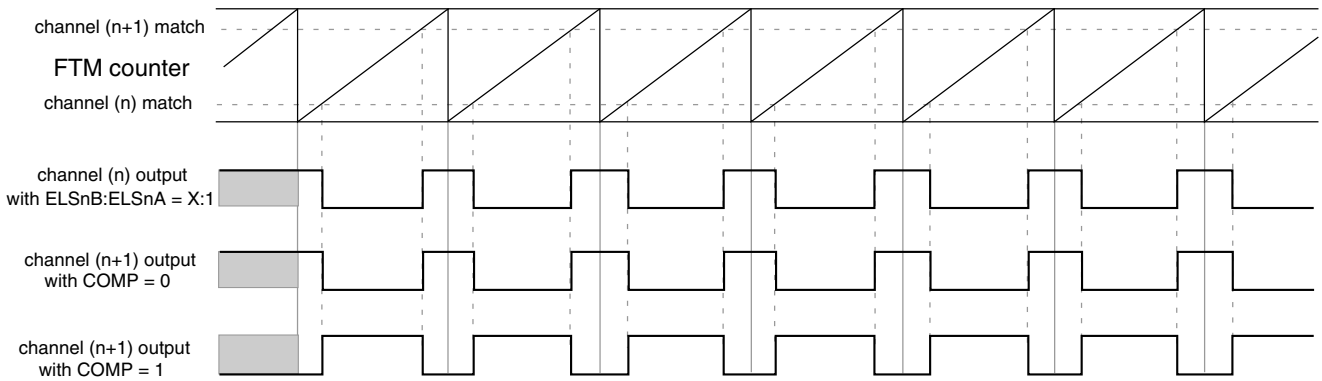


Figure 12-38. Channel (n+1) output in complementary mode with (ELSnB:ELSnA = X:1)

12.4.10 Update of the registers with write buffers

This section describes the updating of registers that have write buffers.

12.4.10.1 CNTINH:L registers

CNTINH:L registers are always updated with their write buffer after both bytes have been written.

12.4.10.2 MODH:L registers

If (CLKS[1:0] = 0:0), then MODH:L registers are updated when their second byte is written, independent of FTMEN bit.

If (CLKS[1:0] ≠ 0:0 and FTMEN = 0), then MODH:L registers are updated according to the CPWMS bit:

- If the selected mode is not CPWM mode, then MODH:L registers are updated after both bytes have been written and the FTM counter changes from (MODH:L) to (CNTINH:L). If the FTM counter is a free-running counter, then this update is made when the FTM counter changes from 0xFFFF to 0x0000.
- If the selected mode is CPWM mode, then MODH:L registers are updated after both bytes have been written and the FTM counter changes from MODH:L to (MODH:L – 0x0001).

If (CLKS[1:0] ≠ 0:0 and FTMEN = 1), then MODH:L registers are updated by PWM synchronization. See MODH:L registers synchronization.

12.4.10.3 CnVH:L registers

If (CLKS[1:0] = 0:0), then CnVH:L registers are updated when their second byte is written, independent of FTMEN bit.

If (CLKS[1:0] ≠ 0:0 and FTMEN = 0), then CnVH:L registers are updated according to the selected mode:

- If the selected mode is output compare mode, then CnVH:L registers are updated after their second byte is written and on the next change of the FTM counter.
- If the selected mode is EPWM mode, the CnVH:L registers are updated after both bytes have been written and the FTM counter changes from MODH:L to CNTINH:L. If the FTM counter is a free running counter, then this update is made when the FTM counter changes from 0xFFFF to 0x0000.
- If the selected mode is CPWM mode, then CnVH:L registers are updated after both bytes have been written and the FTM counter changes from MODH:L to (MODH:L – 0x0001).

If (CLKS[1:0] ≠ 0:0 and FTMEN = 1), then CnVH:L registers are updated according to the selected mode:

- If the selected mode is output compare mode, then CnVH:L registers are updated according to the SYNCEN bit. If (SYNCEN = 0), then CnVH:L registers are updated after their second byte is written and on the next change of the FTM counter. If (SYNCEN = 1), then CnVH:L registers are updated by PWM synchronization. See CnVH:L registers synchronization.
- If the selected mode is not output compare mode and (SYNCEN = 1), then CnVH:L registers are updated by PWM synchronization. See CnVH:L registers synchronization.

12.4.11 PWM synchronization

PWM synchronization provides an opportunity to update registers with the contents of their write buffers. It can also be used to synchronize two or more FlexTimer modules on the same MCU.

PWM synchronization updates the MODH:L and CnVH:L registers with their write buffers. It is also possible to force the FTM counter to its initial value and update the CHnOM bits in OUTMASK using PWM synchronization.

Note

PWM synchronization is available only in combine mode.

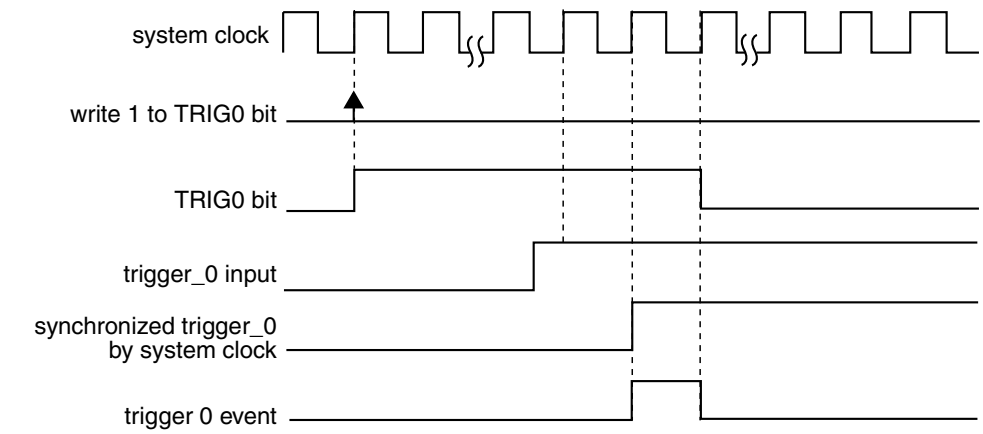
12.4.11.1 Hardware trigger

Each hardware trigger is synchronized by the system clock. The input signals are: trigger_0, trigger_1, and trigger_2.

A rising edge on the selected hardware trigger input (trigger n event) initiates PWM synchronization. A hardware trigger is selected when its enable bit is set (TRIGn = 1 where n = 0, 1, or 2). The TRIGn bit is cleared when 0 is written to it or when the trigger n event is detected.

For example, if TRIG0 and TRIG1 are enabled and only the trigger 1 event occurs, only the TRIG1 bit is cleared.

If a trigger n event occurs together with a write to set the TRIGn bit, then the synchronization is made, but the TRIGn bit remains set because of the last write.



Notes
- All hardware trigger (input signals: trigger_0, trigger_1, and trigger_2) have this same behavior

Figure 12-39. Hardware trigger event

12.4.11.2 Software trigger

A software trigger event occurs when 1 is written to the SWSYNC bit. The SWSYNC bit is cleared when 0 is written to it or when the PWM synchronization, which is initiated by the software event, is completed.

If the software trigger event occurs together with the event that clears the SWSYNC bit, then the synchronization is made using this trigger event and the SWSYNC bit remains set because of the last write.

For example, if PWMSYNC = 0 and REINIT = 0 and there is a software trigger event, then the load of MODH:L and CnVH:L registers is made only at the boundary cycle (CNTMIN and CNTMAX). In this case, the SWSYNC bit is cleared only at the boundary cycle, so you do not know when this bit is cleared. Therefore, it is possible a new write to set SWSYNC happens when FTM is clearing the SWSYNC because it is the selected boundary cycle of PWM synchronization that was started previously by the software trigger event.

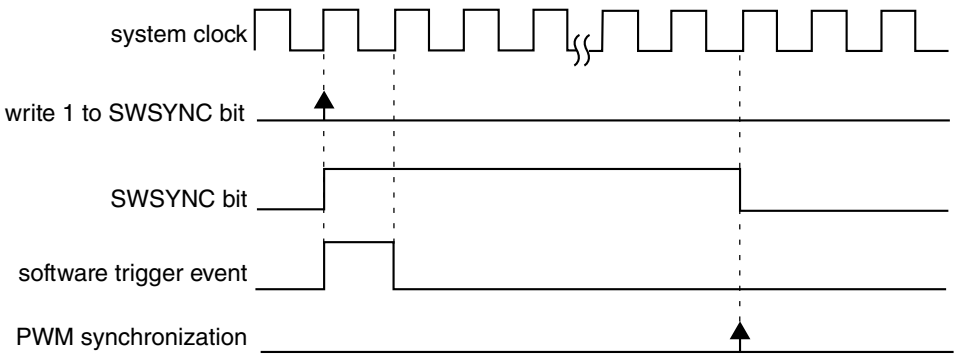


Figure 12-40. Software Trigger event

12.4.11.3 Boundary cycle

The CNTMAX and CNTMIN bits select the boundary cycle when the MODH:L and CnVH:L registers are updated with the value of their write buffer by PWM synchronization, except if (PWMSYNC = 0 and REINIT = 1).

If CNTMIN = 1, then the boundary cycle is the CNTINH:L value. MODH:L and CnVH:L registers are updated when the FTM counter reaches the CNTINH:L value. If CPWMS = 0, then CNTINH:L is reached when the FTM counter changes from MODH:L to CNTINH:L. If CPWMS = 1, then CNTINH:L is reached when the FTM counter changes from (CNTINH:L + 0x0001) to CNTINH:L.

If CNTMAX = 1, then the boundary cycle is the MODH:L value. MODH:L and CnVH:L registers are updated when the FTM counter reaches the MODH:L value. MODH:L is reached when the FTM counter changes from (MODH:L – 0x0001) to MODH:L, regardless of the CPWMS configuration.

If no boundary cycle was selected (CNTMAX = 0 and CNTMIN = 0), then the update of the MODH:L and CnVH:L registers is not made, unless (PWMSYNC = 0 and REINIT = 1).

If both boundary cycles were selected (CNTMAX = 1 and CNTMIN = 1), then the update of the MODH:L and CnVH:L registers is made in the first boundary cycle that occurs with valid conditions for MODH:L or CnVH:L synchronization, except if (PWMSYNC = 0 and REINIT = 1).

The CNTMAX and CNTMIN bits are cleared only by software.

Note

- PWM synchronization boundary cycle is available only when (CNTMIN = 1).
- PWM synchronization with (CNTMAX = 1) is not recommended and its results are not guaranteed.

12.4.11.4 MODH:L registers synchronization

The MODH:L synchronization occurs when the MODH:L registers are updated with the value of their write buffer.

The synchronization requires both bytes of MODH:L to have been written in one of the following situations.

- If PWMSYNC = 0 and REINIT = 0, then the synchronization is made on the next selected boundary cycle after an enabled trigger event takes place. If the trigger event was a software trigger, then the SWSYNC bit is cleared on the next selected boundary cycle. See the following figure.

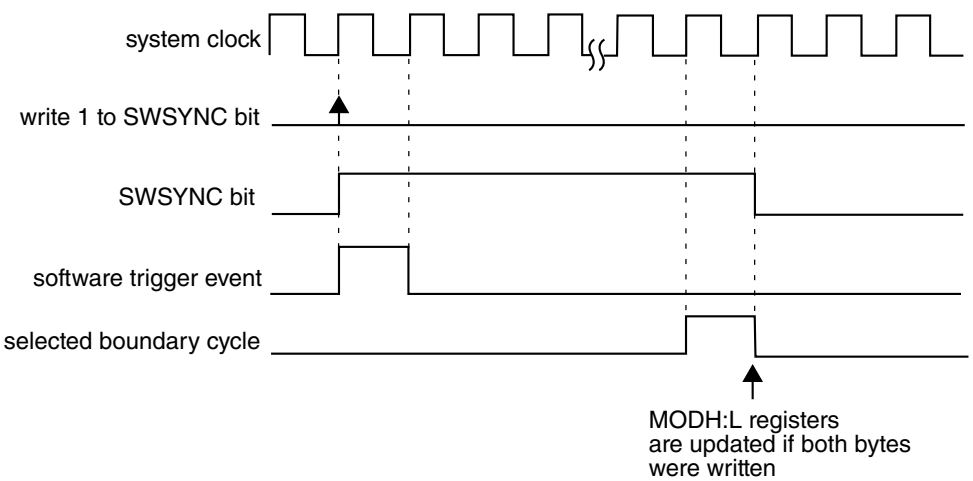


Figure 12-41. MODH:L synchronization when (PWMSYNC = 0), (REINIT = 0), and software trigger was used

If the trigger event was a hardware trigger, then the trigger enable bit (TRIGn) is cleared when the trigger n event is detected. See the following figure.

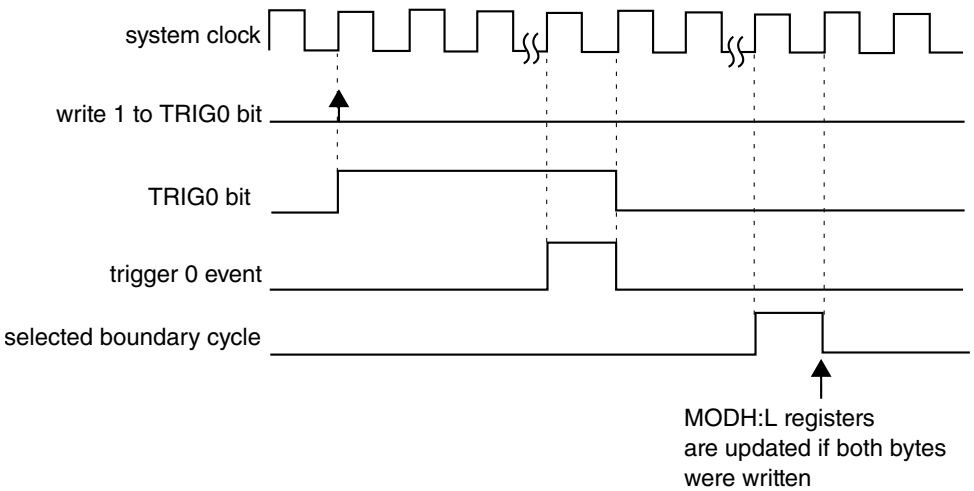


Figure 12-42. MODH:L synchronization when (PWMSYNC = 0), (REINIT = 0), and a hardware trigger was used

- If PWMSYNC = 0 and REINIT = 1, then the synchronization is made on the next enabled trigger event. If the trigger event was a software trigger, then the SWSYNC bit is cleared. See the following figure.

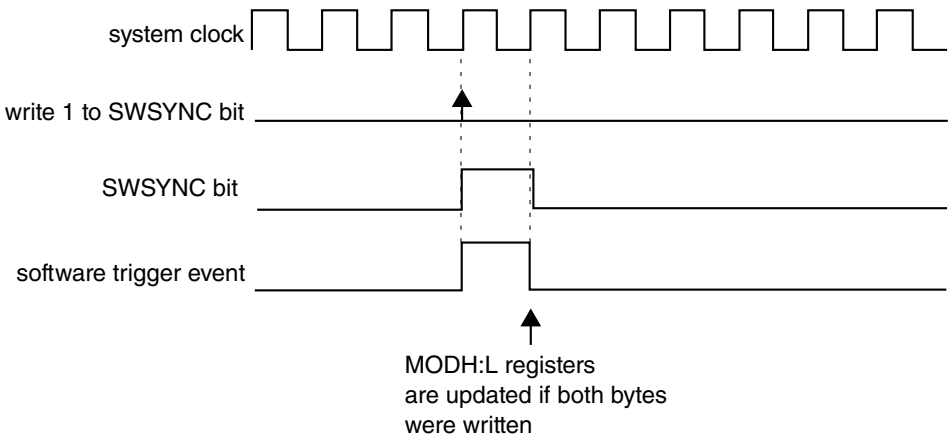


Figure 12-43. MODH:L synchronization when (PWMSYNC = 0), (REINIT = 1), and software trigger was used

If the trigger event was a hardware trigger, then the TRIGn bit is cleared. See the following figure.

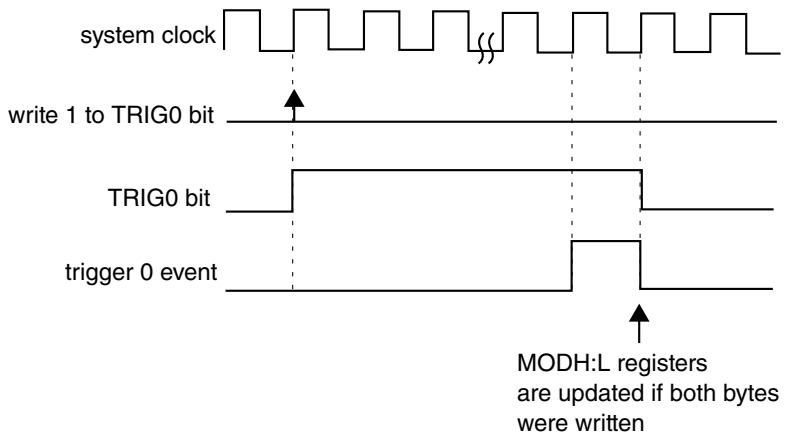


Figure 12-44. MODH:L synchronization when (PWMSYNC = 0), (REINIT = 1), and a hardware trigger was used

- If PWMSYNC = 1, then the synchronization is made on the next selected boundary cycle after the enabled software trigger event takes place. The SWSYNC bit is cleared on the next selected boundary cycle. See the following figure.

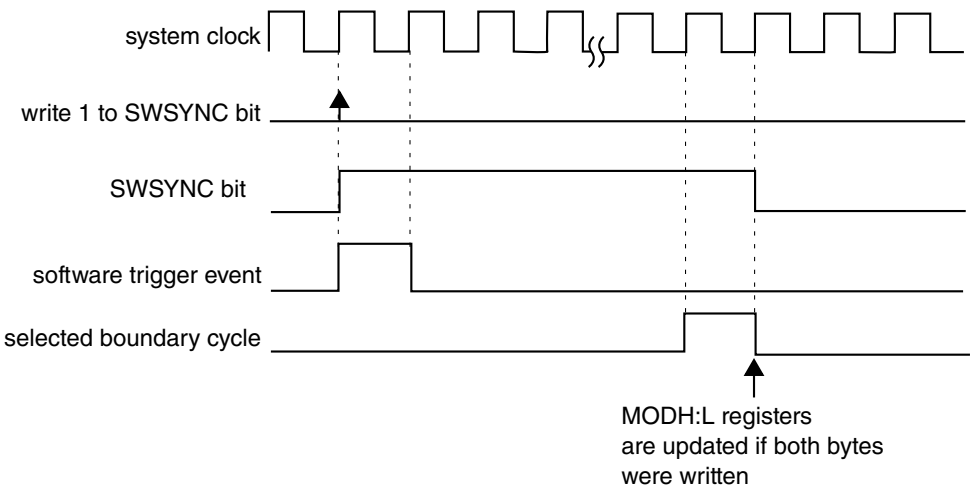


Figure 12-45. MODH:L synchronization when (PWMSYNC = 1)

12.4.11.5 CnVH:L registers synchronization

The CnVH:L synchronization occurs when the CnVH:L registers are updated with the value of their write buffer.

The synchronization requires both bytes of CnVH:L to have been written, SYNCEN = 1 and either a hardware or software trigger event as per MODH:L registers synchronization.

12.4.11.6 OUTMASK register synchronization

Any write to a CHnOM bit updates the OUTMASK write buffer. The CHnOM bit is updated with the value of its corresponding bit in the OUTMASK write buffer according to SYNCHOM and PWMSYNC bits.

- If SYNCHOM = 0, then the CHnOM bit is updated with the value of its write buffer equivalent in all rising edges of the system clock.

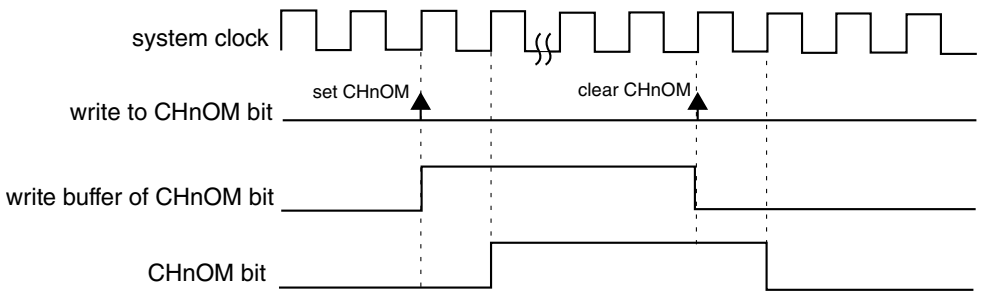


Figure 12-46. CHnOM synchronization when (SYNCHOM = 0)

- If SYNCHOM = 1 and PWMSYNC = 0, then this synchronization is made on the next enabled trigger event. If the trigger event was a software trigger, then the SWSYNC bit is cleared on the next selected boundary cycle. See the following figure.

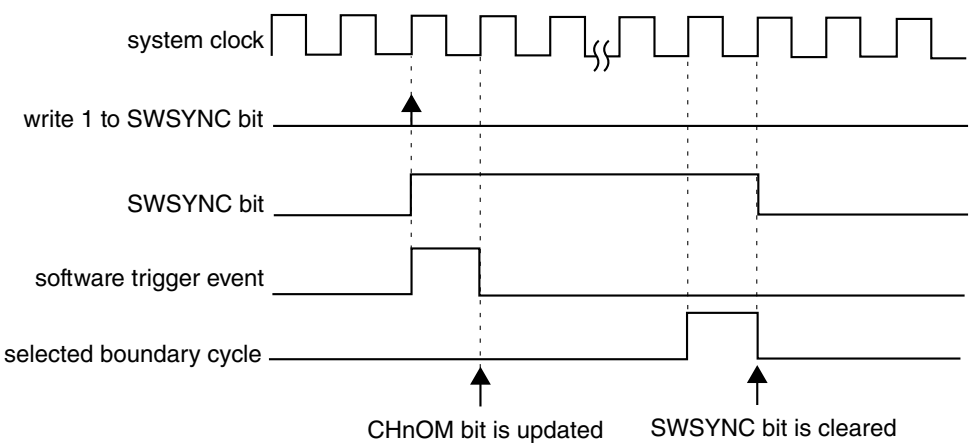


Figure 12-47. CHnOM synchronization when (SYNCHOM = 1), (PWMSYNC = 0) and software trigger was used

If the trigger event was a hardware trigger, then the trigger enable bit (TRIGn) is cleared when the trigger n event is detected. See the following figure.

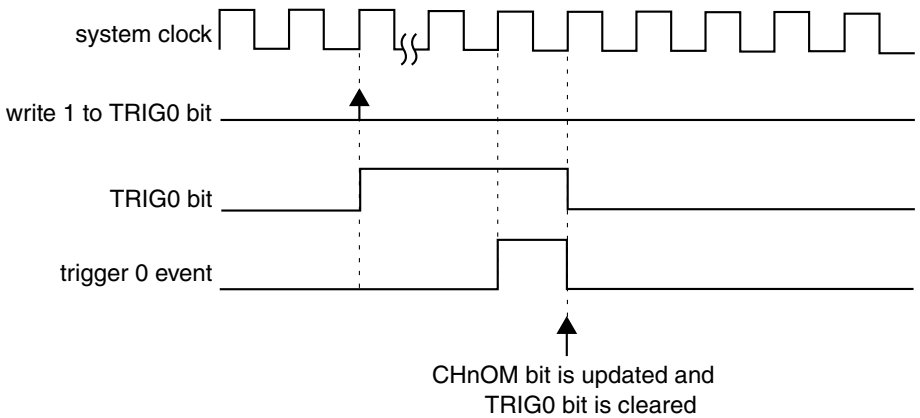


Figure 12-48. CHnOM synchronization when (SYNCHOM = 1), (PWMSYNC = 0), and a hardware trigger was used

- If SYNCHOM = 1 and PWMSYNC = 1, then this synchronization is made on the next enabled hardware trigger event. The trigger enable bit (TRIGn) is cleared when the enabled hardware trigger n event is detected. See the following figure.

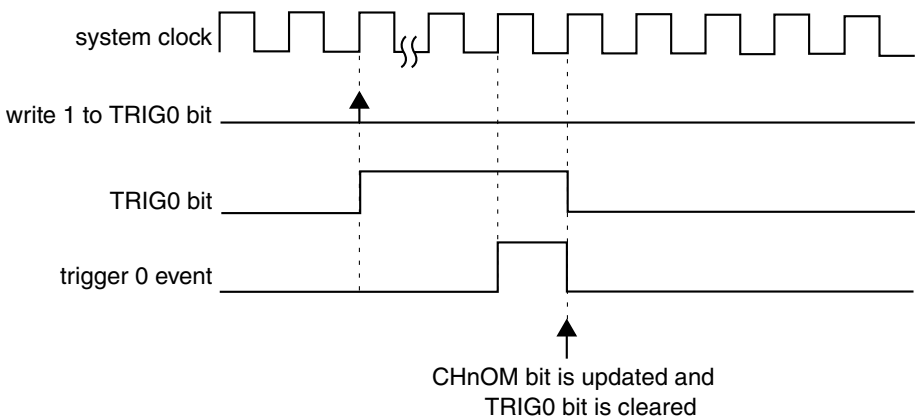


Figure 12-49. CHnOM Synchronization when (SYNCHOM = 1), (PWMSYNC = 1), and a hardware trigger was used

12.4.11.7 FTM counter synchronization

The FTM counter synchronization occurs when the FTM counter is updated with the value of the CNTINH:L registers and the channel outputs are forced to their initial value as defined by the channel configuration.

- If REINIT = 0, then this synchronization is made when the FTM counter changes from MODH:L to CNTINH:L.
- If REINIT = 1 and PWMSYNC = 0, then this synchronization is made on the next enabled trigger event. If the trigger event was a software trigger, then the SWSYNC bit is cleared. See the following figure.

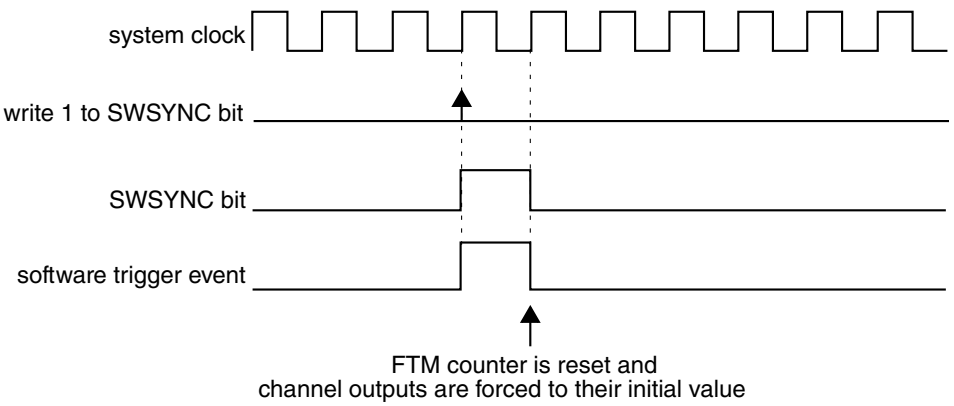


Figure 12-50. FTM counter synchronization when (REINIT = 1), (PWMSYNC = 0), and software trigger was used

If the trigger event was a hardware trigger, then the TRIGn bit is cleared. See the following figure.

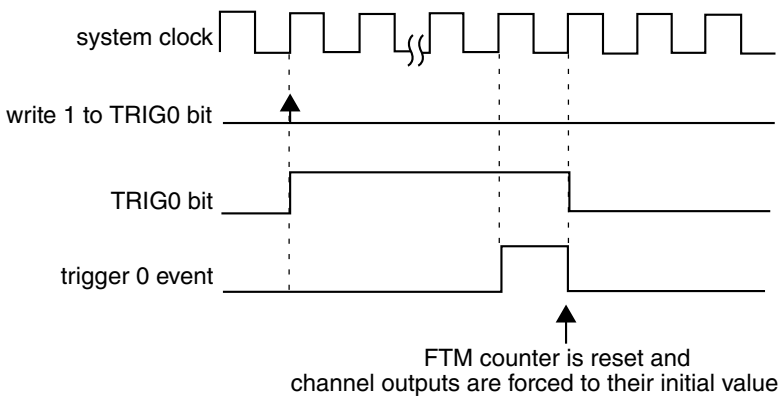


Figure 12-51. FTM counter synchronization when (REINIT = 1), (PWMSYNC = 0), and a hardware trigger was used

- If REINIT = 1 and PWMSYNC = 1, then this synchronization is made on the next enabled hardware trigger event. The trigger enable bit (TRIGn) is cleared when the enabled hardware trigger n event is detected. See the following figure.

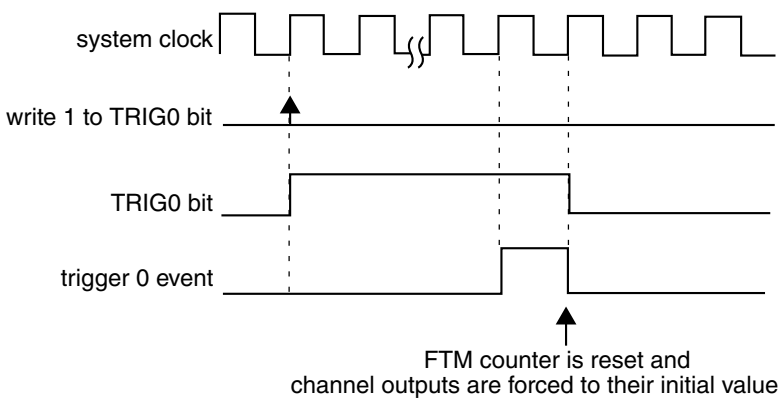


Figure 12-52. FTM counter synchronization when (REINIT = 1), (PWMSYNC = 1), and a hardware trigger was used

12.4.11.8 Summary of PWM synchronization

The following table shows the summary of PWM synchronization.

Table 12-4. Summary of PWM synchronization

Register or bit	PWMSYNC	REINIT	SYNCHOM	CNTMAX	CNTMIN	SYNCEN	Description
CNTINH:L	X	X	X	X	X	X	Changes take effect after the second byte is written. Effect is seen after the next TOF or PWM synchronization.
MODH:L	0	0	X	1	0	X	MODH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled hardware or software trigger has occurred.
	0	0	X	0	1	X	MODH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled hardware or software trigger has occurred.
	0	1	X	X	X	X	MODH:L are updated with their write buffer contents when the enabled hardware or software trigger occurs.
	1	X	X	1	0	X	MODH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled software trigger has occurred.
	1	X	X	0	1	X	MODH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled software trigger has occurred.
CnVH:L	0	0	X	1	0	1	CnVH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled hardware or software trigger has occurred.
	0	0	X	0	1	1	CnVH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled hardware or software trigger has occurred.
	0	1	X	X	X	1	CnVH:L are updated with their write buffer contents when the enabled hardware or software trigger occurs.

Table continues on the next page...

Table 12-4. Summary of PWM synchronization (continued)

Register or bit	PWMSYNC	REINIT	SYNCHOM	CNTMAX	CNTMIN	SYNCEN	Description
	1	X	X	1	0	1	CnVH:L are updated with their write buffer contents when the counter reaches its maximum value after the enabled software trigger has occurred.
	1	X	X	0	1	1	CnVH:L are updated with their write buffer contents when the counter reaches its minimum value after the enabled software trigger has occurred.
CNTH:L	0	1	X	X	X	X	CNTH:L are forced to the FTM counter initial value when the enabled hardware or software trigger occurs.
	1	1	X	X	X	X	CNTH:L are forced to the FTM counter initial value when the enabled hardware trigger occurs.
OUTMASK	X	X	0	X	X	X	Changes to OUTMASK take effect on the next rising edge of the system clock.
	0	X	1	X	X	X	OUTMASK is updated with its write buffer contents when the enabled hardware or software trigger occurs.
	1	X	1	X	X	X	OUTMASK is updated with its write buffer contents when the enabled hardware trigger occurs.
SWSYNC bit	0	0	X	1	0	X	SWSYNC bit is cleared when the counter reaches its maximum value after the enabled software trigger has occurred.
	0	0	X	0	1	X	SWSYNC bit is cleared when the counter reaches its minimum value after the enabled software trigger has occurred.
	0	1	X	X	X	X	SWSYNC bit is cleared when the enabled software trigger occurs.
	1	X	X	1	0	X	SWSYNC bit is cleared when the counter reaches its maximum value after the enabled software trigger has occurred.
	1	X	X	0	1	X	SWSYNC bit is cleared when the counter reaches its minimum value after the enabled software trigger has occurred.
TRIGn bit	X	X	X	X	X	X	TRIGn bit is cleared when the enabled hardware trigger has occurred.

12.4.12 Deadtime insertion

The deadtime insertion is enabled when (DTEN = 1) and (DTVAL[5:0] is non- zero).

DEADTIME register defines the deadtime delay that can be used for all FTM channels. The DTPS[1:0] bits define the prescaler for the system clock and the DTVAL[5:0] bits define the deadtime modulo; that is, the number of deadtime prescaler clocks).

The deadtime delay insertion ensures that no two complementary signals (channel (n) and (n+1)) drive the active state at the same time.

For POL(n) = 0, POL(n+1) = 0, and deadtime enabled, a rising edge on the output of channel (n) remains low for the duration of the deadtime delay, after which the rising edge appears on the output. Similarly, when a falling edge is due on the output of channel (n), the channel (n+1) output remains low for the duration of the deadtime delay, after which the channel (n+1) output will have a rising edge.

For POL(n) = 1, POL(n+1) = 1, and deadtime enabled, a falling edge on the output of channel (n) remains high for the duration of the deadtime delay, after which the falling edge appears on the output. Similarly, when a rising edge is due on the output of channel (n), the channel (n+1) output remains high for the duration of the deadtime delay, after which the channel (n+1) output will have a falling edge.

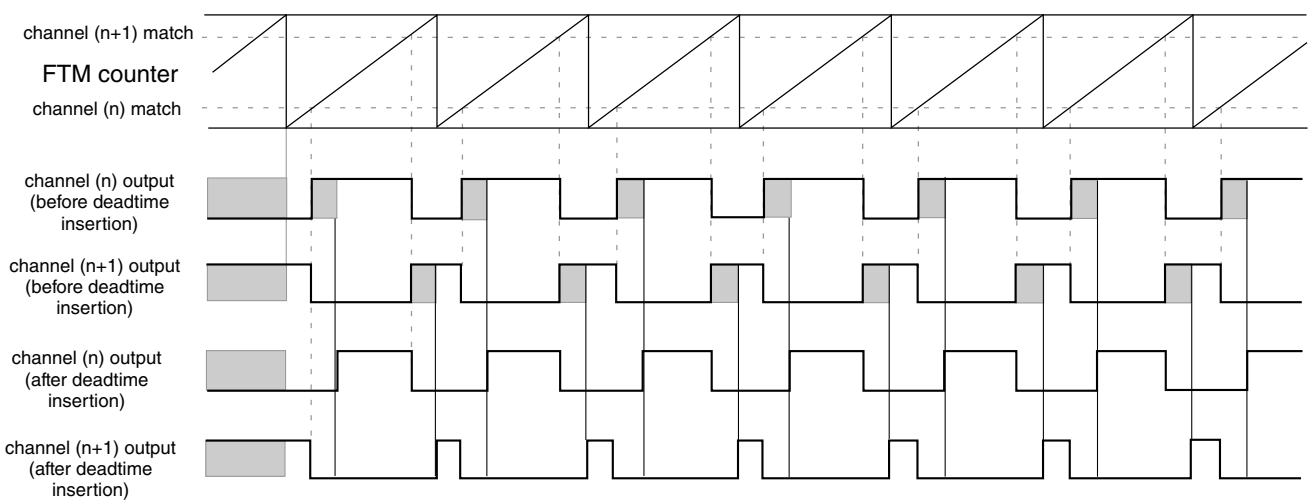


Figure 12-53. Deadtime insertion with ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 0

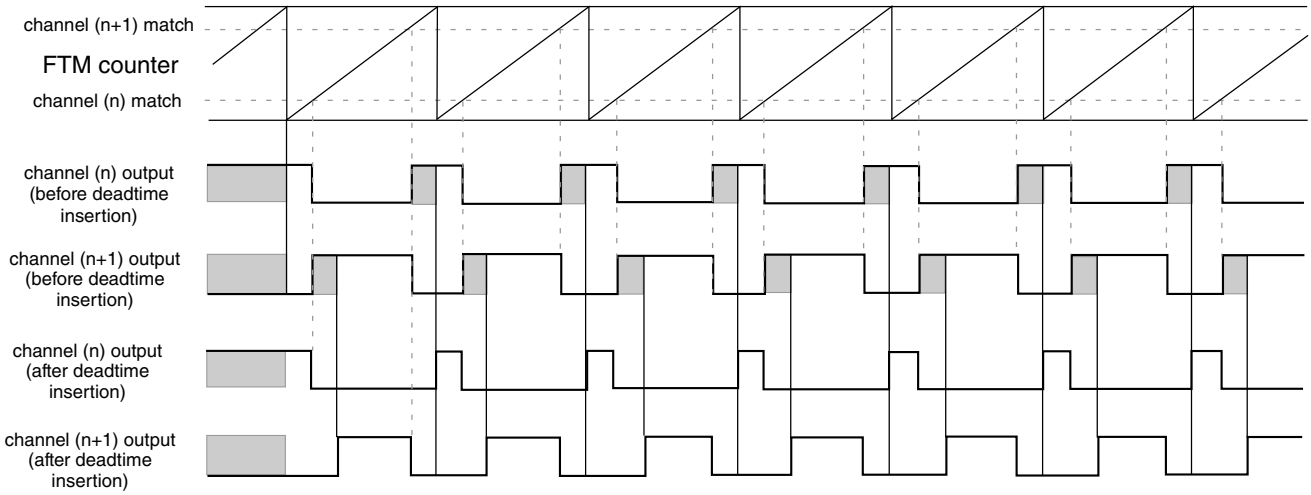


Figure 12-54. Deadtime insertion with ELSnB:ELSnA = X:1, POL(n) = 0, and POL(n+1) = 0

NOTE

Deadtime feature is available only in combine and complementary modes.

12.4.12.1 Deadtime insertion corner cases

If (PS[2:0] bits are cleared), (DTPS[1:0] = 0:0 or DTPS[1:0] = 0:1):

- and the deadtime delay is greater than or equal to the channel (n) duty cycle ((C(n +1)VH:L – C(n)VH:L) × system clock), then the channel (n) output is always the inactive value (POL(n) bit value).
- and the deadtime delay is greater than or equal to the channel (n+1) duty cycle ((MODH:L – CNTINH:L + 1 – (C(n+1)VH:L – C(n)VH:L)) × system clock), then the channel (n+1) output is always the inactive value (POL(n+1) bit value).

Although in most cases the deadtime delay is not comparable to channels (n) and (n+1) duty cycle, the following figures show examples where the deadtime delay is comparable to the duty cycle.

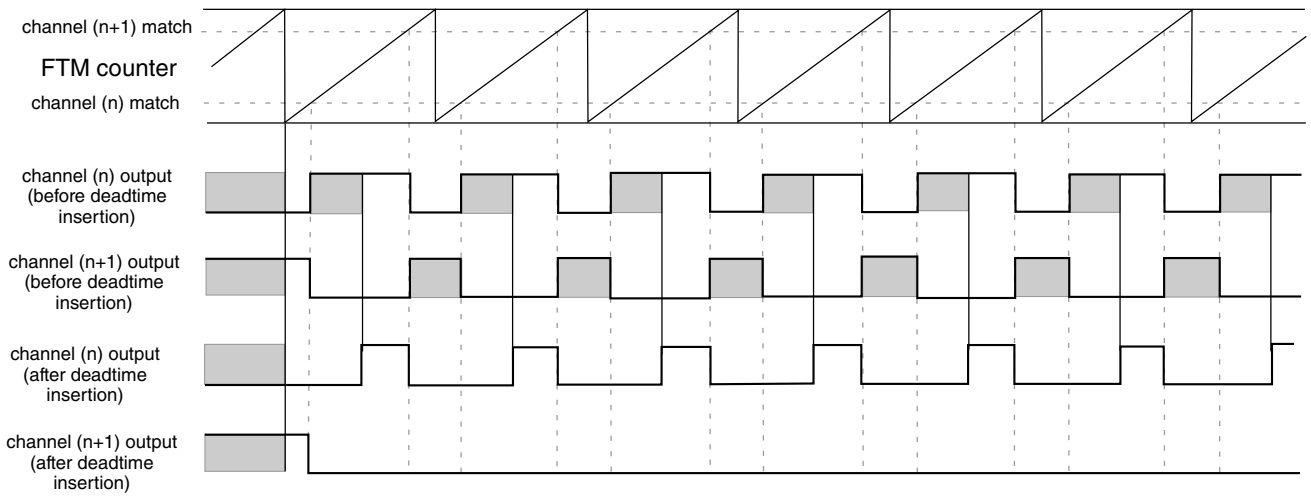


Figure 12-55. Example of the deadtime insertion (ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 0) when the deadtime delay is comparable to channel (n+1) duty cycle

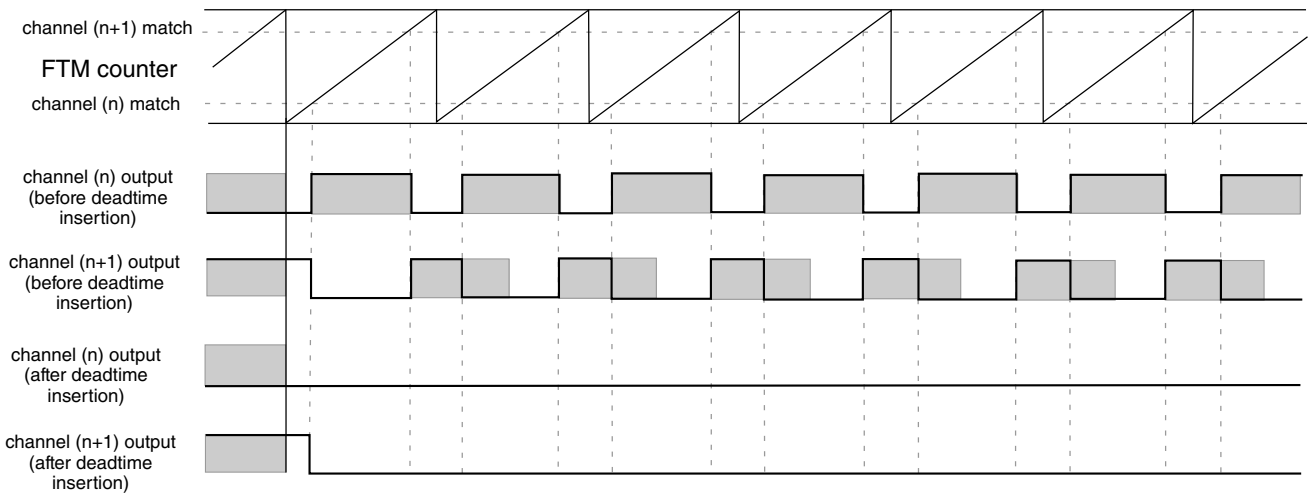


Figure 12-56. Example of the deadtime insertion (ELSnB:ELSnA = 1:0, POL(n) = 0, and POL(n+1) = 0) when the deadtime delay Is comparable to channels (n) and (n+1) duty cycle

12.4.13 Output mask

The output mask register OUTMASK can be used to force channel outputs to their inactive state through software; for example, to control a BLDC motor.

Any write to a CHnOM bit updates the OUTMASK write buffer. The CHnOM bit is updated with the value of its corresponding bit in the OUTMASK write buffer according to OUTMASK register synchronization.

If CHnOM = 1, then the channel (n) output is forced to its inactive state, defined by the POLn bit in register POL. If CHnOM = 0, then the channel (n) output is unaffected by the output mask function.

When a CHnOM bit is cleared, the channel (n) output is enabled. See the following figure.

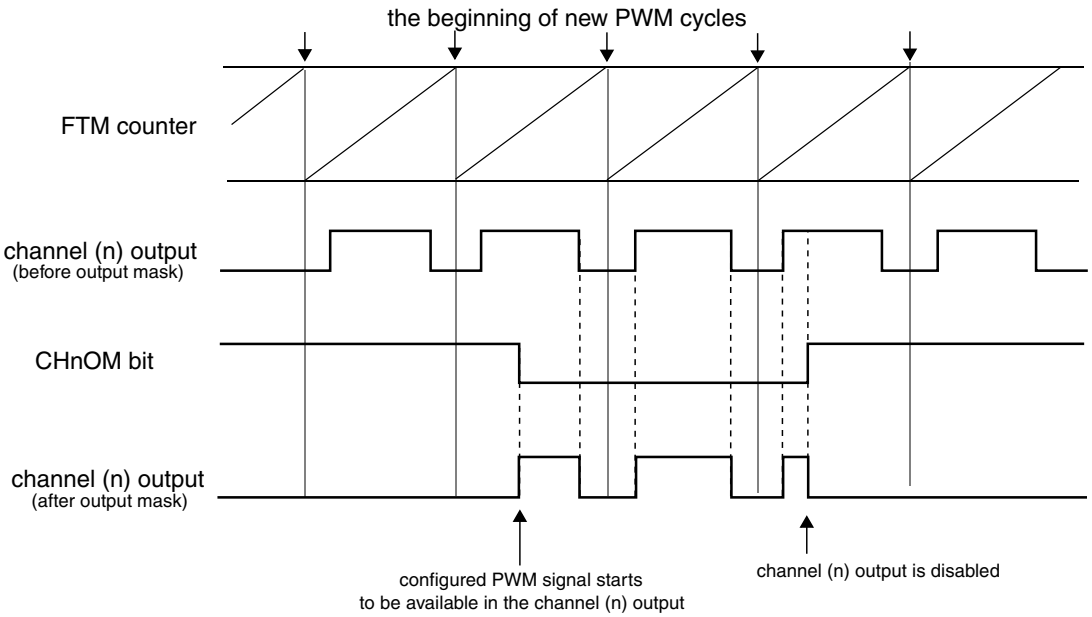


Figure 12-57. Output mask

The following table shows the output mask result before the polarity control.

Table 12-5. Output mask result for channel (n) before the polarity control

CHnOM	Output Mask Input	Output Mask Result
0	inactive state	inactive state
	active state	active state
1	inactive state	inactive state
	active state	

Note

Output mask is available only in combine mode.

12.4.14 Fault control

The fault control is enabled if (FTMEN = 1) and (FAULTM[1:0] ≠ 0:0).

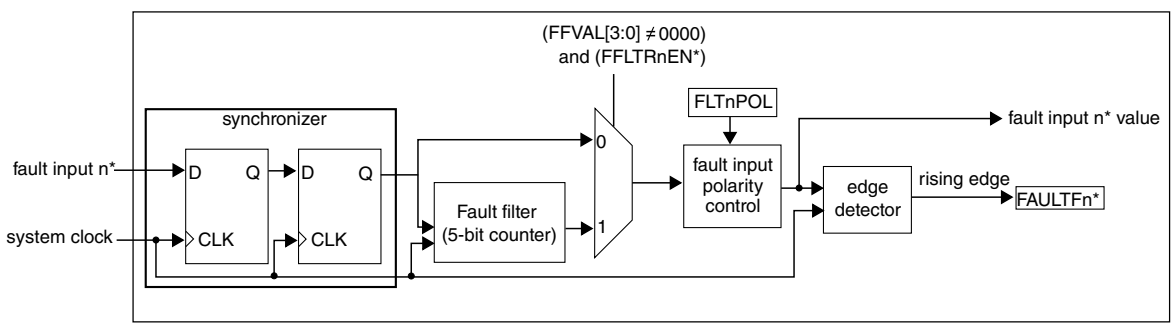
FTM can have up to four fault inputs. FAULTnEN bit (where n = 0, 1, 2, 3) enables the fault input n and FFLTRnEN bit enables the fault input n filter. FFVAL[3:0] bits select the value of the enabled filter in each enabled fault input.

First, each fault input signal is synchronized by the system clock; see the synchronizer block in the following figure. Following synchronization, the fault input n signal enters the filter block. When there is a state change in the fault input n signal, the 5-bit counter is reset and starts counting up. As long as the new state is stable on the fault input n, the counter continues to increment. If the 5-bit counter overflows and exceeds the value of the FFVAL[3:0] bits, the new fault input n value is validated. It is then transmitted as a pulse edge to the edge detector.

If the opposite edge appears on the fault input n signal before validation (counter overflow), the counter is reset. At the next input transition, the counter starts counting again. Any pulse that is shorter than the minimum value selected by FFVAL[3:0] bits (× system clock) is regarded as a glitch and is not passed on to the edge detector.

The fault input n filter is disabled when the FFVAL[3:0] bits are zero or when FAULTnEN = 0. In this case the fault input n signal is delayed two rising edges of the system clock and the FAULTFn bit is set on the third rising edge of the system clock after a rising edge occurs on the fault input n.

If FFVAL[3:0] ≠ 0000 and FAULTnEN = 1, then the fault input n signal is delayed (3 + FFVAL[3:0]) rising edges of the system clock; that is, the FAULTFn bit is set (4 + FFVAL[3:0]) rising edges of the system clock after a rising edge occurs on the fault input n.



* where n = 3, 2, 1, 0

Figure 12-58. Fault input n control block diagram

If the fault control and fault input n are enabled and a rising edge at the fault input n signal is detected, then the FAULTFn bit is set. The FAULTF bit is the logic OR of FAULTFn[3:0] bits. See the following figure.

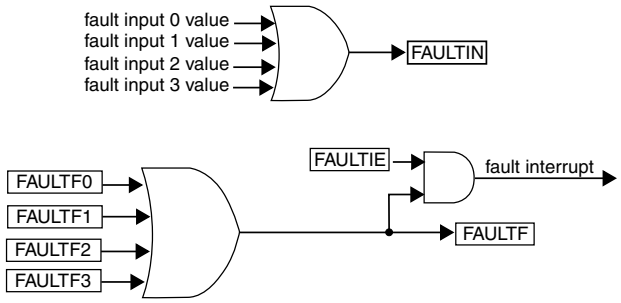


Figure 12-59. FAULTF and FAULTIN bits and fault interrupt

If the fault control is enabled (FAULTM[1:0] ≠ 0:0), a fault condition has occurred (rising edge at the logic OR of the enabled fault input) and (FAULTEN = 1), then channel (n) and (n+1) outputs are forced to their safe value (that is, the channel (n) output is forced to the value of POL(n) and the channel (n+1) is forced to the value of POL(n +1)).

The fault interrupt is generated when (FAULTF = 1) and (FAULTIE = 1). This interrupt request remains set until:

- Software clears the FAULTF bit (by reading FAULTF bit as 1 and writing 0 to it)
- Software clears the FAULTIE bit
- A reset occurs

Note

Fault control is available only in combine mode.

12.4.14.1 Automatic fault clearing

If the automatic fault clearing is selected (FAULTM[1:0] = 1:1), then the disabled channel outputs are enabled when the fault input signal (FAULTIN) returns to zero and a new PWM cycle begins. See the following figure.

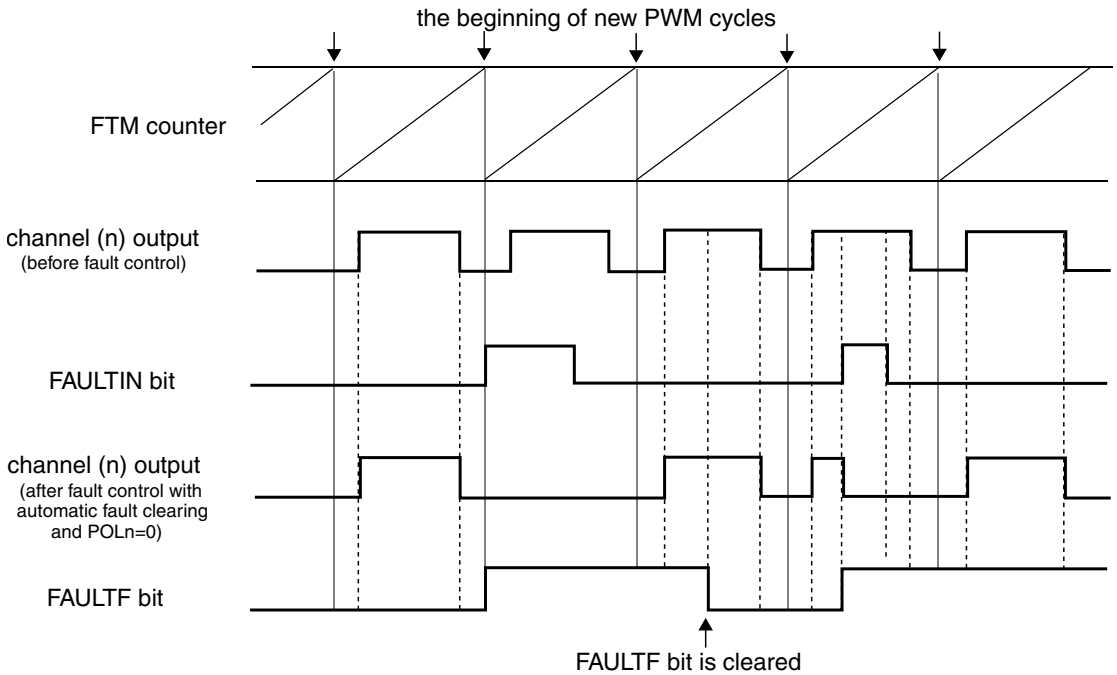


Figure 12-60. Fault control with automatic fault clearing

12.4.14.2 Manual fault clearing

If the manual fault clearing is selected (FAULTM[1:0] = 0:1 or 1:0), then disabled channel outputs are enabled when the FAULTF bit is cleared and a new PWM cycle begins. See the following figure.

It is possible to manually clear a fault by clearing the FAULTF bit, and enable disabled channels regardless of the fault input signal (FAULTIN) (the filter output if the filter is enabled or the synchronizer output if the filter is disabled). However, it is recommended to verify the value of the fault input signal (value of the FAULTIN bit) before clearing the FAULTF bit to avoid unpredictable results.

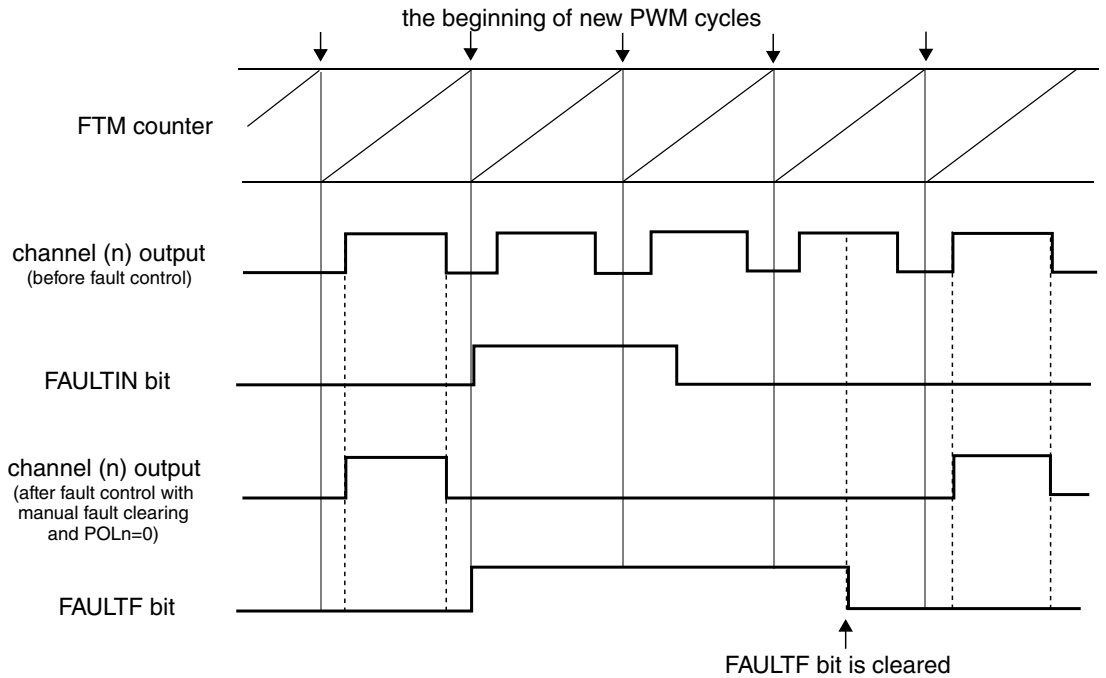


Figure 12-61. Fault control with manual fault clearing

12.4.15 Polarity control

The POLn bit selects the channel (n) output polarity:

- If (POLn = 0), the channel (n) output polarity is active-high: one is the active state; zero is the inactive state.
- If (POLn = 1), the channel (n) output polarity is active-low: zero is the active state; one is the inactive state.

Note

Polarity control is available only in combine mode.

12.4.16 Initialization

The initialization forces the CHnOI bit value to the channel (n) output when a one is written to the INIT bit.

Note

- It is recommended to use the initialization only when the FTM counter is disabled (CLKS[1:0] = 0:0).
- Initialization is available only in combine mode.

12.4.17 Features priority

The following figure shows the priority of the features that can be combined to generate channel (n) and (n+1) outputs.

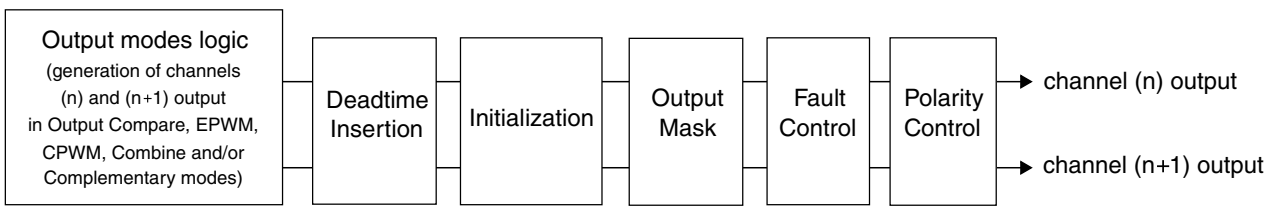


Figure 12-62. FTM features priority

12.4.18 Channel trigger output

The channel trigger output is generated if (FTMEN = 1) and one or more channels were selected by the CHjTRIG bit, where j = 0, 1, 2, 3, 4, or 5. The CHjTRIG bit defines if the channel (j) match (that is, FTM counter = C(j)VH:L) generates the trigger.

The channel trigger output provides a trigger signal that is used for on-chip modules.

The FTM is able to generate multiple triggers in one PWM period. Because each trigger is generated for a specific channel, several channels are required to implement this functionality. This behavior is described in the following figure.

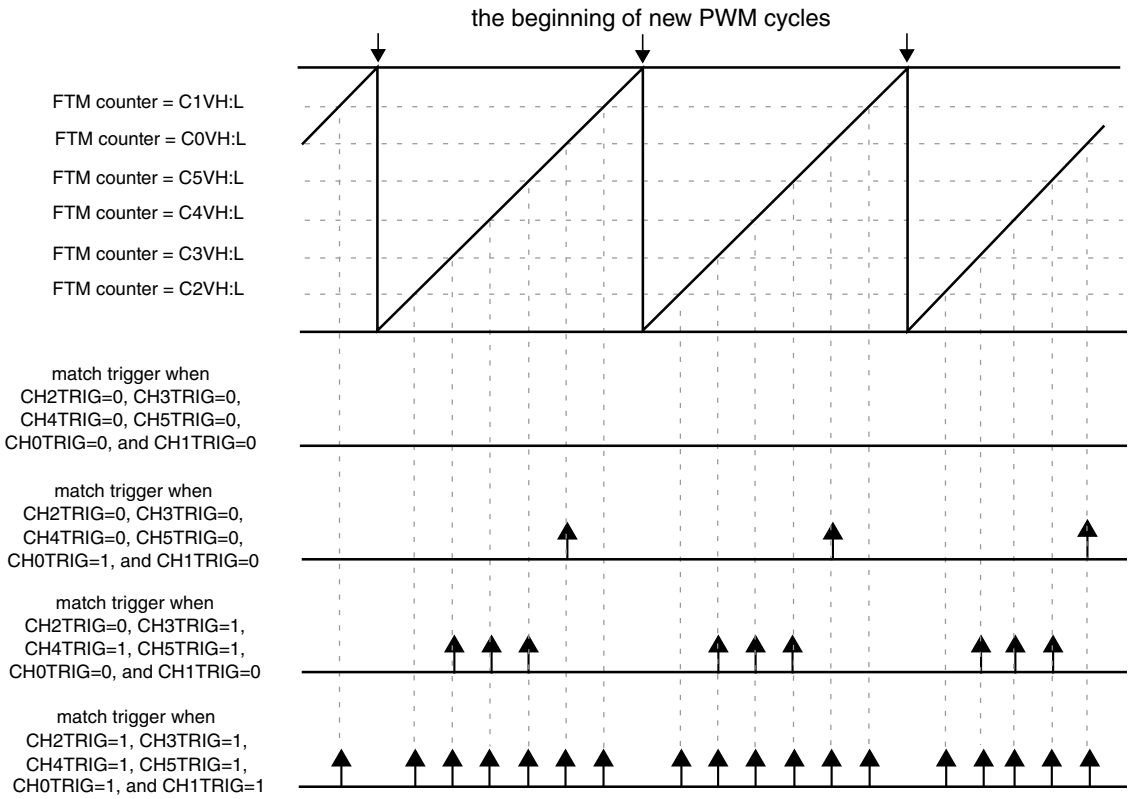


Figure 12-63. Match triggers

Note

Match trigger is available only in combine mode.

12.4.19 Initialization trigger

If INITTRIGEN = 1, the FTM generates a trigger when the FTM counter is updated with the CNTINH:L registers value in the following cases:

- The FTM counter is automatically updated with the CNTINH:L registers value by selected counting mode.

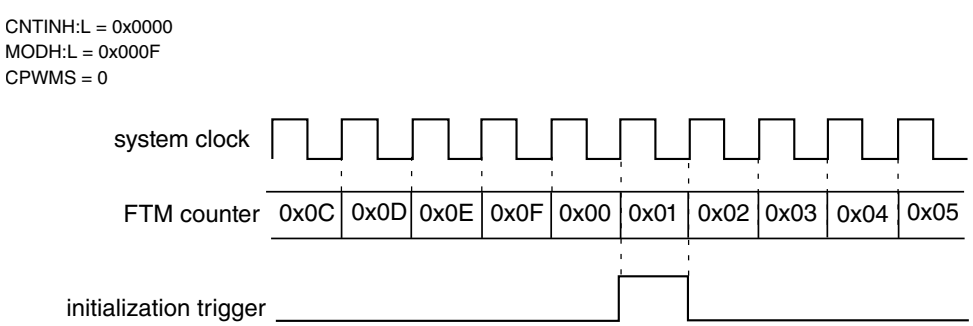


Figure 12-64. Initialization trigger is generated when the FTM counter achieves the value of CNTINH:L

- When there is a write to CNTH or CNTL register

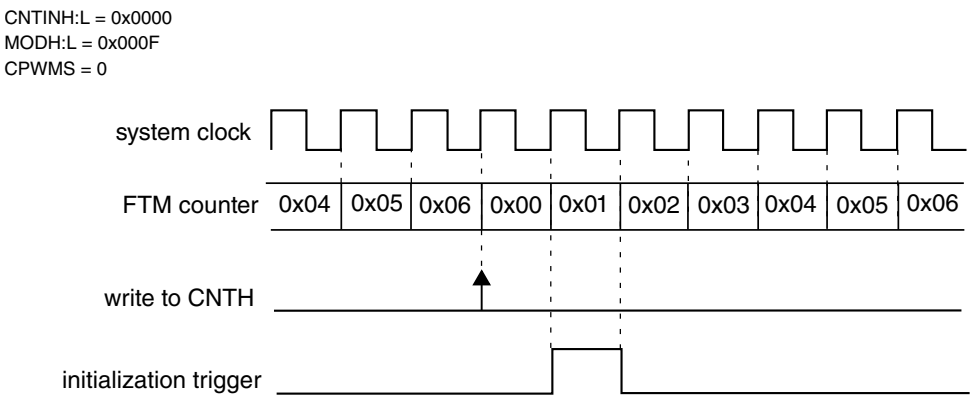


Figure 12-65. Initialization trigger is generated when there is a write to CNTH or CNTL

- When there is the FTM counter synchronization

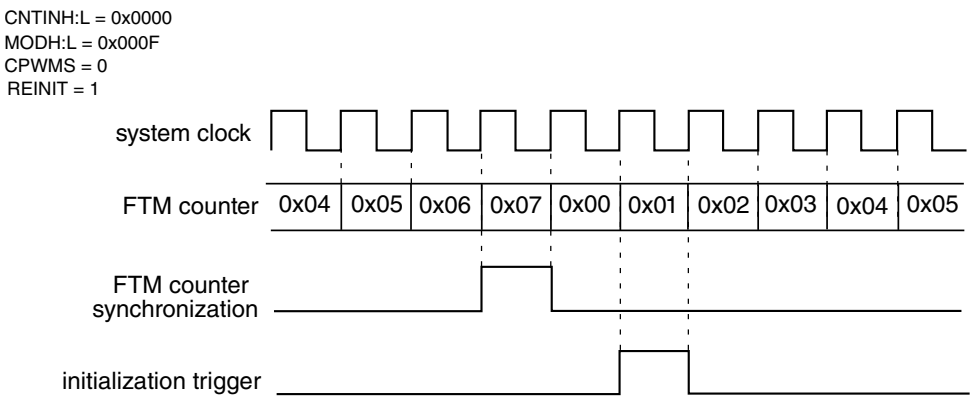


Figure 12-66. Initialization trigger is generated when there is the FTM counter synchronization

- If (CNTH:L = CNTINH:L), (CLKS[1:0] = 0:0), and a value different from zero is written to CLKS[1:0] bits

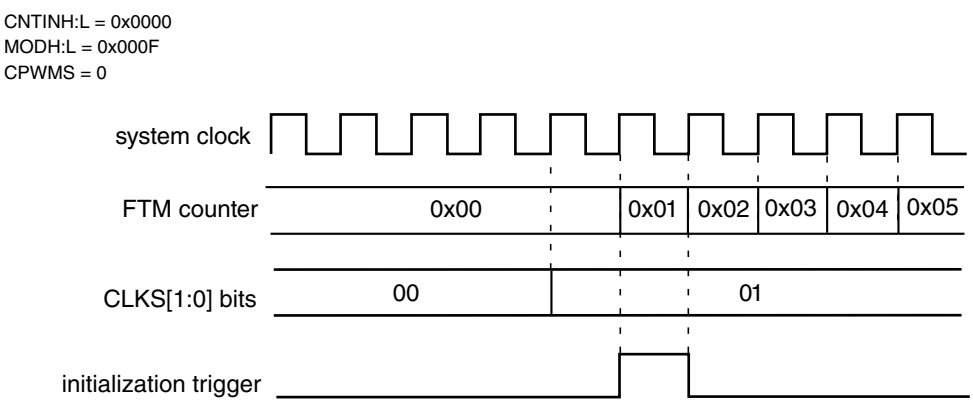


Figure 12-67. Initialization trigger is generated if (CNTH:L = CNTINH:L) and (CLKS[1:0] = 0:0) and a value different from zero is written to CLKS[1:0] bits

The initialization trigger output provides a trigger signal that is used for on-chip modules.

Note

Initialization trigger is available only in combine mode.

12.4.20 Capture test mode

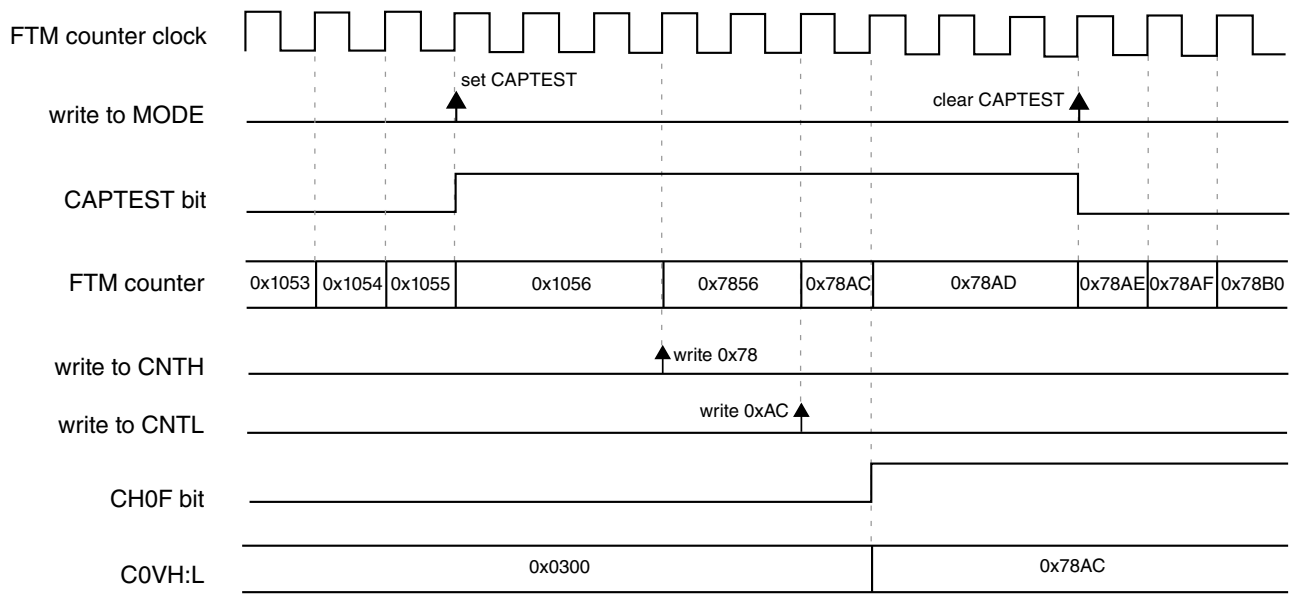
The capture test mode allows the testing of the CnVH:L registers, the FTM counter, and the interconnection logic between the FTM counter and CnVH:L registers.

In this test mode, all channels must be configured for input capture mode (see Input capture mode) and FTM counter must be configured for up-counting (see Up counting).

When the capture test mode is enabled (CAPTEST = 1), the FTM counter is frozen and any write to CNTH and CNTL updates directly the FTM counter; see the following figure. After both bytes were written, independent of the order, all CnVH:L registers are updated with the value that was written to CNTH:L registers and CHnF bits are set. Therefore, the FTM counter is updated with its next value according to its configuration. Its next value depends on CNTINH:L, MODH:L, and the value that was written to FTM counter.

The next reads of CnVH:L registers return the value that was written to FTM counter and the next reads of CNTH:L register return the next value of the FTM counter.

The read coherency mechanism of CNTH:L and CnVH:L registers remains enabled.



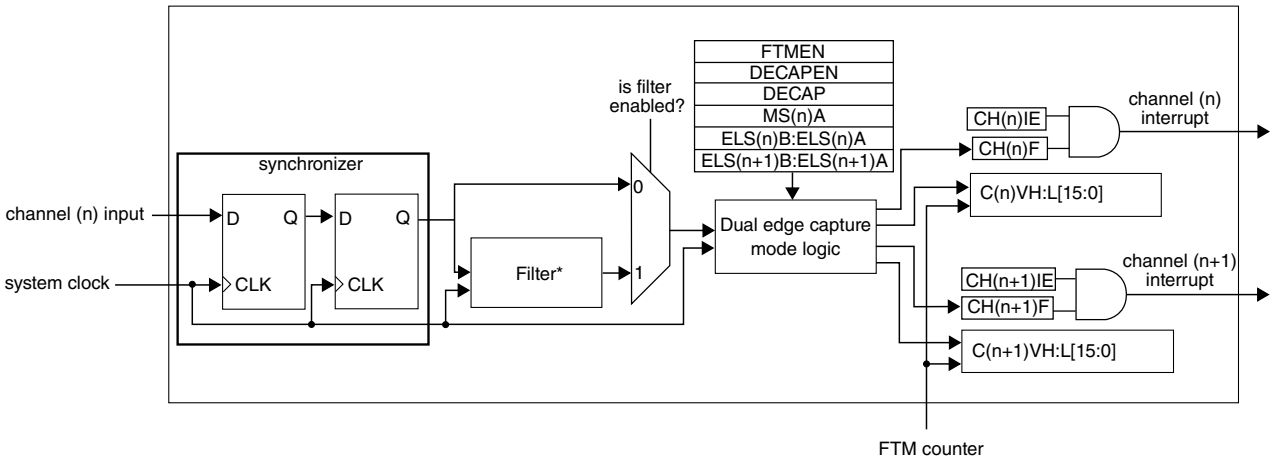
Notes
- FTM counter configuration: (FTMEN = 1), (CAPTEST = 1), (CPWMS = 0), (CNTINH:L = 0x0000) and (MODH:L = 0xFFFF)

- FTM channel n configuration: input capture mode – (DECAPEN = 0), (COMBINE = 0), and (MSnB:MSnA = 0:0)

Figure 12-68. Capture test mode

12.4.21 Dual edge capture mode

The dual edge capture mode is selected if FTMEN = 1 and DECAPEN = 1. This mode allows software to measure a pulse width or period of the signal on the input of channel (n) of a channel pair. The channel (n) filter can be active in this mode when n is the channels 0 or 2.



* Filtering function for dual edge capture mode is only available in the channels 0 and 2

Figure 12-69. Dual edge capture mode block diagram

The MS(n)A bit defines if the dual edge capture mode is one-shot or continuous according to table "Mode, Edge, and Level Selection".

The ELS(n)B:ELS(n)A bits select the edge that is captured by channel (n), and ELS(n +1)B:ELS(n+1)A bits select the edge that is captured by channel (n+1) as described in table "Dual Edge Capture Mode — Edge Polarity Selection". If both ELS(n)B:ELS(n)A and ELS(n+1)B:ELS(n+1)A bits select the same edge, then it is the period measurement. If these bits select different edges, then it is a pulse width measurement.

In the dual edge capture mode, only channel (n) input is used and channel (n+1) input is ignored.

If the selected edge by channel (n) bits is detected at channel (n) input, then CH(n)F bit is set and the channel (n) interrupt is generated (if CH(n)IE = 1). If the selected edge by channel (n+1) bits is detected at channel (n) input and (CH(n)F = 1), then CH(n+1)F bit is set and the channel (n+1) interrupt is generated (if CH(n+1)IE = 1).

The C(n)VH:L registers store the value of FTM counter when the selected edge by channel (n) is detected at channel (n) input. The C(n+1)VH:L registers store the value of FTM counter when the selected edge by channel (n+1) is detected at channel (n) input.

In this mode, the coherency mechanism of the pair of channels ensures that data is coherent when the C(n)VH:L and C(n+1)VH:L registers are read. Note that the C(n)VH:L registers must be read first before reading the C(n+1)VH:L registers. C(n)VH:L registers must be read first than C(n+1)VH:L registers.

Note

- The CH(n)F, CH(n)IE, MS(n)A, ELS(n)B, and ELS(n)A bits are channel (n) bits.

- The CH(n+1)F, CH(n+1)IE, MS(n+1)A, ELS(n+1)B, and ELS(n+1)A bits are channel (n+1) bits.
- It is expected that the dual edge capture mode be used with ELS(n)B:ELS(n)A = 0:1 or 1:0, ELS(n+1)B:ELS(n+1)A = 0:1 or 1:0 and the FTM counter in free running counter mode. See Free running counter.

12.4.21.1 One-shot capture mode

The one-shot capture mode is selected when (FTMEN = 1), (DECAPEN = 1), and (MS(n)A = 0). In this capture mode, only one pair of edges at the channel (n) input is captured. The ELS(n)B:ELS(n)A bits select the first edge to be captured, and ELS(n +1)B:ELS(n+1)A bits select the second edge to be captured.

The edge captures are enabled while DECAP bit is set. For each new measurement in one-shot capture mode, first the CH(n)F and CH(n+1) bits must be cleared, and then the DECAP bit must be set.

In this mode, the DECAP bit is automatically cleared by FTM when the edge selected by channel (n+1) is captured. Therefore, while DECAP bit is set, the one-shot capture is in process. When this bit is cleared, both edges were captured and the captured values are ready for reading in the C(n)VH:L and C(n+1)VH:L registers.

Similarly, when the CH(n+1)F bit is set, both edges were captured and the captured values are ready for reading in the C(n)VH:L and C(n+1)VH:L registers.

12.4.21.2 Continuous capture mode

The continuous capture mode is selected when (FTMEN = 1), (DECAPEN = 1), and (MS(n)A = 1). In this capture mode, the edges at the channel (n) input are captured continuously. The ELS(n)B:ELS(n)A bits select the initial edge to be captured, and ELS(n+1)B:ELS(n+1)A bits select the final edge to be captured.

The edge captures are enabled while DECAP bit is set. For the initial use, first the CH(n)F and CH(n+1)F bits must be cleared, and then DECAP bit must be set to start the continuous measurements.

When the CH(n+1)F bit is set, both edges are captured and the captured values are ready for reading in the C(n)VH:L and C(n+1)VH:L registers. The latest captured values are always available in these registers even after the DECAP bit is cleared.

In this mode, it is possible to clear only the CH(n+1)F bit. Therefore, when the CH(n+1)F bit is set again, the latest captured values are available in C(n)VH:L and C(n+1)VH:L registers.

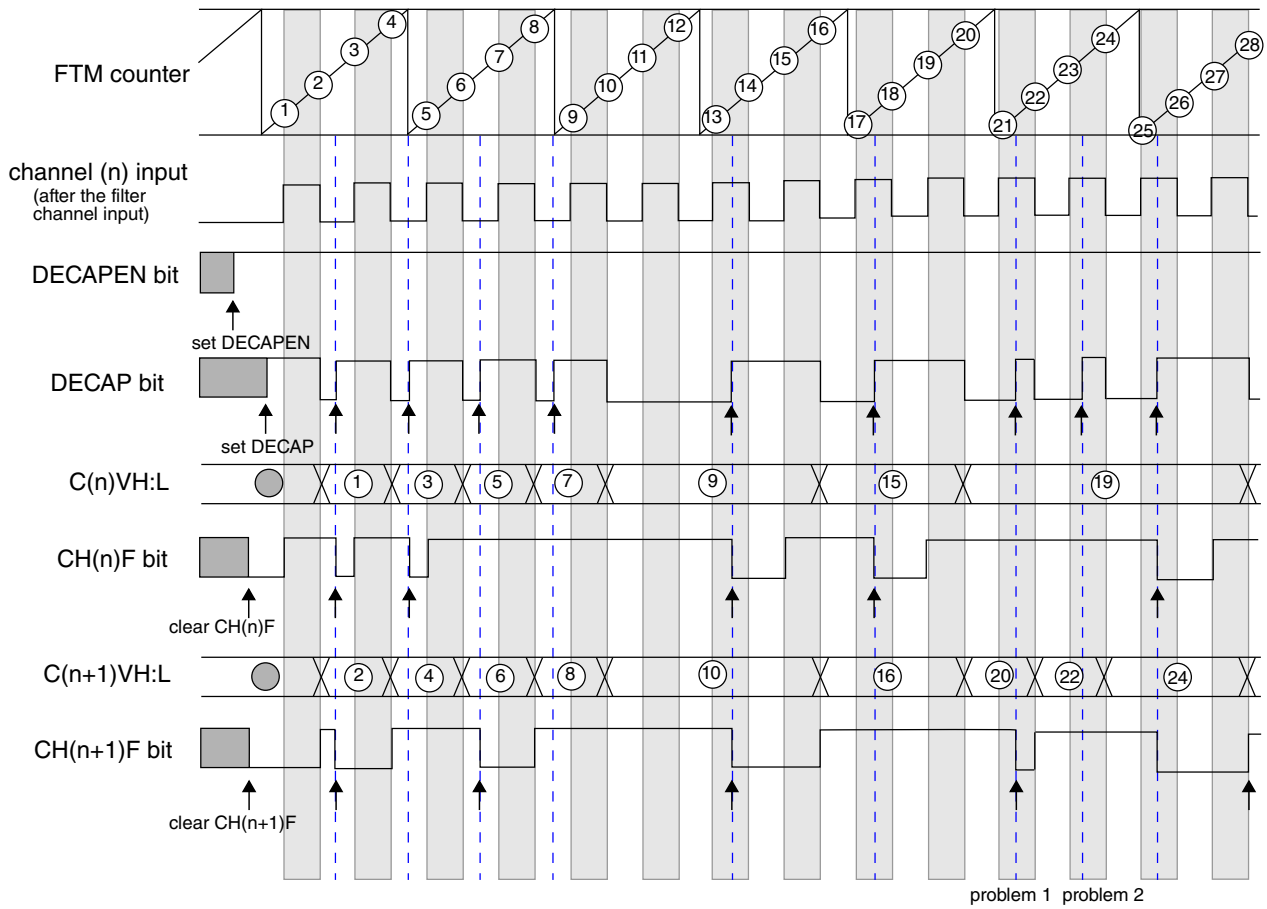
For a new sequence of the measurements in the dual edge capture – continuous mode, it is recommended to clear the CH(n)F and CH(n+1) bits to start new measurements.

12.4.21.3 Pulse width measurement

If the channel (n) is configured to capture rising edges (ELS(n)B:ELS(n)A = 0:1) and the channel (n+1) to capture falling edges (ELS(n+1)B:ELS(n+1)A = 1:0), then the positive polarity pulse width is measured. If the channel (n) is configured to capture falling edges (ELS(n)B:ELS(n)A = 1:0) and the channel (n+1) to capture rising edges (ELS(n +1)B:ELS(n+1)A = 0:1), then the negative polarity pulse width is measured.

The pulse width measurement can be made in one-shot capture mode (One-shot capture mode) or continuous capture mode (Continuous capture mode).

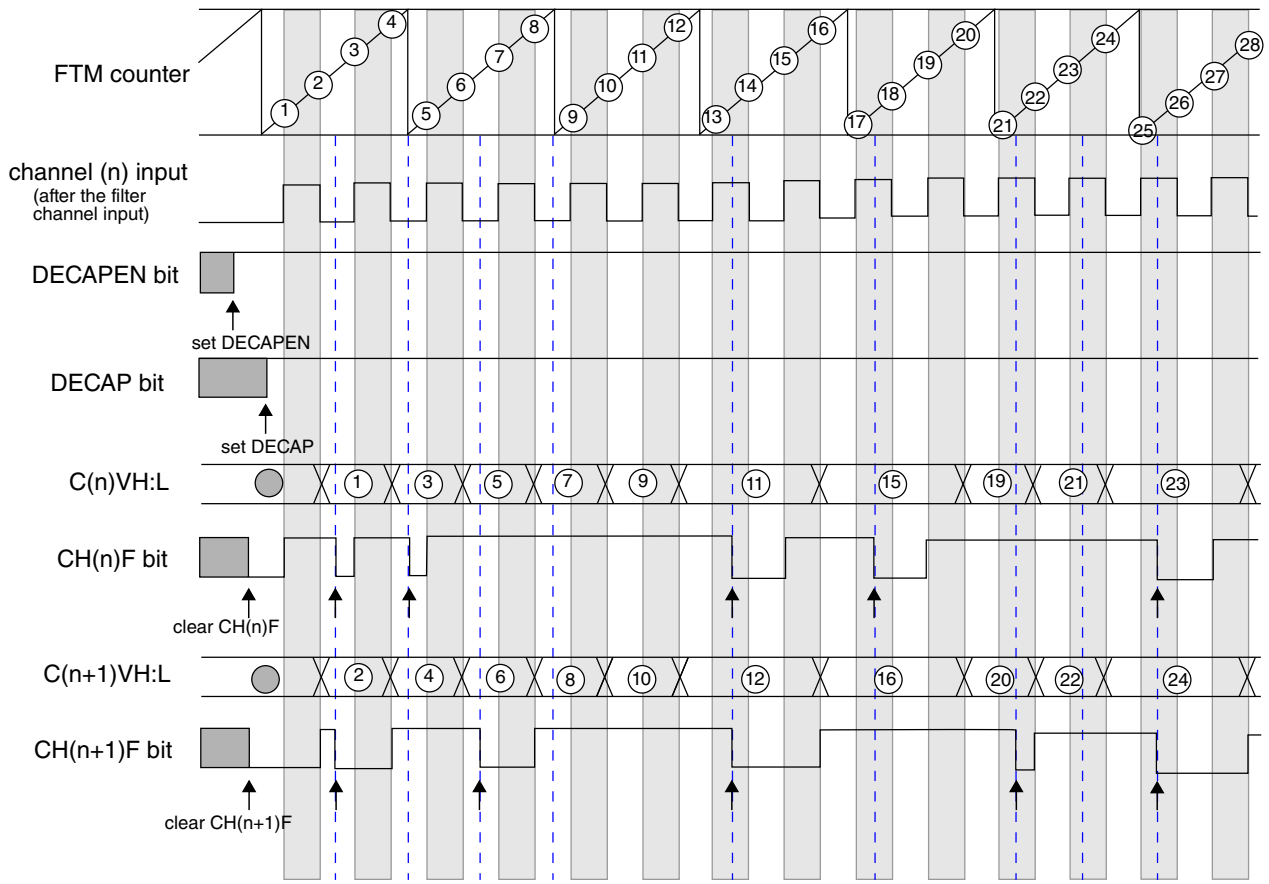
The following figure shows an example of the dual edge capture – one-shot mode used to measure the positive polarity pulse width. The DECAPEN bit selects the dual edge capture mode. The DECAP bit is set to enable the measurement of next positive polarity pulse width. The CH(n)F bit is set when the first edge of this pulse is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set and DECAP bit is cleared when the second edge of this pulse is detected, that is, the edge selected by ELS(n +1)B:ELS(n+1)A bits. Both DECAP and CH(n+1)F bits indicate when two edges of the pulse were captured and the C(n)VH:L and C(n+1)VH:L registers are ready for reading.



Note:
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.
- Problem 1: channel (n) input = 1, set DECAP, not clear CH(n)F, and clear CH(n+1)F.
- Problem 2: channel (n) input = 1, set DECAP, not clear CH(n)F, and not clear CH(n+1)F.

Figure 12-70. Dual edge capture – one-shot mode for positive polarity pulse width measurement

The following figure shows an example of the dual edge capture – continuous mode used to measure the positive polarity pulse width. The DECAPEN bit selects the dual edge capture mode, so it keeps set in all operation mode. While the DECAP bit is set the configured measurements are made. The CH(n)F bit is set when the first edge of the positive polarity pulse is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set when the second edge of this pulse is detected, that is, the edge selected by ELS(n+1)B:ELS(n+1)A bits. The CH(n+1)F bit indicates when two edges of the pulse were captured and the C(n)VH:L and C(n+1)VH:L registers are ready for reading.



Note
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.

Figure 12-71. Dual edge capture – continuous mode for positive polarity pulse width measurement

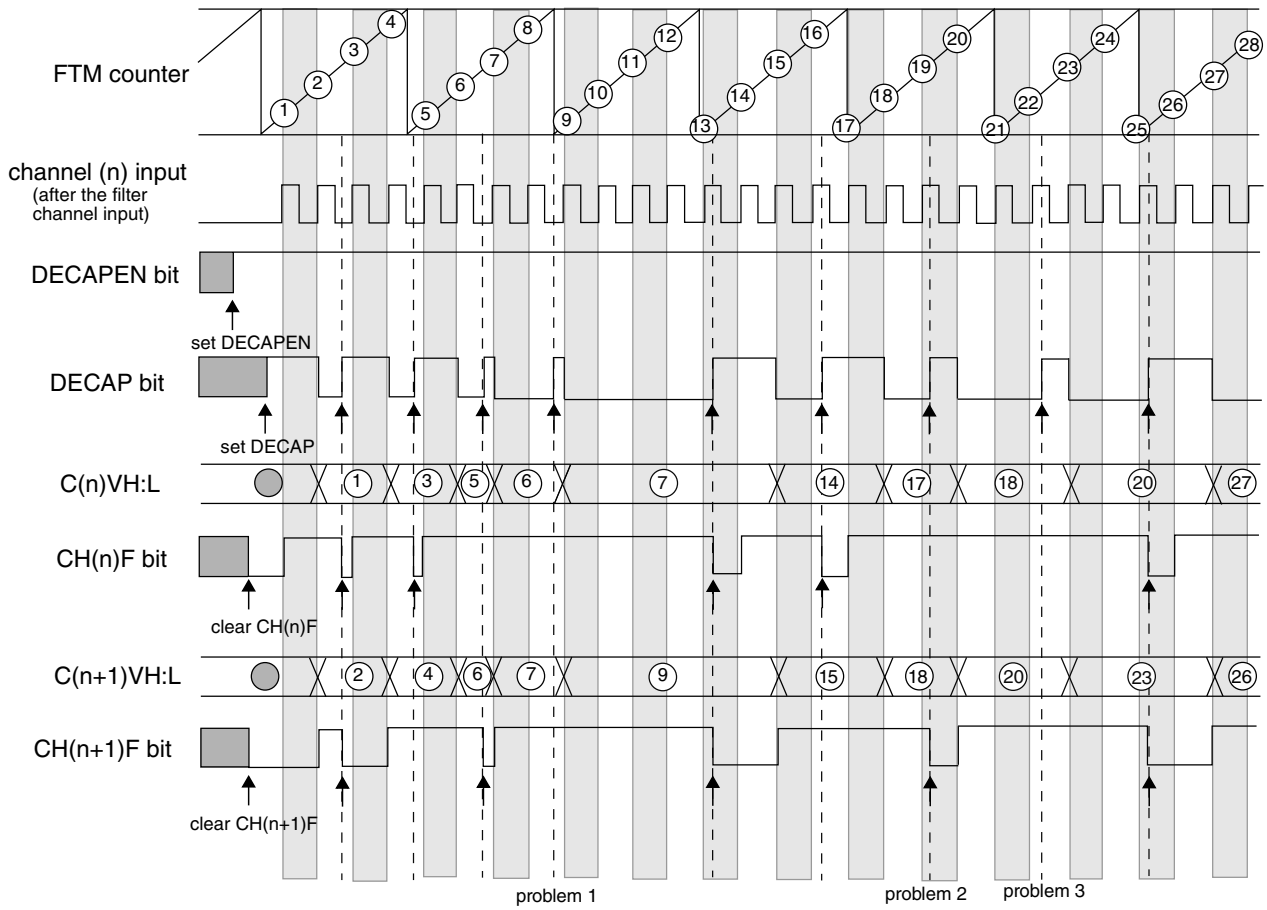
12.4.21.4 Period measurement

If the channels (n) and (n+1) are configured to capture consecutive edges of the same polarity, then the period of the channel (n) input signal is measured. If both channels (n) and (n+1) are configured to capture rising edges (ELS(n)B:ELS(n)A = 0:1 and ELS(n +1)B:ELS(n+1)A = 0:1), then the period between two consecutive rising edges is measured. If both channels (n) and (n+1) are configured to capture falling edges (ELS(n)B:ELS(n)A = 1:0 and ELS(n+1)B:ELS(n+1)A = 1:0), then the period between two consecutive rising edges is measured.

The period measurement can be made in one-shot capture mode (One-shot capture mode) or continuous capture mode (Continuous capture mode).

The following figure shows an example of the dual edge capture – one-shot mode used to measure the period between two consecutive rising edges. The DECAPEN bit selects the dual edge capture mode, so it keeps set in all operation mode. The DECAP bit is set to

enable the measurement of next period. The CH(n)F bit is set when the first rising edge is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit is set and DECAP bit is cleared when the second rising edge is detected, that is, the edge selected by ELS(n+1)B:ELS(n+1)A bits. Both DECAP and CH(n+1)F bits indicate when two selected edges were captured and the C(n)VH:L and C(n+1)VH:L registers are ready for reading.

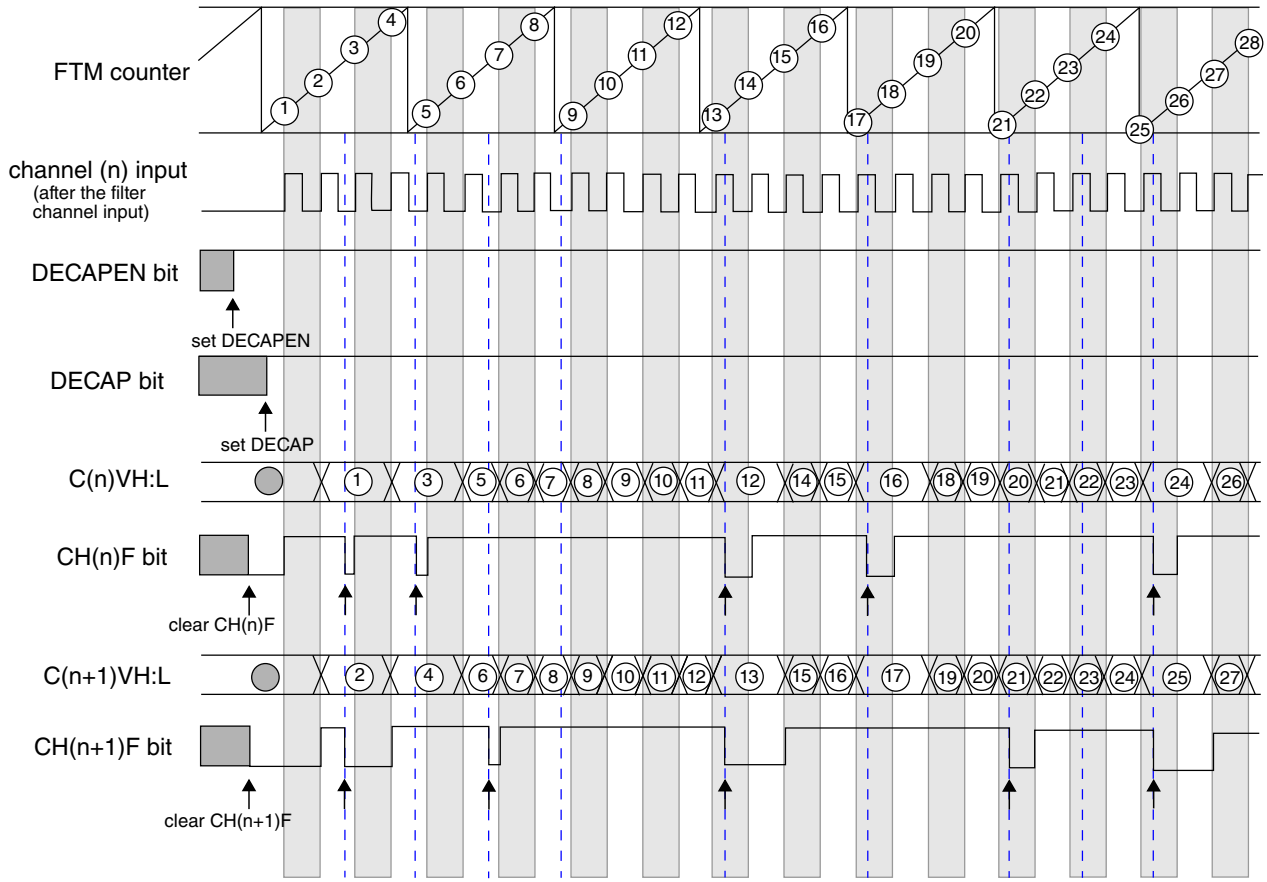


Note
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.
- Problem 1: channel (n) input = 0, set DECAP, not clear CH(n)F, and not clear CH(n+1)F.
- Problem 2: channel (n) input = 1, set DECAP, not clear CH(n)F, and clear CH(n+1)F.
- Problem 3: channel (n) input = 1, set DECAP, not clear CH(n)F, and not clear CH(n+1)F.

Figure 12-72. Dual edge capture – one-shot mode to measure of the period between two consecutive rising edges

The following figure shows an example of the dual edge capture – continuous mode used to measure the period between two consecutive rising edges. The DECAPEN bit selects the dual edge capture mode, so it keeps set in all operation mode. While the DECAP bit is set the configured measurements are made. The CH(n)F bit is set when the first rising edge is detected, that is, the edge selected by ELS(n)B:ELS(n)A bits. The CH(n+1)F bit

is set when the second rising edge is detected, that is, the edge selected by ELS(n +1)B:ELS(n+1)A bits. The CH(n+1)F bit indicates when two edges of the period were captured and the C(n)VH:L and C(n+1)VH:L registers are ready for reading.



Note:
- The commands set DECAPEN, set DECAP, clear CH(n)F, and clear CH(n+1)F are made by the user.

Figure 12-73. Dual edge capture – continuous mode to measure of the period between two consecutive rising edges

12.4.21.5 Read coherency mechanism

The dual edge capture mode implements a read coherency mechanism between the FTM counter value captured in C(n)VH:L and C(n+1)VH:L registers. The read coherency mechanism is illustrated in the following figure. In this example, the channels (n) and (n +1) are in dual edge capture – continuous mode for positive polarity pulse width measurement. Thus, the channel (n) is configured to capture the FTM counter value when there is a rising edge at channel (n) input signal, and channel (n+1) to capture the FTM counter value when there is a falling edge at channel (n) input signal.

When a rising edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n) capture buffer. The channel (n) capture buffer value is transferred to C(n)VH:L registers when a falling edge occurs in the channel (n) input signal. C(n)VH:L registers have the FTM counter value when the previous rising edge occurred, and the channel (n) capture buffer has the FTM counter value when the last rising edge occurred.

When a negative edge occurs in the channel (n) input signal, the FTM counter value is captured into channel (n+1) capture buffer. The channel (n+1) capture buffer value is transferred to C(n+1)VH:L registers when the first byte of C(n)VH:L registers is read.

In the following figure, the read of C(n)VH returns the FTM counter high byte value when the event 1 occurred, and the read of C(n+1)VL returns the FTM counter low byte value when the event 1 occurred. The read of C(n+1)VL returns the FTM counter low byte value when the event 2 occurred, and the read of C(n+1)VH returns the FTM counter high byte value when the event 2 occurred.

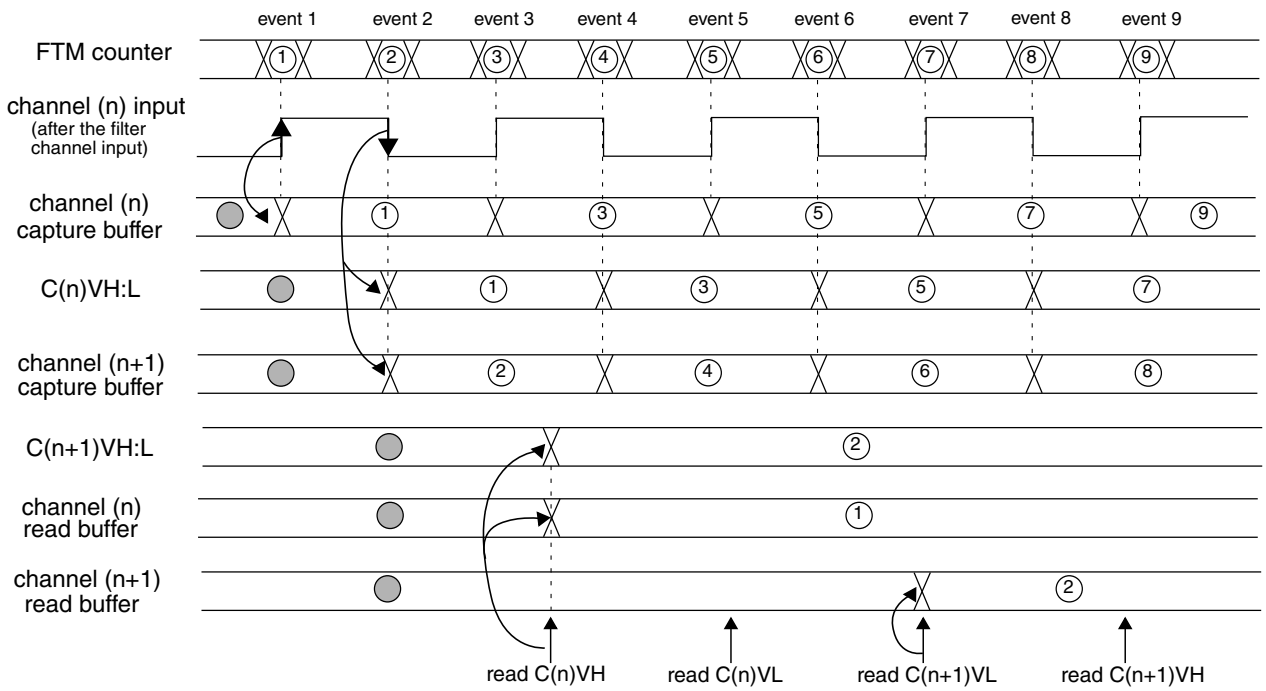


Figure 12-74. Dual edge capture mode read coherency mechanism

C(n)VH:L registers must be read prior to C(n+1)VH:L registers in dual edge capture one-shot and continuous modes for the read coherency mechanism works properly. Either the high or low bytes of C(n)VH:L and C(n+1)VH:L registers can be accessed first; however, the C(n)VH:L registers must be read prior to the C(n+1)VH:L registers in dual edge capture oneshot and continuous modes for the read coherency mechanism to work properly.

12.4.22 TPM emulation

This section describe the FTM features that are selected according to the FTMEN bit.

12.4.22.1 MODH:L and CnVH:L synchronization

If (FTMEN = 0), then the MODH:L and CnVH:L registers are updated according to the Update of the registers with write buffers and they are not updated by PWM synchronization.

If (FTMEN = 1), then the MODH:L and CnVH:L registers are updated only by PWM synchronization (PWM synchronization).

12.4.22.2 Free running counter

If (FTMEN = 0), then the FTM counter is a free running counter when (MODH:L = 0x0000) or (MODH:L = 0xFFFF).

If (FTMEN = 1), then the FTM counter is a free running counter when (CPWMS = 0), (CNTINH:L = 0x0000), and (MODH:L = 0xFFFF).

12.4.22.3 Write to SC

If (FTMEN = 0), then a write to the SC register resets the write coherency mechanism of MODH:L registers.

If (FTMEN = 1), then a write to the SC register does not reset the write coherency mechanism of MODH:L registers.

12.4.22.4 Write to CnSC

If (FTMEN = 0), then a write to the CnSC register resets the write coherency mechanism of CnVH:L registers.

If (FTMEN = 1), then a write to the CnSC register does not reset the write coherency mechanism of CnVH:L registers.

12.4.23 BDM mode

When BDM mode is active, the FlexTimer counter and the channels output are frozen.

However, the value of FlexTimer counter or the channels output are modified in BDM mode when:

- A write of any value to the CNTH or CNTL registers (Counter reset) resets the FTM counter to the value of CNTINH:L and the channels output to their initial value, except for channels in output compare mode.
- The PWM synchronization with REINIT = 1 (see FTM counter synchronization) resets the FTM counter to the value of CNTINH:L registers and the channels output to their initial value, except for channels in output compare mode.
- The initialization (Initialization) forces the value of the CHnOI bit to the channel (n) output.

Note

Do not use the above cases together with fault control (Fault control). If fault control is enabled and the fault condition is at the enabled fault input, these cases reset the FTM counter to the CNTINH:L value and the channels output to their initial value.

12.5 Reset overview

The FTM is reset whenever any chip reset occurs.

When the FTM exits from reset:

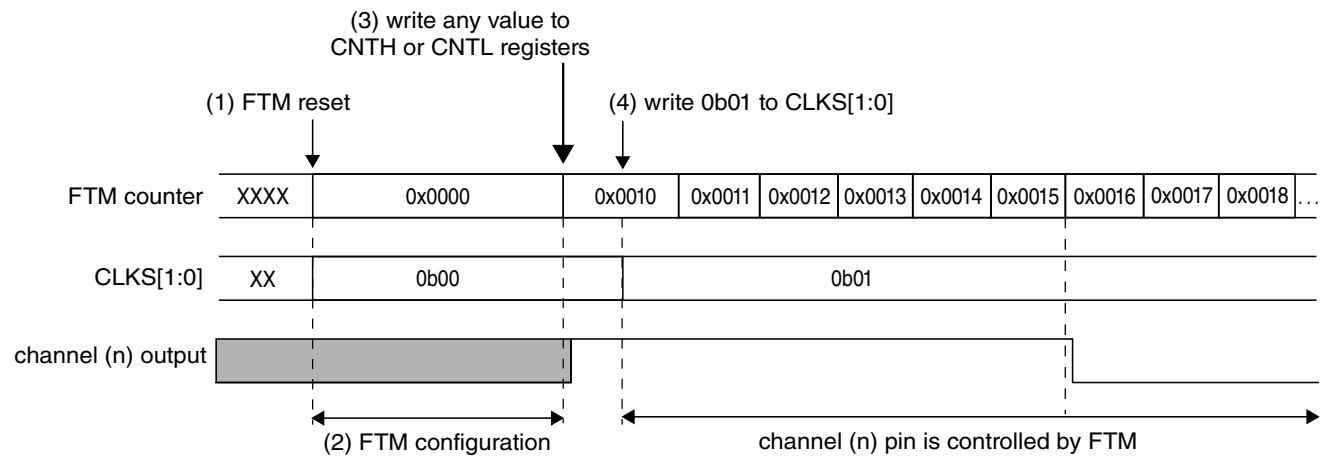
- The FTM counter and the prescaler counter are zero and are stopped (CLKS[1:0] = 0b00)
- The timer overflow interrupt is zero (Timer overflow interrupt)
- The channels interrupts are zero (Channel (n) interrupt)
- The fault interrupt is zero (Fault interrupt)
- The channels are in input capture mode (Input capture mode)
- The channels outputs are zero
- The channels pins are not controlled by FTM (ELS(n)B:ELS(n)A = 0b00). See table "Mode, Edge, and Level Selection"

The following figure shows the FTM behavior after the reset. At the reset (item 1), the FTM counter is disabled (see table "FTM Clock Source Selection"), its value is updated to zero and the pins are not controlled by FTM (table "Mode, Edge, and Level Selection").

After the reset, the FTM should be configured (item 2). It is necessary to define the FTM counter mode, the FTM counting limits (MODH:L and CNTINH:L registers value), the channels mode and CnVH:L registers value according to the channels mode.

Because of this, you should write any value to CNTH or CNTL registers (item 3). This write updates the FTM counter with the value of CNTINH:L and the channels output with its initial value (except for channels in output compare mode) (Counter reset).

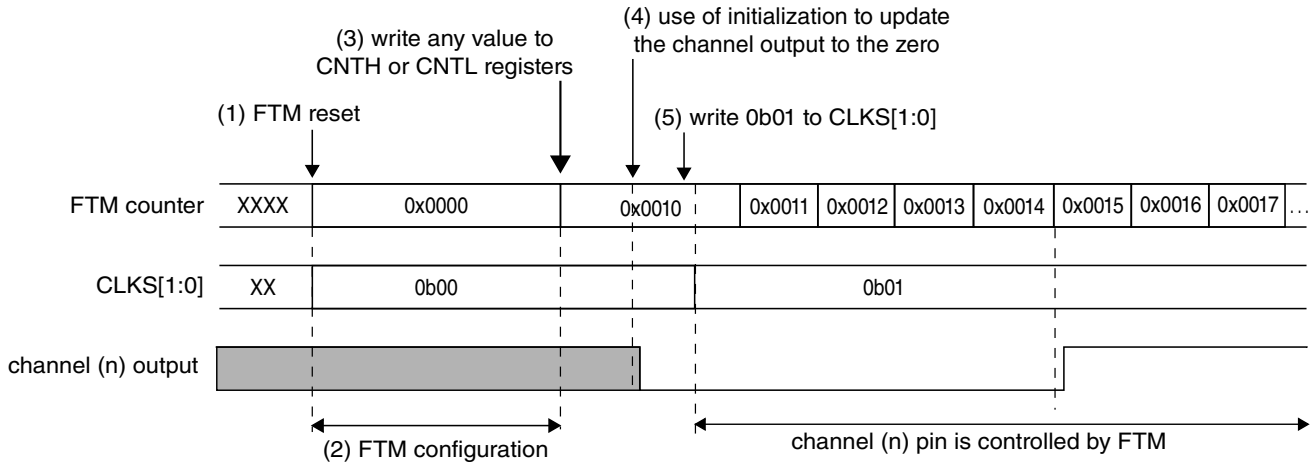
The next step is to select the FTM counter clock by the CLKS[1:0] bits (item 4). It is important to highlight that the pins are controlled only by FTM when CLKS[1:0] bits are different from zero (table "Mode, Edge, and Level Selection").



Note
– CNTINH:L = 0x0010
– Channel (n) is in low-true combine mode with CNTINH:L < C(n)VH:L < C(n+1)VH:L < MODH:L
– C(n)VH:L = 0x0015

Figure 12-75. FTM behavior after the reset when the channel (n) is in combine mode

The following figure shows an example when the channel (n) is in output compare mode and the channel (n) output is toggled when there is a match. In the output compare mode, the channel output is not updated to its initial value when there is a write to CNTH or CNTL registers (item 3). In this case, it is recommended to use the initialization (Initialization) to update the channel output to the selected value (item 4).



Note
– CNTINH:L = 0x0010
– Channel (n) is in output compare and the channel (n) output is toggled when there is a match
– C(n)VH:L = 0x0014

Figure 12-76. FTM behavior after the reset when the channel (n) is in output compare mode

12.6 FTM Interrupts

12.6.1 Timer overflow interrupt

The timer overflow interrupt is generated when (TOIE = 1) and (TOF = 1).

12.6.2 Channel (n) interrupt

The channel (n) interrupt is generated when (CHnIE = 1) and (CHnF = 1).

12.6.3 Fault interrupt

The fault interrupt is generated when (FAULTIE = 1) and (FAULTF = 1).

Chapter 13
8-bit modulo timer (MTIM)

13.1 Introduction

The MTIM is a simple 8-bit timer with several software selectable clock sources and a programmable interrupt.

For MCUs that have more than one MTIM, the MTIMs are collectively called MTIMx. For example, MTIMx for an MCU with two MTIMs would refer to MTIM0 and MTIM1. For MCUs that have exactly one MTIM, it is always referred to as MTIM.

13.2 Features

Timer system features include:

- 8-bit up-counter:
  - Free-running or 8-bit modulo limit
  - Software controllable interrupt on overflow
  - Counter reset bit (TRST)
  - Counter stop bit (TSTP)
- Four software selectable clock sources for input to prescaler:
  - System bus clock - rising edge
  - Fixed frequency clock (XCLK) - rising edge
  - External clock source on the TCLK pin - rising edge
  - External clock source on the TCLK pin - falling edge
- Nine selectable clock prescale values:
  - Clock source divide by 1, 2, 4, 8, 16, 32, 64, 128, or 256

13.3 Modes of operation

This section defines the MTIM's operation in stop, wait, and background debug modes.

13.3.1 MTIM in wait mode

The MTIM continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the MTIM can be used to bring the MCU out of wait mode if the timer overflow interrupt is enabled. For lowest possible current consumption, the MTIM must be stopped by software if not needed as an interrupt source during wait mode.

13.3.2 MTIM in stop mode

The MTIM is disabled in stop mode, regardless of the settings before executing the STOP instruction. Therefore, the MTIM cannot be used as a wakeup source from stop modes.

If stop3 is exited with a reset, the MTIM will be put into its reset state. If stop3 is exited with an interrupt, the MTIM continues from the state it was in when stop3 was entered. If the counter was active upon entering stop3, the count will resume from the current value.

13.3.3 MTIM in active background mode

The MTIM suspends all counting until the microcontroller returns to normal user operating mode. Counting resumes from the suspended value as long as an MTIM reset did not occur, MTIM_SC[TRST] written to a 1 or MTIM_MOD written.

13.4 Block diagram

The block diagram for the modulo timer module is shown in the following figure.

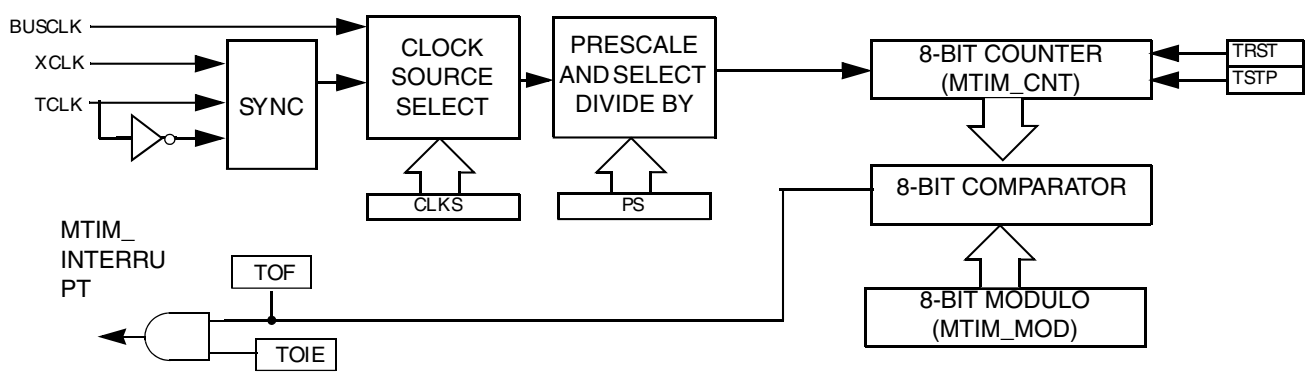


Figure 13-1. Modulo timer (MTIM) block diagram

13.5 External signal description

The MTIM includes one external signal, TCLK, used to input an external clock when selected as the MTIM clock source. The signal properties of TCLK are shown in the following table.

Table 13-1. MTIM external signal

Signal	Function	I/O
TCLK	External clock source input into MTIM	I

The TCLK input must be synchronized by the bus clock. Also, variations in duty cycle and clock jitter must be accommodated. Therefore, the TCLK signal must be limited to one-fourth of the bus frequency.

The TCLK pin can be muxed with a general-purpose port pin.

13.6 Register definition

MTIM memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
18	MTIM Status and Control Register (MTIM0_SC)	8	R/W	10h	13.6.1/396
19	MTIM Clock Configuration Register (MTIM0_CLK)	8	R/W	00h	13.6.2/397
1A	MTIM Counter Register (MTIM0_CNT)	8	R	00h	13.6.3/398
1B	MTIM Modulo Register (MTIM0_MOD)	8	R/W	00h	13.6.4/398
1C	MTIM Status and Control Register (MTIM1_SC)	8	R/W	10h	13.6.1/396
1D	MTIM Clock Configuration Register (MTIM1_CLK)	8	R/W	00h	13.6.2/397
1E	MTIM Counter Register (MTIM1_CNT)	8	R	00h	13.6.3/398
1F	MTIM Modulo Register (MTIM1_MOD)	8	R/W	00h	13.6.4/398

13.6.1 MTIM Status and Control Register (MTIMx_SC)

MTIM_SC contains the overflow status flag and control bits that are used to configure the interrupt enable, reset the counter, and stop the counter.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read	TOF	TOIE	0	TSTP	0			
Write			TRST					
Reset	0	0	0	1	0	0	0	0

MTIMx_SC field descriptions

Field	Description
7 TOF	MTIM Overflow Flag This bit is set when the MTIM counter register overflows to 0x00 after reaching the value in the MTIM modulo register. Clear TOF by reading the MTIM_SC register while TOF is set, then write a 0 to TOF. TOF is also cleared when TRST is written to a 1 or when any value is written to the MTIM_MOD register. 0 MTIM counter has not reached the overflow value in the MTIM modulo register. 1 MTIM counter has reached the overflow value in the MTIM modulo register.
6 TOIE	MTIM Overflow Interrupt Enable This read/write bit enables MTIM overflow interrupts. If TOIE is set, then an interrupt is generated when TOF = 1. Reset clears TOIE. Do not set TOIE if TOF = 1. Clear TOF first, then set TOIE. 0 TOF interrupts are disabled. Use software polling. 1 TOF interrupts are enabled.
5 TRST	MTIM Counter Reset When a 1 is written to this write-only bit, the MTIM counter register resets to 0x00 and TOF is cleared. Reading this bit always returns 0. 0 No effect. MTIM counter remains at current state. 1 MTIM counter is reset to 0x00.
4 TSTP	MTIM Counter Stop When set, this read/write bit stops the MTIM counter at its current value. Counting resumes from the current value when TSTP is cleared. Reset sets TSTP to prevent the MTIM from counting. 0 MTIM counter is active. 1 MTIM counter is stopped.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

13.6.2 MTIM Clock Configuration Register (MTIMx_CLK)

MTIM_CLK contains the clock select bits (CLKS) and the prescaler select bits (PS).

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read	0		CLKS		PS			
Write								
Reset	0	0	0	0	0	0	0	0

MTIMx_CLK field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 CLKS	Clock Source Select These two read/write bits select one of four different clock sources as the input to the MTIM prescaler. Changing the clock source while the counter is active does not clear the counter. The count continues with the new clock source. Reset clears CLKS to 000b. 00 Encoding 0. Bus clock (BUSCLK). 01 Encoding 1. Fixed-frequency clock (XCLK). 10 Encoding 2. External source (TCLK pin), falling edge. 11 Encoding 3. External source (TCLK pin), rising edge.
PS	Clock Source Prescaler These four read/write bits select one of nine outputs from the 8-bit prescaler. Changing the prescaler value while the counter is active does not clear the counter. The count continues with the new prescaler value. Reset clears PS to 0000b. 0000 Encoding 0. MTIM clock source. 0001 Encoding 1. MTIM clock source/2. 0010 Encoding 2. MTIM clock source/4. 0011 Encoding 3. MTIM clock source/8. 0100 Encoding 4. MTIM clock source/16. 0101 Encoding 5. MTIM clock source/32. 0110 Encoding 6. MTIM clock source/64. 0111 Encoding 7. MTIM clock source/128. 1000 Encoding 8. MTIM clock source/256. Others Default to MTIM clock source/256.

13.6.3 MTIM Counter Register (MTIMx_CNT)

MTIM_CNT is the read-only value of the current MTIM count of the 8-bit counter.

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read	COUNT							
Write								
Reset	0	0	0	0	0	0	0	0

MTIMx_CNT field descriptions

Field	Description
COUNT	MTIM Count These eight read-only bits contain the current value of the 8-bit counter. Writes have no effect to this register. Reset clears the count to 0x00.

13.6.4 MTIM Modulo Register (MTIMx_MOD)

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read Write	MOD							
Reset	0	0	0	0	0	0	0	0

MTIMx_MOD field descriptions

Field	Description
MOD	MTIM Modulo These eight read/write bits contain the modulo value used to reset the count and set TOF. A value of 0x00 puts the MTIM in free-running mode. Writing to MTIM_MOD resets the COUNT to 0x00 and clears TOF. Reset sets the modulo to 0x00.

13.7 Functional description

The MTIM consists of a main 8-bit up-counter with an 8-bit modulo register, a clock source selector, and a prescaler block with nine selectable values. The module also contains software-selectable interrupt logic.

The MTIM counter (MTIM_CNT) has three modes of operation: stopped, free-running, and modulo. Out of reset, the counter is stopped. If the counter is started without writing a new value to the modulo register, then the counter will be in free-running mode. The counter is in modulo mode when a value other than 0x00 is in the modulo register while the counter is running.

After any MCU reset, the counter is stopped and reset to 0x00, and the modulus is set to 0x00. The bus clock is selected as the default clock source and the prescale value is divide by 1. To start the MTIM in free-running mode, simply write to the MTIM status and control register (MTIM_SC), and clear the MTIM stop bit (TSTP).

Four clock sources are software selectable: the internal bus clock, the fixed frequency clock (XCLK), and an external clock on the TCLK pin, selectable as incrementing on either rising or falling edges. The MTIM clock select bits, CLKS1:CLKS0, in MTIM_CLK are used to select the desired clock source. If the counter is active (SC[TSTP] = 0) when a new clock source is selected, the counter will continue counting from the previous value using the new clock source.

Nine prescale values are software selectable: clock source divided by 1, 2, 4, 8, 16, 32, 64, 128, or 256. The prescaler select bits (CLK[PS]) in MTIM_CLK select the desired prescale value. If the counter is active (SC[TSTP] = 0) when a new prescaler value is selected, the counter will continue counting from the previous value using the new prescaler value.

The MTIM modulo register (MTIM_MOD) allows the overflow compare value to be set to any value from 0x01 to 0xFF. Reset clears the modulo value to 0x00, which results in a free running counter.

When the counter is active (SC[TSTP] = 0), the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter overflows to 0x00 and continues counting. The MTIM overflow flag (SC[TOF]) is set whenever the counter overflows. The flag sets on the transition from the modulo value to 0x00. Writing to MTIM_MOD while the counter is active resets the counter to 0x00 and clears SC[TOF].

Clearing SC[TOF] is a two-step process. The first step is to read the MTIM_SC register while SC[TOF] is set. The second step is to write a 0 to SC[TOF]. If another overflow occurs between the first and second step, the clearing process is reset and SC[TOF] will remain set after the second step is performed. This will prevent the second occurrence from being missed. SC[TOF] is also cleared when a 1 is written to SC[TRST] or when any value is written to the MTIM_MOD register.

The MTIM allows for an optional interrupt to be generated whenever SC[TOF] is set. To enable the MTIM overflow interrupt, set the MTIM overflow interrupt enable bit (SC[TOIE]). SC[TOIE] must never be written to a 1 while SC[TOF] = 1. Instead, SC[TOF] must be cleared first, then the SC[TOIE] can be set to 1.

13.7.1 MTIM operation example

This section shows an example of the MTIM operation as the counter reaches a matching value from the modulo register.

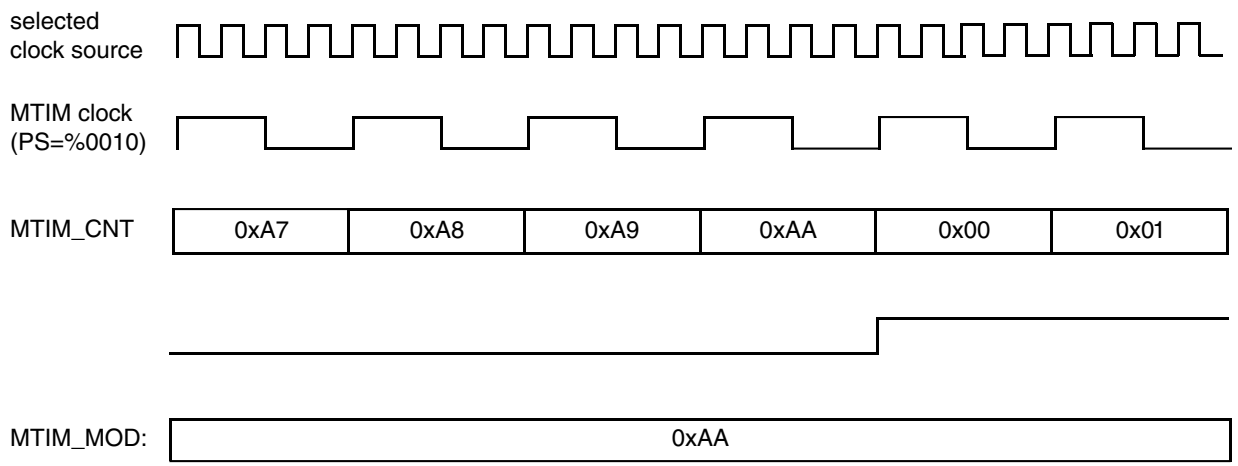


Figure 13-2. MTIM counter overflow example

In the above example, the selected clock source could be any of the four possible choices. The prescaler is set to CLK[PS] = 0010b or divide-by-4. The modulo value in the MTIM_MOD register is set to 0xAA. When the counter, MTIM_CNT, reaches the modulo value of 0xAA, it overflows to 0x00 and continues counting. The timer overflow flag, SC[TOF], sets when the counter value changes from 0xAA to 0x00. An MTIM overflow interrupt is generated when SC[TOF] is set, if SC[TOIE] = 1.

Chapter 14
Real-time counter (RTC)

14.1 Introduction

The real-time counter (RTC) consists of one 16-bit counter, one 16-bit comparator, several binary-based and decimal-based prescaler dividers, three clock sources, one programmable periodic interrupt, and one programmable external toggle pulse output. This module can be used for time-of-day, calendar or any task scheduling functions. It can also serve as a cyclic wake-up from low-power modes, Stop3 and Wait without the need of external components.

14.2 Features

Features of the RTC module include:

- 16-bit up-counter
  - 16-bit modulo match limit
  - Software controllable periodic interrupt on match
- Software selectable clock sources for input to prescaler with programmable 16 bit prescaler
  - XOSC 32.768KHz nominal.
  - LPO (~1 kHz)
  - Bus clock

14.2.1 Modes of operation

This section defines the RTC operation in Stop, Wait, and Background Debug modes.

14.2.1.1 Wait mode

The RTC continues to run in Wait mode if enabled before executing the WAIT instruction. Therefore, the RTC can be used to bring the MCU out of Wait mode if the real-time interrupt is enabled. For lowest possible current consumption, the RTC must be stopped by software if not needed as an interrupt source during Wait mode.

14.2.1.2 Stop modes

The RTC continues to run in Stop3 mode if the RTC is enabled before executing the STOP instruction. Therefore, the RTC can be used to bring the MCU out of stop modes with no external components, if the real-time interrupt is enabled.

14.2.2 Block diagram

The block diagram for the RTC module is shown in the following figure.

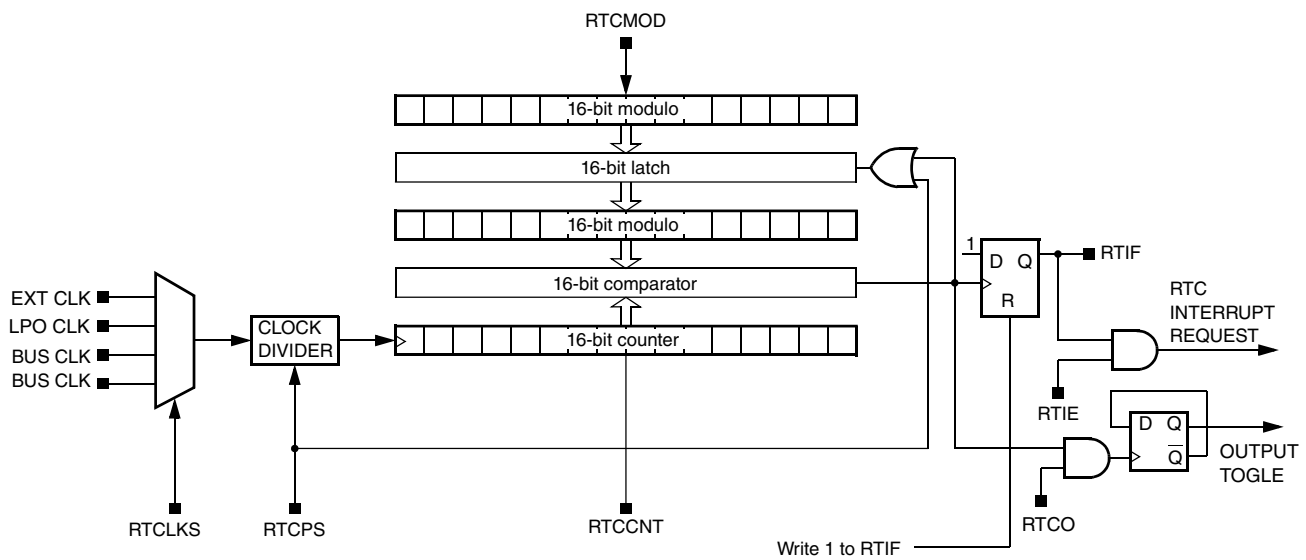


Figure 14-1. Real-time counter (RTC) block diagram

14.3 External signal description

RTCO is the output of RTC. After MCU reset, the RTC_SC1[RTCO] is set to high. When the counter overflows, the output is toggled.

14.4 Register definition

The RTC includes a status and control register, a 16-bit counter register, and a 16-bit modulo register.

RTC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
306A	RTC Status and Control Register 1 (RTC_SC1)	8	R/W	00h	14.4.1/403
306B	RTC Status and Control Register 2 (RTC_SC2)	8	R/W	00h	14.4.2/404
306C	RTC Modulo Register: High (RTC_MODH)	8	R/W	00h	14.4.3/405
306D	RTC Modulo Register: Low (RTC_MODL)	8	R/W	00h	14.4.4/405
306E	RTC Counter Register: High (RTC_CNTH)	8	R	00h	14.4.5/406
306F	RTC Counter Register: Low (RTC_CNTL)	8	R	00h	14.4.6/406

14.4.1 RTC Status and Control Register 1 (RTC_SC1)

RTC_SC1 contains the real-time interrupt status flag (RTIF), and the toggle output enable bit (RTCO).

Address: 306Ah base + 0h offset = 306Ah

Bit	7	6	5	4	3	2	1	0
Read	RTIF	RTIE	0	RTCO	0			
Write								
Reset	0	0	0	0	0	0	0	0

RTC_SC1 field descriptions

Field	Description
7 RTIF	Real-Time Interrupt Flag This status bit indicates the RTC counter register reached the value in the RTC modulo register. Writing a logic 0 has no effect. Writing a logic 1 clears the bit and the real-time interrupt request. Reset clears RTIF to 0. 0 RTC counter has not reached the value in the RTC modulo register. 1 RTC counter has reached the value in the RTC modulo register.
6 RTIE	Real-Time Interrupt Enable This read/write bit enables real-time interrupts. If RTIE is set, then an interrupt is generated when RTIF is set. Reset clears RTIE to 0.

Table continues on the next page...

RTC_SC1 field descriptions (continued)

Field	Description
	0 Real-time interrupt requests are disabled. Use software polling. 1 Real-time interrupt requests are enabled.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 RTCO	Real-Time Counter Output The read/write bit enables real-time to toggle output on pinout. If this bit is set, the RTCO pinout will be toggled when RTC counter overflows. 0 Real-time counter output disabled. 1 Real-time counter output enabled.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

14.4.2 RTC Status and Control Register 2 (RTC_SC2)

RTC_SC2 contains the clock select bits (RTCLKS) and the prescaler select bits (RTCPS).

Address: 306Ah base + 1h offset = 306Bh

Bit	7	6	5	4	3	2	1	0
Read	RTCLKS		0			RTCPS		
Write								
Reset	0	0	0	0	0	0	0	0

RTC_SC2 field descriptions

Field	Description
7–6 RTCLKS	Real-Time Clock Source Select These two read/write bits select the clock source input to the RTC prescaler. Changing the clock source clears the prescaler and RTCCNT counters. Reset clears RTCLKS to 00. 00 External clock source. 01 Real-time clock source is 1 kHz. 10 Bus clock. 11 Bus clock.
5–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RTCPS	Real-Time Clock Prescaler Select These four read/write bits select binary-based or decimal-based divide-by values for the clock source. Changing the prescaler value clears the prescaler and RTCCNT counters. Reset clears RTCPS to 0000. 000 Off 001 If RTCLKS = x0, it is 1; if RTCLKS = x1, it is 128.

Table continues on the next page...

RTC_SC2 field descriptions (continued)

Field	Description
	010 If RTCLKS = x0, it is 2; if RTCLKS = x1, it is 256. 011 If RTCLKS = x0, it is 4; if RTCLKS = x1, it is 512. 100 If RTCLKS = x0, it is 8; if RTCLKS = x1, it is 1024. 101 If RTCLKS = x0, it is 16; if RTCLKS = x1, it is 2048. 110 If RTCLKS = x0, it is 32; if RTCLKS = x1, it is 100. 111 If RTCLKS = x0, it is 64; if RTCLKS = x1, it is 1000.

14.4.3 RTC Modulo Register: High (RTC_MODH)

RTC_MODH, together with RTC_MODL, indicates the value of the 16-bit modulo value.

Address: 306Ah base + 2h offset = 306Ch

Bit	7	6	5	4	3	2	1	0
Read Write	MODH							
Reset	0	0	0	0	0	0	0	0

RTC_MODH field descriptions

Field	Description
MODH	RTC Modulo High These sixteen read/write bits, MODH and MODL, contain the modulo value used to reset the count to 0x0000 upon a compare match and set the RTIF status bit. A value of 0x00 of the MODH an MODL sets the RTIF bit on each rising edge of the prescaler output. Reset sets the modulo to 0x00.

14.4.4 RTC Modulo Register: Low (RTC_MODL)

RTC_MODL, together with RTC_MODH, indicates the value of the 16-bit modulo value.

Address: 306Ah base + 3h offset = 306Dh

Bit	7	6	5	4	3	2	1	0
Read Write	MODL							
Reset	0	0	0	0	0	0	0	0

RTC_MODL field descriptions

Field	Description
MODL	RTC Modulo Low

RTC_MODL field descriptions (continued)

Field	Description
	These sixteen read/write bits, MODH and MODL, contain the modulo value used to reset the count to 0x0000 upon a compare match and set the RTIF status bit. A value of 0x00 of the MODH an MODL sets the RTIF bit on each rising edge of the prescaler output. Reset sets the modulo to 0x00.

14.4.5 RTC Counter Register: High (RTC_CNTH)

RTC_CNTH, together with RTC_CNTL, indicates the read-only value of the current RTC count of the 16-bit counter.

NOTE

The RTC_CNTL must be read first to lock the counter and then read RTC_CNTH to correctly read 16-bit counter.

Address: 306Ah base + 4h offset = 306Eh

Bit	7	6	5	4	3	2	1	0
Read	CNTH							
Write								
Reset	0	0	0	0	0	0	0	0

RTC_CNTH field descriptions

Field	Description
CNTH	RTC Count High CNTH and CNTL contain the current value of the 16-bit counter. Writes have no effect to this register. Reset or writing different values to RTCLKS and RTCPS clear the count to 0x00.

14.4.6 RTC Counter Register: Low (RTC_CNTL)

RTC_CNTL, together with RTC_CNTH, indicates the read-only value of the current RTC count of the 16-bit counter.

Address: 306Ah base + 5h offset = 306Fh

Bit	7	6	5	4	3	2	1	0
Read	CNTL							
Write								
Reset	0	0	0	0	0	0	0	0

RTC_CNTL field descriptions

Field	Description
CNTL	RTC Count Low CNTH and CNTL contain the current value of the 16-bit counter. Writes have no effect to this register. Reset or writing different values to RTCLKS and RTCPS clear the count to 0x00.

14.5 Functional description

The RTC is composed of a main 16-bit up-counter with a 16-bit modulo register, a clock source selector, and a prescaler block with binary-based and decimal-based selectable values. The module also contains software selectable interrupt logic and toggle logic for pinout.

After any MCU reset, the counter is stopped and reset to 0x0000, the modulus register is set to 0x0000, and the prescaler is off. The external oscillator clock is selected as the default clock source. To start the prescaler, write any value other than 0 to the Prescaler Select field (RTC_SC2[RTCPS]).

The clock sources are software selectable: the external oscillator (XOSC), on-chip low power oscillator (LPO), and bus clock. The RTC Clock Select field (RTC_SC2[RTCLKS]) is used to select the desired clock source to the prescaler dividers. If a different value is written to RTC_SC2[RTCLKS], the prescaler and CNTH and RTC_CNTL counters are reset to 0x00.

RTC_SC2[RTCPS] and RTC_SC2[RTCLKS] select the desired divide-by value. If a different value is written to RTC_SC2[RTCPS], the prescaler and RTCCNT counters are reset to 0x00. The following table shows different prescaler period values.

Table 14-1. Prescaler period

RTCPS	32768Hz XOSC clock source prescaler period (RTCLKS = 00)	LPO clock (1 kHz) source prescaler period (RTCLKS = 01)	Bus clock (8 MHz) source prescaler period (RTCLKS = 10)	Bus clock (8 MHz) source prescaler period (RTCLKS = 11)
000	Off	Off	Off	Off
001	30.5176 µs	128 ms	125 ns	16 µs
010	61.0351 µs	256 ms	250 ns	32 µs
011	122.0703 µs	512 ms	500 ns	64 µs
100	244.1406 µs	1024 ms	1 µs	128 µs
101	488.28125 µs	2048 ms	2 µs	256 µs
110	976.5625 µs	100 ms	4 µs	12.5 µs
111	1.9531 ms	1 s	8 µs	125 µs

The RTC Modulo register (RTC_MODH and RTC_MODL) allows the compare value to be set to any value from 0x0000 to 0xFFFF. When the counter is active, the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter resets to 0x0000 and continues counting. The Real-Time Interrupt Flag (RTC_SC1[RTIF]) is set whenever a match occurs. The flag sets on the transition from the modulo value to 0x0000. The modulo value written to RTC_MODH and RTC_MODL is latched until the RTC counter overflows or RTC_SC2[RTCPS] is selected nonzero.

The RTC allows for an interrupt to be generated whenever RTC_SC1[RTIF] is set. To enable the real-time interrupt, set the Real-Time Interrupt Enable field (RTC_SC1[RTIE]). RTC_SC1[RTIF] is cleared by writing a 1 to RTC_SC1[RTIF].

The RTC also allows an output to external pinout by toggling the level. RTC_SC1[RTCO] must be set to enable toggling external pinout. The level depends on the previous state of the pinout when the counter overflows if this function is active.

14.5.1 RTC operation example

This section shows an example of the RTC operation as the counter reaches a matching value from the modulo register.

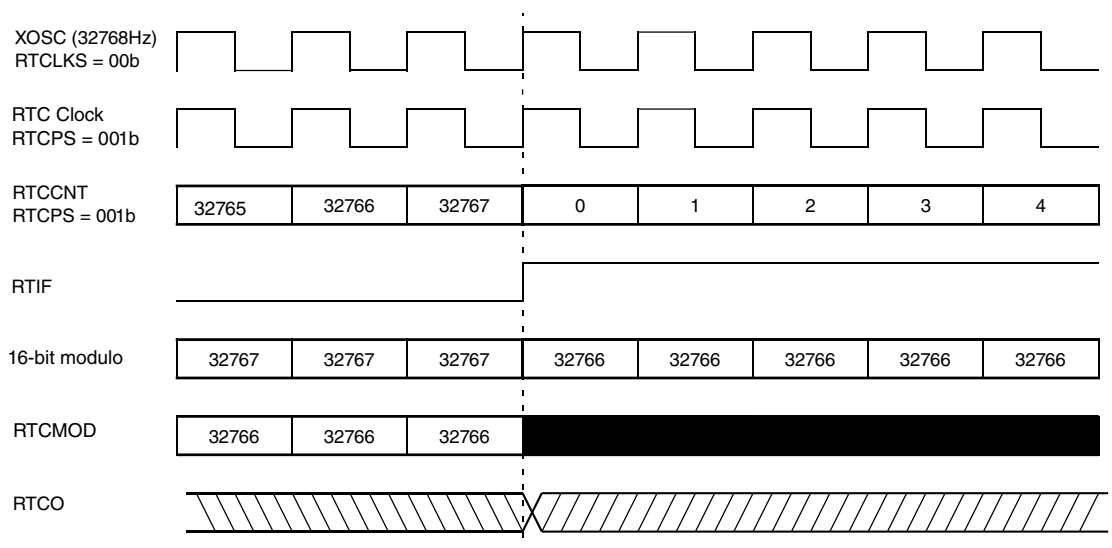


Figure 14-2. RTC counter overflow example

In the above example, the external clock source is selected. The prescaler is set to RTC_SC2[RTCPS] = 001b or passthrough. The actual modulo value used by 16-bit comparator is 32767, when the modulo value in the RTC_MODH and RTC_MODL registers is set to 32766. When the counter, RTC_CNTH and RTC_CNTL, reaches the

modulo value of 32767, the counter overflows to 0x00 and continues counting. The modulo value is updated by fetching from RTC_MODH and RTC_MODL registers. The real-time interrupt flag, RTC_SC1[RTIF], sets when the counter value changes from 0x7FFF to 0x0000. The RTC_SC1[RTCO] toggles as well when the RTC_SC1[RTIF] is set.

14.6 Initialization/application information

This section provides example code to give some basic direction to a user on how to initialize and configure the RTC module. The example software is implemented in C language.

The example below shows how to implement time of day with the RTC using the XOSC clock source to achieve the lowest possible power consumption.

Example: 14.6.1 Software calendar implementation in RTC ISR

```
/* Initialize the elapsed time counters */
Seconds = 0;
Minutes = 0;
Hours = 0;
Days=0;

/* Configure RTC to interrupt every 1 second from XOSC (32.768KHz) clock source */
RTC_MOD = 511; // overflow every 512 times
RTC_SC2 = RTC_SC2_RTCPS_MASK; // external 32768 clock selected with 1/64 predivider.
RTC_SC1 = RTC_SC1_RTIF_MASK | RTC_SC1_RTIE_MASK; // interrupt cleared and enabled

/*********************************************************************
Function Name : RTC_ISR
Notes : Interrupt service routine for RTC module.
*********************************************************************/
void RTC_ISR(void)
{
/* Clears the interrupt flag, RTIF, and interrupt request */
RTC_SC1 |= RTC_SC1_RTIF_MASK;

/* RTC interrupts every 1 Second */
Seconds++;

/* 60 seconds in a minute */
if (Seconds > 59)
{
Minutes++;
Seconds = 0;
}

/* 60 minutes in an hour */
if (Minutes > 59)
{
Hours++;
Minutes = 0;
}

/* 24 hours in a day */
if (Hours > 23)
{
```

```
Days ++;
Hours = 0;
}
}
```

Chapter 15
Serial communications interface (SCI)

15.1 Introduction

15.1.1 Features

Features of SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Programmable 1-bit or 2-bit stop bits (SCI2 does not support 2-bit stop bits)
- Receiver wakeup by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

15.1.2 Modes of operation

See Section Functional description for details concerning SCI operation in these modes:

- 8- and 9-bit data modes
- Stop mode operation

- Loop mode
- Single-wire mode

15.1.3 Block diagram

The following figure shows the transmitter portion of the SCI.

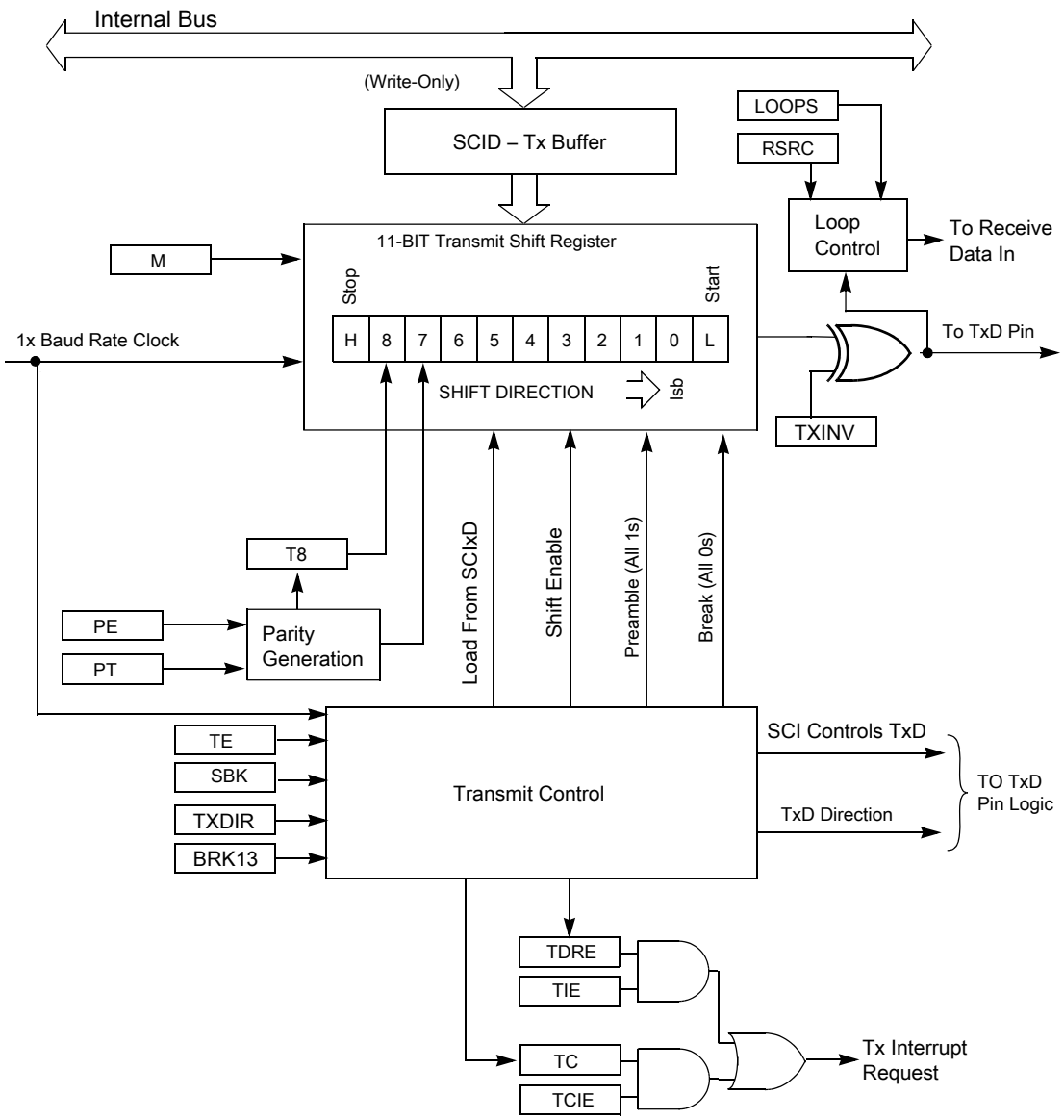


Figure 15-1. SCI transmitter block diagram

The following figure shows the receiver portion of the SCI.

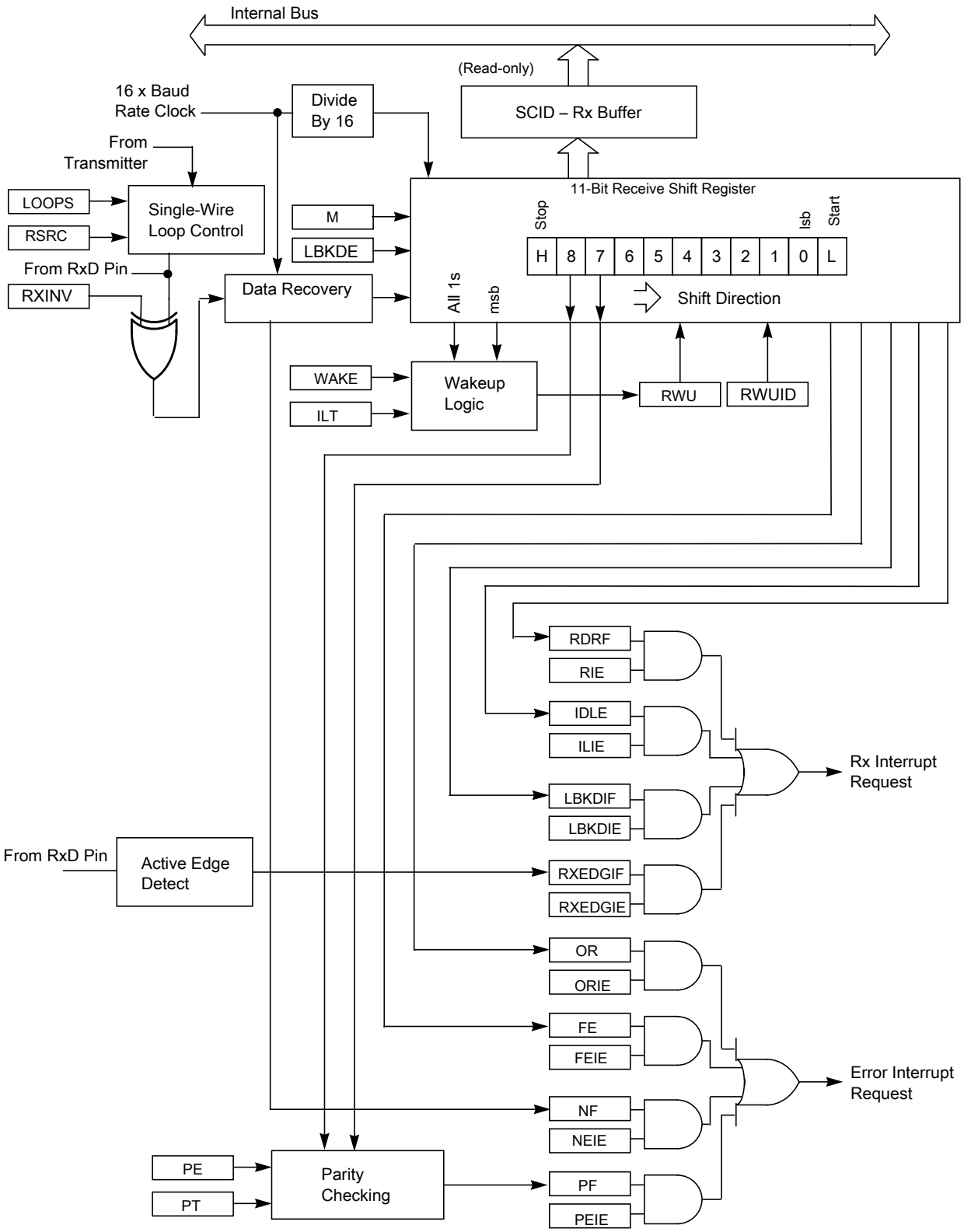


Figure 15-2. SCI receiver block diagram

15.2 SCI signal descriptions

The SCI signals are shown in the table found here.

Table 15-1. SCI signal descriptions

Signal	Description	I/O
RxD	Receive data	I
TxD	Transmit data	I/O

15.2.1 Detailed signal descriptions

The detailed signal descriptions of the SCI are shown in the following table.

Table 15-2. SCI—Detailed signal descriptions

Signal	I/O	Description	
RxD	I	Receive data. Serial data input to receiver.	
		State meaning	Whether RxD is interpreted as a 1 or 0 depends on the bit encoding method along with other configuration settings.
		Timing	Sampled at a frequency determined by the module clock divided by the baud rate.
TxD	I/O	Transmit data. Serial data output from transmitter.	
		State meaning	Whether TxD is interpreted as a 1 or 0 depends on the bit encoding method along with other configuration settings.
		Timing	Driven at the beginning or within a bit time according to the bit encoding method along with other configuration settings. Otherwise, transmissions are independent of reception timing.

15.3 Register definition

The SCI has 8-bit registers to control baud rate, select SCI options, report SCI status, and for transmit/receive data.

Refer to the direct-page register summary in the memory chapter of this document or the absolute address assignments for all SCI registers. This section refers to registers and control bits only by their names. An NXP-provided equate or header file is used to translate these names into the appropriate absolute addresses.

SCI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3080	SCI Baud Rate Register: High (SCI0_BDH)	8	R/W	00h	15.3.1/415
3081	SCI Baud Rate Register: Low (SCI0_BDL)	8	R/W	04h	15.3.2/416
3082	SCI Control Register 1 (SCI0_C1)	8	R/W	00h	15.3.3/417
3083	SCI Control Register 2 (SCI0_C2)	8	R/W	00h	15.3.4/418
3084	SCI Status Register 1 (SCI0_S1)	8	R	C0h	15.3.5/419
3085	SCI Status Register 2 (SCI0_S2)	8	R/W	00h	15.3.6/421
3086	SCI Control Register 3 (SCI0_C3)	8	R/W	00h	15.3.7/423
3087	SCI Data Register (SCI0_D)	8	R/W	00h	15.3.8/424
3088	SCI Baud Rate Register: High (SCI1_BDH)	8	R/W	00h	15.3.1/415
3089	SCI Baud Rate Register: Low (SCI1_BDL)	8	R/W	04h	15.3.2/416
308A	SCI Control Register 1 (SCI1_C1)	8	R/W	00h	15.3.3/417
308B	SCI Control Register 2 (SCI1_C2)	8	R/W	00h	15.3.4/418
308C	SCI Status Register 1 (SCI1_S1)	8	R	C0h	15.3.5/419
308D	SCI Status Register 2 (SCI1_S2)	8	R/W	00h	15.3.6/421
308E	SCI Control Register 3 (SCI1_C3)	8	R/W	00h	15.3.7/423
308F	SCI Data Register (SCI1_D)	8	R/W	00h	15.3.8/424
3090	SCI Baud Rate Register: High (SCI2_BDH)	8	R/W	00h	15.3.1/415
3091	SCI Baud Rate Register: Low (SCI2_BDL)	8	R/W	04h	15.3.2/416
3092	SCI Control Register 1 (SCI2_C1)	8	R/W	00h	15.3.3/417
3093	SCI Control Register 2 (SCI2_C2)	8	R/W	00h	15.3.4/418
3094	SCI Status Register 1 (SCI2_S1)	8	R	C0h	15.3.5/419
3095	SCI Status Register 2 (SCI2_S2)	8	R/W	00h	15.3.6/421
3096	SCI Control Register 3 (SCI2_C3)	8	R/W	00h	15.3.7/423
3097	SCI Data Register (SCI2_D)	8	R/W	00h	15.3.8/424

15.3.1 SCI Baud Rate Register: High (SCIx_BDH)

This register, along with SCI_BDL, controls the prescale divisor for SCI baud rate generation. To update the 13-bit baud rate setting [SBR12:SBR0], first write to SCI_BDH to buffer the high half of the new value and then write to SCI_BDL. The working value in SCI_BDH does not change until SCI_BDL is written.

Address: Base address + 0h offset

Bit	7	6	5	4	3	2	1	0
Read Write	LBKDIE	RXEDGIE	SBNS	SBR				
Reset	0	0	0	0	0	0	0	0

SCIx_BDH field descriptions

Field	Description
7 LBKDIE	LIN Break Detect Interrupt Enable (for LBKDIF) 0 Hardware interrupts from SCI_S2[LBKDIF] disabled (use polling). 1 Hardware interrupt requested when SCI_S2[LBKDIF] flag is 1.
6 RXEDGIE	RxD Input Active Edge Interrupt Enable (for RXEDGIF) 0 Hardware interrupts from SCI_S2[RXEDGIF] disabled (use polling). 1 Hardware interrupt requested when SCI_S2[RXEDGIF] flag is 1.
5 SBNS	Stop Bit Number Select SBNS determines whether data characters are one or two stop bits. **NOTE:** For SCI2, this field is masked. 0 One stop bit. 1 Two stop bit.
SBR	Baud Rate Modulo Divisor. The 13 bits in SBR[12:0] are referred to collectively as BR, and they set the modulo divide rate for the SCI baud rate generator. When BR is cleared, the SCI baud rate generator is disabled to reduce supply current. When BR is 1 - 8191, the SCI baud rate equals BUSCLK/(16×BR).

15.3.2 SCI Baud Rate Register: Low (SCIx_BDL)

This register, along with SCI_BDH, control the prescale divisor for SCI baud rate generation. To update the 13-bit baud rate setting [SBR12:SBR0], first write to SCI_BDH to buffer the high half of the new value and then write to SCI_BDL. The working value in SCI_BDH does not change until SCI_BDL is written.

SCI_BDL is reset to a non-zero value, so after reset the baud rate generator remains disabled until the first time the receiver or transmitter is enabled; that is, SCI_C2[RE] or SCI_C2[TE] bits are written to 1.

Address: Base address + 1h offset

Bit	7	6	5	4	3	2	1	0
Read Write	SBR							
Reset	0	0	0	0	0	1	0	0

SCIx_BDL field descriptions

Field	Description
SBR	Baud Rate Modulo Divisor These 13 bits in SBR[12:0] are referred to collectively as BR. They set the modulo divide rate for the SCI baud rate generator. When BR is cleared, the SCI baud rate generator is disabled to reduce supply current. When BR is 1 - 8191, the SCI baud rate equals BUSCLK/(16×BR).

15.3.3 SCI Control Register 1 (SCIx_C1)

This read/write register controls various optional features of the SCI system.

Address: Base address + 2h offset

Bit	7	6	5	4	3	2	1	0
Read Write	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
Reset	0	0	0	0	0	0	0	0

SCIx_C1 field descriptions

Field	Description
7 LOOPS	Loop Mode Select Selects between loop back modes and normal 2-pin full-duplex modes. When LOOPS is set, the transmitter output is internally connected to the receiver input. 0 Normal operation - RxD and TxD use separate pins. 1 Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input. (See RSRC bit.) RxD pin is not used by SCI.
6 SCISWAI	SCI Stops in Wait Mode 0 SCI clocks continue to run in wait mode so the SCI can be the source of an interrupt that wakes up the CPU. 1 SCI clocks freeze while CPU is in wait mode.
5 RSRC	Receiver Source Select This bit has no meaning or effect unless the LOOPS bit is set to 1. When LOOPS is set, the receiver input is internally connected to the TxD pin and RSRC determines whether this connection is also connected to the transmitter output. 0 Provided LOOPS is set, RSRC is cleared, selects internal loop back mode and the SCI does not use the RxD pins. 1 Single-wire SCI mode where the TxD pin is connected to the transmitter output and receiver input.
4 M	9-Bit or 8-Bit Mode Select 0 Normal - start + 8 data bits (lsb first) + stop. 1 Receiver and transmitter use 9-bit data characters start + 8 data bits (lsb first) + 9th data bit + stop.
3 WAKE	Receiver Wakeup Method Select 0 Idle-line wakeup. 1 Address-mark wakeup.
2 ILT	Idle Line Type Select Setting this bit to 1 ensures that the stop bits and logic 1 bits at the end of a character do not count toward the 10 or 11 bit times of logic high level needed by the idle line detection logic. 0 Idle character bit count starts after start bit. 1 Idle character bit count starts after stop bit.

Table continues on the next page...

SCIx_C1 field descriptions (continued)

Field	Description
1 PE	Parity Enable Enables hardware parity generation and checking. When parity is enabled, the most significant bit (msb) of the data character, eighth or ninth data bit, is treated as the parity bit. 0 No hardware parity generation or checking. 1 Parity enabled.
0 PT	Parity Type Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even. 0 Even parity. 1 Odd parity.

15.3.4 SCI Control Register 2 (SCIx_C2)

This register can be read or written at any time.

Address: Base address + 3h offset

Bit	7	6	5	4	3	2	1	0
Read Write	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0

SCIx_C2 field descriptions

Field	Description
7 TIE	Transmit Interrupt Enable for TDRE 0 Hardware interrupts from TDRE disabled; use polling. 1 Hardware interrupt requested when TDRE flag is 1.
6 TCIE	Transmission Complete Interrupt Enable for TC 0 Hardware interrupts from TC disabled; use polling. 1 Hardware interrupt requested when TC flag is 1.
5 RIE	Receiver Interrupt Enable for RDRF 0 Hardware interrupts from RDRF disabled; use polling. 1 Hardware interrupt requested when RDRF flag is 1.
4 ILIE	Idle Line Interrupt Enable for IDLE 0 Hardware interrupts from IDLE disabled; use polling. 1 Hardware interrupt requested when IDLE flag is 1.
3 TE	Transmitter Enable

Table continues on the next page...

SCIx_C2 field descriptions (continued)

Field	Description
	TE must be 1 to use the SCI transmitter. When TE is set, the SCI forces the TxD pin to act as an output for the SCI system. When the SCI is configured for single-wire operation (LOOPS = RSRC = 1), TXDIR controls the direction of traffic on the single SCI communication line (TxD pin). TE can also queue an idle character by clearing TE then setting TE while a transmission is in progress. When TE is written to 0, the transmitter keeps control of the port TxD pin until any data, queued idle, or queued break character finishes transmitting before allowing the pin to revert to a general-purpose I/O pin. 0 Transmitter off. 1 Transmitter on.
2 RE	Receiver Enable When the SCI receiver is off, the RxD pin reverts to being a general-purpose port I/O pin. If LOOPS is set the RxD pin reverts to being a general-purpose I/O pin even if RE is set. 0 Receiver off. 1 Receiver on.
1 RWU	Receiver Wakeup Control This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wakeup condition. The wakeup condition is an idle line between messages, WAKE = 0, idle-line wakeup, or a logic 1 in the most significant data bit in a character, WAKE = 1, address-mark wakeup. Application software sets RWU and, normally, a selected hardware condition automatically clears RWU. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wakeup condition.
0 SBK	Send Break Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 or 12, 13 or 14 or 15 if BRK13 = 1, bit times of logic 0 are queued as long as SBK is set. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

15.3.5 SCI Status Register 1 (SCIx_S1)

This register has eight read-only status flags. Writes have no effect. Special software sequences, which do not involve writing to this register, clear these status flags.

Address: Base address + 4h offset

Bit	7	6	5	4	3	2	1	0
Read	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write								
Reset	1	1	0	0	0	0	0	0

SCIx_S1 field descriptions

Field	Description
7 TDRE	Transmit Data Register Empty Flag TDRE is set out of reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCI_S1 with TDRE set and then write to the SCI data register (SCI_D). 0 Transmit data register (buffer) full. 1 Transmit data register (buffer) empty.
6 TC	Transmission Complete Flag TC is set out of reset and when TDRE is set and no data, preamble, or break character is being transmitted. TC is cleared automatically by reading SCI_S1 with TC set and then doing one of the following: • Write to the SCI data register (SCI_D) to transmit new data • Queue a preamble by changing TE from 0 to 1 • Queue a break character by writing 1 to SCI_C2[SBK] 0 Transmitter active (sending data, a preamble, or a break). 1 Transmitter idle (transmission activity complete).
5 RDRF	Receive Data Register Full Flag RDRF becomes set when a character transfers from the receive shifter into the receive data register (SCI_D). To clear RDRF, read SCI_S1 with RDRF set and then read the SCI data register (SCI_D). 0 Receive data register empty. 1 Receive data register full.
4 IDLE	Idle Line Flag IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT is cleared, the receiver starts counting idle bit times after the start bit. If the receive character is all 1s, these bit times and the stop bits time count toward the full character time of logic high, 10 or 11 bit times depending on the M control bit, needed for the receiver to detect an idle line. When ILT is set, the receiver doesn't start counting idle bit times until after the stop bits. The stop bits and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line. To clear IDLE, read SCI_S1 with IDLE set and then read the SCI data register (SCI_D). After IDLE has been cleared, it cannot become set again until after a new character has been received and RDRF has been set. IDLE is set only once even if the receive line remains idle for an extended period. 0 No idle line detected. 1 Idle line was detected.
3 OR	Receiver Overrun Flag OR is set when a new serial character is ready to be transferred to the receive data register (buffer), but the previously received character has not been read from SCI_D yet. In this case, the new character, and all associated error information, is lost because there is no room to move it into SCI_D. To clear OR, read SCI_S1 with OR set and then read the SCI data register (SCI_D). 0 No overrun. 1 Receive overrun (new SCI data lost).
2 NF	Noise Flag The advanced sampling technique used in the receiver takes seven samples during the start bit and three samples in each data bit and the stop bits. If any of these samples disagrees with the rest of the samples

Table continues on the next page...

SCIx_S1 field descriptions (continued)

Field	Description
	within any bit time in the frame, the flag NF is set at the same time as RDRF is set for the character. To clear NF, read SCI_S1 and then read the SCI data register (SCI_D). 0 No noise detected. 1 Noise detected in the received character in SCI_D.
1 FE	Framing Error Flag FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bits was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCI_S1 with FE set and then read the SCI data register (SCI_D). 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
0 PF	Parity Error Flag PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCI_S1 and then read the SCI data register (SCI_D). 0 No parity error. 1 Parity error.

15.3.6 SCI Status Register 2 (SCIx_S2)

This register contains one read-only status flag.

When using an internal oscillator in a LIN system, it is necessary to raise the break detection threshold one bit time. Under the worst case timing conditions allowed in LIN, it is possible that a 0x00 data character can appear to be 10.26 bit times long at a slave running 14% faster than the master. This would trigger normal break detection circuitry designed to detect a 10-bit break symbol. When the LBKDE bit is set, framing errors are inhibited and the break detection threshold changes from 10 bits to 11 bits, preventing false detection of a 0x00 data character as a LIN break symbol.

Address: Base address + 5h offset

Bit	7	6	5	4	3	2	1	0
Read	LBKDIF	RXEDGIF	0	RXINV	RWUID	BRK13	LBKDE	RAF
Write								
Reset	0	0	0	0	0	0	0	0

SCIx_S2 field descriptions

Field	Description
7 LBKDIF	LIN Break Detect Interrupt Flag LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a 1 to it.

Table continues on the next page...

SCIx_S2 field descriptions (continued)

Field	Description
	0 No LIN break character has been detected. 1 LIN break character has been detected.
6 RXEDGIF	RxD Pin Active Edge Interrupt Flag RXEDGIF is set when an active edge, falling if RXINV = 0, rising if RXINV=1, on the RxD pin occurs. RXEDGIF is cleared by writing a 1 to it. 0 No active edge on the receive pin has occurred. 1 An active edge on the receive pin has occurred.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 RXINV	Receive Data Inversion Setting this bit reverses the polarity of the received data input. **NOTE:** Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle. 0 Receive data not inverted. 1 Receive data inverted.
3 RWUID	Receive Wake Up Idle Detect RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit. 0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. 1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character.
2 BRK13	Break Character Generation Length BRK13 selects a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. 0 Break character is transmitted with length of 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1). 1 Break character is transmitted with length of 13 bit times (if M = 0, SBNS = 0) or 14 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 15 (if M = 1, SBNS = 1).
1 LBKDE	LIN Break Detection Enable LBKDE selects a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting. 0 Break character is detected at length 10 bit times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1). 1 Break character is detected at length of 11 bit times (if M = 0, SBNS = 0) or 12 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 13 (if M = 1, SBNS = 1).
0 RAF	Receiver Active Flag RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. 0 SCI receiver idle waiting for a start bit. 1 SCI receiver active (RxD input not idle).

15.3.7 SCI Control Register 3 (SCIx_C3)

Address: Base address + 6h offset

Bit	7	6	5	4	3	2	1	0
Read	R8	T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
Write								
Reset	0	0	0	0	0	0	0	0

SCIx_C3 field descriptions

Field	Description
7 R8	Ninth Data Bit for Receiver When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the msb of the buffered data in the SCI_D register. When reading 9-bit data, read R8 before reading SCI_D because reading SCI_D completes automatic flag clearing sequences that could allow R8 and SCI_D to be overwritten with new data.
6 T8	Ninth Data Bit for Transmitter When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the msb of the data in the SCI_D register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCI_D is written so T8 should be written, if it needs to change from its previous value, before SCI_D is written. If T8 does not need to change in the new value, such as when it is used to generate mark or space parity, it need not be written each time SCI_D is written.
5 TXDIR	TxD Pin Direction in Single-Wire Mode When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin. 0 TxD pin is an input in single-wire mode. 1 TxD pin is an output in single-wire mode.
4 TXINV	Transmit Data Inversion Setting this bit reverses the polarity of the transmitted data output. **NOTE:** Setting TXINV inverts the TxD output for all cases: data bits, start and stop bits, break, and idle. 0 Transmit data not inverted. 1 Transmit data inverted.
3 ORIE	Overrun Interrupt Enable This bit enables the overrun flag (OR) to generate hardware interrupt requests. 0 OR interrupts disabled; use polling. 1 Hardware interrupt requested when OR is set.
2 NEIE	Noise Error Interrupt Enable This bit enables the noise flag (NF) to generate hardware interrupt requests. 0 NF interrupts disabled; use polling). 1 Hardware interrupt requested when NF is set.

Table continues on the next page...

SCIx_C3 field descriptions (continued)

Field	Description
1 FEIE	Framing Error Interrupt Enable This bit enables the framing error flag (FE) to generate hardware interrupt requests. 0 FE interrupts disabled; use polling). 1 Hardware interrupt requested when FE is set.
0 PEIE	Parity Error Interrupt Enable This bit enables the parity error flag (PF) to generate hardware interrupt requests. 0 PF interrupts disabled; use polling). 1 Hardware interrupt requested when PF is set.

15.3.8 SCI Data Register (SCIx_D)

This register is actually two separate registers. Reads return the contents of the read-only receive data buffer and writes go to the write-only transmit data buffer. Reads and writes of this register are also involved in the automatic flag clearing mechanisms for the SCI status flags.

Address: Base address + 7h offset

Bit	7	6	5	4	3	2	1	0
Read Write	R7T7	R6T6	R5T5	R4T4	R3T3	R2T2	R1T1	R0T0
Reset	0	0	0	0	0	0	0	0

SCIx_D field descriptions

Field	Description
7 R7T7	Read receive data buffer 7 or write transmit data buffer 7.
6 R6T6	Read receive data buffer 6 or write transmit data buffer 6.
5 R5T5	Read receive data buffer 5 or write transmit data buffer 5.
4 R4T4	Read receive data buffer 4 or write transmit data buffer 4.
3 R3T3	Read receive data buffer 3 or write transmit data buffer 3.
2 R2T2	Read receive data buffer 2 or write transmit data buffer 2.
1 R1T1	Read receive data buffer 1 or write transmit data buffer 1.
0 R0T0	Read receive data buffer 0 or write transmit data buffer 0.

SCIx_D field descriptions (continued)

Field	Description

15.4 Functional description

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs.

The SCI comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. During normal operation, the MCU monitors the status of the SCI, writes the data to be transmitted, and processes received data. The following describes each of the blocks of the SCI.

15.4.1 Baud rate generation

As shown in the figure found here, the clock source for the SCI baud rate generator is the bus-rate clock.

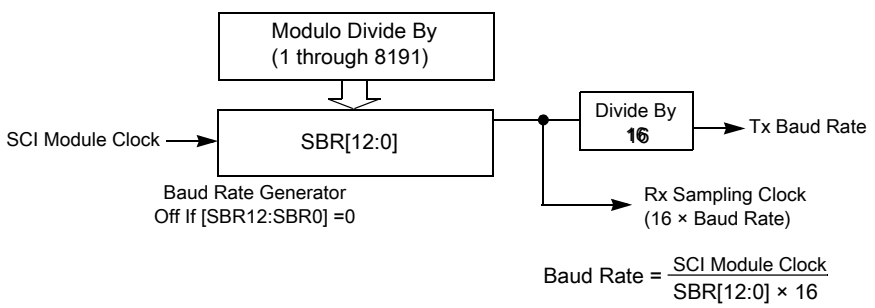


Figure 15-3. SCI baud rate generation

SCI communications require the transmitter and receiver, which typically derive baud rates from independent clock sources, to use the same baud rate. Allowed tolerance on this baud frequency depends on the details of how the receiver synchronizes to the leading edge of the start bit and how bit sampling is performed.

The MCU resynchronizes to bit boundaries on every high-to-low transition. In the worst case, there are no such transitions in the full 10- or 11-bit or 12-bittime character frame so any mismatch in baud rate is accumulated for the whole character time. For an NXP SCI system whose bus frequency is driven by a crystal, the allowed baud rate mismatch is about ±4.5 percent for 8-bit data format and about ±4 percent for 9-bit data format.

Although baud rate modulo divider settings do not always produce baud rates that exactly match standard rates, it is normally possible to get within a few percent, which is acceptable for reliable communications.

15.4.2 Transmitter functional description

This section describes the overall block diagram for the SCI transmitter, as well as specialized functions for sending break and idle characters.

The transmitter output (TxD) idle state defaults to logic high, SCI_C3[TXINV] is cleared following reset. The transmitter output is inverted by setting SCI_C3[TXINV]. The transmitter is enabled by setting the TE bit in SCI_C2. This queues a preamble character that is one full character frame of the idle state. The transmitter then remains idle until data is available in the transmit data buffer. Programs store data into the transmit data buffer by writing to the SCI data register (SCI_D).

The central element of the SCI transmitter is the transmit shift register that is 10 or 11 or 12 bits long depending on the setting in the SCI_C1[M] control bit and SCI_BDH[SBNS] bit. For the remainder of this section, assume SCI_C1[M] is cleared, SCI_BDH[SBNS] is also cleared, selecting the normal 8-bit data mode. In 8-bit data mode, the shift register holds a start bit, eight data bits, and a stop bit. When the transmit shift register is available for a new SCI character, the value waiting in the transmit data register is transferred to the shift register, synchronized with the baud rate clock, and the transmit data register empty (SCI_S1[TDRE]) status flag is set to indicate another character may be written to the transmit data buffer at SCI_D.

NOTE

Always read SCI_S1 before writing to SCI_D to allow data to be transmitted.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TxD pin, the transmitter sets the transmit complete flag and enters an idle mode, with TxD high, waiting for more characters to transmit.

Writing 0 to SCI_C2[TE] does not immediately release the pin to be a general-purpose I/O pin. Any transmit activity in progress must first be completed. This includes data characters in progress, queued idle characters, and queued break characters.

15.4.2.1 Send break and queued idle

SCI_C2[SBK] sends break characters originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0, 10 bit times including the start and stop bits. A longer break of 13 bit times can be enabled by setting SCI_S2[BRK13]. Normally, a program would wait for SCI_S1[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, write 1, and then write 0 to SCI_C2[SBK]. This action queues a break character to be sent as soon as the shifter is available. If SCI_C2[SBK] remains 1 when the queued break moves into the shifter, synchronized to the baud rate clock, an additional break character is queued. If the receiving device is another NXP SCI, the break characters are received as 0s in all eight data bits and a framing error (SCI_S1[FE] = 1) occurs.

When idle-line wake-up is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for SCI_S1[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the SCI_C2[TE] bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while SCI_C2[TE] is cleared, the SCI transmitter never actually releases control of the TxD pin. If there is a possibility of the shifter finishing while SCI_C2[TE] is cleared, set the general-purpose I/O controls so the pin shared with TxD is an output driving a logic 1. This ensures that the TxD line looks like a normal idle line even if the SCI loses control of the port pin between writing 0 and then 1 to SCI_C2[TE].

The length of the break character is affected by the SCI_S2[BRK13] and SCI_C1[M] as shown below.

Table 15-3. Break character length

BRK13	M	SBNS	Break character length
0	0	0	10 bit times
0	0	1	11 bit times
0	1	0	11 bit times
0	1	1	12 bit times
1	0	0	13 bit times
1	0	1	14 bit times
1	1	0	14 bit times
1	1	1	15 bit times

15.4.3 Receiver functional description

In this section, the receiver block diagram is a guide for the overall receiver functional description.

Next, the data sampling technique used to reconstruct receiver data is described in more detail. Finally, two variations of the receiver wakeup function are explained.

The receiver input is inverted by setting SCI_S2[RXINV]. The receiver is enabled by setting the SCI_C2[RE] bit. Character frames consist of a start bit of logic 0, eight (or nine) data bits (lsb first), and one (or two) stop bits of logic 1. For information about 9-bit data mode, refer to 8- and 9-bit data modes. For the remainder of this discussion, assume the SCI is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (SCI_S1[RDRF]) status flag is set. If SCI_S1[RDRF] was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program has one full character time after SCI_S1[RDRF] is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (SCI_S1[RDRF] = 1), it gets the data from the receive data register by reading SCI_D. The SCI_S1[RDRF] flag is cleared automatically by a two-step sequence normally satisfied in the course of the user's program that manages receive data. Refer to Interrupts and status flags for more details about flag clearing.

15.4.3.1 Data sampling technique

The SCI receiver uses a 16× baud rate clock for sampling. The oversampling ratio is fixed at 16. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock divides the bit time into 16 segments labeled SCI_D[RT1] through SCI_D[RT16]. When a falling edge is located, three more samples are taken at SCI_D[RT3], SCI_D[RT5], and SCI_D[RT7] to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at SCI_D[RT8], SCI_D[RT9], and SCI_D[RT10] to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at

SCI_D[RT3], SCI_D[RT5], and SCI_D[RT7] are 0 even if one or all of the samples taken at SCI_D[RT8], SCI_D[RT9], and SCI_D[RT10] are 1s. If any sample in any bit time, including the start and stop bits, in a character frame fails to agree with the logic level for that bit, the noise flag (SCI_S1[NF]) is set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges. If an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

In the case of a framing error, the receiver is inhibited from receiving any new characters until the framing error flag is cleared. The receive shift register continues to function, but a complete character cannot transfer to the receive data buffer if SCI_S1[FE] remains set.

15.4.3.2 Receiver wake-up operation

Receiver wake-up is a hardware mechanism that allows an SCI receiver to ignore the characters in a message intended for a different SCI receiver. In such a system, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up control field (SCI_C2[RWU]). When SCI_C2[RWU] is set, the status flags associated with the receiver, (with the exception of the idle bit, IDLE, when SCI_S2[RWUID] is set), are inhibited from setting, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force SCI_C2[RWU] to 0, so all receivers wake up in time to look at the first character(s) of the next message.

15.4.3.2.1 Idle-line wakeup

When wake is cleared, the receiver is configured for idle-line wakeup. In this mode, SCI_C2[RWU] is cleared automatically when the receiver detects a full character time of the idle-line level. The SCI_C1[M] control field selects 8-bit or 9-bit data mode and SCI_BDH[SBNS] selects 1-bit or 2-bit stop bit number that determines how many bit times of idle are needed to constitute a full character time, 10 or 11 or 12 bit times because of the start and stop bits.

When SCII_C2[RWU] is 1 and SCI_S2[RWUID] is 0, the idle condition that wakes up the receiver does not set SCI_S1[IDLE]. The receiver wakes up and waits for the first data character of the next message that sets SCI_S1[RDRF] and generates an interrupt, if enabled. When SCI_S2[RWUID] is 1, any idle condition sets SCI_S1[IDLE] flag and generates an interrupt if enabled, regardless of whether SCI_C2[RWU] is 0 or 1.

The idle-line type (SCI_C1[ILT]) control bit selects one of two ways to detect an idle line. When SCI_C1[ILT] is cleared, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When SCI_C1[ILT] is set, the idle bit counter does not start until after a stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

15.4.3.2.2 Address-mark wakeup

When wake is set, the receiver is configured for address-mark wakeup. In this mode, SCI_C2[RWU] is cleared automatically when the receiver detects a, or two, if SCI_BDH[SBNS] = 1, logic 1 in the most significant bits of a received character, eighth bit when SCI_C1[M] is cleared and ninth bit when SCI_C1[M] is set.

Address-mark wakeup allows messages to contain idle characters, but requires the msb be reserved for use in address frames. The one, or two, if SCI_BDH[SBNS] = 1, logic 1s msb of an address frame clears the SCI_C2[RWU] bit before the stop bits are received and sets the SCI_S1[RDRF] flag. In this case, the character with the msb set is received even though the receiver was sleeping during most of this character time.

15.4.4 Interrupts and status flags

The SCI system has three separate interrupt vectors to reduce the amount of software needed to isolate the cause of the interrupt.

One interrupt vector is associated with the transmitter for SCI_S1[TDRE] and SCI_S1[TC] events. Another interrupt vector is associated with the receiver for RDRF, IDLE, RXEDGIF, and LBKDIF events. A third vector is used for OR, NF, FE, and PF error conditions. Each of these ten interrupt sources can be separately masked by local interrupt enable masks. The flags can be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags that can optionally generate hardware interrupt requests. Transmit data register empty (SCI_S1[TDRE]) indicates when there is room in the transmit data buffer to write another transmit character to SCI_D. If the transmit interrupt enable (SCI_C2[TIE]) bit is set, a hardware interrupt is requested when SCI_S1[TDRE] is set. Transmit complete (SCI_S1[TC]) indicates that the transmitter is

finished transmitting all data, preamble, and break characters and is idle with TxD at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (SCI_C2[TCIE]) bit is set, a hardware interrupt is requested when SCI_S1[TC] is set. Instead of hardware interrupts, software polling may be used to monitor the SCI_S1[TDRE] and SCI_S1[TC] status flags if the corresponding SCI_C2[TIE] or SCI_C2[TCIE] local interrupt masks are cleared.

When a program detects that the receive data register is full (SCI_S1[RDRF] = 1), it gets the data from the receive data register by reading SCI_D. The SCI_S1[RDRF] flag is cleared by reading SCI_S1 while SCI_S1[RDRF] is set and then reading SCI_D.

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCI_S1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RxD line remains idle for an extended period of time. IDLE is cleared by reading SCI_S1 while SCI_S1[IDLE] is set and then reading SCI_D. After SCI_S1[IDLE] has been cleared, it cannot become set again until the receiver has received at least one new character and has set SCI_S1[RDRF].

If the associated error was detected in the received character that caused SCI_S1[RDRF] to be set, the error flags - noise flag (SCI_S1[NF]), framing error (SCI_S1[FE]), and parity error flag (SCI_S1[PF]) - are set at the same time as SCI_S1[RDRF]. These flags are not set in overrun cases.

If SCI_S1[RDRF] was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (SCI_S1[OR]) flag is set instead of the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the SCI_S2[RXEDGIF] flag to set. The SCI_S2[RXEDGIF] flag is cleared by writing a 1 to it. This function depends on the receiver being enabled (SCI_C2[RE] = 1).

15.4.5 Baud rate tolerance

A transmitting device may operate at a baud rate below or above that of the receiver.

Accumulated bit time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the actual stop bit. A noise error will occur if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error will occur if the receiver clock is misaligned in such a way that the majority of the RT8, RT9, and RT10 stop bit samples are a logic zero.

As the receiver samples an incoming frame, it re-synchronizes the RT clock on any valid falling edge within the frame. Resynchronization within frames will correct a misalignment between transmitter bit times and receiver bit times.

15.4.5.1 Slow data tolerance

Figure 15-4 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

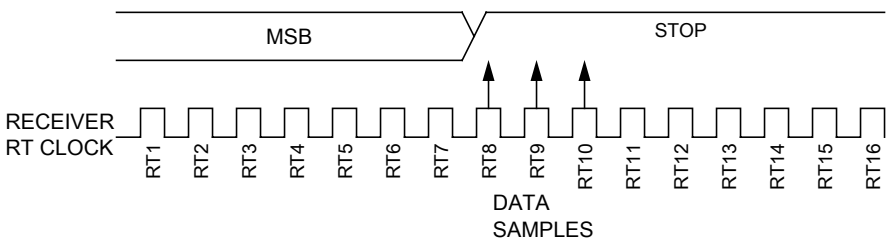


Figure 15-4. Slow data

For an 8-bit data and 1 stop bit character, data sampling of the stop bit takes the receiver 9 bit times x 16 RT cycles +10 RT cycles =154 RT cycles.

With the misaligned character shown in Figure 15-4, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 9 bit times x 16 RT cycles + 3 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data and 1 stop bit character with no errors is:

((154 - 147) / 154) x 100 = 4.54%

For a 9-bit data or 2 stop bits character, data sampling of the stop bit takes the receiver 10 bit times x 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in Figure 15-4, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles + 3 RT cycles = 163 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit or 2 stop bits character with no errors is:

((170 - 163) / 170) X 100 = 4.12%

For a 9-bit data and 2 stop bit character, data sampling of the stop bit takes the receiver 11 bit times x 16 RT cycles + 10 RT cycles = 186 RT cycles.

With the misaligned character shown in Figure 15-4, the receiver counts 186 RT cycles at the point when the count of the transmitting device is 11 bit times x 16 RT cycles + 3 RT cycles = 179 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit and 2 stop bits character with no errors is: ((186 - 179) / 186) X 100 = 3.76%

15.4.5.2 Fast data tolerance

Figure 15-5 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

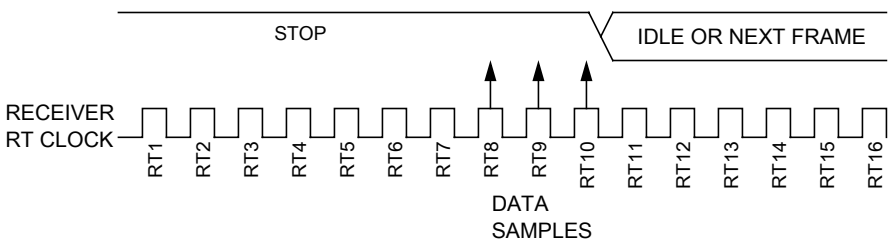


Figure 15-5. Fast data

For an 8-bit data and 1 stop bit character, data sampling of the stop bit takes the receiver 9 bit times x 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in Figure 15-5, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit and 1 stop bit character with no errors is:

((154 - 160) / 154) x 100 = 3.90%

For a 9-bit data or 2 stop bits character, data sampling of the stop bit takes the receiver 10 bit times x 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 11 bit times x 16 RT cycles = 176 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit or 2 stop bits character with no errors is:

((170 - 176) / 170) x 100 = 3.53%

For a 9-bit data and 2 stop bits character, data sampling of the stop bit takes the receiver 11 bit times x 16 RT cycles + 10 RT cycles = 186 RT cycles.

With the misaligned character shown in, the receiver counts 186 RT cycles at the point when the count of the transmitting device is 12 bit times x 16 RT cycles = 192 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit and 2 stop bits character with no errors is:

((186 - 192) / 186) x 100 = 3.23%

15.4.6 Additional SCI functions

The following sections describe additional SCI functions.

15.4.6.1 8- and 9-bit data modes

The SCI system, transmitter and receiver, can be configured to operate in 9-bit data mode by setting SCI_C1[M]. In 9-bit mode, there is a ninth data bit to the left of the most significant bit of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCI_C3. For the receiver, the ninth bit is held in SCI_C3[R8].

For coherent writes to the transmit data buffer, write to SCI_C3[T8] before writing to SCI_D.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to SCI_C3[T8] again. When data is transferred from the transmit data buffer to the transmit shifter, the value in SCI_C3[T8] is copied at the same time data is transferred from SCI_D to the shifter.

The 9-bit data mode is typically used with parity to allow eight bits of data plus the parity in the ninth bit, or it is used with address-mark wake-up so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

15.4.6.2 Stop mode operation

During all stop modes, clocks to the SCI module are halted.

No SCI module registers are affected in Stop3 mode.

The receive input active edge detect circuit remains active in Stop3 mode. An active edge on the receive input brings the CPU out of Stop3 mode if the interrupt is not masked (SCI_BDH[RXEDGIE] = 1).

Because the clocks are halted, the SCI module resumes operation upon exit from stop, only in Stop3 mode. Software must ensure stop mode is not entered while there is a character (including preamble, break and normal data) being transmitted out of or received into the SCI module, that means SCI_S1[TC] =1, SCI_S1[TDRE] = 1, and SCI_S2[RAF] = 0 must all meet before entering stop mode.

15.4.6.3 Loop mode

When SCI_C1[LOOPS] is set, the SCI_C1[RSRC] bit in the same register chooses between loop mode (SCI_C1[RSRC] = 0) or single-wire mode (SCI_C1[RSRC] = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

15.4.6.4 Single-wire operation

When SCI_C1[LOOPS] is set, SCI_C1[RSRC] chooses between loop mode (SCI_C1[RSRC] = 0) or single-wire mode (SCI_C1[RSRC] = 1). Single-wire mode implements a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general-purpose port I/O pin.

In single-wire mode, the SCI_C3[TXDIR] bit controls the direction of serial data on the TxD pin. When SCI_C3[TXDIR] is cleared, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When SCI_C3[TXDIR] is set, the TxD pin is an output driven by the transmitter. In single-wire mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general-purpose port I/O pin.

Chapter 16
8-Bit Serial Peripheral Interface (8-bit SPI)

16.1 Introduction

The serial peripheral interface (SPI) module provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, and memories, among others.

The SPI runs at a baud rate up to the bus clock divided by two in master mode and up to the bus clock divided by four in slave mode. Software can poll the status flags, or SPI operation can be interrupt driven.

NOTE

For the actual maximum SPI baud rate, refer to the Chip Configuration details and to the device's Data Sheet.

The SPI also includes a hardware match feature for the receive data buffer.

16.1.1 Features

The SPI includes these distinctive features:

- Master mode or slave mode operation
- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate
- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output

- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting

16.1.2 Modes of Operation

The SPI functions in three modes, run, wait, and stop.

- Run Mode

  This is the basic mode of operation.

- Wait Mode

  SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPIx_C2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in Run Mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU enters run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

- Stop Mode

  To reduce power consumption, the SPI is inactive in stop modes where the peripheral bus clock is stopped but internal logic states are retained. If the SPI is configured as a master, any transmission in progress stops, but is resumed after the CPU enters run mode. If the SPI is configured as a slave, reception and transmission of a data continues, so that the slave stays synchronized to the master.

  The SPI is completely disabled in stop modes where the peripheral bus clock is stopped and internal logic states are not retained. When the CPU wakes from these stop modes, all SPI register content is reset.

Detailed descriptions of operating modes appear in Low Power Mode Options.

16.1.3 Block Diagrams

This section includes block diagrams showing SPI system connections, the internal organization of the SPI module, and the SPI clock dividers that control the master mode bit rate.

16.1.3.1 SPI System Block Diagram

The following figure shows the SPI modules of two MCUs connected in a master-slave arrangement. The master device initiates all SPI data transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. The transfer effectively exchanges the data that was in the SPI shift registers of the two SPI systems. The SPSCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input (SS pin). In this system, the master device has configured its SS pin as an optional slave select output.

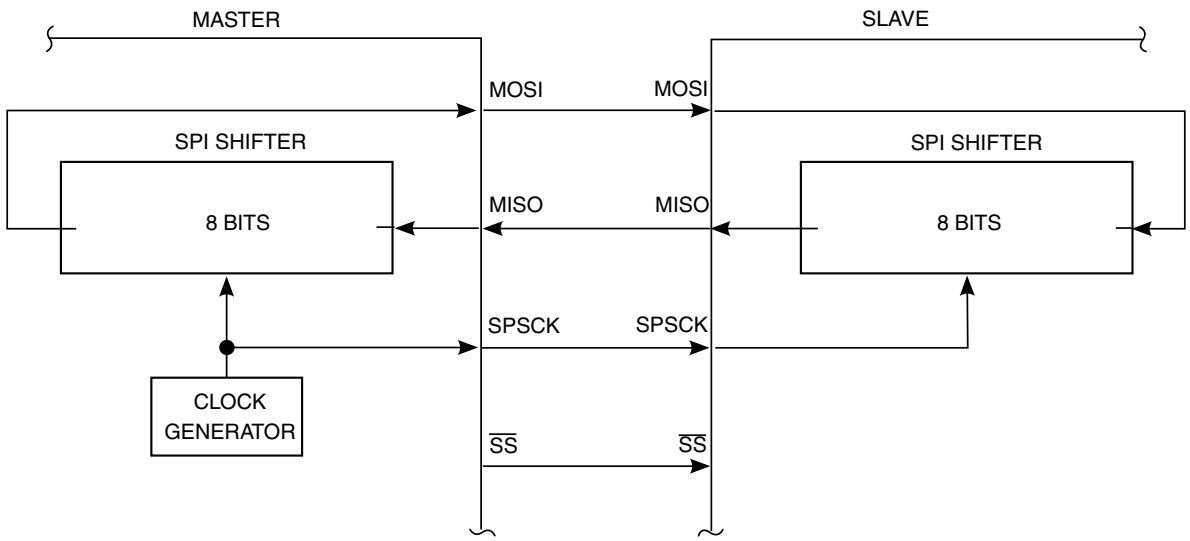


Figure 16-1. SPI System Connections

16.1.3.2 SPI Module Block Diagram

The following is a block diagram of the SPI module. The central element of the SPI is the SPI shift register. Data is written to the double-buffered transmitter (write to SPIx_D) and gets transferred to the SPI shift register at the start of a data transfer. After shifting in 8 bits of data, the data is transferred into the double-buffered receiver where it can be read from SPIx_D. Pin multiplexing logic controls connections between MCU pins and the SPI module.

When the SPI is configured as a master, the clock output is routed to the SPSCK pin, the shifter output is routed to MOSI, and the shifter input is routed from the MISO pin.

When the SPI is configured as a slave, the SPSCK pin is routed to the clock input of the SPI, the shifter output is routed to MISO, and the shifter input is routed from the MOSI pin.

In the external SPI system, simply connect all SPSCK pins to each other, all MISO pins together, and all MOSI pins together. Peripheral devices often use slightly different names for these pins.

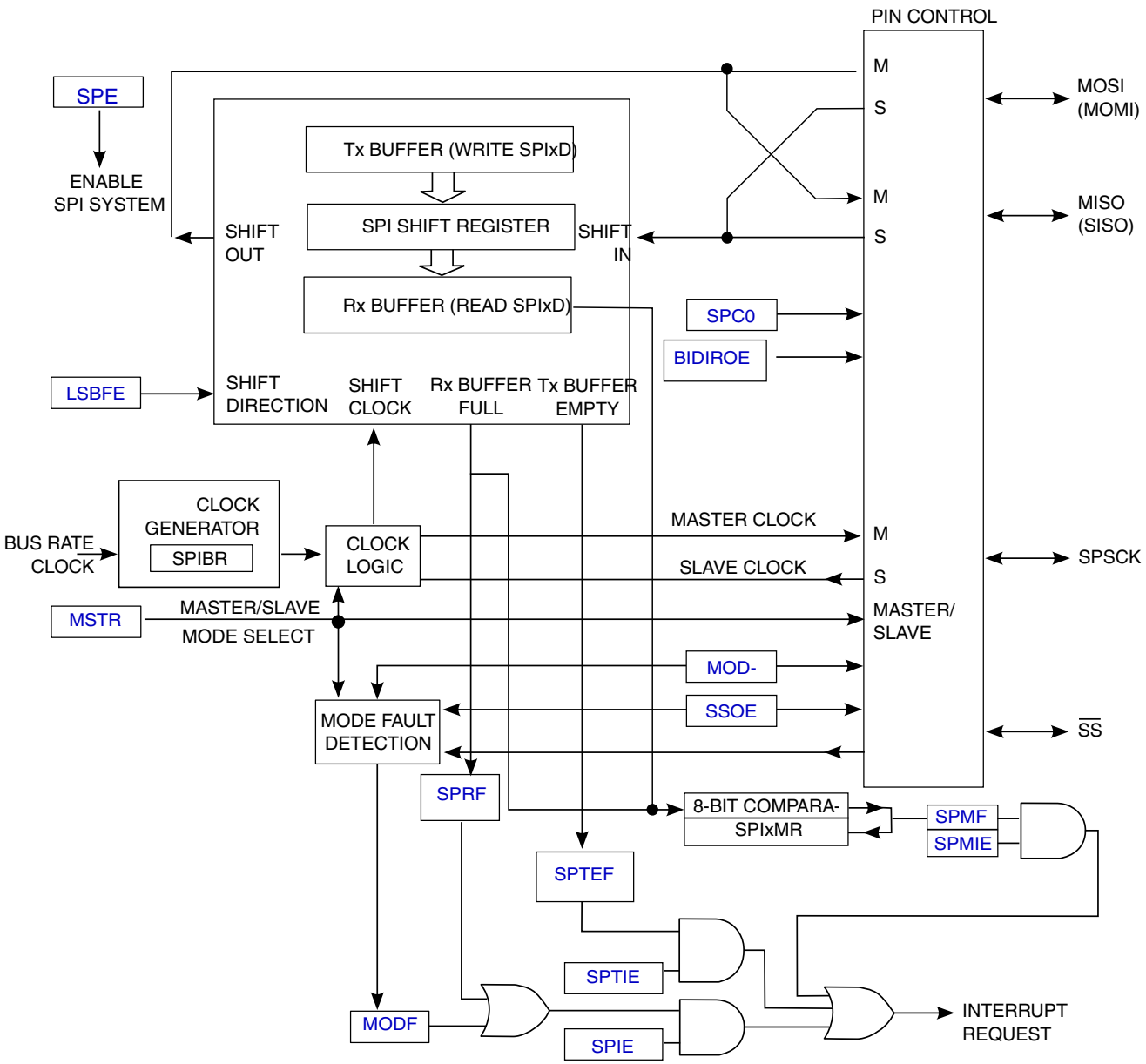


Figure 16-2. SPI Module Block Diagram without FIFO

16.2 External Signal Description

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled (SPE = 0), these four pins revert to other functions that are not controlled by the SPI (based on chip configuration).

16.2.1 SPSCK — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

16.2.2 MOSI — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and SPC0 is 0, this pin is the serial data input. If SPC0 is 1 to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE is 0) or an output (BIDIROE is 1). If SPC0 is 1 and slave mode is selected, this pin is not used by the SPI and reverts to other functions (based on chip configuration).

16.2.3 MISO — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and SPC0 is 0, this pin is the serial data output. If SPC0 is 1 to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO), and the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE is 0) or an output (BIDIROE is 1). If SPC0 is 1 and master mode is selected, this pin is not used by the SPI and reverts to other functions (based on chip configuration).

16.2.4 $\overline{SS}$ — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off (MODFEN is 0), this pin is not used by the SPI and reverts to other functions (based on chip configuration). When the SPI is enabled as a master and MODFEN is 1, the slave select output enable bit determines whether this pin acts as the mode fault input (SSOE is 0) or as the slave select output (SSOE is 1).

16.3 Register Definition

The SPI has 8-bit registers to select SPI options, to control baud rate, to report SPI status, to hold an SPI data match value, and for transmit/receive data.

SPI memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3098	SPI control register 1 (SPI0_C1)	8	R/W	04h	16.3.1/442
3099	SPI control register 2 (SPI0_C2)	8	R/W	00h	16.3.2/444
309A	SPI baud rate register (SPI0_BR)	8	R/W	00h	16.3.3/445
309B	SPI status register (SPI0_S)	8	R/W	20h	16.3.4/446
309D	SPI data register (SPI0_D)	8	R/W	00h	16.3.5/447
309F	SPI match register (SPI0_M)	8	R/W	00h	16.3.6/448

16.3.1 SPI control register 1 (SPIx_C1)

This read/write register includes the SPI enable control, interrupt enables, and configuration options.

Address: 3098h base + 0h offset = 3098h

Bit	7	6	5	4	3	2	1	0
Read Write	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

SPI0_C1 field descriptions

Field	Description
7 SPIE	SPI interrupt enable: for SPRF and MODF This bit enables the interrupt for SPI receive buffer full (SPRF) and mode fault (MODF) events. 0 Interrupts from SPRF and MODF are inhibited—use polling 1 Request a hardware interrupt when SPRF or MODF is 1
6 SPE	SPI system enable This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, the SPI is disabled and forced into an idle state, and all status bits in the S register are reset.

Table continues on the next page...

SPI0_C1 field descriptions (continued)

Field	Description
	0 SPI system inactive 1 SPI system enabled
5 SPTIE	SPI transmit interrupt enable This is the interrupt enable bit for SPI transmit buffer empty (SPTEF). An interrupt occurs when the SPI transmit buffer is empty (SPTEF is set). 0 Interrupts from SPTEF inhibited (use polling) 1 When SPTEF is 1, hardware interrupt requested
4 MSTR	Master/slave mode select This bit selects master or slave mode operation. 0 SPI module configured as a slave SPI device 1 SPI module configured as a master SPI device
3 CPOL	Clock polarity This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. This bit effectively places an inverter in series with the clock signal either from a master SPI device or to a slave SPI device. Refer to the description of “SPI Clock Formats” for details. 0 Active-high SPI clock (idles low) 1 Active-low SPI clock (idles high)
2 CPHA	Clock phase This bit selects one of two clock formats for different kinds of synchronous serial peripheral devices. Refer to the description of “SPI Clock Formats” for details. 0 First edge on SPSCK occurs at the middle of the first cycle of a data transfer 1 First edge on SPSCK occurs at the start of the first cycle of a data transfer
1 SSOE	Slave select output enable This bit is used in combination with the mode fault enable (MODFEN) bit in the C2 register and the master/slave (MSTR) control bit to determine the function of the $\overline{SS}$ pin. 0 When MODFEN is 0: In master mode, $\overline{SS}$ pin function is general-purpose I/O (not SPI). In slave mode, $\overline{SS}$ pin function is slave select input. When MODFEN is 1: In master mode, $\overline{SS}$ pin function is $\overline{SS}$ input for mode fault. In slave mode, $\overline{SS}$ pin function is slave select input. 1 When MODFEN is 0: In master mode, $\overline{SS}$ pin function is general-purpose I/O (not SPI). In slave mode, $\overline{SS}$ pin function is slave select input. When MODFEN is 1: In master mode, $\overline{SS}$ pin function is automatic $\overline{SS}$ output. In slave mode: $\overline{SS}$ pin function is slave select input.
0 LSBFE	LSB first (shifter direction) This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7. 0 SPI serial data transfers start with most significant bit 1 SPI serial data transfers start with least significant bit

16.3.2 SPI control register 2 (SPIx_C2)

This read/write register is used to control optional features of the SPI system. Bit 6 is not implemented and always reads 0.

Address: 3098h base + 1h offset = 3099h

Bit	7	6	5	4	3	2	1	0
Read	SPMIE	0	Reserved	MODFEN	BIDIROE	Reserved	SPISWAI	SPC0
Write								
Reset	0	0	0	0	0	0	0	0

SPI0_C2 field descriptions

Field	Description
7 SPMIE	SPI match interrupt enable This is the interrupt enable bit for the SPI receive data buffer hardware match (SPMF) function. 0 Interrupts from SPMF inhibited (use polling) 1 When SPMF is 1, requests a hardware interrupt
6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 Reserved	This field is reserved. Do not write to this reserved bit.
4 MODFEN	Master mode-fault function enable When the SPI is configured for slave mode, this bit has no meaning or effect. (The $\overline{SS}$ pin is the slave select input.) In master mode, this bit determines how the $\overline{SS}$ pin is used. For details, refer to the description of the SSOE bit in the C1 register. 0 Mode fault function disabled, master $\overline{SS}$ pin reverts to general-purpose I/O not controlled by SPI 1 Mode fault function enabled, master $\overline{SS}$ pin acts as the mode fault input or the slave select output
3 BIDIROE	Bidirectional mode output enable When bidirectional mode is enabled because SPI pin control 0 (SPC0) is set to 1, the BIDIROE bit determines whether the SPI data output driver is enabled to the single bidirectional SPI I/O pin. Depending on whether the SPI is configured as a master or a slave, it uses the MOSI (MOMI) or MISO (SISO) pin, respectively, as the single SPI data I/O pin. When SPC0 is 0, BIDIROE has no meaning or effect. 0 Output driver disabled so SPI data I/O pin acts as an input 1 SPI I/O pin enabled as an output
2 Reserved	This field is reserved. Do not write to this reserved bit.
1 SPISWAI	SPI stop in wait mode This bit is used for power conservation while the device is in wait mode. 0 SPI clocks continue to operate in wait mode 1 SPI clocks stop when the MCU enters wait mode

Table continues on the next page...

SPI0_C2 field descriptions (continued)

Field	Description
0 SPC0	SPI pin control 0 This bit enables bidirectional pin configurations. 0 SPI uses separate pins for data input and data output (pin mode is normal). In master mode of operation: MISO is master in and MOSI is master out. In slave mode of operation: MISO is slave out and MOSI is slave in. 1 SPI configured for single-wire bidirectional operation (pin mode is bidirectional). In master mode of operation: MISO is not used by SPI; MOSI is master in when BIDIROE is 0 or master I/O when BIDIROE is 1. In slave mode of operation: MISO is slave in when BIDIROE is 0 or slave I/O when BIDIROE is 1; MOSI is not used by SPI.

16.3.3 SPI baud rate register (SPIx_BR)

Use this register to set the prescaler and bit rate divisor for an SPI master. This register may be read or written at any time.

Address: 3098h base + 2h offset = 309Ah

Bit	7	6	5	4	3	2	1	0
Read	0	SPPR[2:0]			SPR[3:0]			
Write								
Reset	0	0	0	0	0	0	0	0

SPI0_BR field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–4 SPPR[2:0]	SPI baud rate prescale divisor This 3-bit field selects one of eight divisors for the SPI baud rate prescaler. The input to this prescaler is the bus rate clock (BUSCLK). The output of this prescaler drives the input of the SPI baud rate divider. Refer to the description of “SPI Baud Rate Generation” for details. 000 Baud rate prescaler divisor is 1 001 Baud rate prescaler divisor is 2 010 Baud rate prescaler divisor is 3 011 Baud rate prescaler divisor is 4 100 Baud rate prescaler divisor is 5 101 Baud rate prescaler divisor is 6 110 Baud rate prescaler divisor is 7 111 Baud rate prescaler divisor is 8

Table continues on the next page...

SPI0_BR field descriptions (continued)

Field	Description
SPR[3:0]	SPI baud rate divisor This 4-bit field selects one of nine divisors for the SPI baud rate divider. The input to this divider comes from the SPI baud rate prescaler. Refer to the description of “SPI Baud Rate Generation” for details. 0000 Baud rate divisor is 2 0001 Baud rate divisor is 4 0010 Baud rate divisor is 8 0011 Baud rate divisor is 16 0100 Baud rate divisor is 32 0101 Baud rate divisor is 64 0110 Baud rate divisor is 128 0111 Baud rate divisor is 256 1000 Baud rate divisor is 512 All others Reserved

16.3.4 SPI status register (SPIx_S)

NOTE

Bits 3 through 0 are not implemented and always read 0.

Address: 3098h base + 3h offset = 309Bh

Bit	7	6	5	4	3	2	1	0
Read	SPRF	SPMF	SPTEF	MODF	0			
Write		w1c						
Reset	0	0	1	0	0	0	0	0

SPI0_S field descriptions

Field	Description
7 SPRF	SPI read buffer full flag SPRF is set at the completion of an SPI transfer to indicate that received data may be read from the SPI data (D) register. SPRF is cleared by reading SPRF while it is set and then reading the SPI data register. 0 No data available in the receive data buffer 1 Data available in the receive data buffer
6 SPMF	SPI Match Flag SPMF is set after SPRF is 1 when the value in the receive data buffer matches the value in the M register. **NOTE:** This SPMF can be cleared only when it is read as 1. To clear this flag, read SPMF first and then write a 1 to it.

Table continues on the next page...

SPI0_S field descriptions (continued)

Field	Description
	0 Value in the receive data buffer does not match the value in the M register 1 Value in the receive data buffer matches the value in the M register
5 SPTEF	SPI transmit buffer empty flag This bit is set when the transmit data buffer is empty. SPTEF is cleared by reading the S register with SPTEF set and then writing a data value to the transmit buffer at D. The S register must be read with SPTEF set to 1 before writing data to the D register; otherwise, the D write is ignored. SPTEF is automatically set when all data from the transmit buffer transfers into the transmit shift register. For an idle SPI, data written to D is transferred to the shifter almost immediately so that SPTEF is set within two bus cycles, allowing a second set of data to be queued into the transmit buffer. After completion of the transfer of the data in the shift register, the queued data from the transmit buffer automatically moves to the shifter, and SPTEF is set to indicate that room exists for new data in the transmit buffer. If no new data is waiting in the transmit buffer, SPTEF simply remains set and no data moves from the buffer to the shifter. If a transfer does not stop, the last data that was transmitted is sent out again. 0 SPI transmit buffer not empty 1 SPI transmit buffer empty
4 MODF	Master mode fault flag MODF is set if the SPI is configured as a master and the slave select input goes low, indicating some other SPI device is also configured as a master. The $\overline{SS}$ pin acts as a mode fault error input only when MSTR is 1, MODFEN is 1, and SSOE is 0; otherwise, MODF will never be set. MODF is cleared by reading MODF while it is 1 and then writing to the SPI control register 1 (C1). 0 No mode fault error 1 Mode fault error detected
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

16.3.5 SPI data register (SPIx_D)

This register is both the input and output register for SPI data. A write to the register writes to the transmit data buffer, allowing data to be queued and transmitted.

When the SPI is configured as a master, data queued in the transmit data buffer is transmitted immediately after the previous transmission has completed.

The SPTEF bit in the S register indicates when the transmit data buffer is ready to accept new data. The S register must be read when SPTEF is set before writing to the SPI data register; otherwise, the write is ignored.

Data may be read from the SPI data register any time after SPRF is set and before another transfer is finished. Failure to read the data out of the receive data buffer before a new transfer ends causes a receive overrun condition, and the data from the new transfer is lost. The new data is lost because the receive buffer still held the previous character and

was not ready to accept the new data. There is no indication for a receive overrun condition, so the application system designer must ensure that previous data has been read from the receive buffer before a new transfer is initiated.

Address: 3098h base + 5h offset = 309Dh

Bit	7	6	5	4	3	2	1	0
Read Write	Bits[7:0]							
Reset	0	0	0	0	0	0	0	0

SPI0_D field descriptions

Field	Description
Bits[7:0]	Data (low byte)

16.3.6 SPI match register (SPIx_M)

This register contains the hardware compare value. When the value received in the SPI receive data buffer equals this hardware compare value, the SPI match flag (SPMF) sets.

Address: 3098h base + 7h offset = 309Fh

Bit	7	6	5	4	3	2	1	0
Read Write	Bits[7:0]							
Reset	0	0	0	0	0	0	0	0

SPI0_M field descriptions

Field	Description
Bits[7:0]	Hardware compare value (low byte)

16.4 Functional Description

This section provides the functional description of the module.

16.4.1 General

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI Control Register 1. While the SPE bit is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select (SS)
- Serial clock (SPSCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

An SPI transfer is initiated in the master SPI device by reading the SPI status register (SPIx_S) when SPTEF = 1 and then writing data to the transmit data buffer (write to SPIxD). When a transfer is complete, received data is moved into the receive data buffer. The SPIxD register acts as the SPI receive data buffer for reads and as the SPI transmit data buffer for writes.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI Control Register 1 (SPIx_C1) select one of four possible clock formats to be used by the SPI system . The CPOL bit simply selects a non-inverted or inverted clock . The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SPSCK edges or on even numbered SPSCK edges .

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI control register 1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

16.4.2 Master Mode

The SPI operates in master mode when the MSTR bit is set. Only a master SPI module can initiate transmissions. A transmission begins by reading the SPIx_S register while SPTEF = 1 and writing to the master SPI data registers. If the shift register is empty, the byte immediately transfers to the shift register. The data begins shifting out on the MOSI pin under the control of the serial clock.

- SPSCK
  - The SPR3, SPR2, SPR1, and SPR0 baud rate selection bits in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI Baud Rate register control the baud rate generator and determine the speed of the transmission. The SPSCK pin is the SPI clock output. Through the SPSCK pin, the baud rate generator of the master controls the shift register of the slave peripheral.
- MOSI, MISO pin

- In master mode, the function of the serial data output pin (MOSI) and the serial data input pin (MISO) is determined by the SPC0 and BIDIROE control bits.

- $\overline{SS}$ pin
  - If MODFEN and SSOE bit are set, the SS pin is configured as slave select output. The SS output becomes low during each transmission and is high when the SPI is in idle state. If MODFEN is set and SSOE is cleared, the $\overline{SS}$ pin is configured as input for detecting mode fault error. If the SS input becomes low this indicates a mode fault error where another master tries to drive the MOSI and SPSCK lines. In this case, the SPI immediately switches to slave mode by clearing the MSTR bit and also disables the slave output buffer MISO (or SISO in bidirectional mode). As a result, all outputs are disabled, and SPSCK, MOSI and MISO are inputs. If a transmission is in progress when the mode fault occurs, the transmission is aborted and the SPI is forced into idle state. This mode fault error also sets the mode fault (MODF) flag in the SPI Status Register (SPIx_S). If the SPI interrupt enable bit (SPIE) is set when the MODF flag gets set, then an SPI interrupt sequence is also requested. When a write to the SPI Data Register in the master occurs, there is a half SPSCK-cycle delay. After the delay, SPSCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI Control Register 1 (see SPI Clock Formats).

Note

A change of the bits CPOL, CPHA, SSOE, LSBFE, MODFEN, SPC0, BIDIROE with SPC0 set, SPPR2-SPPR0 and SPR3-SPR0 in master mode abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master has to ensure that the remote slave is set back to idle state.

16.4.3 Slave Mode

The SPI operates in slave mode when the MSTR bit in SPI Control Register1 is clear.

- SPSCK

  In slave mode, SPSCK is the SPI clock input from the master.

- MISO, MOSI pin

In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI Control Register 2.

- SS pin

  The SS pin is the slave select input. Before a data transmission occurs, the SS pin of the slave SPI must be low. SS must remain low until the transmission is complete . If SS goes high, the SPI is forced into idle state.

  The SS input also controls the serial data output pin, if SS is high (not selected), the serial data output pin is high impedance, and, if SS is low the first bit in the SPI Data Register is driven out of the serial data output pin . Also, if the slave is not selected (SS is high), then the SPSCK input is ignored and no internal shifting of the SPI shift register takes place.

  Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

Note

When peripherals with duplex capability are used, take care not to simultaneously enable two receivers whose serial outputs drive the same system slave's serial data output line.

As long as no more than one slave device drives the system slave's serial data output line, it is possible for several slaves to receive the same transmission from a master, although the master would not receive return information from all of the receiving slaves.

If the CPHA bit in SPI Control Register 1 is clear, odd numbered edges on the SPSCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit .

If the CPHA bit is set, even numbered edges on the SPSCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

When CPHA is set, the first edge is used to get the first data bit onto the serial data output pin. When CPHA is clear and the SS input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the eighth shift, the transfer is considered complete and the received data is transferred into the SPI data registers. To indicate transfer is complete, the SPRF flag in the SPI Status Register is set.

Note

A change of the bits BIDIROE with SPC0 set, CPOL, CPHA, SSOE, LSBFE, MODFEN, and SPC0 in slave mode will corrupt a transmission in progress and must be avoided.

16.4.4 SPI Clock Formats

To accommodate a wide variety of synchronous serial peripherals from different manufacturers, the SPI system has a clock polarity (CPOL) bit and a clock phase (CPHA) control bit to select one of four clock formats for data transfers. CPOL selectively inserts an inverter in series with the clock. CPHA chooses between two different clock phase relationships between the clock and data.

The following figure shows the clock formats when CPHA = 1. At the top of the figure, the eight bit times are shown for reference with bit 1 starting at the first SPSCK edge and bit 8 ending one-half SPSCK cycle after the eighth SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master $\overline{SS}$ output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

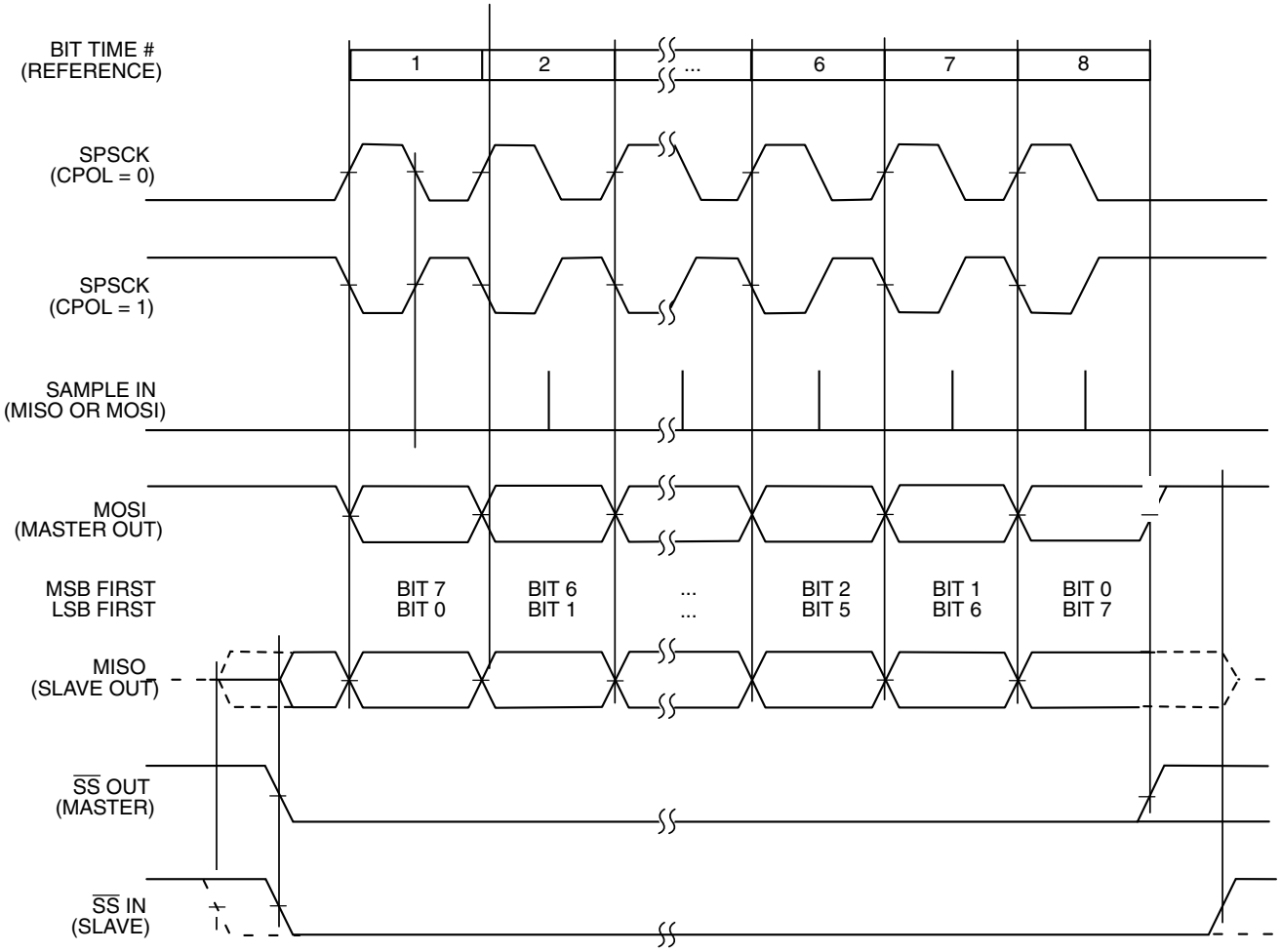


Figure 16-3. SPI Clock Formats (CPHA = 1)

When CPHA = 1, the slave begins to drive its MISO output when $\overline{SS}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively.

When CPHA = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers. In this clock format, a back-to-back transmission can occur, as follows:

1. A transmission is in progress.
2. A new data byte is written to the transmit buffer before the in-progress transmission is complete.
3. When the in-progress transmission is complete, the new, ready data byte is transmitted immediately.

Between these two successive transmissions, no pause is inserted; the $\overline{SS}$ pin remains low.

The following figure shows the clock formats when CPHA = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected (SS IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The SS OUT waveform applies to the slave select output from a master (provided MODFEN and SSOE = 1). The master SS output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCK cycle after the end of the eighth bit time of the transfer. The SS IN waveform applies to the slave select input of a slave.

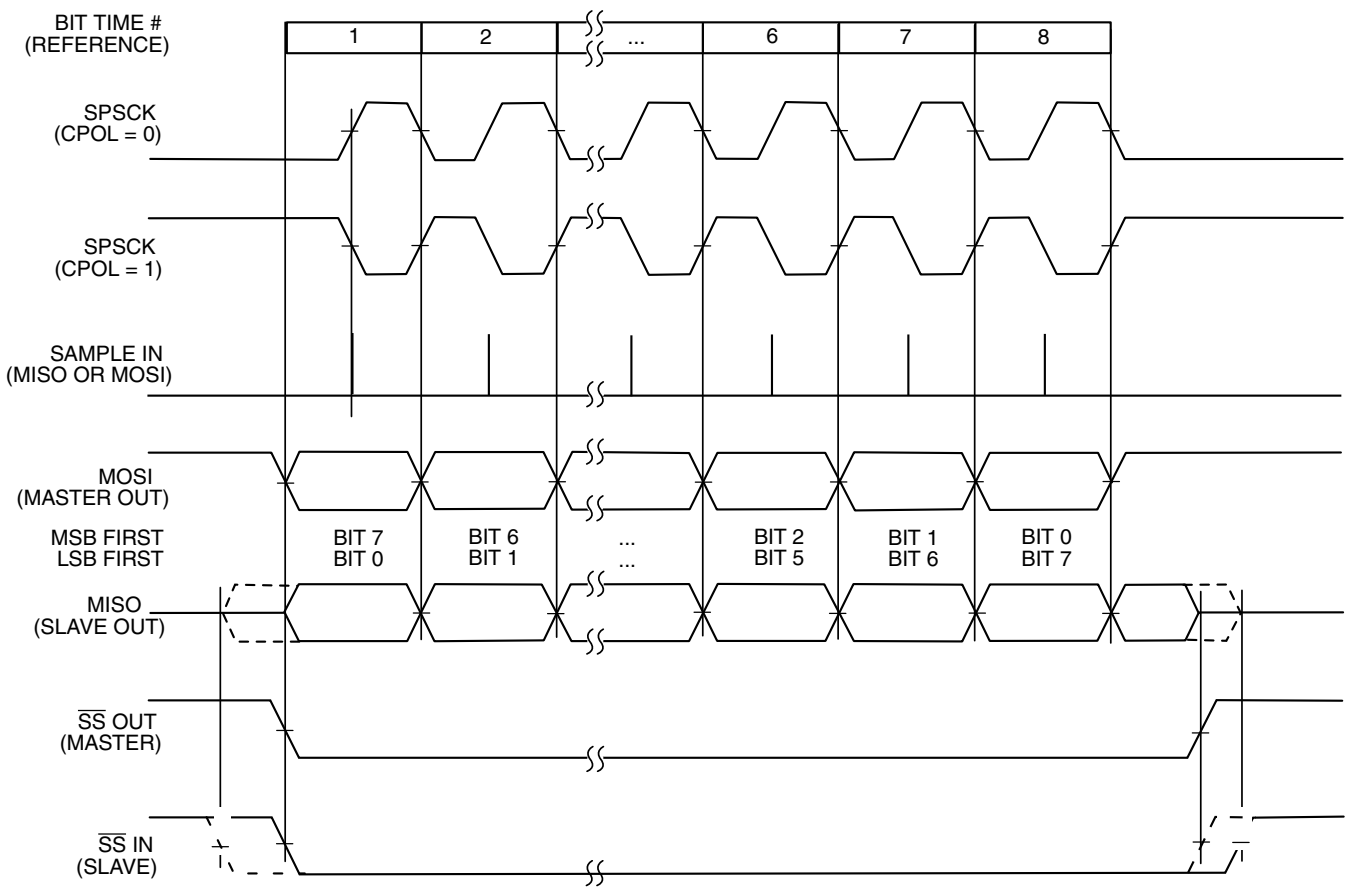


Figure 16-4. SPI Clock Formats (CPHA = 0)

When CPHA = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when SS goes to active low. The first SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When CPHA = 0, the slave's SS input must go to its inactive high level between transfers.

16.4.5 SPI Baud Rate Generation

As shown in the following figure, the clock source for the SPI baud rate generator is the bus clock. The three prescale bits (SPPR2:SPPR1:SPPR0) choose a prescale divisor of 1, 2, 3, 4, 5, 6, 7, or 8. The three rate select bits (SPR3:SPR2:SPR1:SPR0) divide the output of the prescaler stage by 2, 4, 8, 16, 32, 64, 128, 256, or 512 to get the internal SPI master mode bit-rate clock.

The baud rate generator is activated only when the SPI is in the master mode and a serial transfer is taking place. In the other cases, the divider is disabled to decrease I_{DD} current.

The baud rate divisor equation is as follows (except those reserved combinations in the SPI Baud Rate Divisor table).

$$BaudRateDivisor = (SPPR + 1) \times 2^{(SPR + 1)}$$

The baud rate can be calculated with the following equation:

$$BaudRate = BusClock / BaudRateDivisor$$

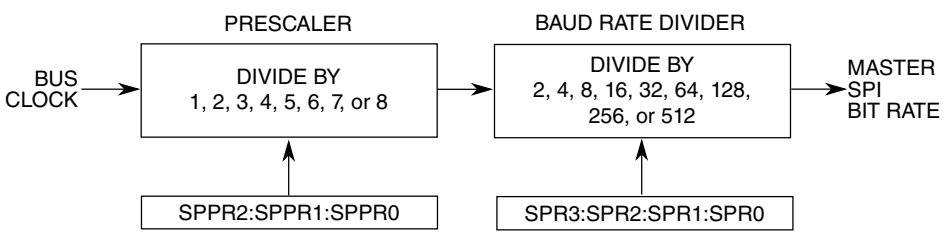


Figure 16-5. SPI Baud Rate Generation

16.4.6 Special Features

The following section shows the module special features.

16.4.6.1 $\overline{SS}$ Output

The $\overline{SS}$ output feature automatically drives the $\overline{SS}$ pin low during transmission to select external devices and drives the $\overline{SS}$ pin high during idle to deselect external devices. When the $\overline{SS}$ output is selected, the $\overline{SS}$ output pin is connected to the $\overline{SS}$ input pin of the external device.

The $\overline{SS}$ output is available only in master mode during normal SPI operation by asserting the SSOE and MODFEN bits as shown in the description of the C1[SSOE] bit.

The mode fault feature is disabled while $\overline{SS}$ output is enabled.

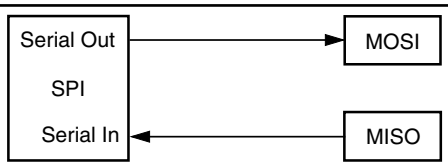
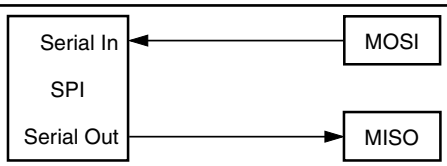
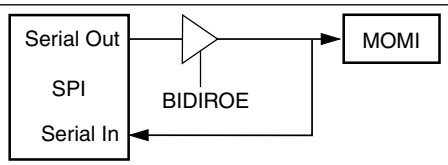
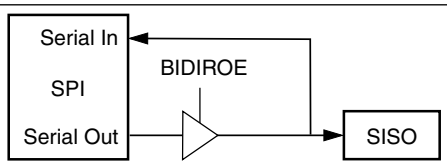
Note

Be careful when using the $\overline{SS}$ output feature in a multimaster system because the mode fault feature is not available for detecting system errors between masters.

16.4.6.2 Bidirectional Mode (MOMI or SISO)

The bidirectional mode is selected when the SPC0 bit is set in SPI Control Register 2 (see the following table). In this mode, the SPI uses only one serial data pin for the interface with one or more external devices. The MSTR bit decides which pin to use. The MOSI pin becomes the serial data I/O (MOMI) pin for the master mode, and the MISO pin becomes serial data I/O (SISO) pin for the slave mode. The MISO pin in master mode and MOSI pin in slave mode are not used by the SPI.

Table 16-1. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

The direction of each serial I/O pin depends on the BIDIROE bit. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

The SPSCK is an output for the master mode and an input for the slave mode.

$\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.

The bidirectional mode does not affect SPSCK and $\overline{SS}$ functions.

Note

In bidirectional master mode, with the mode fault feature enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode. In this case, MISO becomes occupied by the SPI and MOSI is not used. Consider this scenario if the MISO pin is used for another purpose.

16.4.7 Error Conditions

The SPI module has one error condition: the mode fault error.

16.4.7.1 Mode Fault Error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SPSCK lines simultaneously. This condition is not permitted in normal operation, and it sets the MODF bit in the SPI status register automatically provided that the MODFEN bit is set.

In the special case where the SPI is in master mode and the MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. If the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. A mode fault error does not occur in slave mode.

If a mode fault error occurs, the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So the SPSCK, MISO and MOSI pins are forced to be high impedance inputs to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for an SPI system configured in master mode, the output enable of MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for the SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI Status Register (with MODF set) followed by a write to SPI Control Register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

16.4.8 Low Power Mode Options

This section describes the low power mode options.

16.4.8.1 SPI in Run Mode

In run mode with the SPI system enable (SPE) bit in the SPI control register clear, the SPI system is in a low-power, disabled state. SPI registers can still be accessed, but clocks to the core of this module are disabled .

16.4.8.2 SPI in Wait Mode

SPI operation in wait mode depends upon the state of the SPISWAI bit in SPI Control Register 2.

- If SPISWAI is clear, the SPI operates normally when the CPU is in wait mode.
- If SPISWAI is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
  - If SPISWAI is set and the SPI is configured for master, any transmission and reception in progress stops at wait mode entry. The transmission and reception resumes when the SPI exits wait mode.
  - If SPISWAI is set and the SPI is configured as a slave, any transmission and reception in progress continues if the SPSCK continues to be driven from the master. This keeps the slave synchronized to the master and the SPSCK.

    If the master transmits data while the slave is in wait mode, the slave continues to send data consistent with the operation mode at the start of wait mode (that is, if the slave is currently sending its SPIx_D to the master, it continues to send the same byte. Otherwise, if the slave is currently sending the last data received byte from the master, it continues to send each previously received data from the master byte).

Note

Care must be taken when expecting data from a master while the slave is in a wait mode or a stop mode where the peripheral bus clock is stopped but internal logic states are retained. Even though the shift register continues to operate, the rest of the SPI is shut down (that is, an SPRF interrupt is not generated until an exit from stop or wait mode). Also, the data from the shift register is not copied into the SPIx_D registers until after the slave SPI has exited wait or stop mode. An SPRF flag and SPIx_D copy is only generated if wait mode is entered or exited during a transmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither an SPRF nor a SPIx_D copy occurs.

16.4.8.3 SPI in Stop Mode

Operation in a stop mode where the peripheral bus clock is stopped but internal logic states are retained depends on the SPI system. The stop mode does not depend on the SPISWAI bit. Upon entry to this type of stop mode, the SPI module clock is disabled (held high or low).

- If the SPI is in master mode and exchanging data when the CPU enters the stop mode, the transmission is frozen until the CPU exits stop mode. After the exit from stop mode, data to and from the external SPI is exchanged correctly.
- In slave mode, the SPI remains synchronized with the master.

The SPI is completely disabled in a stop mode where the peripheral bus clock is stopped and internal logic states are not retained. After an exit from this type of stop mode, all registers are reset to their default values, and the SPI module must be re-initialized.

16.4.9 Reset

The reset values of registers and signals are described in Register Definition, which details the registers and their bitfields.

- If a data transmission occurs in slave mode after a reset without a write to SPIx_D, the transmission consists of "garbage" or the data last received from the master before the reset.
- Reading from SPIx_D after reset always returns zeros.

16.4.10 Interrupts

The SPI originates interrupt requests only when the SPI is enabled (the SPE bit in the SPIx_C1 register is set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

Four flag bits, three interrupt mask bits, and one interrupt vector are associated with the SPI system. The SPI interrupt enable mask (SPIE) enables interrupts from the SPI receiver full flag (SPRF) and mode fault flag (MODF). The SPI transmit interrupt enable mask (SPTIE) enables interrupts from the SPI transmit buffer empty flag (SPTEF). The SPI match interrupt enable mask bit (SPIMIE) enables interrupts from the SPI match flag (SPMF). When one of the flag bits is set, and the associated interrupt mask bit is set, a hardware interrupt request is sent to the CPU. If the interrupt mask bits are cleared, software can poll the associated flag bits instead of using interrupts. The SPI interrupt service routine (ISR) should check the flag bits to determine which event caused the interrupt. The service routine should also clear the flag bit(s) before returning from the ISR (usually near the beginning of the ISR).

16.4.10.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see the description of the C1[SSOE] bit). Once MODF is set, the current transfer is aborted and the master (MSTR) bit in the SPIx_C1 register resets to 0.

The MODF interrupt is reflected in the status register's MODF flag. Clearing the flag also clears the interrupt. This interrupt stays active while the MODF flag is set. MODF has an automatic clearing process that is described in the SPI Status Register.

16.4.10.2 SPRF

SPRF occurs when new data has been received and copied to the SPI receive data buffer.

After SPRF is set, it does not clear until it is serviced. SPRF has an automatic clearing process that is described in the SPI Status Register details. If the SPRF is not serviced before the end of the next transfer (that is, SPRF remains active throughout another transfer), the subsequent transfers are ignored and no new data is copied into the Data register.

16.4.10.3 SPTEF

SPTEF occurs when the SPI transmit buffer is ready to accept new data.

After SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process that is described in the SPI Status Register details.

16.4.10.4 SPMF

SPMF occurs when the data in the receive data buffer is equal to the data in the SPI match register.

16.5 Initialization/Application Information

This section discusses an example of how to initialize and use the SPI.

16.5.1 Initialization Sequence

Before the SPI module can be used for communication, an initialization procedure must be carried out, as follows:

1. Update control register 1 (SPIx_C1) to enable the SPI and to control interrupt enables. This register also sets the SPI as master or slave, determines clock phase and polarity, and configures the main SPI options.
2. Update control register 2 (SPIx_C2) to enable additional SPI functions such as the SPI match interrupt feature, the master mode-fault function, and bidirectional mode output and other optional features are controlled here as well.
3. Update the baud rate register (SPIx_BR) to set the prescaler and bit rate divisor for an SPI master.
4. Update the hardware match register (SPIx_M) with the value to be compared to the receive data register for triggering an interrupt if hardware match interrupts are enabled.
5. In the master, read SPIx_S while SPTEF = 1, and then write to the transmit data register (SPIx_D) to begin transfer.

16.5.2 Pseudo-Code Example

In this example, the SPI module will be set up for master mode with only hardware match interrupts enabled. The SPI will run at a maximum baud rate of bus clock divided by 2. Clock phase and polarity will be set for an active-high SPI clock where the first edge on SPSCK occurs at the start of the first cycle of a data transfer.

SPIx_C1=0x54(%01010100)				
Bit 7	SPIE	=	0	Disables receive and mode fault interrupts
Bit 6	SPE	=	1	Enables the SPI system
Bit 5	SPTIE	=	0	Disables SPI transmit interrupts
Bit 4	MSTR	=	1	Sets the SPI module as a master SPI device
Bit 3	CPOL	=	0	Configures SPI clock as active-high
Bit 2	CPHA	=	1	First edge on SPSCK at start of first data transfer cycle
Bit 1	SSOE	=	0	Determines SS pin function when mode fault enabled
Bit 0	LSBFE	=	0	SPI serial data transfers start with most significant bit

SPIx_C2 = 0x80(%10000000)				
Bit 7	SPMIE	=	1	SPI hardware match interrupt enabled
Bit 6		=	0	Unimplemented
Bit 5		=	0	Reserved
Bit 4	MODFEN	=	0	Disables mode fault function
Bit 3	BIDIROE	=	0	SPI data I/O pin acts as input
Bit 2		=	0	Reserved
Bit 1	SPISWAI	=	0	SPI clocks operate in wait mode
Bit 0	SPC0	=	0	uses separate pins for data input and output

SPIx_BR = 0x00(%00000000)				
Bit 7		=	0	Reserved
Bit 6:4		=	000	Sets prescale divisor to 1
Bit 3:0		=	0000	Sets baud rate divisor to 2

SPIx_S = 0x00(%00000000)				
Bit 7	SPRF	=	0	Flag is set when receive data buffer is full
Bit 6	SPMF	=	0	Flag is set when SPI_M = receive data buffer
Bit 5	SPTEF	=	0	Flag is set when transmit data buffer is empty
Bit 4	MODF	=	0	Mode fault flag for master mode
Bit 3:0		=	0	Reserved

SPIx_M = 0xXX
Holds bits 0–7 of the hardware match buffer.

SPIx_D = 0xxx
Holds bits 0–7 of the data to be transmitted by the transmit buffer and received by the receive buffer.

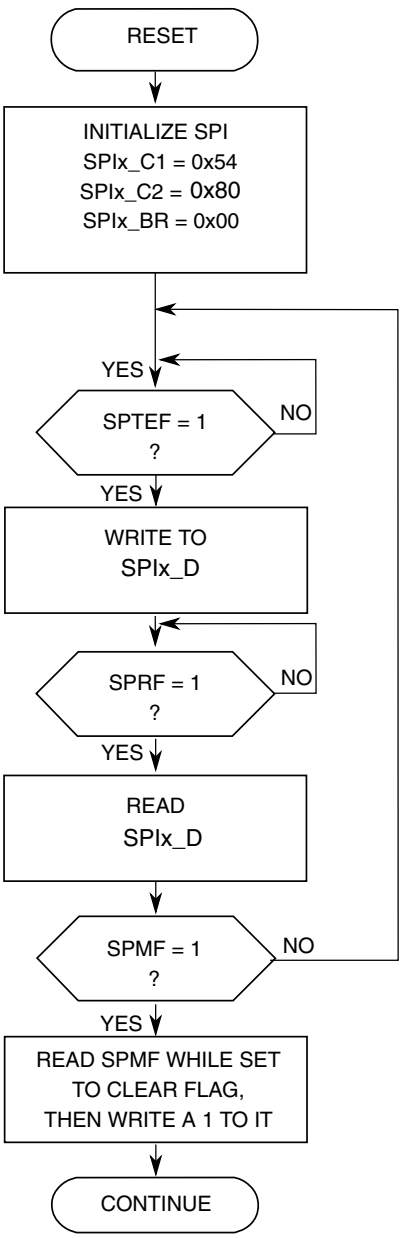


Figure 16-6. Initialization Flowchart Example for SPI Master Device

Chapter 17
16-Bit Serial Peripheral Interface (16-Bit SPI)

17.1 Introduction

NOTE

For the chip-specific implementation details of this module's instances, see the chip configuration information.

The serial peripheral interface (SPI) module provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, and memories, among others.

The SPI runs at a baud rate up to the bus clock divided by two in master mode and up to the bus clock divided by four in slave mode. Software can poll the status flags, or SPI operation can be interrupt driven.

NOTE

For the actual maximum SPI baud rate, refer to the Chip Configuration details and to the device’s Data Sheet.

The SPI also supports a data length of 8 or 16 bits and includes a hardware match feature for the receive data buffer.

17.1.1 Features

The SPI includes these distinctive features:

- Master mode or slave mode operation
- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate

- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers

17.1.2 Modes of operation

The SPI functions in the following three modes.

- Run mode

  This is the basic mode of operation.

- Wait mode

  SPI operation in Wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPIx_C2 register. In Wait mode, if C2[SPISWAI] is clear, the SPI operates like in Run mode. If C2[SPISWAI] is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU enters Run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

- Stop mode

  To reduce power consumption, the SPI is inactive in stop modes where the peripheral bus clock is stopped but internal logic states are retained. If the SPI is configured as a master, any transmission in progress stops, but is resumed after the CPU enters run mode. If the SPI is configured as a slave, reception and transmission of a data continues, so that the slave stays synchronized to the master.

The SPI is completely disabled in Stop modes where the peripheral bus clock is stopped and internal logic states are not retained. When the CPU wakes from these Stop modes, all SPI register content is reset.

Detailed descriptions of operating modes appear in Low-power mode options.

17.1.3 Block diagrams

This section includes block diagrams showing SPI system connections, the internal organization of the SPI module, and the SPI clock dividers that control the master mode bit rate.

17.1.3.1 SPI system block diagram

The following figure shows the SPI modules of two MCUs connected in a master-slave arrangement. The master device initiates all SPI data transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. The transfer effectively exchanges the data that was in the SPI shift registers of the two SPI systems. The SPSCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input (SS pin). In this system, the master device has configured its SS pin as an optional slave select output.

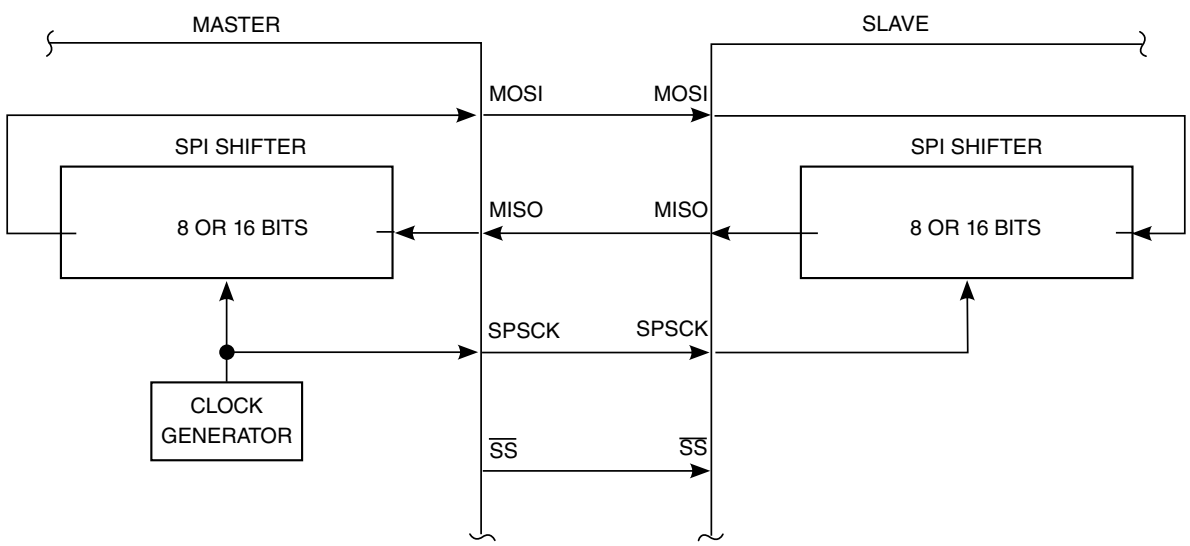


Figure 17-1. SPI system connections

17.1.3.2 SPI module block diagram

The following is a block diagram of the SPI module. The central element of the SPI is the SPI shift register. Data is written to the double-buffered transmitter (write to SPIx_DH:SPIx_DL) and gets transferred to the SPI Shift Register at the start of a data transfer. After shifting in 8 bits or 16 bits (as determined by the SPIMODE bit) of data, the data is transferred into the double-buffered receiver where it can be read from SPIx_DH:SPIx_DL. Pin multiplexing logic controls connections between MCU pins and the SPI module.

When the FIFO feature is supported: Additionally there is an 8-byte receive FIFO and an 8-byte transmit FIFO that (once enabled) provide features to allow fewer CPU interrupts to occur when transmitting/receiving high volume/high speed data. When FIFO mode is enabled, the SPI can still function in either 8-bit or 16-bit mode (as per SPIMODE bit) and three additional flags help monitor the FIFO status. Two of these flags can provide CPU interrupts.

When the SPI is configured as a master, the clock output is routed to the SPSCK pin, the shifter output is routed to MOSI, and the shifter input is routed from the MISO pin.

When the SPI is configured as a slave, the SPSCK pin is routed to the clock input of the SPI, the shifter output is routed to MISO, and the shifter input is routed from the MOSI pin.

In the external SPI system, simply connect all SPSCK pins to each other, all MISO pins together, and all MOSI pins together. Peripheral devices often use slightly different names for these pins.

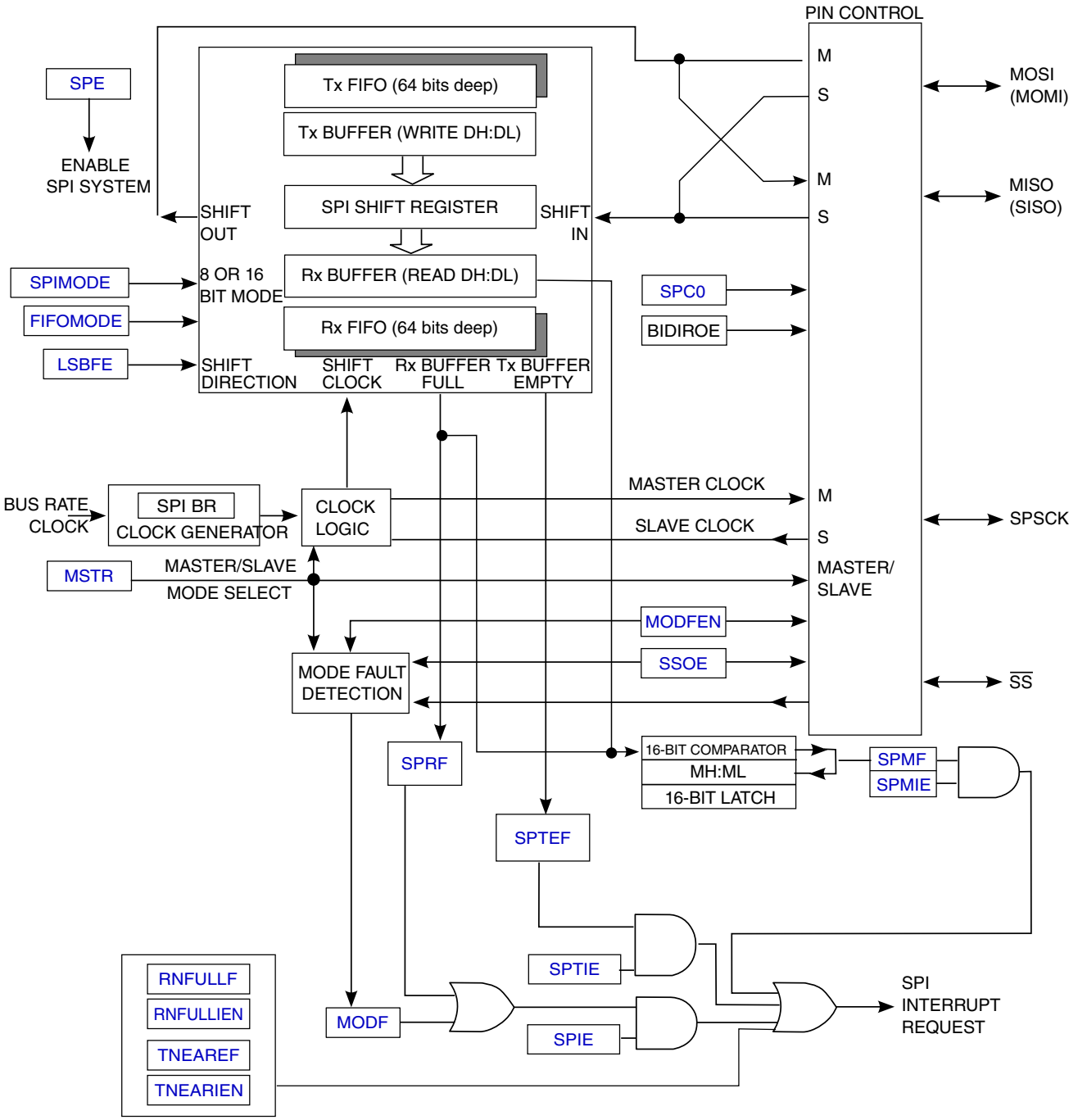


Figure 17-2. SPI Module Block Diagram with FIFO

17.2 External signal description

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled (SPE = 0), these four pins revert to other functions that are not controlled by the SPI (based on chip configuration).

17.2.1 SPSCK — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

17.2.2 MOSI — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and SPC0 is 0, this pin is the serial data input. If SPC0 is 1 to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE is 0) or an output (BIDIROE is 1). If SPC0 is 1 and slave mode is selected, this pin is not used by the SPI and reverts to other functions (based on chip configuration).

17.2.3 MISO — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero (SPC0) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and SPC0 is 0, this pin is the serial data output. If SPC0 is 1 to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO), and the bidirectional mode output enable bit determines whether the pin acts as an input (BIDIROE is 0) or an output (BIDIROE is 1). If SPC0 is 1 and master mode is selected, this pin is not used by the SPI and reverts to other functions (based on chip configuration).

17.2.4 $\overline{SS}$ — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off (MODFEN is 0), this pin is not used by the SPI and reverts to other functions (based on chip configuration). When the SPI is enabled as a master and MODFEN is 1, the slave select output enable bit determines whether this pin acts as the mode fault input (SSOE is 0) or as the slave select output (SSOE is 1).

17.3 Memory map/register definition

The SPI has 8-bit registers to select SPI options, to control baud rate, to report SPI status, to hold an SPI data match value, and for transmit/receive data.

SPI memory map

Address offset (hex)	Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	30A0	SPI Control Register 1 (SPI1_C1)	8	R/W	04h	17.3.1/471
1	30A1	SPI Control Register 2 (SPI1_C2)	8	R/W	00h	17.3.2/473
2	30A2	SPI Baud Rate Register (SPI1_BR)	8	R/W	00h	17.3.3/474
3	30A3	SPI Status Register (SPI1_S)	8	R/W	20h	17.3.4/476
4	30A4	SPI data register high (SPI1_DH)	8	R/W	00h	17.3.5/479
5	30A5	SPI Data Register low (SPI1_DL)	8	R/W	00h	17.3.6/479
6	30A6	SPI match register high (SPI1_MH)	8	R/W	00h	17.3.7/480
7	30A7	SPI Match Register low (SPI1_ML)	8	R/W	00h	17.3.8/480
8	30A8	SPI control register 3 (SPI1_C3)	8	R/W	00h	17.3.9/481
9	30A9	SPI clear interrupt register (SPI1_CI)	8	R/W	00h	17.3.10/482

17.3.1 SPI Control Register 1 (SPIx_C1)

This read/write register includes the SPI enable control, interrupt enables, and configuration options.

Address: 30A0h base + 0h offset = 30A0h

Bit	7	6	5	4	3	2	1	0
Read Write	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

SPI1_C1 field descriptions

Field	Description
7 SPIE	SPI Interrupt Enable: for SPRF and MODF (when FIFO is not supported or not enabled) or for read FIFO (when FIFO is supported and enabled) When the FIFO is not supported or not enabled (FIFOMODE is not present or is 0): Enables the interrupt for SPI receive buffer full (SPRF) and mode fault (MODF) events.

Table continues on the next page...

SPI1_C1 field descriptions (continued)

Field	Description
	When the FIFO is supported and enabled (FIFOMODE is 1): This bit enables the SPI to interrupt the CPU when the receive FIFO is full. An interrupt occurs when the SPRF bit is set or the MODF bit is set. 0 Interrupts from SPRF and MODF are inhibited—use polling (when FIFOMODE is not present or is 0) or Read FIFO Full Interrupts are disabled (when FIFOMODE is 1) 1 Request a hardware interrupt when SPRF or MODF is 1 (when FIFOMODE is not present or is 0) or Read FIFO Full Interrupts are enabled (when FIFOMODE is 1)
6 SPE	SPI System Enable Enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, the SPI is disabled and forced into an idle state, and all status bits in the S register are reset. 0 SPI system inactive 1 SPI system enabled
5 SPTIE	SPI Transmit Interrupt Enable When the FIFO is not supported or not enabled (FIFOMODE is not present or is 0): This is the interrupt enable bit for SPI transmit buffer empty (SPTEF). An interrupt occurs when the SPI transmit buffer is empty (SPTEF is set). When the FIFO is supported and enabled (FIFOMODE is 1): This is the interrupt enable bit for SPI transmit FIFO empty (SPTEF). An interrupt occurs when the SPI transmit FIFO is empty (SPTEF is set). 0 Interrupts from SPTEF inhibited (use polling) 1 When SPTEF is 1, hardware interrupt requested
4 MSTR	Master/Slave Mode Select Selects master or slave mode operation. 0 SPI module configured as a slave SPI device 1 SPI module configured as a master SPI device
3 CPOL	Clock Polarity Selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. This bit effectively places an inverter in series with the clock signal either from a master SPI device or to a slave SPI device. Refer to the description of “SPI Clock Formats” for details. 0 Active-high SPI clock (idles low) 1 Active-low SPI clock (idles high)
2 CPHA	Clock Phase Selects one of two clock formats for different kinds of synchronous serial peripheral devices. Refer to the description of “SPI Clock Formats” for details. 0 First edge on SPSCK occurs at the middle of the first cycle of a data transfer. 1 First edge on SPSCK occurs at the start of the first cycle of a data transfer.
1 SSOE	Slave Select Output Enable This bit is used in combination with the Mode Fault Enable (MODFEN) field in the C2 register and the Master/Slave (MSTR) control bit to determine the function of the $\overline{SS}$ pin. 0 When C2[MODFEN] is 0: In master mode, $\overline{SS}$ pin function is general-purpose I/O (not SPI). In slave mode, $\overline{SS}$ pin function is slave select input.

Table continues on the next page...

SPI1_C1 field descriptions (continued)

Field	Description
	When C2[MODFEN] is 1: In master mode, $\overline{SS}$ pin function is $\overline{SS}$ input for mode fault. In slave mode, $\overline{SS}$ pin function is slave select input. 1 When C2[MODFEN] is 0: In master mode, $\overline{SS}$ pin function is general-purpose I/O (not SPI). In slave mode, $\overline{SS}$ pin function is slave select input. When C2[MODFEN] is 1: In master mode, $\overline{SS}$ pin function is automatic $\overline{SS}$ output. In slave mode: $\overline{SS}$ pin function is slave select input.
0 LSBFE	LSB First (shifter direction) This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7 (or bit 15 in 16-bit mode). 0 SPI serial data transfers start with the most significant bit. 1 SPI serial data transfers start with the least significant bit.

17.3.2 SPI Control Register 2 (SPIx_C2)

This read/write register is used to control optional features of the SPI system.

Address: 30A0h base + 1h offset = 30A1h

Bit	7	6	5	4	3	2	1	0
Read Write	SPMIE	SPIMODE	Reserved	MODFEN	BIDIROE	Reserved	SPISWAI	SPC0
Reset	0	0	0	0	0	0	0	0

SPI1_C2 field descriptions

Field	Description
7 SPMIE	SPI Match Interrupt Enable This is the interrupt enable bit for the SPI receive data buffer hardware match (SPMF) function. 0 Interrupts from SPMF inhibited (use polling) 1 When SPMF is 1, requests a hardware interrupt
6 SPIMODE	SPI 8-bit or 16-bit mode This bit allows the user to select either an 8-bit or 16-bit SPI data transmission length. In master mode, a change of this bit aborts a transmission in progress, forces the SPI system into an idle state, and resets all status bits in the S register. Refer to the description of “Data Transmission Length” for details. 0 8-bit SPI shift register, match register, and buffers 1 16-bit SPI shift register, match register, and buffers
5 Reserved	This field is reserved. Do not write to this reserved bit.
4 MODFEN	Master Mode-Fault Function Enable

Table continues on the next page...

SPI1_C2 field descriptions (continued)

Field	Description
	When the SPI is configured for slave mode, this bit has no meaning or effect. (The $\overline{SS}$ pin is the slave select input.) In master mode, this bit determines how the $\overline{SS}$ pin is used. For details, refer to the description of the SSOE bit in the C1 register. 0 Mode fault function disabled, master $\overline{SS}$ pin reverts to general-purpose I/O not controlled by SPI 1 Mode fault function enabled, master $\overline{SS}$ pin acts as the mode fault input or the slave select output
3 BIDIROE	Bidirectional Mode Output Enable When bidirectional mode is enabled because SPI pin control 0 (SPC0) is set to 1, BIDIROE determines whether the SPI data output driver is enabled to the single bidirectional SPI I/O pin. Depending on whether the SPI is configured as a master or a slave, it uses the MOSI (MOMI) or MISO (SISO) pin, respectively, as the single SPI data I/O pin. When SPC0 is 0, BIDIROE has no meaning or effect. 0 Output driver disabled so SPI data I/O pin acts as an input 1 SPI I/O pin enabled as an output
2 Reserved	This field is reserved. Do not write to this reserved bit.
1 SPISWAI	SPI Stop in Wait Mode This bit is used for power conservation while the device is in Wait mode. 0 SPI clocks continue to operate in Wait mode. 1 SPI clocks stop when the MCU enters Wait mode.
0 SPC0	SPI Pin Control 0 Enables bidirectional pin configurations. 0 SPI uses separate pins for data input and data output (pin mode is normal). In master mode of operation: MISO is master in and MOSI is master out. In slave mode of operation: MISO is slave out and MOSI is slave in. 1 SPI configured for single-wire bidirectional operation (pin mode is bidirectional). In master mode of operation: MISO is not used by SPI; MOSI is master in when BIDIROE is 0 or master I/O when BIDIROE is 1. In slave mode of operation: MISO is slave in when BIDIROE is 0 or slave I/O when BIDIROE is 1; MOSI is not used by SPI.

17.3.3 SPI Baud Rate Register (SPIx_BR)

Use this register to set the prescaler and bit rate divisor for an SPI master. This register may be read or written at any time.

Address: 30A0h base + 2h offset = 30A2h

Bit	7	6	5	4	3	2	1	0
Read	0	SPPR[2:0]			SPR[3:0]			
Write								
Reset	0	0	0	0	0	0	0	0

SPI1_BR field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–4 SPPR[2:0]	SPI Baud Rate Prescale Divisor This 3-bit field selects one of eight divisors for the SPI baud rate prescaler. The input to this prescaler is the bus rate clock (BUSCLK). The output of this prescaler drives the input of the SPI baud rate divider. Refer to the description of “SPI Baud Rate Generation” for details. 000 Baud rate prescaler divisor is 1. 001 Baud rate prescaler divisor is 2. 010 Baud rate prescaler divisor is 3. 011 Baud rate prescaler divisor is 4. 100 Baud rate prescaler divisor is 5. 101 Baud rate prescaler divisor is 6. 110 Baud rate prescaler divisor is 7. 111 Baud rate prescaler divisor is 8.
SPR[3:0]	SPI Baud Rate Divisor This 4-bit field selects one of nine divisors for the SPI baud rate divider. The input to this divider comes from the SPI baud rate prescaler. Refer to the description of “SPI Baud Rate Generation” for details. 0000 Baud rate divisor is 2. 0001 Baud rate divisor is 4. 0010 Baud rate divisor is 8. 0011 Baud rate divisor is 16. 0100 Baud rate divisor is 32. 0101 Baud rate divisor is 64. 0110 Baud rate divisor is 128. 0111 Baud rate divisor is 256. 1000 Baud rate divisor is 512. All others Reserved

17.3.4 SPI Status Register (SPIx_S)

When the FIFO is supported and enabled (FIFOMODE is 1): This register has four flags that provide mechanisms to support an 8-byte FIFO mode: RNFULLF, TNEARF, TXFULLF, and RFIFOEF. When the SPI is in 8-byte FIFO mode, the function of SPRF and SPTEF differs slightly from their function in the normal buffered modes, mainly regarding how these flags are cleared by the amount available in the transmit and receive FIFOs.

- The RNFULLF and TNEAREF help improve the efficiency of FIFO operation when transfering large amounts of data. These flags provide a "watermark" feature of the FIFOs to allow continuous transmissions of data when running at high speed.
- The RNFULLF can generate an interrupt if the RNFULLIEN bit in the C3 register is set, which allows the CPU to start emptying the receive FIFO without delaying the reception of subsequent bytes. The user can also determine if all data in the receive FIFO has been read by monitoring the RFIFOEF.
- The TNEAREF can generate an interrupt if the TNEARIEN bit in the C3 register is set, which allows the CPU to start filling the transmit FIFO before it is empty and thus to prevent breaks in SPI transmission.

NOTE

At an initial POR, the values of TNEAREF and RFIFOEF are 0. However, the status (S) register and both TX and RX FIFOs are reset due to a change of SPIMODE, FIFOMODE or SPE. If this type of reset occurs and FIFOMODE is 0, TNEAREF and RFIFOEF continue to reset to 0. If this type of reset occurs and FIFOMODE is 1, TNEAREF and RFIFOEF reset to 1.

Address: 30A0h base + 3h offset = 30A3h

Bit	7	6	5	4	3	2	1	0
Read	SPRF	SPMF	SPTEF	MODF	RNFULLF	TNEAREF	TXFULLF	RFIFOEF
Write		w1c						
Reset	0	0	1	0	0	0	0	0

SPI1_S field descriptions

Field	Description
7 SPRF	SPI Read Buffer Full Flag (when FIFO is not supported or not enabled) or SPI read FIFO FULL flag (when FIFO is supported and enabled) When the FIFO is not supported or not enabled (FIFOMODE is not present or is 0): SPRF is set at the completion of an SPI transfer to indicate that received data may be read from the SPI data (DH:DL) register. SPRF is cleared by reading SPRF while it is set and then reading the SPI data register.

Table continues on the next page...

SPI1_S field descriptions (continued)

Field	Description
	When FIFOMODE is 1: This bit indicates the status of the read FIFO when FIFOMODE is enabled. The SPRF is set when the read FIFO has received 64 bits (4 words or 8 bytes) of data from the shifter and there have been no CPU reads of the SPI data (DH:DL) register. SPRF is cleared by reading the SPI data register, which empties the FIFO assuming another SPI message is not received. 0 No data available in the receive data buffer (when FIFOMODE is not present or is 0) or Read FIFO is not full (when FIFOMODE is 1) 1 Data available in the receive data buffer (when FIFOMODE is not present or is 0) or Read FIFO is full (when FIFOMODE is 1)
6 SPMF	SPI Match Flag SPMF is set after SPRF is 1 when the value in the receive data buffer matches the value in the MH:ML registers. **NOTE:** This SPMF can be cleared only when it is read as 1. To clear this flag, read SPMF first and then write a 1 to it. 0 Value in the receive data buffer does not match the value in the MH:ML registers 1 Value in the receive data buffer matches the value in the MH:ML registers
5 SPTEF	SPI Transmit Buffer Empty Flag (when FIFO is not supported or not enabled) or SPI transmit FIFO empty flag (when FIFO is supported and enabled) When the FIFO is not supported or not enabled (FIFOMODE is not present or is 0): This bit is set when the transmit data buffer is empty. SPTEF is cleared by reading the S register with SPTEF set and then writing a data value to the transmit buffer at DH:DL. The S register must be read with SPTEF set to 1 before writing data to the DH:DL register; otherwise, the DH:DL write is ignored. SPTEF is automatically set when all data from the transmit buffer transfers into the transmit shift register. For an idle SPI, data written to DH:DL is transferred to the shifter almost immediately so that SPTEF is set within two bus cycles, allowing a second set of data to be queued into the transmit buffer. After completion of the transfer of the data in the shift register, the queued data from the transmit buffer automatically moves to the shifter, and SPTEF is set to indicate that room exists for new data in the transmit buffer. If no new data is waiting in the transmit buffer, SPTEF simply remains set and no data moves from the buffer to the shifter. When the FIFO is supported and enabled (FIFOMODE is 1): This bit provides the status of the FIFO rather than of an 8-bit or a 16-bit buffer. This bit is set when the transmit FIFO is empty. SPTEF is cleared by writing a data value to the transmit FIFO at DH:DL. SPTEF is automatically set when all data from the transmit FIFO transfers into the transmit shift register. For an idle SPI, data written to the DH:DL register is transferred to the shifter almost immediately, so that SPTEF is set within two bus cycles. A second write of data to the DH:DL register clears this SPTEF flag. After completion of the transfer of the data in the shift register, the queued data from the transmit FIFO automatically moves to the shifter, and SPTEF will be set only when all data written to the transmit FIFO has been transfered to the shifter. If no new data is waiting in the transmit FIFO, SPTEF simply remains set and no data moves from the buffer to the shifter. 0 SPI transmit buffer not empty (when FIFOMODE is not present or is 0) or SPI FIFO not empty (when FIFOMODE is 1) 1 SPI transmit buffer empty (when FIFOMODE is not present or is 0) or SPI FIFO empty (when FIFOMODE is 1)
4 MODF	Master Mode Fault Flag MODF is set if the SPI is configured as a master and the slave select input goes low, indicating some other SPI device is also configured as a master. The $\overline{SS}$ pin acts as a mode fault error input only when C1[MSTR] is 1, C2[MODFEN] is 1, and C1[SSOE] is 0; otherwise, MODF will never be set. MODF is cleared by reading MODF while it is 1 and then writing to the SPI Control Register 1 (C1).

Table continues on the next page...

SPI1_S field descriptions (continued)

Field	Description
	0 No mode fault error 1 Mode fault error detected
3 RNFULLF	Receive FIFO nearly full flag This flag is set when more than three 16-bit words or six 8-bit bytes of data remain in the receive FIFO, provided C3[4] is 0, or when more than two 16-bit words or four 8-bit bytes of data remain in the receive FIFO, provided C3[4] is 1. It has no function if FIFOMODE is not present or is 0. 0 Receive FIFO has received less than 48 bits (when C3[4] is 0) or less than 32 bits (when C3[4] is 1) 1 Receive FIFO has received data of an amount equal to or greater than 48 bits (when C3[4] is 0) or 32 bits (when C3[4] is 1)
2 TNEAREF	Transmit FIFO nearly empty flag This flag is set when only one 16-bit word or two 8-bit bytes of data remain in the transmit FIFO, provided C3[5] is 0, or when only two 16-bit words or four 8-bit bytes of data remain in the transmit FIFO, provided C3[5] is 1. If FIFOMODE is not enabled, ignore this bit. **NOTE:** At an initial POR, the values of TNEAREF and RFIFOEF are 0. However, the status (S) register and both TX and RX FIFOs are reset due to a change of SPIMODE, FIFOMODE or SPE. If this type of reset occurs and FIFOMODE is 0, TNEAREF and RFIFOEF continue to reset to 0. If this type of reset occurs and FIFOMODE is 1, TNEAREF and RFIFOEF reset to 1. 0 Transmit FIFO has more than 16 bits (when C3[5] is 0) or more than 32 bits (when C3[5] is 1) remaining to transmit 1 Transmit FIFO has an amount of data equal to or less than 16 bits (when C3[5] is 0) or 32 bits (when C3[5] is 1) remaining to transmit
1 TXFULLF	Transmit FIFO full flag This bit indicates the status of the transmit FIFO when FIFOMODE is enabled. This flag is set when there are 8 bytes in the transmit FIFO. If FIFOMODE is not enabled, ignore this bit. 0 Transmit FIFO has less than 8 bytes 1 Transmit FIFO has 8 bytes of data
0 RFIFOEF	SPI read FIFO empty flag This bit indicates the status of the read FIFO when FIFOMODE is enabled. If FIFOMODE is not enabled, ignore this bit. **NOTE:** At an initial POR, the values of TNEAREF and RFIFOEF are 0. However, the status (S) register and both TX and RX FIFOs are reset due to a change of SPIMODE, FIFOMODE or SPE. If this type of reset occurs and FIFOMODE is 0, TNEAREF and RFIFOEF continue to reset to 0. If this type of reset occurs and FIFOMODE is 1, TNEAREF and RFIFOEF reset to 1. 0 Read FIFO has data. Reads of the DH:DL registers in 16-bit mode or the DL register in 8-bit mode will empty the read FIFO. 1 Read FIFO is empty.

17.3.5 SPI data register high (SPIx_DH)

Refer to the description of the DL register.

Address: 30A0h base + 4h offset = 30A4h

Bit	7	6	5	4	3	2	1	0
Read Write	Bits[15:8]							
Reset	0	0	0	0	0	0	0	0

SPI1_DH field descriptions

Field	Description
Bits[15:8]	Data (high byte)

17.3.6 SPI Data Register low (SPIx_DL)

This register, together with the DH register, is both the input and output register for SPI data. A write to the registers writes to the transmit data buffer, allowing data to be queued and transmitted.

When the SPI is configured as a master, data queued in the transmit data buffer is transmitted immediately after the previous transmission has completed.

The SPTEF bit in the S register indicates when the transmit data buffer is ready to accept new data. The S register must be read when S[SPTEF] is set before writing to the SPI data registers; otherwise, the write is ignored.

Data may be read from the SPI data registers any time after S[SPRF] is set and before another transfer is finished. Failure to read the data out of the receive data buffer before a new transfer ends causes a receive overrun condition, and the data from the new transfer is lost. The new data is lost because the receive buffer still held the previous character and was not ready to accept the new data. There is no indication for a receive overrun condition, so the application system designer must ensure that previous data has been read from the receive buffer before a new transfer is initiated.

In 8-bit mode, only the DL register is available. Reads of the DH register return all zeros. Writes to the DH register are ignored.

In 16-bit mode, reading either byte (the DH or DL register) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. Writing to either byte (the DH or DL register) latches the value into a buffer. When both bytes have been written, they are transferred as a coherent 16-bit value into the transmit data buffer.

Address: 30A0h base + 5h offset = 30A5h

Bit	7	6	5	4	3	2	1	0
Read Write	Bits[7:0]							
Reset	0	0	0	0	0	0	0	0

SPI1_DL field descriptions

Field	Description
Bits[7:0]	Data (low byte)

17.3.7 SPI match register high (SPIx_MH)

Refer to the description of the ML register.

Address: 30A0h base + 6h offset = 30A6h

Bit	7	6	5	4	3	2	1	0
Read Write	Bits[15:8]							
Reset	0	0	0	0	0	0	0	0

SPI1_MH field descriptions

Field	Description
Bits[15:8]	Hardware compare value (high byte)

17.3.8 SPI Match Register low (SPIx_ML)

This register, together with the MH register, contains the hardware compare value. When the value received in the SPI receive data buffer equals this hardware compare value, the SPI Match Flag in the S register (S[SPMF]) sets.

In 8-bit mode, only the ML register is available. Reads of the MH register return all zeros. Writes to the MH register are ignored.

In 16-bit mode, reading either byte (the MH or ML register) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. Writing to either byte (the MH or ML register) latches the value into a buffer. When both bytes have been written, they are transferred as a coherent value into the SPI match registers.

Address: 30A0h base + 7h offset = 30A7h

Bit	7	6	5	4	3	2	1	0
Read Write	Bits[7:0]							
Reset	0	0	0	0	0	0	0	0

SPI1_ML field descriptions

Field	Description
Bits[7:0]	Hardware compare value (low byte)

17.3.9 SPI control register 3 (SPIx_C3)

This register introduces a 64-bit FIFO function on both transmit and receive buffers. It applies only for an instance of the SPI module that supports the FIFO feature.

FIFO mode is enabled by setting the FIFOMODE bit to 1. A write to this register occurs only when it sets the FIFOMODE bit to 1.

Using this FIFO feature allows the SPI to provide high speed transfers of large amounts of data without consuming large amounts of the CPU bandwidth.

Enabling this FIFO function affects the behavior of some of the read/write buffer flags in the S register as follows:

- The SPRF of the S register is 1 when the receive FIFO is filled. As a result:
  - If the SPIE bit in the C1 register is 1, SPRF interrupts the CPU.
- The SPTEF of the S register is 1 when the transmit FIFO is empty. As a result:
  - If the SPTIE bit in the C1 register is 1, SPTEF interrupts the CPU.

Two interrupt enable bits, TNEARIEN and RNFULLIEN, provide CPU interrupts based on the "watermark" feature of the TNEARF and RNFULLF flags of the S register.

Address: 30A0h base + 8h offset = 30A8h

Bit	7	6	5	4	3	2	1	0
Read	0		TNEAREF_MARK	RNFULLF_MARK	INTCLR	TNEARIEN	RNFULLIEN	FIFOMODE
Write								
Reset	0	0	0	0	0	0	0	0

SPI1_C3 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5 TNEAREF_ MARK	Transmit FIFO nearly empty watermark This bit selects the mark after which the TNEAREF flag is asserted. 0 TNEAREF is set when the transmit FIFO has 16 bits or less 1 TNEAREF is set when the transmit FIFO has 32 bits or less
4 RNFULLF_ MARK	Receive FIFO nearly full watermark This bit selects the mark after which the RNFULLF flag is asserted. 0 RNFULLF is set when the receive FIFO has 48 bits or more 1 RNFULLF is set when the receive FIFO has 32 bits or more
3 INTCLR	Interrupt clearing mechanism select This bit selects the mechanism by which the SPRF, SPTEF, TNEAREF, and RNFULLF interrupts are cleared. 0 These interrupts are cleared when the corresponding flags are cleared depending on the state of the FIFOs 1 These interrupts are cleared by writing the corresponding bits in the CI register
2 TNEARIEN	Transmit FIFO nearly empty interrupt enable Writing 1 to this bit enables the SPI to interrupt the CPU when the TNEAREF flag is set. This bit is ignored and has no function if the FIFOMODE bit is 0. 0 No interrupt upon TNEAREF being set 1 Enable interrupts upon TNEAREF being set
1 RNFULLIEN	Receive FIFO nearly full interrupt enable Writing 1 to this bit enables the SPI to interrupt the CPU when the RNFULLF flag is set. This bit is ignored and has no function if the FIFOMODE bit is 0. 0 No interrupt upon RNFULLF being set 1 Enable interrupts upon RNFULLF being set
0 FIFOMODE	FIFO mode enable This bit enables the SPI to use a 64-bit FIFO (8 bytes or four 16-bit words) for both transmit and receive buffers. 0 Buffer mode disabled 1 Data available in the receive data buffer

17.3.10 SPI clear interrupt register (SPIx_CI)

This register applies only for an instance of the SPI module that supports the FIFO feature.

The register has four bits dedicated to clearing the interrupts. Writing 1 to these bits clears the corresponding interrupts if the INTCLR bit in the C3 register is 1. Reading these bits always returns 0.

This register also has two read-only bits to indicate the transmit FIFO and receive FIFO overrun conditions. When the receive FIFO is full and data is received, RXFOF is set. Similarily, when the transmit FIFO is full and a write to the data register occurs, TXFOF is set. These flags are cleared when the CI register is read while the flags are set.

The register has two more read-only bits to indicate the error flags. These flags are set when, due to some spurious reason, entries in the FIFO total more than 64 bits of data. At this point, all the flags in the status register are reset, and entries in the FIFO are flushed with the corresponding error flags set. These flags are cleared when the CI register is read while the flags are set.

Address: 30A0h base + 9h offset = 30A9h

Bit	7	6	5	4	3	2	1	0
Read	TXFERR	RXFERR	TXFOF	RXFOF	0	0	0	0
Write					TNEAREFCI	RNFULLFCI	SPTEFCI	SPRFCI
Reset	0	0	0	0	0	0	0	0

SPI1_CI field descriptions

Field	Description
7 TXFERR	Transmit FIFO error flag This flag indicates that a transmit FIFO error occurred because entries in the FIFO total more than 64 bits of data. 0 No transmit FIFO error occurred 1 A transmit FIFO error occurred
6 RXFERR	Receive FIFO error flag This flag indicates that a receive FIFO error occurred because entries in the FIFO total more than 64 bits of data. 0 No receive FIFO error occurred 1 A receive FIFO error occurred
5 TXFOF	Transmit FIFO overflow flag This flag indicates that a transmit FIFO overflow condition has occurred. 0 Transmit FIFO overflow condition has not occurred 1 Transmit FIFO overflow condition occurred
4 RXFOF	Receive FIFO overflow flag This flag indicates that a receive FIFO overflow condition has occurred. 0 Receive FIFO overflow condition has not occurred 1 Receive FIFO overflow condition occurred

Table continues on the next page...

SPI1_CI field descriptions (continued)

Field	Description
3 TNEAREFCI	Transmit FIFO nearly empty flag clear interrupt Writing 1 to this bit clears the TNEAREF interrupt provided that C3[3] is set.
2 RNFULLFCI	Receive FIFO nearly full flag clear interrupt Writing 1 to this bit clears the RNFULLF interrupt provided that C3[3] is set.
1 SPTEFCI	Transmit FIFO empty flag clear interrupt Writing 1 to this bit clears the SPTEF interrupt provided that C3[3] is set.
0 SPRFCI	Receive FIFO full flag clear interrupt Writing 1 to this bit clears the SPRF interrupt provided that C3[3] is set.

17.4 Functional description

This section provides the functional description of the module.

17.4.1 General

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI Control Register 1. While C1[SPE] is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select (SS)
- Serial clock (SPSCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

An SPI transfer is initiated in the master SPI device by reading the SPI status register (SPIx_S) when S[SPTEF] = 1 and then writing data to the transmit data buffer (write to SPIx_DH:SPIx_DL). When a transfer is complete, received data is moved into the receive data buffer. The SPIx_DH:SPIx_DL registers act as the SPI receive data buffer for reads and as the SPI transmit data buffer for writes.

The Clock Phase Control (CPHA) and Clock Polarity Control (CPOL) bits in the SPI Control Register 1 (SPIx_C1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. C1[CPHA] is used to accommodate two fundamentally different protocols by sampling data on odd numbered SPSCK edges or on even numbered SPSCK edges.

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI Control Register 1 is set, master mode is selected; when C1[MSTR] is clear, slave mode is selected.

17.4.2 Master mode

The SPI operates in master mode when C1[MSTR] is set. Only a master SPI module can initiate transmissions. A transmission begins by reading the SPIx_S register while S[SPTEF] = 1 and writing to the master SPI data registers. If the shift register is empty, the byte immediately transfers to the shift register. The data begins shifting out on the MOSI pin under the control of the serial clock.

- SPSCK
  - The SPR3, SPR2, SPR1, and SPR0 baud rate selection bits in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI Baud Rate register control the baud rate generator and determine the speed of the transmission. The SPSCK pin is the SPI clock output. Through the SPSCK pin, the baud rate generator of the master controls the shift register of the slave peripheral.
- MOSI, MISO pin
  - In master mode, the function of the serial data output pin (MOSI) and the serial data input pin (MISO) is determined by the SPC0 and BIDIROE control bits.
- $\overline{SS}$ pin
  - If C2[MODFEN] and C1[SSOE] are set, the SS pin is configured as slave select output. The SS output becomes low during each transmission and is high when the SPI is in idle state. If C2[MODFEN] is set and C1[SSOE] is cleared, the $\overline{SS}$ pin is configured as input for detecting mode fault error. If the SS input becomes low this indicates a mode fault error where another master tries to drive the MOSI and SPSCK lines. In this case, the SPI immediately switches to slave mode by clearing C1[MSTR] and also disables the slave output buffer MISO (or SISO in bidirectional mode). As a result, all outputs are disabled, and SPSCK, MOSI and MISO are inputs. If a transmission is in progress when the mode fault occurs, the transmission is aborted and the SPI is forced into idle state. This mode fault error also sets the Mode Fault (MODF) flag in the SPI Status Register (SPIx_S). If the SPI Interrupt Enable bit (SPIE) is set when S[MODF] gets set, then an SPI interrupt sequence is also requested. When a write to the SPI Data Register in the master occurs, there is a half SPSCK-cycle delay. After the delay,

SPSCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI Control Register 1 (see SPI clock formats).

Note

A change of C1[CPOL], C1[CPHA], C1[SSOE], C1[LSBFE], C2[MODFEN], C2[SPC0], C2[BIDIROE] with C2[SPC0] set, SPIMODE, FIFOMODE, SPPR2-SPPR0 and SPR3-SPR0 in master mode abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master has to ensure that the remote slave is set back to idle state.

17.4.3 Slave mode

The SPI operates in slave mode when the MSTR bit in SPI Control Register 1 is clear.

- SPSCK

  In slave mode, SPSCK is the SPI clock input from the master.

- MISO, MOSI pin

  In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI Control Register 2.

- SS pin

  The SS pin is the slave select input. Before a data transmission occurs, the SS pin of the slave SPI must be low. SS must remain low until the transmission is complete. If SS goes high, the SPI is forced into an idle state.

  The SS input also controls the serial data output pin. If SS is high (not selected), the serial data output pin is high impedance. If SS is low, the first bit in the SPI Data Register is driven out of the serial data output pin. Also, if the slave is not selected (SS is high), then the SPSCK input is ignored and no internal shifting of the SPI shift register occurs.

  Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

Note

When peripherals with duplex capability are used, take care not to simultaneously enable two receivers whose serial outputs drive the same system slave's serial data output line.

As long as no more than one slave device drives the system slave's serial data output line, it is possible for several slaves to receive the same transmission from a master, although the master would not receive return information from all of the receiving slaves.

If the CPHA bit in SPI Control Register 1 is clear, odd numbered edges on the SPSCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

If C1[CPHA] is set, even numbered edges on the SPSCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on C1[LSBFE].

When C1[CPHA] is set, the first edge is used to get the first data bit onto the serial data output pin. When C1[CPHA] is clear and the SS input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the eighth (SPIMODE = 0) or sixteenth (SPIMODE = 1) shift, the transfer is considered complete and the received data is transferred into the SPI Data register. To indicate transfer is complete, the SPRF flag in the SPI Status Register is set.

Note

A change of the bits FIFOMODE,SPIMODE, C2[BIDIROE] with C2[SPC0] set, C1[CPOL], C1[CPHA], C1[SSOE], C1[LSBFE], C2[MODFEN], and C2[SPC0] in slave mode will corrupt a transmission in progress and must be avoided.

17.4.4 SPI FIFO Mode

When the FIFO feature is supported: The SPI works in FIFO mode when the C3[FIFOMODE] bit is set. When the module is in FIFO mode, the SPI RX buffer and SPI TX buffer are replaced by an 8-byte-deep FIFO, as the following figures show.

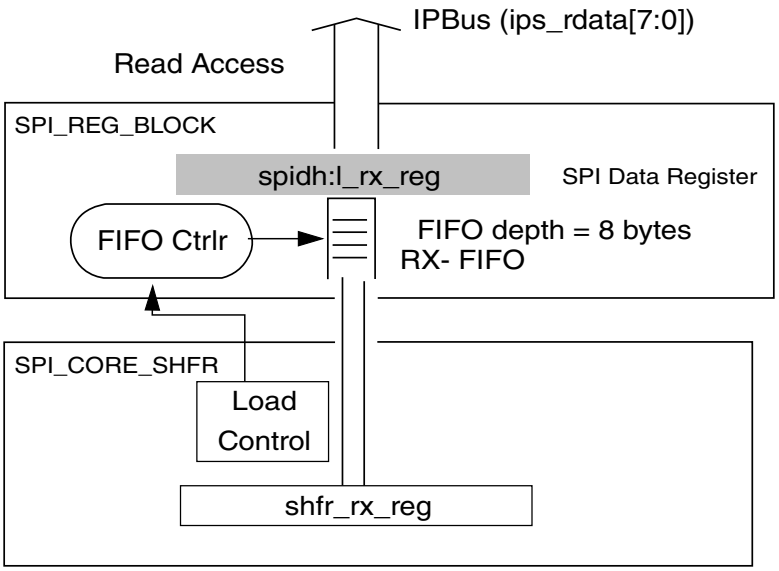


Figure 17-3. SPIH:L read side structural overview in FIFO mode

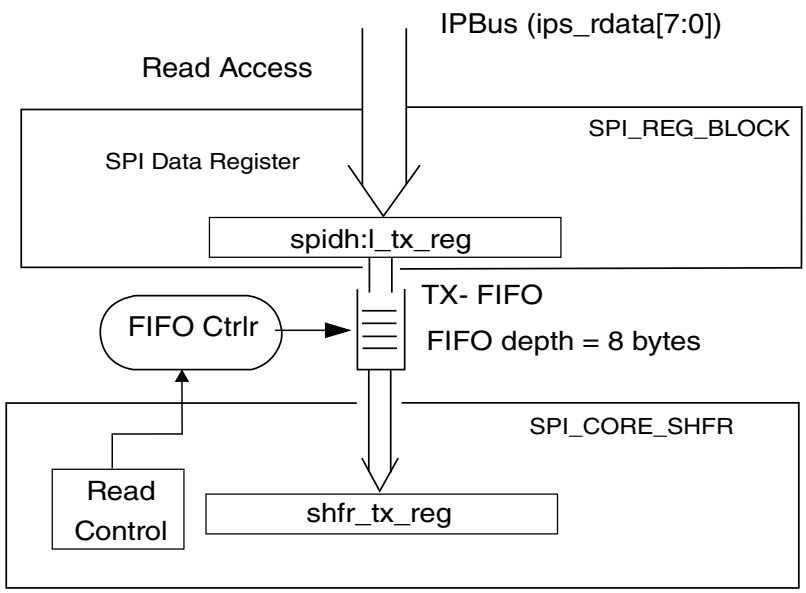


Figure 17-4. SPIH:L write side structural overview in FIFO mode

17.4.5 Data Transmission Length

The SPI can support data lengths of 8 or 16 bits. The length can be configured with the SPIMODE bit in the SPIx_C2 register.

In 8-bit mode (SPIMODE = 0), the SPI Data Register is comprised of one byte: SPIx_DL. The SPI Match Register is also comprised of only one byte: SPIx_ML. Reads of SPIx_DH and SPIx_MH will return zero. Writes to SPIx_DH and SPIx_MH will be ignored.

In 16-bit mode (SPIMODE = 1), the SPI Data Register is comprised of two bytes: SPIx_DH and SPIx_DL. Reading either byte (SPIx_DH or SPIx_DL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. Writing to either byte (SPIx_DH or SPIx_DL) latches the value into a buffer. When both bytes have been written, they are transferred as a coherent 16-bit value into the transmit data buffer.

In 16-bit mode, the SPI Match Register is also comprised of two bytes: SPIx_MH and SPIx_ML. There is no buffer mechanism for the reading of SPIxMH and SPIxML since they can only be changed by writing at CPU side. Writing to either byte (SPIx_MH or SPIx_ML) latches the value into a buffer. When both bytes have been written, they are transferred as a coherent 16-bit value into the SPI Match Register.

Any switching between 8- and 16-bit data transmission length (controlled by SPIMODE bit) in master mode will abort a transmission in progress, force the SPI system into idle state, and reset all status bits in the SPIx_S register. To initiate a transfer after writing to SPIMODE, the SPIx_S register must be read with SPTEF = 1, and data must be written to SPIx_DH:SPIx_DL in 16-bit mode (SPIMODE = 1) or SPIx_DL in 8-bit mode (SPIMODE = 0).

In slave mode, user software should write to SPIMODE only once to prevent corrupting a transmission in progress.

Note

Data can be lost if the data length is not the same for both master and slave devices.

17.4.6 SPI clock formats

To accommodate a wide variety of synchronous serial peripherals from different manufacturers, the SPI system has a Clock Polarity (CPOL) bit and a Clock Phase (CPHA) control bit in the Control Register 1 to select one of four clock formats for data transfers. C1[CPOL] selectively inserts an inverter in series with the clock. C1[CPHA] chooses between two different clock phase relationships between the clock and data.

The following figure shows the clock formats when SPIMODE = 0 (8-bit mode) and CPHA = 1. At the top of the figure, the eight bit times are shown for reference with bit 1 starting at the first SPSCK edge and bit 8 ending one-half SPSCK cycle after the eighth SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in C1[CPOL]. The SAMPLE IN waveform applies to the MOSI input of a slave or the

MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The $\overline{SS}$ OUT waveform applies to the slave select output from a master (provided C2[MODFEN] and C1[SSOE] = 1). The master $\overline{SS}$ output goes to active low one-half SPSCK cycle before the start of the transfer and goes back high at the end of the eighth bit time of the transfer. The $\overline{SS}$ IN waveform applies to the slave select input of a slave.

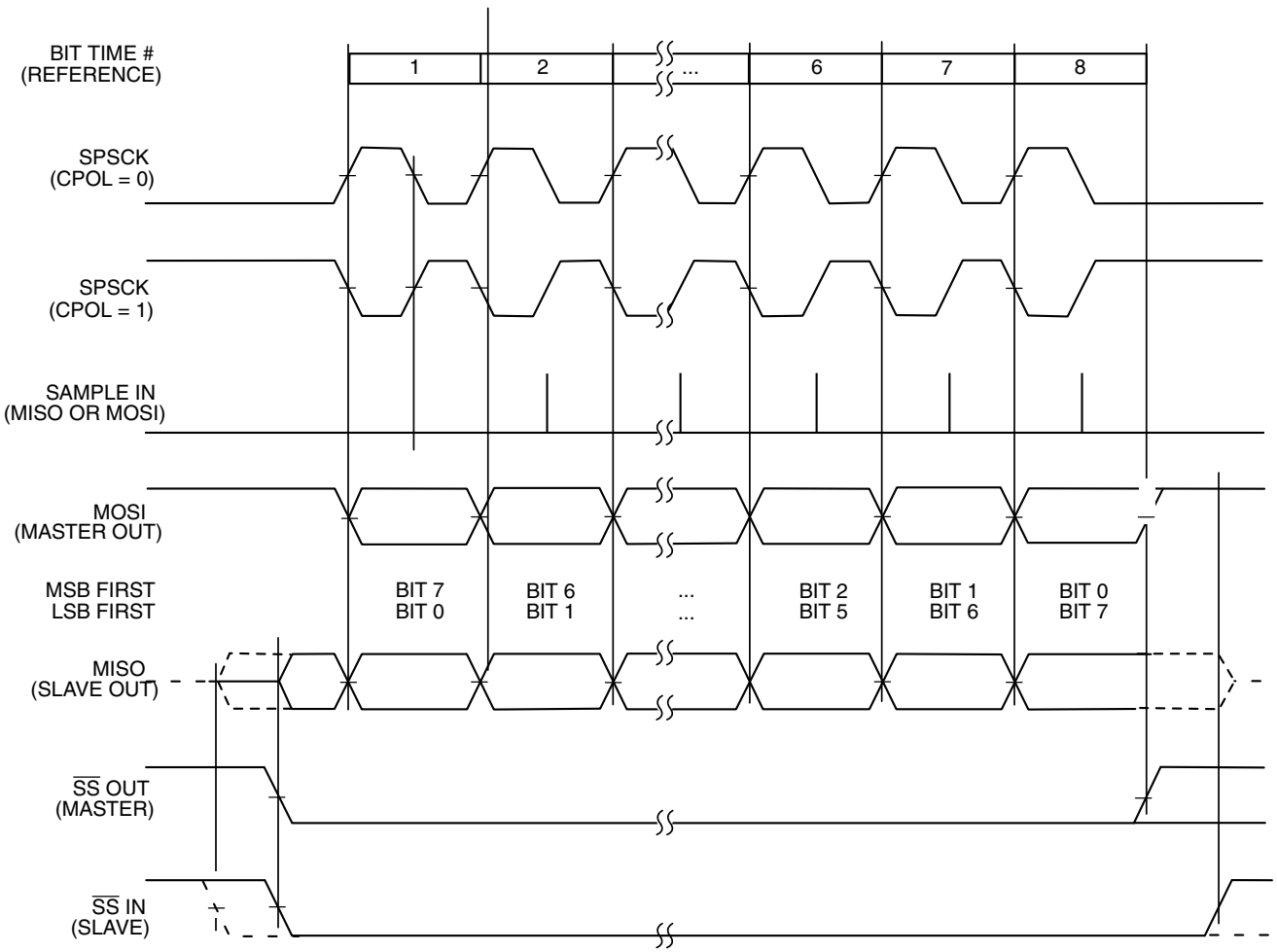


Figure 17-5. SPI clock formats (CPHA = 1)

When C1[CPHA] = 1, the slave begins to drive its MISO output when $\overline{SS}$ goes to active low, but the data is not defined until the first SPSCK edge. The first SPSCK edge shifts the first bit of data from the shifter onto the MOSI output of the master and the MISO output of the slave. The next SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the third SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled, and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively.

When C1[CPHA] = 1, the slave's $\overline{SS}$ input is not required to go to its inactive high level between transfers. In this clock format, a back-to-back transmission can occur, as follows:

1. A transmission is in progress.
2. A new data byte is written to the transmit buffer before the in-progress transmission is complete.
3. When the in-progress transmission is complete, the new, ready data byte is transmitted immediately.

Between these two successive transmissions, no pause is inserted; the $\overline{SS}$ pin remains low.

The following figure shows the clock formats when SPIMODE = 0 and C1[CPHA] = 0. At the top of the figure, the eight bit times are shown for reference with bit 1 starting as the slave is selected (SS IN goes low), and bit 8 ends at the last SPSCK edge. The MSB first and LSB first lines show the order of SPI data bits depending on the setting in LSBFE. Both variations of SPSCK polarity are shown, but only one of these waveforms applies for a specific transfer, depending on the value in CPOL. The SAMPLE IN waveform applies to the MOSI input of a slave or the MISO input of a master. The MOSI waveform applies to the MOSI output pin from a master and the MISO waveform applies to the MISO output from a slave. The SS OUT waveform applies to the slave select output from a master (provided C2[MODFEN] and C1[SSOE] = 1). The master SS output goes to active low at the start of the first bit time of the transfer and goes back high one-half SPSCK cycle after the end of the eighth bit time of the transfer. The SS IN waveform applies to the slave select input of a slave.

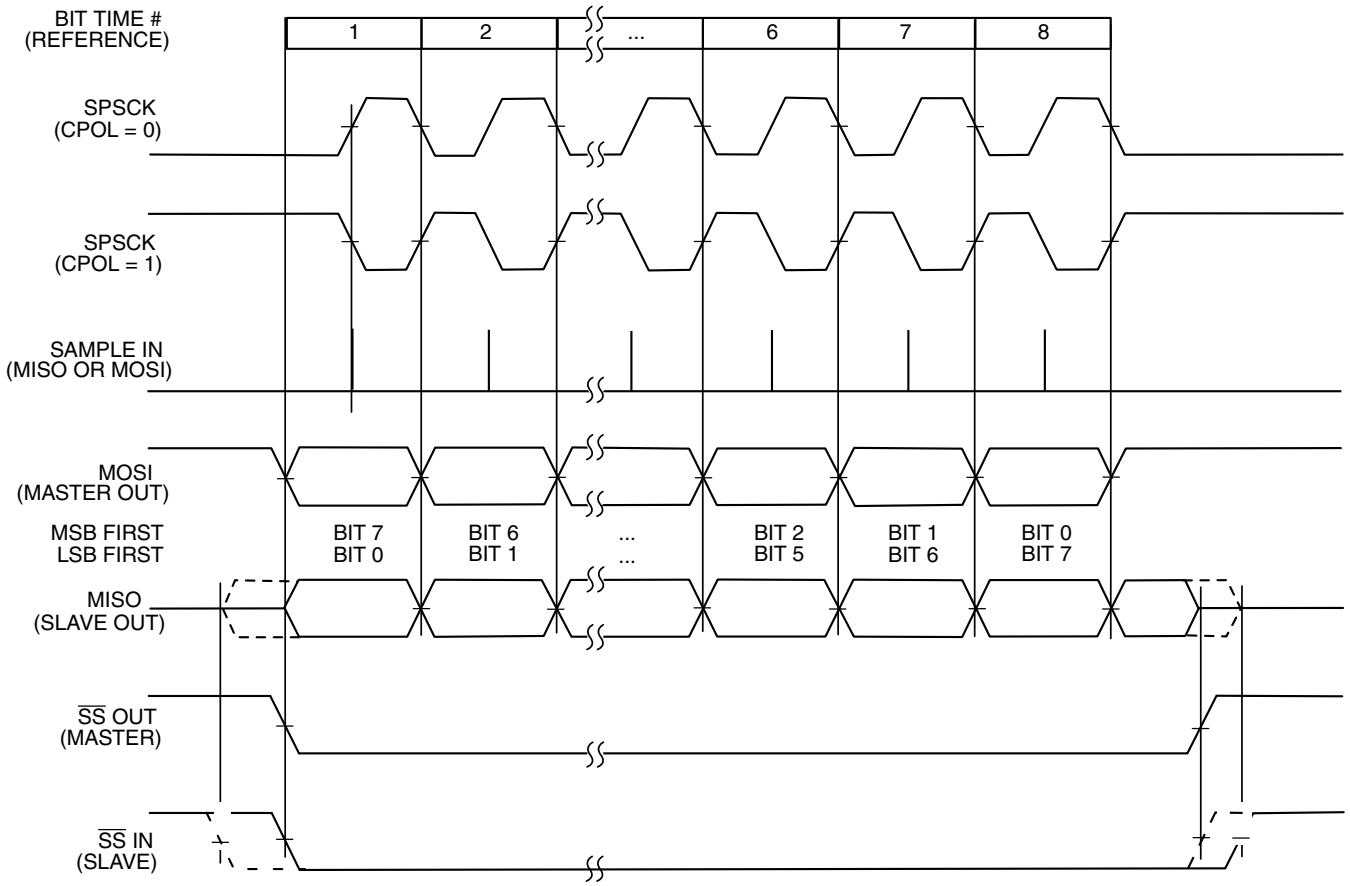


Figure 17-6. SPI clock formats (CPHA = 0)

When C1[CPHA] = 0, the slave begins to drive its MISO output with the first data bit value (MSB or LSB depending on LSBFE) when SS goes to active low. The first SPSCK edge causes both the master and the slave to sample the data bit values on their MISO and MOSI inputs, respectively. At the second SPSCK edge, the SPI shifter shifts one bit position which shifts in the bit value that was just sampled and shifts the second data bit value out the other end of the shifter to the MOSI and MISO outputs of the master and slave, respectively. When C1[CPHA] = 0, the slave's SS input must go to its inactive high level between transfers.

17.4.7 SPI baud rate generation

As shown in the following figure, the clock source for the SPI baud rate generator is the bus clock. The three prescale bits (SPPR2:SPPR1:SPPR0) choose a prescale divisor of 1, 2, 3, 4, 5, 6, 7, or 8. The three rate select bits (SPR3:SPR2:SPR1:SPR0) divide the output of the prescaler stage by 2, 4, 8, 16, 32, 64, 128, 256, or 512 to get the internal SPI master mode bit-rate clock.

The baud rate generator is activated only when the SPI is in the master mode and a serial transfer is taking place. In the other cases, the divider is disabled to decrease I_{DD} current.

The baud rate divisor equation is as follows (except those reserved combinations in the SPI Baud Rate Divisor table).

```
BaudRateDivisor = (SPPR + 1) × 2^(SPR + 1)
```

The baud rate can be calculated with the following equation:

```
BaudRate = BusClock / BaudRateDivisor
```

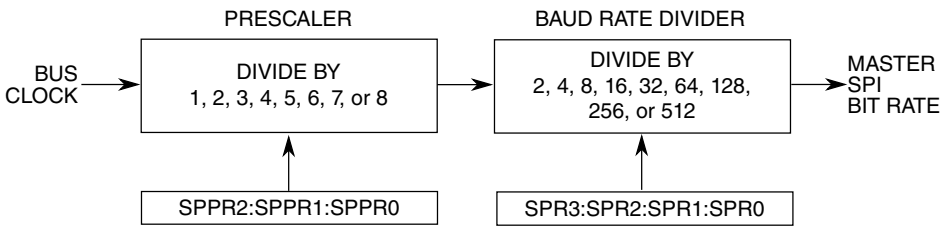


Figure 17-7. SPI baud rate generation

17.4.8 Special features

The following section describes the special features of SPI module.

17.4.8.1 $\overline{SS}$ Output

The $\overline{SS}$ output feature automatically drives the $\overline{SS}$ pin low during transmission to select external devices and drives the $\overline{SS}$ pin high during idle to deselect external devices. When the $\overline{SS}$ output is selected, the $\overline{SS}$ output pin is connected to the $\overline{SS}$ input pin of the external device.

The $\overline{SS}$ output is available only in master mode during normal SPI operation by asserting C1[SSOE] and C2[MODFEN] as shown in the description of C1[SSOE].

The mode fault feature is disabled while $\overline{SS}$ output is enabled.

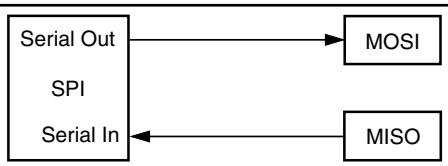
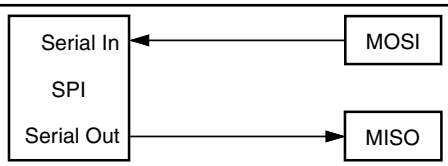
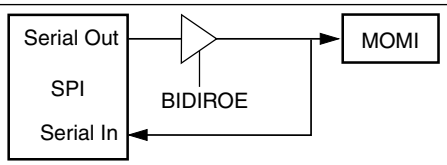
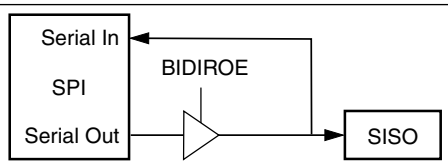
Note

Be careful when using the $\overline{SS}$ output feature in a multimaster system because the mode fault feature is not available for detecting system errors between masters.

17.4.8.2 Bidirectional mode (MOMI or SISO)

The bidirectional mode is selected when the SPC0 bit is set in SPI Control Register 2 (see the following table). In this mode, the SPI uses only one serial data pin for the interface with one or more external devices. C1[MSTR] decides which pin to use. The MOSI pin becomes the serial data I/O (MOMI) pin for the master mode, and the MISO pin becomes serial data I/O (SISO) pin for the slave mode. The MISO pin in master mode and MOSI pin in slave mode are not used by the SPI.

Table 17-1. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode **SPC0 = 0**		
Bidirectional Mode **SPC0 = 1**		

The direction of each serial I/O pin depends on C2[BIDIROE]. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

The SPSCK is an output for the master mode and an input for the slave mode.

$\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.

The bidirectional mode does not affect SPSCK and $\overline{SS}$ functions.

Note

In bidirectional master mode, with the mode fault feature enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode. In this case, MISO becomes occupied by the SPI and MOSI is not used. Consider this scenario if the MISO pin is used for another purpose.

17.4.9 Error conditions

The SPI module has one error condition: the mode fault error.

17.4.9.1 Mode fault error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SPSCK lines simultaneously. This condition is not permitted in normal operation, and it sets the MODF bit in the SPI status register automatically provided that C2[MODFEN] is set.

In the special case where the SPI is in master mode and C2[MODFEN] is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. If the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. A mode fault error does not occur in slave mode.

If a mode fault error occurs, the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So the SPSCK, MISO and MOSI pins are forced to be high impedance inputs to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for an SPI system configured in master mode, the output enable of MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for the SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI Status Register (with MODF set) followed by a write to SPI Control Register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

17.4.10 Low-power mode options

This section describes the low-power mode options.

17.4.10.1 SPI in Run mode

In Run mode, with the SPI system enable (SPE) bit in the SPI Control Register 1 clear, the SPI system is in a low-power, disabled state. SPI registers can still be accessed, but clocks to the core of this module are disabled.

17.4.10.2 SPI in Wait mode

SPI operation in Wait mode depends upon the state of the SPISWAI bit in SPI Control Register 2.

- If C2[SPISWAI] is clear, the SPI operates normally when the CPU is in Wait mode.
- If C2[SPISWAI] is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
  - If C2[SPISWAI] is set and the SPI is configured for master, any transmission and reception in progress stops at Wait mode entry. The transmission and reception resumes when the SPI exits Wait mode.
  - If C2[SPISWAI] is set and the SPI is configured as a slave, any transmission and reception in progress continues if the SPSCK continues to be driven from the master. This keeps the slave synchronized to the master and the SPSCK.

    If the master transmits data while the slave is in wait mode, the slave continues to send data consistent with the operation mode at the start of wait mode (that is, if the slave is currently sending its SPIx_DH:SPIx_DL to the master, it continues to send the same byte. Otherwise, if the slave is currently sending the last data received byte from the master, it continues to send each previously received data from the master byte).

Note

Care must be taken when expecting data from a master while the slave is in a Wait mode or a Stop mode where the peripheral bus clock is stopped but internal logic states are retained. Even though the shift register continues to operate, the rest of the SPI is shut down (that is, an SPRF interrupt is not generated until an exit from Stop or Wait mode). Also, the data from the shift register is not copied into the SPIx_DH:SPIx_DL registers until after the slave SPI has exited Wait or Stop mode. An SPRF flag and SPIx_DH:SPIx_DL copy is only generated if Wait mode is entered or exited during a transmission. If the slave enters Wait mode in idle mode and exits Wait mode in idle mode, neither an SPRF nor a SPIx_DH:SPIx_DL copy occurs.

17.4.10.3 SPI in Stop mode

Operation in a Stop mode where the peripheral bus clock is stopped but internal logic states are retained depends on the SPI system. The Stop mode does not depend on C2[SPISWAI]. Upon entry to this type of stop mode, the SPI module clock is disabled (held high or low).

- If the SPI is in master mode and exchanging data when the CPU enters the Stop mode, the transmission is frozen until the CPU exits stop mode. After the exit from stop mode, data to and from the external SPI is exchanged correctly.
- In slave mode, the SPI remains synchronized with the master.

The SPI is completely disabled in a stop mode where the peripheral bus clock is stopped and internal logic states are not retained. After an exit from this type of stop mode, all registers are reset to their default values, and the SPI module must be reinitialized.

17.4.11 Reset

The reset values of registers and signals are described in the Memory Map and Register Descriptions content, which details the registers and their bitfields.

- If a data transmission occurs in slave mode after a reset without a write to SPIx_DH:SPIx_DL, the transmission consists of "garbage" or the data last received from the master before the reset.
- Reading from SPIx_DH:SPIx_DL after reset always returns zeros.

17.4.12 Interrupts

The SPI originates interrupt requests only when the SPI is enabled (the SPE bit in the SPIx_C1 register is set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

Four flag bits, three interrupt mask bits, and one interrupt vector are associated with the SPI system. The SPI interrupt enable mask (SPIE) enables interrupts from the SPI receiver full flag (SPRF) and mode fault flag (MODF). The SPI transmit interrupt enable mask (SPTIE) enables interrupts from the SPI transmit buffer empty flag (SPTEF). The SPI match interrupt enable mask bit (SPIMIE) enables interrupts from the SPI match flag (SPMF). When one of the flag bits is set, and the associated interrupt mask bit is set, a hardware interrupt request is sent to the CPU. If the interrupt mask bits are cleared, software can poll the associated flag bits instead of using interrupts. The SPI interrupt

service routine (ISR) should check the flag bits to determine which event caused the interrupt. The service routine should also clear the flag bit(s) before returning from the ISR (usually near the beginning of the ISR).

17.4.12.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see the description of the C1[SSOE] bit). Once MODF is set, the current transfer is aborted and the master (MSTR) bit in the SPIx_C1 register resets to 0.

The MODF interrupt is reflected in the status register's MODF flag. Clearing the flag also clears the interrupt. This interrupt stays active while the MODF flag is set. MODF has an automatic clearing process that is described in the SPI Status Register.

17.4.12.2 SPRF

SPRF occurs when new data has been received and copied to the SPI receive data buffer. In 8-bit mode, SPRF is set only after all 8 bits have been shifted out of the shift register and into SPIx_DL. In 16-bit mode, SPRF is set only after all 16 bits have been shifted out of the shift register and into SPIx_DH:SPIx_DL.

After SPRF is set, it does not clear until it is serviced. SPRF has an automatic clearing process that is described in the SPI Status Register details. If the SPRF is not serviced before the end of the next transfer (that is, SPRF remains active throughout another transfer), the subsequent transfers are ignored and no new data is copied into the Data register.

17.4.12.3 SPTEF

SPTEF occurs when the SPI transmit buffer is ready to accept new data. In 8-bit mode, SPTEF is set only after all 8 bits have been moved from SPIx_DL into the shifter. In 16-bit mode, SPTEF is set only after all 16 bits have been moved from SPIx_DH:SPIx_DL into the shifter.

After SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process that is described in the SPI Status Register details.

17.4.12.4 SPMF

SPMF occurs when the data in the receive data buffer is equal to the data in the SPI Match Register. In 8-bit mode, SPMF is set only after bits 7–0 in the receive data buffer are determined to be equivalent to the value in SPIx_ML. In 16-bit mode, SPMF is set after bits 15–0 in the receive data buffer are determined to be equivalent to the value in SPIx_MH:SPIx_ML.

17.4.12.5 TNEAREF

The TNEAREF bit applies when the FIFO feature is supported.

The TNEAREF flag is set when only one 16-bit word or two 8-bit bytes of data remain in the transmit FIFO provided C3[5] = 0 or when only two 16-bit words or four 8-bit bytes of data remain in the transmit FIFO provided C3[5] =1. If FIFOMODE is not enabled, ignore this bit.

Clearing this interrupt depends on the state of C3[3] and the status of TNEAREF. Refer to the description of the SPI status (S) register.

17.4.12.6 RNFULLF

The RNFULLF bit applies when the FIFO feature is supported.

RNFULLF is set when more than three 16-bit words or six 8-bit bytes of data remain in the receive FIFO provided C3[4] = 0 or when more than two 16-bit words or four 8-bit bytes of data remain in the receive FIFO provided C3[4] = 1.

Clearing this interrupt depends on the state of C3[3] and the status of RNFULLF. Refer to the description of the SPI status (S) register.

17.5 Initialization/application information

This section discusses an example of how to initialize and use the SPI.

17.5.1 Initialization sequence

Before the SPI module can be used for communication, an initialization procedure must be carried out, as follows:

1. Update the Control Register 1 (SPIx_C1) to enable the SPI and to control interrupt enables. This register also sets the SPI as master or slave, determines clock phase and polarity, and configures the main SPI options.
2. Update the Control Register 2 (SPIx_C2) to enable additional SPI functions such as the SPI match interrupt feature, the master mode-fault function, and bidirectional mode output as well as to control 8- or 16-bit mode selection and other optional features.
3. Update the Baud Rate Register (SPIx_BR) to set the prescaler and bit rate divisor for an SPI master.
4. Update the Hardware Match Register (SPIx_MH:SPIx_ML) with the value to be compared to the receive data register for triggering an interrupt if hardware match interrupts are enabled.
5. In the master, read SPIx_S while S[SPTEF] = 1, and then write to the transmit data register (SPIx_DH:SPIx_DL) to begin transfer.

17.5.2 Pseudo-Code Example

In this example, the SPI module is set up for master mode with only hardware match interrupts enabled. The SPI runs in 16-bit mode at a maximum baud rate of bus clock divided by 2. Clock phase and polarity are set for an active-high SPI clock where the first edge on SPSCK occurs at the start of the first cycle of a data transfer.

SPIx_C1=0x54(%01010100)				
Bit 7	SPIE	=	0	Disables receive and mode fault interrupts
Bit 6	SPE	=	1	Enables the SPI system
Bit 5	SPTIE	=	0	Disables SPI transmit interrupts
Bit 4	MSTR	=	1	Sets the SPI module as a master SPI device
Bit 3	CPOL	=	0	Configures SPI clock as active-high
Bit 2	CPHA	=	1	First edge on SPSCK at start of first data transfer cycle
Bit 1	SSOE	=	0	Determines SS pin function when mode fault enabled
Bit 0	LSBFE	=	0	SPI serial data transfers start with most significant bit

SPIx_C2 = 0xC0(%11000000)				
Bit 7	SPMIE	=	1	SPI hardware match interrupt enabled
Bit 6	SPIMODE	=	1	Configures SPI for 16-bit mode
Bit 5		=	0	Reserved
Bit 4	MODFEN	=	0	Disables mode fault function

Table continues on the next page...

SPIx_C2 = 0xC0(%11000000)				
Bit 3	BIDIROE	=	0	SPI data I/O pin acts as input
Bit 2		=	0	Reserved
Bit 1	SPISWAI	=	0	SPI clocks operate in wait mode
Bit 0	SPC0	=	0	uses separate pins for data input and output

SPIx_BR = 0x00(%00000000)			
Bit 7	=	0	Reserved
Bit 6:4	=	000	Sets prescale divisor to 1
Bit 3:0	=	0000	Sets baud rate divisor to 2

SPIx_S = 0x00(%00000000)				
Bit 7	SPRF	=	0	Flag is set when receive data buffer is full
Bit 6	SPMF	=	0	Flag is set when SPIx_MH/ML = receive data buffer
Bit 5	SPTEF	=	0	Flag is set when transmit data buffer is empty
Bit 4	MODF	=	0	Mode fault flag for master mode
Bit 3:0		=	0	FIFOMODE is not enabled

SPIx_MH = 0xXX
In 16-bit mode, this register holds bits 8–15 of the hardware match buffer. In 8-bit mode, writes to this register will be ignored.

SPIx_ML = 0xXX
Holds bits 0–7 of the hardware match buffer.

SPIx_DH = 0xxx
In 16-bit mode, this register holds bits 8–15 of the data to be transmitted by the transmit buffer and received by the receive buffer.

SPIx_DL = 0xxx
Holds bits 0–7 of the data to be transmitted by the transmit buffer and received by the receive buffer.

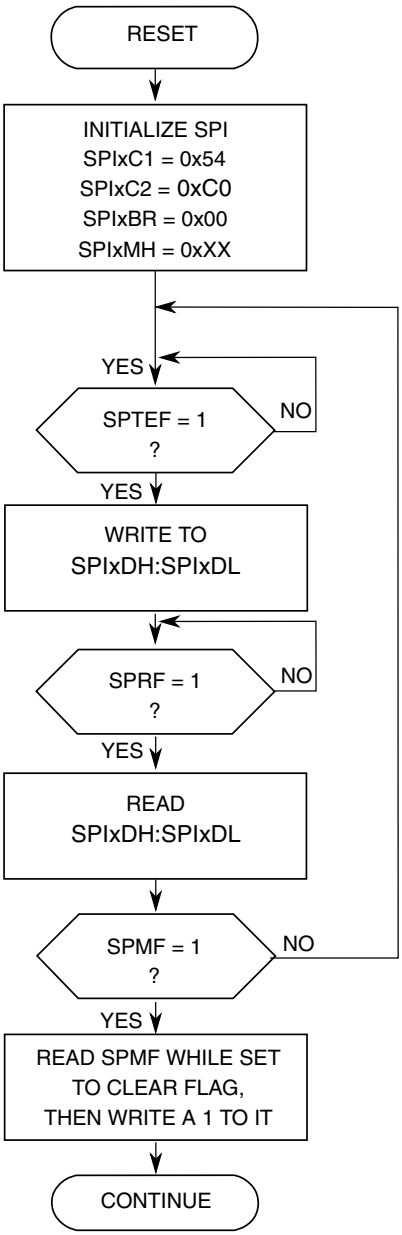


Figure 17-8. Initialization Flowchart Example for SPI Master Device in 16-bit Mode for FIFOMODE = 0

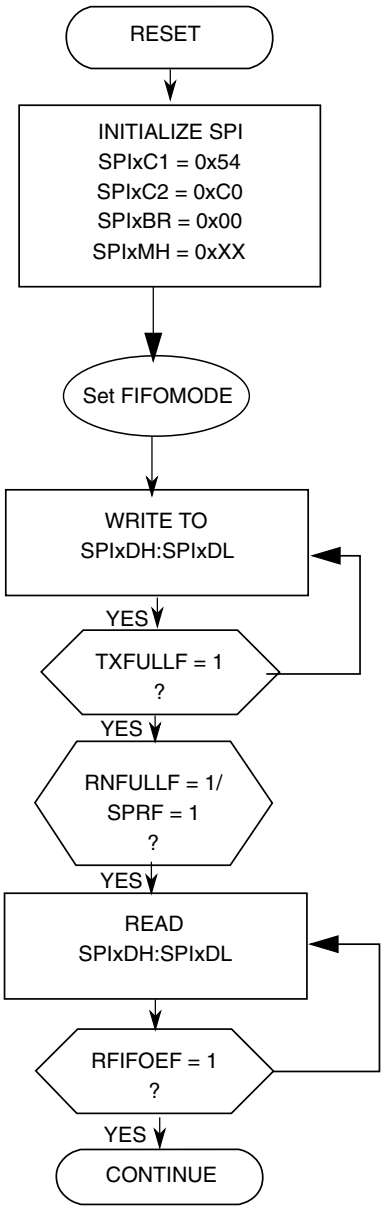


Figure 17-9. Initialization Flowchart Example for SPI Master Device in 16-bit Mode for FIFOMODE = 1

Chapter 18
Inter-Integrated Circuit (I2C)

18.1 Introduction

NOTE

For the chip-specific implementation details of this module's instances, see the chip configuration information.

The inter-integrated circuit (I^2C, I2C, or IIC) module provides a method of communication between a number of devices.

The interface is designed to operate up to at least 400 kbit/s with maximum bus loading and timing. The I2C device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF. The I2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

18.1.1 Features

The I2C module has the following features:

- Compatible with *The I^2C-Bus Specification*
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection

- Bus busy detection
- General call recognition
- 10-bit address extension
- Support for *System Management Bus (SMBus) Specification, version 2*
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support

18.1.2 Modes of operation

The I2C module's operation in various low power modes is as follows:

- Run mode: This is the basic mode of operation. To conserve power in this mode, disable the module.
- Wait mode: The module continues to operate when the core is in Wait mode and can provide a wakeup interrupt.
- Stop mode: The module is inactive in Stop3 mode for reduced power consumption, except that address matching is enabled in Stop3 mode. The STOP instruction does not affect the I2C module's register states.

18.1.3 Block diagram

The following figure is a functional block diagram of the I2C module.

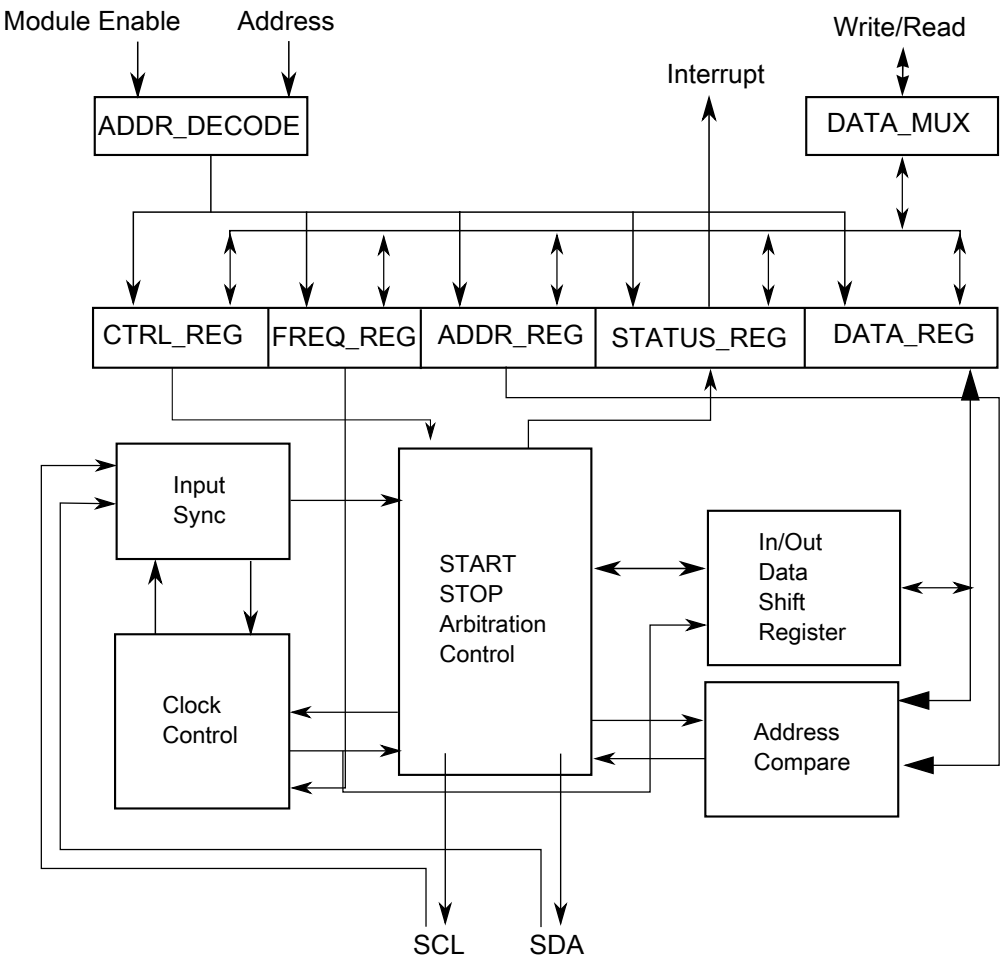


Figure 18-1. I2C Functional block diagram

18.2 I²C signal descriptions

The signal properties of I²C are shown in the table found here.

Table 18-1. I²C signal descriptions

Signal	Description	I/O
SCL	Bidirectional serial clock line of the I²C system.	I/O
SDA	Bidirectional serial data line of the I²C system.	I/O

18.3 Memory map/register definition

This section describes in detail all I2C registers accessible to the end user.

I2C memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3070	I2C Address Register 1 (I2C_A1)	8	R/W	00h	18.3.1/508
3071	I2C Frequency Divider register (I2C_F)	8	R/W	00h	18.3.2/509
3072	I2C Control Register 1 (I2C_C1)	8	R/W	00h	18.3.3/510
3073	I2C Status register (I2C_S)	8	R/W	80h	18.3.4/511
3074	I2C Data I/O register (I2C_D)	8	R/W	00h	18.3.5/513
3075	I2C Control Register 2 (I2C_C2)	8	R/W	00h	18.3.6/514
3076	I2C Programmable Input Glitch Filter Register (I2C_FLT)	8	R/W	00h	18.3.7/515
3077	I2C Range Address register (I2C_RA)	8	R/W	00h	18.3.8/515
3078	I2C SMBus Control and Status register (I2C_SMB)	8	R/W	00h	18.3.9/516
3079	I2C Address Register 2 (I2C_A2)	8	R/W	C2h	18.3.10/ 517
307A	I2C SCL Low Timeout Register High (I2C_SLTH)	8	R/W	00h	18.3.11/ 518
307B	I2C SCL Low Timeout Register Low (I2C_SLTL)	8	R/W	00h	18.3.12/ 518

18.3.1 I2C Address Register 1 (I2C_A1)

This register contains the slave address to be used by the I2C module.

Address: 3070h base + 0h offset = 3070h

Bit	7	6	5	4	3	2	1	0
Read	AD[7:1]							0
Write								
Reset	0	0	0	0	0	0	0	0

I2C_A1 field descriptions

Field	Description
7–1 AD[7:1]	Address Contains the primary slave address used by the I2C module when it is addressed as a slave. This field is used in the 7-bit address scheme and the lower seven bits in the 10-bit address scheme.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

18.3.2 I2C Frequency Divider register (I2C_F)

Address: 3070h base + 1h offset = 3071h

Bit	7	6	5	4	3	2	1	0
Read Write	MULT		ICR					
Reset	0	0	0	0	0	0	0	0

I2C_F field descriptions

Field	Description
7–6 MULT	Multiplier Factor Defines the multiplier factor (mul). This factor is used along with the SCL divider to generate the I2C baud rate. 00 mul = 1 01 mul = 2 10 mul = 4 11 Reserved

ICR	ClockRate
	
	Prescales the I2C module clock for bit rate selection. This field and the MULT field determine the I2C baud rate, the SDA hold time, the SCL start hold time, and the SCL stop hold time. For a list of values corresponding to each ICR setting, see I2C divider and hold values.
	
	The SCL divider multiplied by multiplier factor (mul) determines the I2C baud rate.
	
	`I2C baud rate = I2C module clock speed (Hz)/(mul × SCL divider)`
	
	The SDA hold time is the delay from the falling edge of SCL (I2C clock) to the changing of SDA (I2C data).
	
	`SDA hold time = I2C module clock period (s) × mul × SDA hold value`
	
	The SCL start hold time is the delay from the falling edge of SDA (I2C data) while SCL is high (start condition) to the falling edge of SCL (I2C clock).
	
	`SCL start hold time = I2C module clock period (s) × mul × SCL start hold value`
	
	The SCL stop hold time is the delay from the rising edge of SCL (I2C clock) to the rising edge of SDA (I2C data) while SCL is high (stop condition).
	
	`SCL stop hold time = I2C module clock period (s) × mul × SCL stop hold value`
	
	For example, if the I2C module clock speed is 8 MHz, the following table shows the possible hold time values with different ICR and MULT selections to achieve an I^2C baud rate of 100 kbit/s.

MULT	ICR	Hold times (µs)		
		SDA	SCL Start	SCL Stop
2h	00h	3.500	3.000	5.500
1h	07h	2.500	4.000	5.250
1h	0Bh	2.250	4.000	5.250
0h	14h	2.125	4.250	5.125

Table continues on the next page...

I2C_F field descriptions (continued)

Field	Description				
	MULT	ICR	Hold times (µs)		
			SDA	SCL Start	SCL Stop
	0h	18h	1.125	4.750	5.125

18.3.3 I2C Control Register 1 (I2C_C1)

Address: 3070h base + 2h offset = 3072h

Bit	7	6	5	4	3	2	1	0
Read	IICEN	IICIE	MST	TX	TXAK	0	WUEN	0
Write						RSTA		
Reset	0	0	0	0	0	0	0	0

I2C_C1 field descriptions

Field	Description
7 IICEN	I2C Enable Enables I2C module operation. 0 Disabled 1 Enabled
6 IICIE	I2C Interrupt Enable Enables I2C interrupt requests. 0 Disabled 1 Enabled
5 MST	Master Mode Select When MST is changed from 0 to 1, a START signal is generated on the bus and master mode is selected. When this bit changes from 1 to 0, a STOP signal is generated and the mode of operation changes from master to slave. 0 Slave mode 1 Master mode
4 TX	Transmit Mode Select Selects the direction of master and slave transfers. In master mode this bit must be set according to the type of transfer required. Therefore, for address cycles, this bit is always set. When addressed as a slave this bit must be set by software according to the SRW bit in the status register. 0 Receive 1 Transmit

Table continues on the next page...

I2C_C1 field descriptions (continued)

Field	Description
3 TXAK	Transmit Acknowledge Enable Specifies the value driven onto the SDA during data acknowledge cycles for both master and slave receivers. The value of SMB[FACK] affects NACK/ACK generation. **NOTE:** SCL is held low until TXAK is written. 0 An acknowledge signal is sent to the bus on the following receiving byte (if FACK is cleared) or the current receiving byte (if FACK is set). 1 No acknowledge signal is sent to the bus on the following receiving data byte (if FACK is cleared) or the current receiving data byte (if FACK is set).
2 RSTA	Repeat START Writing 1 to this bit generates a repeated START condition provided it is the current master. This bit will always be read as 0. Attempting a repeat at the wrong time results in loss of arbitration.
1 WUEN	Wakeup Enable The I2C module can wake the MCU from low power mode with no peripheral bus running when slave address matching occurs. 0 Normal operation. No interrupt generated when address matching in low power mode. 1 Enables the wakeup function in low power mode.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

18.3.4 I2C Status register (I2C_S)

Address: 3070h base + 3h offset = 3073h

Bit	7	6	5	4	3	2	1	0
Read	TCF	IAAS	BUSY	ARBL	RAM	SRW	IICIF	RXAK
Write				w1c			w1c	
Reset	1	0	0	0	0	0	0	0

I2C_S field descriptions

Field	Description
7 TCF	Transfer Complete Flag Acknowledges a byte transfer; TCF is set on the completion of a byte transfer. This bit is valid only during or immediately following a transfer to or from the I2C module. TCF is cleared by reading the I2C data register in receive mode or by writing to the I2C data register in transmit mode. 0 Transfer in progress 1 Transfer complete
6 IAAS	Addressed As A Slave This bit is set by one of the following conditions:

Table continues on the next page...

I2C_S field descriptions (continued)

Field	Description
	• The calling address matches the programmed primary slave address in the A1 register, or matches the range address in the RA register (which must be set to a nonzero value and under the condition I2C_C2[RMEN] = 1). • C2[GCAEN] is set and a general call is received. • SMB[SIICAEN] is set and the calling address matches the second programmed slave address. • ALERTEN is set and an SMBus alert response address is received • RMEN is set and an address is received that is within the range between the values of the A1 and RA registers. IAAS sets before the ACK bit. The CPU must check the SRW bit and set TX/RX accordingly. Writing the C1 register with any value clears this bit. 0 Not addressed 1 Addressed as a slave
5 BUSY	Bus Busy Indicates the status of the bus regardless of slave or master mode. This bit is set when a START signal is detected and cleared when a STOP signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	Arbitration Lost This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software, by writing 1 to it. 0 Standard bus operation. 1 Loss of arbitration.
3 RAM	Range Address Match This bit is set to 1 by any of the following conditions, if I2C_C2[RMEN] = 1: • Any nonzero calling address is received that matches the address in the RA register. • The calling address is within the range of values of the A1 and RA registers. Writing the C1 register with any value clears this bit to 0. 0 Not addressed 1 Addressed as a slave
2 SRW	Slave Read/Write When addressed as a slave, SRW indicates the value of the R/$\overline{W}$ command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	Interrupt Flag This bit sets when an interrupt is pending. This bit must be cleared by software by writing 1 to it, such as in the interrupt routine. One of the following events can set this bit: • One byte transfer, including ACK/NACK bit, completes if FACK is 0. An ACK or NACK is sent on the bus by writing 0 or 1 to TXAK after this bit is set in receive mode. • One byte transfer, excluding ACK/NACK bit, completes if FACK is 1.

Table continues on the next page...

I2C_S field descriptions (continued)

Field	Description
	• Match of slave address to calling address including primary slave address, range slave address, alert response address, second slave address, or general call address. • Arbitration lost • In SMBus mode, any timeouts except SCL and SDA high timeouts 0 No interrupt pending 1 Interrupt pending
0 RXAK	Receive Acknowledge 0 Acknowledge signal was received after the completion of one byte of data transmission on the bus 1 No acknowledge signal detected

18.3.5 I2C Data I/O register (I2C_D)

Address: 3070h base + 4h offset = 3074h

Bit	7	6	5	4	3	2	1	0
Read Write	DATA							
Reset	0	0	0	0	0	0	0	0

I2C_D field descriptions

Field	Description
DATA	Data In master transmit mode, when data is written to this register, a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates receiving of the next byte of data. **NOTE:** When making the transition out of master receive mode, switch the I2C mode before reading the Data register to prevent an inadvertent initiation of a master receive data transfer. In slave mode, the same functions are available after an address match occurs. The C1[TX] bit must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For example, if the I2C module is configured for master transmit but a master receive is desired, reading the Data register does not initiate the receive. Reading the Data register returns the last byte received while the I2C module is configured in master receive or slave receive mode. The Data register does not reflect every byte that is transmitted on the I2C bus, and neither can software verify that a byte has been written to the Data register correctly by reading it back. In master transmit mode, the first byte of data written to the Data register following assertion of MST (start bit) or assertion of RSTA (repeated start bit) is used for the address transfer and must consist of the calling address (in bits 7-1) concatenated with the required R/$\overline{W}$ bit (in position bit 0).

18.3.6 I2C Control Register 2 (I2C_C2)

Address: 3070h base + 5h offset = 3075h

Bit	7	6	5	4	3	2	1	0
Read	GCAEN	ADEXT	0	Reserved	RMEN	AD[10:8]		
Write								
Reset	0	0	0	0	0	0	0	0

I2C_C2 field descriptions

Field	Description
7 GCAEN	General Call Address Enable Enables general call address. 0 Disabled 1 Enabled
6 ADEXT	Address Extension Controls the number of bits used for the slave address. 0 7-bit address scheme 1 10-bit address scheme
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 Reserved	This field is reserved. **NOTE:** Do not write 1 to this bitfield (write only zeros) or indeterminate results will occur.
3 RMEN	Range Address Matching Enable This bit controls the slave address matching for addresses between the values of the A1 and RA registers. When this bit is set, a slave address matching occurs for any address greater than the value of the A1 register and less than or equal to the value of the RA register. 0 Range mode disabled. No address matching occurs for an address within the range of values of the A1 and RA registers. 1 Range mode enabled. Address matching occurs when a slave receives an address within the range of values of the A1 and RA registers.
AD[10:8]	Slave Address Contains the upper three bits of the slave address in the 10-bit address scheme. This field is valid only while the ADEXT bit is set.

18.3.7 I2C Programmable Input Glitch Filter Register (I2C_FLT)

Address: 3070h base + 6h offset = 3076h

Bit	7	6	5	4	3	2	1	0
Read	Reserved	0			FLT			
Write								
Reset	0	0	0	0	0	0	0	0

I2C_FLT field descriptions

Field	Description
7 Reserved	This field is reserved. Writing this bit has no effect.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
FLT	I2C Programmable Filter Factor Controls the width of the glitch, in terms of I2C module clock cycles, that the filter must absorb. For any glitch whose size is less than or equal to this width setting, the filter does not allow the glitch to pass. 00h No filter/bypass 01-1Fh Filter glitches up to width of *n* I2C module clock cycles, where *n*=1-31d

18.3.8 I2C Range Address register (I2C_RA)

Address: 3070h base + 7h offset = 3077h

Bit	7	6	5	4	3	2	1	0
Read	RAD							0
Write								
Reset	0	0	0	0	0	0	0	0

I2C_RA field descriptions

Field	Description
7–1 RAD	Range Slave Address This field contains the slave address to be used by the I2C module. The field is used in the 7-bit address scheme. If I2C_C2[RMEN] is set to 1, any nonzero value write enables this register. This register value can be considered as a maximum boundary in the range matching mode.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

18.3.9 I2C SMBus Control and Status register (I2C_SMB)

NOTE

When the SCL and SDA signals are held high for a length of time greater than the high timeout period, the SHTF1 flag sets. Before reaching this threshold, while the system is detecting how long these signals are being held high, a master assumes that the bus is free. However, the SHTF1 bit is set to 1 in the bus transmission process with the idle bus state.

NOTE

When the TCKSEL bit is set, there is no need to monitor the SHTF1 bit because the bus speed is too high to match the protocol of SMBus.

Address: 3070h base + 8h offset = 3078h

Bit	7	6	5	4	3	2	1	0
Read	FACK	ALERTEN	SIICAEN	TCKSEL	SLTF	SHTF1	SHTF2	SHTF2IE
Write					w1c		w1c	
Reset	0	0	0	0	0	0	0	0

I2C_SMB field descriptions

Field	Description
7 FACK	Fast NACK/ACK Enable For SMBus packet error checking, the CPU must be able to issue an ACK or NACK according to the result of receiving data byte. 0 An ACK or NACK is sent on the following receiving data byte 1 Writing 0 to TXAK after receiving a data byte generates an ACK. Writing 1 to TXAK after receiving a data byte generates a NACK.
6 ALERTEN	SMBus Alert Response Address Enable Enables or disables SMBus alert response address matching. **NOTE:** After the host responds to a device that used the alert response address, you must use software to put the device's address on the bus. The alert protocol is described in the SMBus specification. 0 SMBus alert response address matching is disabled 1 SMBus alert response address matching is enabled
5 SIICAEN	Second I2C Address Enable Enables or disables SMBus device default address. 0 I2C address register 2 matching is disabled 1 I2C address register 2 matching is enabled

Table continues on the next page...

I2C_SMB field descriptions (continued)

Field	Description
4 TCKSEL	Timeout Counter Clock Select Selects the clock source of the timeout counter. 0 Timeout counter counts at the frequency of the I2C module clock / 64 1 Timeout counter counts at the frequency of the I2C module clock
3 SLTF	SCL Low Timeout Flag This bit is set when the SLT register (consisting of the SLTH and SLTL registers) is loaded with a non-zero value (LoValue) and an SCL low timeout occurs. Software clears this bit by writing a logic 1 to it. **NOTE:** The low timeout function is disabled when the SLT register's value is 0. 0 No low timeout occurs 1 Low timeout occurs
2 SHTF1	SCL High Timeout Flag 1 This read-only bit sets when SCL and SDA are held high more than clock × LoValue / 512, which indicates the bus is free. This bit is cleared automatically. 0 No SCL high and SDA high timeout occurs 1 SCL high and SDA high timeout occurs
1 SHTF2	SCL High Timeout Flag 2 This bit sets when SCL is held high and SDA is held low more than clock × LoValue / 512. Software clears this bit by writing 1 to it. 0 No SCL high and SDA low timeout occurs 1 SCL high and SDA low timeout occurs
0 SHTF2IE	SHTF2 Interrupt Enable Enables SCL high and SDA low timeout interrupt. 0 SHTF2 interrupt is disabled 1 SHTF2 interrupt is enabled

18.3.10 I2C Address Register 2 (I2C_A2)

Address: 3070h base + 9h offset = 3079h

Bit	7	6	5	4	3	2	1	0
Read Write	SAD							0
Reset	1	1	0	0	0	0	1	0

I2C_A2 field descriptions

Field	Description
7–1 SAD	SMBus Address

Table continues on the next page...

I2C_A2 field descriptions (continued)

Field	Description
	Contains the slave address used by the SMBus. This field is used on the device default address or other related addresses.
0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

18.3.11 I2C SCL Low Timeout Register High (I2C_SLTH)

Address: 3070h base + Ah offset = 307Ah

Bit	7	6	5	4	3	2	1	0
Read Write	SSLT[15:8]							
Reset	0	0	0	0	0	0	0	0

I2C_SLTH field descriptions

Field	Description
SSLT[15:8]	SSLT[15:8] Most significant byte of SCL low timeout value that determines the timeout period of SCL low.

18.3.12 I2C SCL Low Timeout Register Low (I2C_SLTL)

Address: 3070h base + Bh offset = 307Bh

Bit	7	6	5	4	3	2	1	0
Read Write	SSLT[7:0]							
Reset	0	0	0	0	0	0	0	0

I2C_SLTL field descriptions

Field	Description
SSLT[7:0]	SSLT[7:0] Least significant byte of SCL low timeout value that determines the timeout period of SCL low.

18.4 Functional description

This section provides a comprehensive functional description of the I2C module.

18.4.1 I2C protocol

The I2C bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers.

All devices connected to it must have open drain or open collector outputs. A logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors depends on the system.

Normally, a standard instance of communication is composed of four parts:

1. START signal
2. Slave address transmission
3. Data transfer
4. STOP signal

The STOP signal should not be confused with the CPU STOP instruction. The following figure illustrates I2C bus system communication.

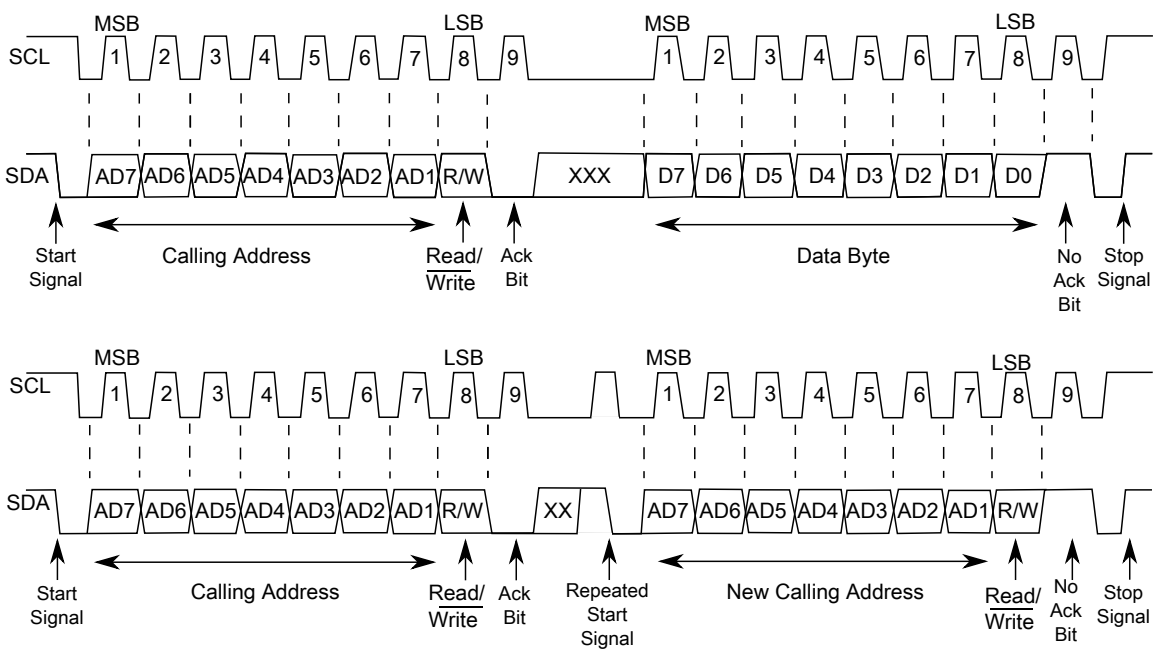


Figure 18-2. I2C bus transmission signals

18.4.1.1 START signal

The bus is free when no master device is engaging the bus (both SCL and SDA are high). When the bus is free, a master may initiate communication by sending a START signal. A START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer—each data transfer might contain several bytes of data—and brings all slaves out of their idle states.

18.4.1.2 Slave address transmission

Immediately after the START signal, the first byte of a data transfer is the slave address transmitted by the master. This address is a 7-bit calling address followed by an R/$\overline{W}$ bit. The R/$\overline{W}$ bit tells the slave the desired direction of data transfer.

- 1 = Read transfer: The slave transmits data to the master
- 0 = Write transfer: The master transmits data to the slave

Only the slave with a calling address that matches the one transmitted by the master responds by sending an acknowledge bit. The slave sends the acknowledge bit by pulling SDA low at the ninth clock.

No two slaves in the system can have the same address. If the I2C module is the master, it must not transmit an address that is equal to its own slave address. The I2C module cannot be master and slave at the same time. However, if arbitration is lost during an address cycle, the I2C module reverts to slave mode and operates correctly even if it is being addressed by another master.

18.4.1.3 Data transfers

When successful slave addressing is achieved, data transfer can proceed on a byte-by-byte basis in the direction specified by the R/$\overline{W}$ bit sent by the calling master.

All transfers that follow an address cycle are referred to as data transfers, even if they carry subaddress information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCL is low. Data must be held stable while SCL is high. There is one clock pulse on SCL for each data bit, and the MSB is transferred first. Each data byte is followed by a ninth (acknowledge) bit, which is signaled from the receiving device by pulling SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit, the slave must leave SDA high. The master interprets the failed acknowledgement as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets it as an end to data transfer and releases the SDA line.

In the case of a failed acknowledgement by either the slave or master, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a STOP signal.
- Commences a new call by generating a repeated START signal.

18.4.1.4 STOP signal

The master can terminate the communication by generating a STOP signal to free the bus. A STOP signal is defined as a low-to-high transition of SDA while SCL is asserted.

The master can generate a STOP signal even if the slave has generated an acknowledgement, at which point the slave must release the bus.

18.4.1.5 Repeated START signal

The master may generate a START signal followed by a calling command without generating a STOP signal first. This action is called a repeated START. The master uses a repeated START to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.

18.4.1.6 Arbitration procedure

The I2C bus is a true multimaster bus that allows more than one master to be connected on it.

If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock. The bus clock's low period is equal to the longest clock low period, and the high period is equal to the shortest one among the masters.

The relative priority of the contending masters is determined by a data arbitration procedure. A bus master loses arbitration if it transmits logic level 1 while another master transmits logic level 0. The losing masters immediately switch to slave receive mode and

stop driving SDA output. In this case, the transition from master to slave mode does not generate a STOP condition. Meanwhile, hardware sets a status bit to indicate the loss of arbitration.

18.4.1.7 Clock synchronization

Because wire AND logic is performed on SCL, a high-to-low transition on SCL affects all devices connected on the bus. The devices start counting their low period and, after a device's clock has gone low, that device holds SCL low until the clock reaches its high state. However, the change of low to high in this device clock might not change the state of SCL if another device clock is still within its low period. Therefore, the synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time; see the following diagram. When all applicable devices have counted off their low period, the synchronized clock SCL is released and pulled high. Afterward there is no difference between the device clocks and the state of SCL, and all devices start counting their high periods. The first device to complete its high period pulls SCL low again.

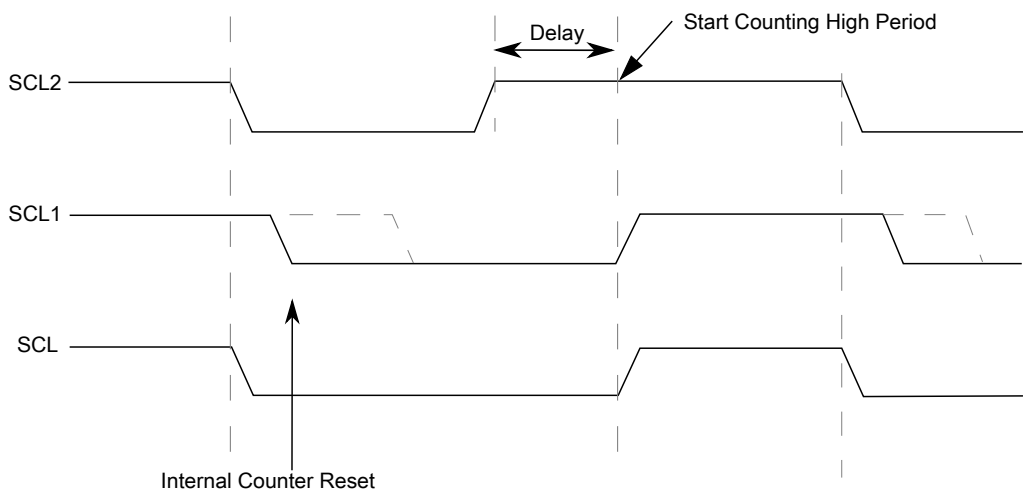


Figure 18-3. I2C clock synchronization

18.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfers. A slave device may hold SCL low after completing a single byte transfer (9 bits). In this case, it halts the bus clock and forces the master clock into wait states until the slave releases SCL.

18.4.1.9 Clock stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master drives SCL low, a slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal's low period is stretched. In other words, the SCL bus signal's low period is increased to be the same length as the slave's SCL low period.

18.4.1.10 I2C divider and hold values

NOTE

For some cases on some devices, the SCL divider value may vary by ±2 or ±4 when ICR's value ranges from 00h to 0Fh. These potentially varying SCL divider values are highlighted in the following table.

Table 18-2. I2C divider and hold values

ICR (hex)	SCL divider	SDA hold value	SCL hold (start) value	SCL hold (stop) value	ICR (hex)	SCL divider (clocks)	SDA hold (clocks)	SCL hold (start) value	SCL hold (stop) value
00	20	7	6	11	20	160	17	78	81
01	22	7	7	12	21	192	17	94	97
02	24	8	8	13	22	224	33	110	113
03	26	8	9	14	23	256	33	126	129
04	28	9	10	15	24	288	49	142	145
05	30	9	11	16	25	320	49	158	161
06	34	10	13	18	26	384	65	190	193
07	40	10	16	21	27	480	65	238	241
08	28	7	10	15	28	320	33	158	161
09	32	7	12	17	29	384	33	190	193
0A	36	9	14	19	2A	448	65	222	225
0B	40	9	16	21	2B	512	65	254	257
0C	44	11	18	23	2C	576	97	286	289
0D	48	11	20	25	2D	640	97	318	321
0E	56	13	24	29	2E	768	129	382	385
0F	68	13	30	35	2F	960	129	478	481
10	48	9	18	25	30	640	65	318	321
11	56	9	22	29	31	768	65	382	385
12	64	13	26	33	32	896	129	446	449
13	72	13	30	37	33	1024	129	510	513
14	80	17	34	41	34	1152	193	574	577

Table continues on the next page...

Table 18-2. I2C divider and hold values (continued)

ICR (hex)	SCL divider	SDA hold value	SCL hold (start) value	SCL hold (stop) value	ICR (hex)	SCL divider (clocks)	SDA hold (clocks)	SCL hold (start) value	SCL hold (stop) value
15	88	17	38	45	35	1280	193	638	641
16	104	21	46	53	36	1536	257	766	769
17	128	21	58	65	37	1920	257	958	961
18	80	9	38	41	38	1280	129	638	641
19	96	9	46	49	39	1536	129	766	769
1A	112	17	54	57	3A	1792	257	894	897
1B	128	17	62	65	3B	2048	257	1022	1025
1C	144	25	70	73	3C	2304	385	1150	1153
1D	160	25	78	81	3D	2560	385	1278	1281
1E	192	33	94	97	3E	3072	513	1534	1537
1F	240	33	118	121	3F	3840	513	1918	1921

18.4.2 10-bit address

For 10-bit addressing, 0x11110 is used for the first 5 bits of the first address byte. Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing.

18.4.2.1 Master-transmitter addresses a slave-receiver

The transfer direction is not changed. When a 10-bit address follows a START condition, each slave compares the first 7 bits of the first byte of the slave address (11110XX) with its own address and tests whether the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device finds a match and generates an acknowledge (A1). Each slave that finds a match compares the 8 bits of the second byte of the slave address with its own address, but only one slave finds a match and generates an acknowledge (A2). The matching slave remains addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.

Table 18-3. Master-transmitter addresses slave-receiver with a 10-bit address

S	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 0	A1	Slave address second byte AD[8:1]	A2	Data	A	...	Data	A/A	P

After the master-transmitter has sent the first byte of the 10-bit address, the slave-receiver sees an I2C interrupt. User software must ensure that for this interrupt, the contents of the Data register are ignored and not treated as valid data.

18.4.2.2 Master-receiver addresses a slave-transmitter

The transfer direction is changed after the second R/$\overline{W}$ bit. Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks whether the first seven bits of the first byte of the slave address following Sr are the same as they were after the START condition (S), and it tests whether the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.

After a repeated START condition (Sr), all other slave devices also compare the first seven bits of the first byte of the slave address with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them are addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match.

Table 18-4. Master-receiver addresses a slave-transmitter with a 10-bit address

S	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 0	A1	Slave address second byte AD[8:1]	A2	Sr	Slave address first 7 bits 11110 + AD10 + AD9	R/$\overline{W}$ 1	A3	Data	A	...	Data	A	P

After the master-receiver has sent the first byte of the 10-bit address, the slave-transmitter sees an I2C interrupt. User software must ensure that for this interrupt, the contents of the Data register are ignored and not treated as valid data.

18.4.3 Address matching

All received addresses can be requested in 7-bit or 10-bit address format.

- AD[7:1] in Address Register 1, which contains the I2C primary slave address, always participates in the address matching process. It provides a 7-bit address.
- If the ADEXT bit is set, AD[10:8] in Control Register 2 participates in the address matching process. It extends the I2C primary slave address to a 10-bit address.

Additional conditions that affect address matching include:

- If the GCAEN bit is set, general call participates the address matching process.
- If the ALERTEN bit is set, alert response participates the address matching process.
- If the SIICAEN bit is set, Address Register 2 participates in the address matching process.
- If the RMEN bit is set, when the Range Address register is programmed to a nonzero value, any address within the range of values of Address Register 1 (excluded) and the Range Address register (included) participates in the address matching process. The Range Address register must be programmed to a value greater than the value of Address Register 1.

When the I2C module responds to one of these addresses, it acts as a slave-receiver and the IAAS bit is set after the address cycle. Software must read the Data register after the first byte transfer to determine that the address is matched.

18.4.4 System management bus specification

SMBus provides a control bus for system and power management related tasks. A system can use SMBus to pass messages to and from devices instead of tripping individual control lines.

Removing the individual control lines reduces pin count. Accepting messages ensures future expandability. With the system management bus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

18.4.4.1 Timeouts

The $T_{TIMEOUT,MIN}$ parameter allows a master or slave to conclude that a defective device is holding the clock low indefinitely or a master is intentionally trying to drive devices off the bus. The slave device must release the bus (stop driving the bus and let SCL and SDA float high) when it detects any single clock held low longer than $T_{TIMEOUT,MIN}$. Devices that have detected this condition must reset their communication and be able to receive a new START condition within the timeframe of $T_{TIMEOUT,MAX}$.

SMBus defines a clock low timeout, $T_{TIMEOUT}$, of 35 ms, specifies $T_{LOW:SEXT}$ as the cumulative clock low extend time for a slave device, and specifies $T_{LOW:MEXT}$ as the cumulative clock low extend time for a master device.

18.4.4.1.1 SCL low timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than a timeout value condition. Devices that have detected the timeout condition must reset the communication. When the I2C module is an active master, if it detects that SMBCLK low has exceeded the value of $T_{TIMEOUT,MIN}$, it must generate a stop condition within or after the current data byte in the transfer process. When the I2C module is a slave, if it detects the $T_{TIMEOUT,MIN}$ condition, it resets its communication and is then able to receive a new START condition.

18.4.4.1.2 SCL high timeout

When the I2C module has determined that the SMBCLK and SMBDAT signals have been high for at least $T_{HIGH:MAX}$, it assumes that the bus is idle.

A HIGH timeout occurs after a START condition appears on the bus but before a STOP condition appears on the bus. Any master detecting this scenario can assume the bus is free when either of the following occurs:

- SHTF1 rises.
- The BUSY bit is high and SHTF1 is high.

When the SMBDAT signal is low and the SMBCLK signal is high for a period of time, another kind of timeout occurs. The time period must be defined in software. SHTF2 is used as the flag when the time limit is reached. This flag is also an interrupt resource, so it triggers IICIF.

18.4.4.1.3 CSMBCLK TIMEOUT MEXT and CSMBCLK TIMEOUT SEXT

The following figure illustrates the definition of the timeout intervals $T_{LOW:SEXT}$ and $T_{LOW:MEXT}$. When in master mode, the I2C module must not cumulatively extend its clock cycles for a period greater than $T_{LOW:MEXT}$ within a byte, where each byte is defined as START-to-ACK, ACK-to-ACK, or ACK-to-STOP. When CSMBCLK TIMEOUT MEXT occurs, SMBus MEXT rises and also triggers the SLTF.

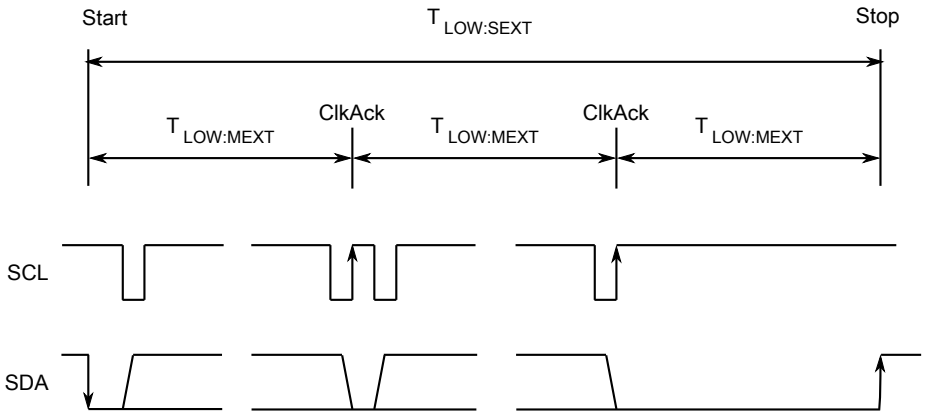


Figure 18-4. Timeout measurement intervals

A master is allowed to abort the transaction in progress to any slave that violates the $T_{LOW:SEXT}$ or $T_{TIMEOUT,MIN}$ specifications. To abort the transaction, the master issues a STOP condition at the conclusion of the byte transfer in progress. When a slave, the I2C module must not cumulatively extend its clock cycles for a period greater than $T_{LOW:SEXT}$ during any message from the initial START to the STOP. When CSMBCLK TIMEOUT SEXT occurs, SEXT rises and also triggers SLTF.

NOTE

CSMBCLK TIMEOUT SEXT and CSMBCLK TIMEOUT MEXT are optional functions that are implemented in the second step.

18.4.4.2 FAST ACK and NACK

To improve reliability and communication robustness, implementation of packet error checking (PEC) by SMBus devices is optional for SMBus devices but required for devices participating in and only during the address resolution protocol (ARP) process. The PEC is a CRC-8 error checking byte, calculated on all the message bytes. The PEC is appended to the message by the device that supplied the last data byte. If the PEC is present but not correct, a NACK is issued by the receiver. Otherwise an ACK is issued. To calculate the CRC-8 by software, this module can hold the SCL line low after receiving the eighth SCL (8th bit) if this byte is a data byte. So software can determine whether an ACK or NACK should be sent to the bus by setting or clearing the TXAK bit if the FACK (fast ACK/NACK enable) bit is enabled.

SMBus requires a device always to acknowledge its own address, as a mechanism to detect the presence of a removable device (such as a battery or docking station) on the bus. In addition to indicating a slave device busy condition, SMBus uses the NACK mechanism to indicate the reception of an invalid command or invalid data. Because such a condition may occur on the last byte of the transfer, SMBus devices are required to

have the ability to generate the not acknowledge after the transfer of each byte and before the completion of the transaction. This requirement is important because SMBus does not provide any other resend signaling. This difference in the use of the NACK signaling has implications on the specific implementation of the SMBus port, especially in devices that handle critical system data such as the SMBus host and the SBS components.

NOTE

In the last byte of master receive slave transmit mode, the master must send a NACK to the bus, so FACK must be switched off before the last byte transmits.

18.4.5 Resets

The I2C module is disabled after a reset. The I2C module cannot cause a core reset.

18.4.6 Interrupts

The I2C module generates an interrupt when any of the events in the table found here occur, provided that the IICIE bit is set.

The interrupt is driven by the IICIF bit (of the I2C Status Register) and masked with the IICIE bit (of the I2C Control Register 1). The IICIF bit must be cleared (by software) by writing 1 to it in the interrupt routine. The SMBus timeouts interrupt is driven by SLTF and masked with the IICIE bit. The SLTF bit must be cleared by software by writing 1 to it in the interrupt routine. You can determine the interrupt type by reading the Status Register.

NOTE

In master receive mode, the FACK bit must be set to zero before the last byte transfer.

Table 18-5. Interrupt summary

Interrupt source	Status	Flag	Local enable
Complete 1-byte transfer	TCF	IICIF	IICIE
Match of received calling address	IAAS	IICIF	IICIE
Arbitration lost	ARBL	IICIF	IICIE
SMBus SCL low timeout	SLTF	IICIF	IICIE
SMBus SCL high SDA low timeout	SHTF2	IICIF	IICIE & SHTF2IE
Wakeup from stop3 or wait mode	IAAS	IICIF	IICIE & WUEN

18.4.6.1 Byte transfer interrupt

The Transfer Complete Flag (TCF) bit is set at the falling edge of the ninth clock to indicate the completion of a byte and acknowledgement transfer. When FACK is enabled, TCF is then set at the falling edge of eighth clock to indicate the completion of byte.

18.4.6.2 Address detect interrupt

When the calling address matches the programmed slave address (I2C Address Register) or when the GCAEN bit is set and a general call is received, the IAAS bit in the Status Register is set. The CPU is interrupted, provided the IICIE bit is set. The CPU must check the SRW bit and set its Tx mode accordingly.

18.4.6.3 Exit from low-power/stop modes

The slave receive input detect circuit and address matching feature are still active on low power modes (wait and stop). An asynchronous input matching slave address or general call address brings the CPU out of low power/stop mode if the interrupt is not masked. Therefore, TCF and IAAS both can trigger this interrupt.

18.4.6.4 Arbitration lost interrupt

The I2C is a true multimaster bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, the relative priority of the contending masters is determined by a data arbitration procedure. The I2C module asserts the arbitration-lost interrupt when it loses the data arbitration process and the ARBL bit in the Status Register is set.

Arbitration is lost in the following circumstances:

1. SDA is sampled as low when the master drives high during an address or data transmit cycle.
2. SDA is sampled as low when the master drives high during the acknowledge bit of a data receive cycle.
3. A START cycle is attempted when the bus is busy.
4. A repeated START cycle is requested in slave mode.

5. A STOP condition is detected when the master did not request it.

The ARBL bit must be cleared (by software) by writing 1 to it.

18.4.6.5 Timeout interrupt in SMBus

When the IICIE bit is set, the I2C module asserts a timeout interrupt (outputs SLTF and SHTF2) upon detection of any of the mentioned timeout conditions, with one exception. The SCL high and SDA high TIMEOUT mechanism must not be used to influence the timeout interrupt output, because this timeout indicates an idle condition on the bus. SHTF1 rises when it matches the SCL high and SDA high TIMEOUT and falls automatically just to indicate the bus status. The SHTF2's timeout period is the same as that of SHTF1, which is short compared to that of SLTF, so another control bit, SHTF2IE, is added to enable or disable it.

18.4.7 Programmable input glitch filter

An I2C glitch filter has been added outside legacy I2C modules but within the I2C package. This filter can absorb glitches on the I2C clock and data lines for the I2C module.

The width of the glitch to absorb can be specified in terms of the number of (half) I2C module clock cycles. A single Programmable Input Glitch Filter control register is provided. Effectively, any down-up-down or up-down-up transition on the data line that occurs within the number of clock cycles programmed in this register is ignored by the I2C module. The programmer must specify the size of the glitch (in terms of I2C module clock cycles) for the filter to absorb and not pass.

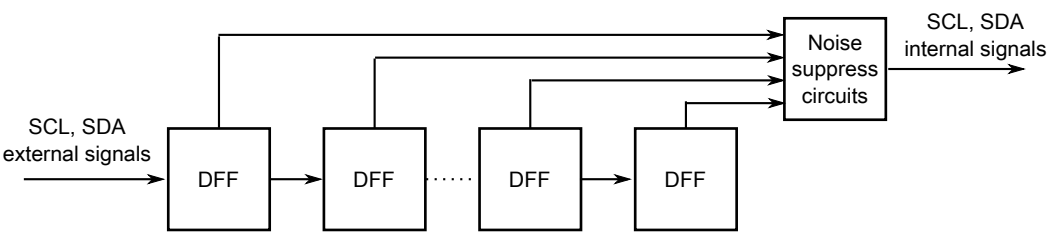


Figure 18-5. Programmable input glitch filter diagram

18.4.8 Address matching wake-up

When a primary, range, or general call address match occurs when the I2C module is in slave receive mode, the MCU wakes from a low power mode where no peripheral bus is running.

Data sent on the bus that is the same as a target device address might also wake the target MCU.

After the address matching IAAS bit is set, an interrupt is sent at the end of address matching to wake the core. The IAAS bit must be cleared after the clock recovery.

NOTE

After the system recovers and is in Run mode, restart the I2C module if it is needed to transfer packets. To avoid I2C transfer problems resulting from the situation, firmware should prevent the MCU execution of a STOP instruction when the I2C module is in the middle of a transfer.

18.5 Initialization/application information

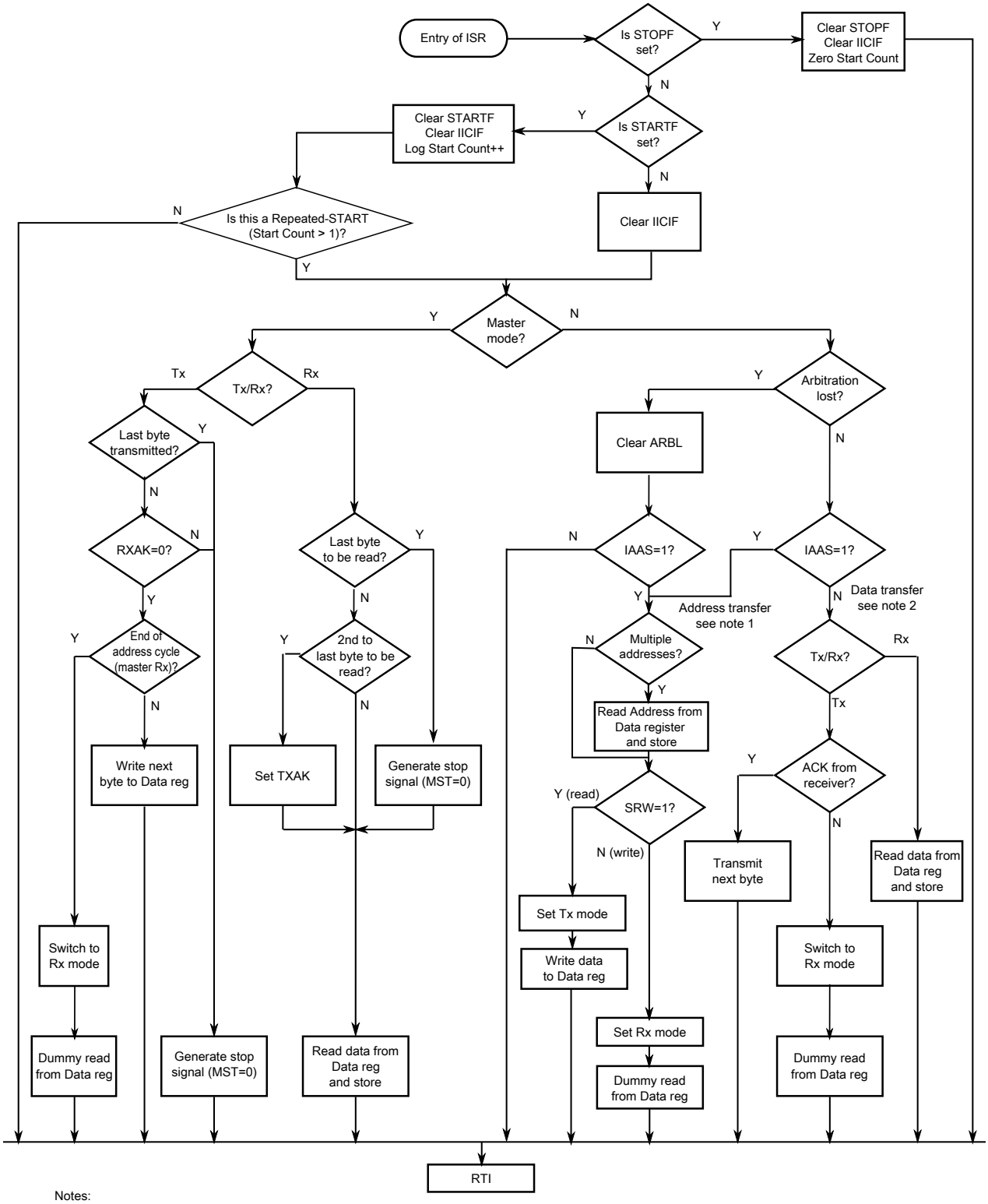
Module Initialization (Slave)

1. Write: Control Register 2
   - to enable or disable general call
   - to select 10-bit or 7-bit addressing mode
2. Write: Address Register 1 to set the slave address
3. Write: Control Register 1 to enable the I2C module and interrupts
4. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
5. Initialize RAM variables used to achieve the routine shown in the following figure

Module Initialization (Master)

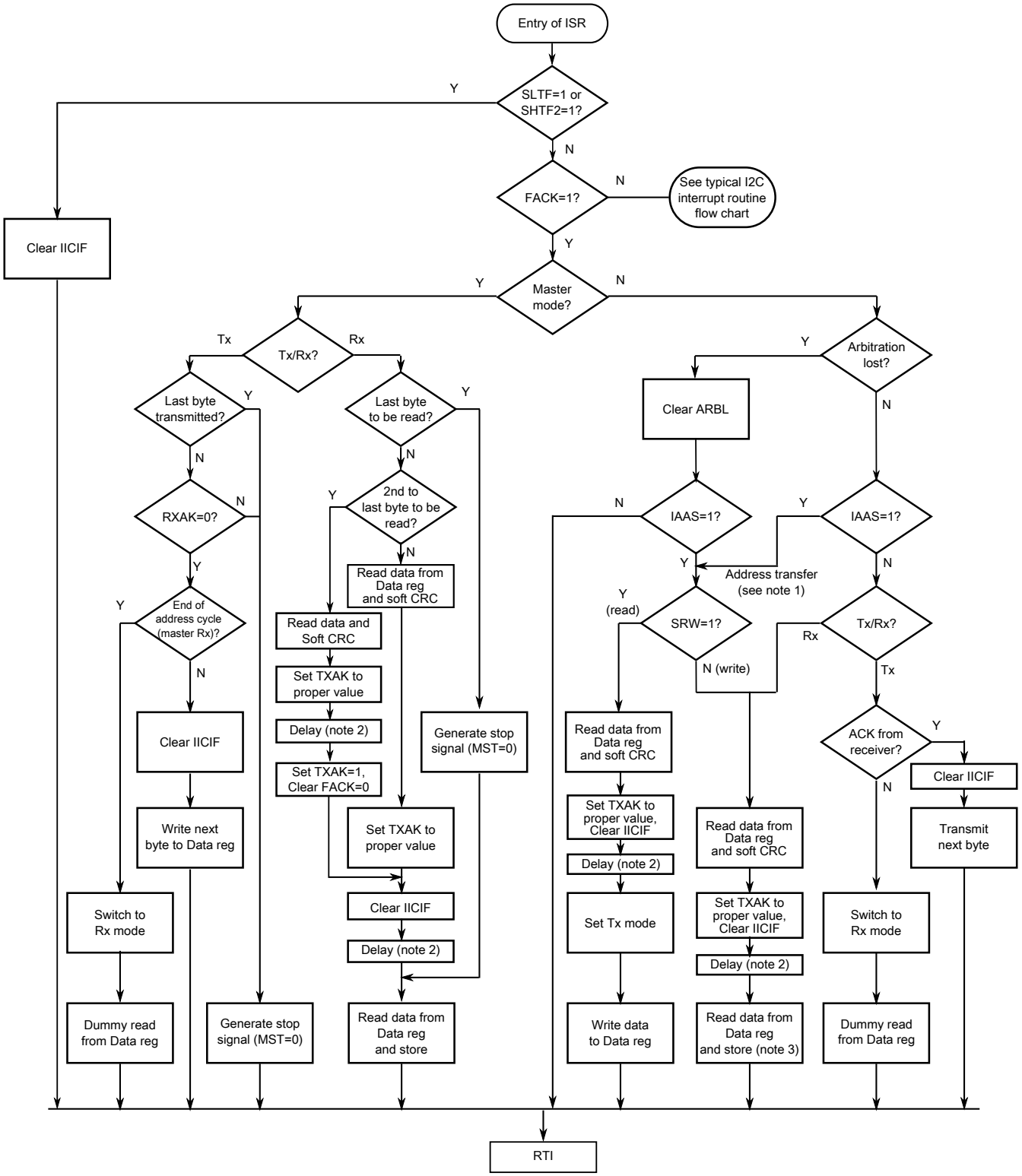
1. Write: Frequency Divider register to set the I2C baud rate (see example in description of ICR)
2. Write: Control Register 1 to enable the I2C module and interrupts
3. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
4. Initialize RAM variables used to achieve the routine shown in the following figure
5. Write: Control Register 1 to enable TX
6. Write: Control Register 1 to enable MST (master mode)
7. Write: Data register with the address of the target slave (the LSB of this byte determines whether the communication is master receive or transmit)

The routine shown in the following figure encompasses both master and slave I2C operations. For slave operation, an incoming I2C message that contains the proper address begins I2C communication. For master operation, communication must be initiated by writing the Data register. An example of an I2C driver which implements many of the steps described here is available in AN4342: Using the Inter-Integrated Circuit on ColdFire+ and Kinetis .



Notes:
1. If general call is enabled, check to determine if the received address is a general call address (0x00).
   If the received address is a general call address, the general call must be handled by user software.
2. When 10-bit addressing addresses a slave, the slave sees an interrupt following the first byte of the extended address.
   Ensure that for this interrupt, the contents of the Data register are ignored and not treated as a valid data transfer.

Figure 18-6. Typical I2C interrupt routine



Notes:
1. If general call or SIICAEN is enabled, check to determine if the received address is a general call address (0x00) or an SMBus device default address. In either case, they must be handled by user software.
2. In receive mode, one bit time delay may be needed before the first and second data reading, to wait for the possible longest time period (in worst case) of the 9th SCL cycle.
3. This read is a dummy read in order to reset the SMBus receiver state machine.

Figure 18-7. Typical I2C SMBus interrupt routine

Chapter 19
Analog-to-digital converter (ADC)

19.1 Introduction

The 12-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

19.1.1 Features

Features of the ADC module include:

- Linear Successive Approximation algorithm with 8-, 10-, or 12-bit resolution
- Up to 16 external analog inputs, external pin inputs, and 5 internal analog inputs including internal bandgap, temperature sensor, and references
- Output formatted in 8-, 10-, or 12-bit right-justified unsigned format
- Single or Continuous Conversion (automatic return to idle after single conversion)
- Support up to eight result FIFO with selectable FIFO depth
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in Wait or Stop3 modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value

19.1.2 Block Diagram

This figure provides a block diagram of the ADC module.

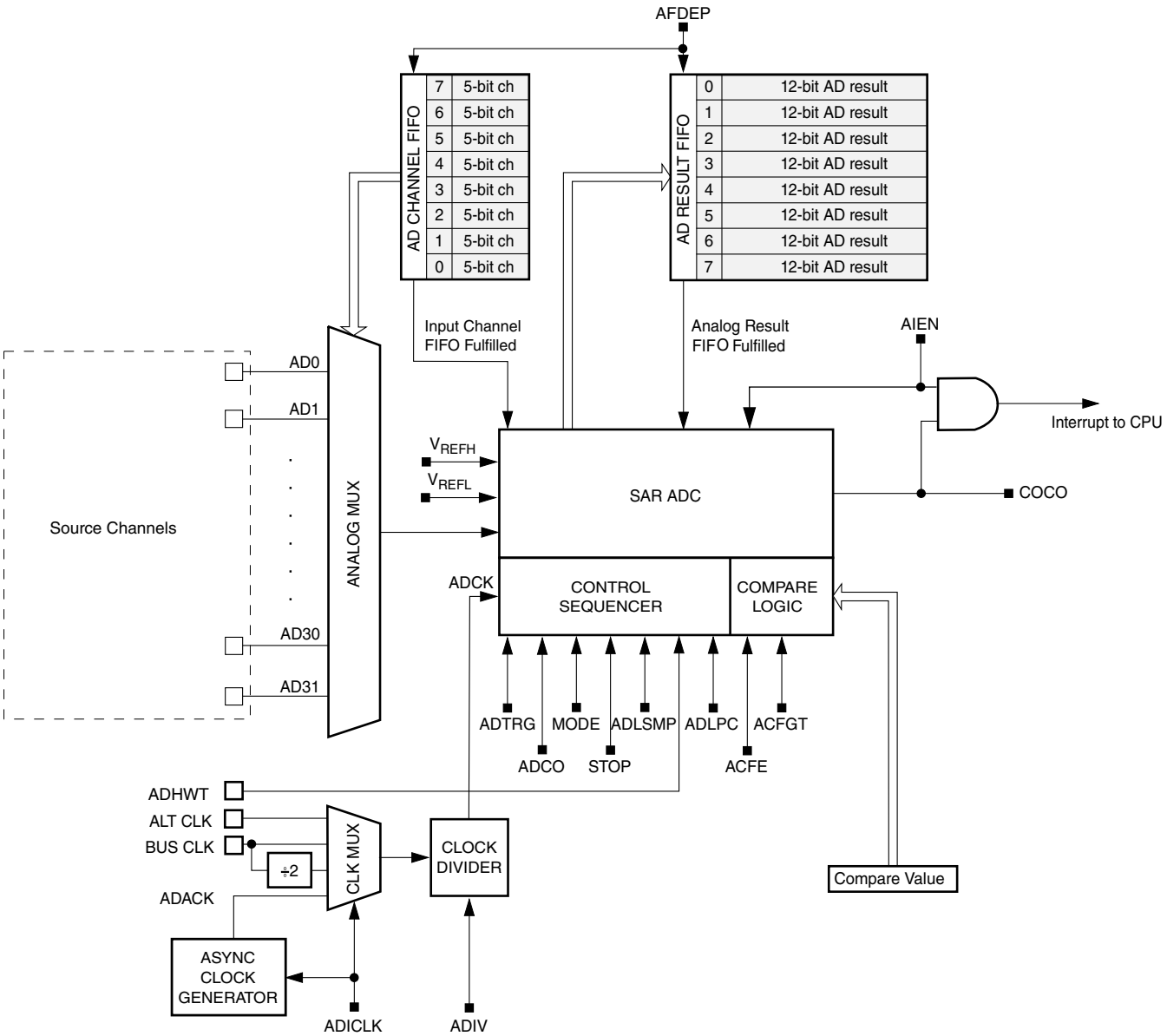


Figure 19-1. ADC Block Diagram

See chip specific sections for the channel assignments.

19.2 External Signal Description

The ADC module supports up to 16 separate analog inputs. It also requires four supply/ reference/ground connections.

Table 19-1. Signal Properties

Name	Function
AD15–AD0	Analog Channel inputs
V_{REFH}	High reference voltage
V_{REFL}	Low reference voltage
V_{DDA}	Analog power supply
V_{SSA}	Analog ground

19.2.1 Analog Power (V_{DDA})

The ADC analog portion uses V_{DDA} as its power connection. In some packages, V_{DDA} is connected internally to V_{DD}. If externally available, connect the V_{DDA} pin to the same voltage potential as V_{DD}. External filtering may be necessary to ensure clean V_{DDA} for good results.

19.2.2 Analog Ground (V_{SSA})

The ADC analog portion uses V_{SSA} as its ground connection. In some packages, V_{SSA} is connected internally to V_{SS}. If externally available, connect the V_{SSA} pin to the same voltage potential as V_{SS}.

19.2.3 Voltage Reference High (V_{REFH})

V_{REFH} is the high reference voltage for the converter. In some packages, V_{REFH} is connected internally to V_{DDA}. If externally available, V_{REFH} may be connected to the same potential as V_{DDA} or may be driven by an external source between the minimum V_{DDA} specified in the data sheet and the V_{DDA} potential (V_{REFH} must never exceed V_{DDA}).

19.2.4 Voltage Reference Low (V_{REFL})

V_{REFL} is the low-reference voltage for the converter. In some packages, V_{REFL} is connected internally to V_{SSA}. If externally available, connect the V_{REFL} pin to the same voltage potential as V_{SSA}.

19.2.5 Analog Channel Inputs (ADx)

The ADC module supports up to 24 separate analog inputs. An input is selected for conversion through the ADCH channel select bits.

19.3 ADC Control Registers

ADC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
10	Status and Control Register 1 (ADC_SC1)	8	R/W	1Fh	19.3.1/540
11	Status and Control Register 2 (ADC_SC2)	8	R/W	08h	19.3.2/542
12	Status and Control Register 3 (ADC_SC3)	8	R/W	00h	19.3.3/543
13	Status and Control Register 4 (ADC_SC4)	8	R/W	00h	19.3.4/544
14	Conversion Result High Register (ADC_RH)	8	R	00h	19.3.5/545
15	Conversion Result Low Register (ADC_RL)	8	R	00h	19.3.6/546
16	Compare Value High Register (ADC_CVH)	8	R/W	00h	19.3.7/547
17	Compare Value Low Register (ADC_CVL)	8	R/W	00h	19.3.8/547
30AC	Pin Control 1 Register (ADC_APCTL1)	8	R/W	00h	19.3.9/548
30AD	Pin Control 2 Register (ADC_APCTL2)	8	R/W	00h	19.3.10/ 549

19.3.1 Status and Control Register 1 (ADC_SC1)

This section describes the function of the ADC status and control register (ADC_SC1). Writing ADC_SC1 aborts the current conversion and initiates a new conversion (if the ADCH bits are equal to a value other than all 1s).

When FIFO is enabled, the analog input channel FIFO is written via ADCH. The analog input channel queue must be written to ADCH continuously. The resulting FIFO follows the order in which the analog input channel is written. The ADC will start conversion

when the input channel FIFO is fulfilled at the depth indicated by the ADC_SC4[AFDEP]. Any write 0x1F to these bits will reset the FIFO and stop the conversion if it is active.

Address: 10h base + 0h offset = 10h

Bit	7	6	5	4	3	2	1	0
Read	COCO	AIEN	ADCO	ADCH				
Write								
Reset	0	0	0	1	1	1	1	1

ADC_SC1 field descriptions

Field	Description
7 COCO	Conversion Complete Flag Conversion Complete Flag. The COCO flag is a read-only bit set each time a conversion is completed when the compare function is disabled (ADC_SC2[ACFE] = 0). When the compare function is enabled (ADC_SC2[ACFE] = 1), the COCO flag is set upon completion of a conversion only if the compare result is true. When the FIFO function is enabled (ADC_SC4[AFDEP] > 0), the COCO flag is set upon completion of the set of FIFO conversion. This bit is cleared when ADC_SC1 is written or when ADC_RL is read. 0 Conversion not completed. 1 Conversion completed.
6 AIEN	Interrupt Enable AIEN enables conversion complete interrupts. When COCO becomes set while AIEN is high, an interrupt is asserted. 0 Conversion complete interrupt disabled. 1 Conversion complete interrupt enabled.
5 ADCO	Continuous Conversion Enable ADCO enables continuous conversions. 0 One conversion following a write to the ADC_SC1 when software triggered operation is selected, or one conversion following assertion of ADHWT when hardware triggered operation is selected. When the FIFO function is enabled (AFDEP > 0), a set of conversions are triggered. 1 Continuous conversions are initiated following a write to ADC_SC1 when software triggered operation is selected. Continuous conversions are initiated by an ADHWT event when hardware triggered operation is selected. When the FIFO function is enabled (AFDEP > 0), a set of conversions are loop triggered.
ADCH	Input Channel Select The ADCH bits form a 5-bit field that selects one of the input channels. See chip specific section for the ADCH configurations.

19.3.2 Status and Control Register 2 (ADC_SC2)

The ADC_SC2 register controls the compare function, conversion trigger, and conversion active of the ADC module.

Address: 10h base + 1h offset = 11h

Bit	7	6	5	4	3	2	1	0
Read	ADACT	ADTRG	ACFE	ACFGT	FEMPTY	FFULL		
Write							0	
Reset	0	0	0	0	1	0	0	0

ADC_SC2 field descriptions

Field	Description
7 ADACT	Conversion Active Indicates that a conversion is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted. 0 Conversion not in progress. 1 Conversion in progress.
6 ADTRG	Conversion Trigger Select Selects the type of trigger used for initiating a conversion. Two types of trigger are selectable: software trigger and hardware trigger. When software trigger is selected, a conversion is initiated following a write to ADC_SC1. When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input. 0 Software trigger selected. 1 Hardware trigger selected.
5 ACFE	Compare Function Enable Enables the compare function. 0 Compare function disabled. 1 Compare function enabled.
4 ACFGT	Compare Function Greater Than Enable Configures the compare function to trigger when the result of the conversion of the input being monitored is greater than or equal to the compare value. The compare function defaults to triggering when the result of the compare of the input being monitored is less than the compare value. 0 Compare triggers when input is less than compare level. 1 Compare triggers when input is greater than or equal to compare level.
3 FEMPTY	Result FIFO empty 0 Indicates that ADC result FIFO have at least one valid new data. 1 Indicates that ADC result FIFO have no valid new data.
2 FFULL	Result FIFO full

Table continues on the next page...

ADC_SC2 field descriptions (continued)

Field	Description
	0 Indicates that ADC result FIFO is not full and next conversion data still can be stored into FIFO. 1 Indicates that ADC result FIFO is full and next conversion will override old data in case of no read action.
Reserved	This field is reserved.

19.3.3 Status and Control Register 3 (ADC_SC3)

ADC_SC3 selects the mode of operation, clock source, clock divide, and configure for low power or long sample time.

Address: 10h base + 2h offset = 12h

Bit	7	6	5	4	3	2	1	0
Read Write	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
Reset	0	0	0	0	0	0	0	0

ADC_SC3 field descriptions

Field	Description
7 ADLPC	Low-Power Configuration ADLPC controls the speed and power configuration of the successive approximation converter. This optimizes power consumption when higher sample rates are not required. 0 High speed configuration. 1 Low power configuration:The power is reduced at the expense of maximum clock speed.
6–5 ADIV	Clock Divide Select ADIV selects the divide ratio used by the ADC to generate the internal clock ADCK. 00 Divide ration = 1, and clock rate = Input clock. 01 Divide ration = 2, and clock rate = Input clock ÷ 2. 10 Divide ration = 3, and clock rate = Input clock ÷ 4. 11 Divide ration = 4, and clock rate = Input clock ÷ 8.
4 ADLSMP	Long Sample Time Configuration ADLSMP selects between long and short sample time. This adjusts the sample period to allow higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required. 0 Short sample time. 1 Long sample time.
3–2 MODE	Conversion Mode Selection MODE bits are used to select between 12-, 10-, or 8-bit operation. 00 8-bit conversion (N=8)

Table continues on the next page...

ADC_SC3 field descriptions (continued)

Field	Description
	01 10-bit conversion (N=10) 10 12-bit conversion (N=12) 11 Reserved
ADICLK	Input Clock Select ADICLK bits select the input clock source to generate the internal clock ADCK. 00 Bus clock 01 Bus clock divided by 2 10 Alternate clock (ALTCLK) 11 Asynchronous clock (ADACK)

19.3.4 Status and Control Register 4 (ADC_SC4)

This register controls the FIFO scan mode, FIFO compare function and FIFO depth selection of the ADC module.

Address: 10h base + 3h offset = 13h

Bit	7	6	5	4	3	2	1	0
Read	0	ASCANE	ACFSEL	0		AFDEP		
Write								
Reset	0	0	0	0	0	0	0	0

ADC_SC4 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 ASCANE	FIFO Scan Mode Enable The FIFO always use the first dummied FIFO channels when it is enabled. When this bit is set and FIFO function is enabled, ADC will repeat using the first FIFO channel as the conversion channel until the result FIFO is fulfilled. In continuous mode (ADCO = 1), ADC will start next conversion with the same channel when COCO is set. 0 FIFO scan mode disabled. 1 FIFO scan mode enabled.
5 ACFSEL	Compare function select OR/AND when the FIFO function is enabled (AFDEP > 0). When this field is cleared, ADC will OR all of compare triggers and set COCO after at least one of compare trigger occurs. When this field is set, ADC will AND all of compare triggers and set COCO after all of compare triggers occur. 0 OR all of compare trigger. 1 AND all of compare trigger.
4–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

ADC_SC4 field descriptions (continued)

Field	Description
AFDEP	FIFO Depth enables the FIFO function and sets the depth of FIFO. When AFDEP is cleared, the FIFO is disabled. When AFDEP is set to nonzero, the FIFO function is enabled and the depth is indicated by the AFDEP bits. The ADCH in ADC_SC1 and ADC_RH:ADC_RL must be accessed by FIFO mode when FIFO function is enabled. ADC starts conversion when the analog channel FIFO is upon the level indicated by AFDEP bits. The COCO bit is set when the set of conversions are completed and the result FIFO is upon the level indicated by AFDEP bits. **NOTE:** The bus clock frequency must be at least double the ADC clock when FIFO mode is enabled. It means, if ICS FBE mode is used, the ADC clock can not be ADACK. 000 FIFO is disabled. 001 2-level FIFO is enabled. 010 3-level FIFO is enabled.. 011 4-level FIFO is enabled. 100 5-level FIFO is enabled. 101 6-level FIFO is enabled. 110 7-level FIFO is enabled. 111 8-level FIFO is enabled.

19.3.5 Conversion Result High Register (ADC_RH)

In 12-bit operation, ADC_RH contains the upper four bits of the result of a 12-bit conversion.

ADC_RH is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. Reading ADC_RH prevents the ADC from transferring subsequent conversion results into the result registers until ADC_RL is read. If ADC_RL is not read until after the next conversion is completed, the intermediate conversion result is lost. In 8-bit mode, there is no interlocking with ADC_RL.

When FIFO is enabled, the result FIFO is read via ADC_RH:ADC_RL. The ADC conversion completes when the input channel FIFO is fulfilled at the depth indicated by the AFDEP. The AD result FIFO can be read via ADC_RH:ADC_RL continuously by the order set in analog input channel ADCH.

If the MODE bits are changed, any data in ADC_RH becomes invalid.

Address: 10h base + 4h offset = 14h

Bit	7	6	5	4	3	2	1	0
Read	0				ADR			
Write								
Reset	0	0	0	0	0	0	0	0

ADC_RH field descriptions

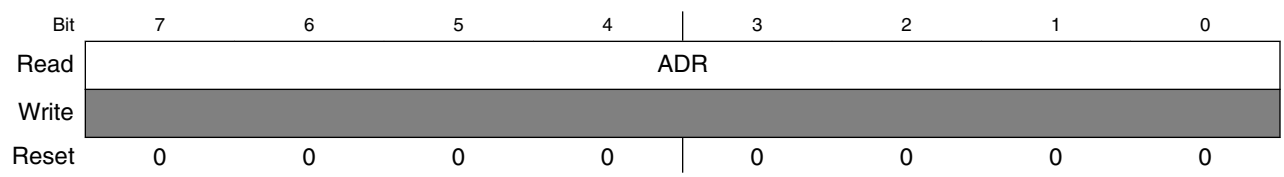
Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ADR	Conversion Result[11:8]

19.3.6 Conversion Result Low Register (ADC_RL)

ADC_RL contains the lower eight bits of the result of a 12-bit conversion. This register is updated each time a conversion completes except when automatic compare is enabled and the compare condition is not met. In 12-bit mode, reading ADC_RH prevents the ADC from transferring subsequent conversion results into the result registers until ADC_RL is read. If ADC_RL is not read until the next conversion is completed, the intermediate conversion results are lost. In 8-bit mode, there is no interlocking with ADC_RH. If the MODE bits are changed, any data in ADC_RL becomes invalid.

When FIFO is enabled, the result FIFO is read via ADC_RH:ADC_RL. The ADC conversion completes when the input channel FIFO is fulfilled at the depth indicated by the AFDEP. The AD result FIFO can be read via ADC_RH:ADC_RL continuously by the order set in analog input channel FIFO.

Address: 10h base + 5h offset = 15h



ADC_RL field descriptions

Field	Description
ADR	Conversion Result[7:0]

19.3.7 Compare Value High Register (ADC_CVH)

In 12-bit mode, this register holds the upper four bits of the 12-bit compare value. These bits are compared to the upper four bits of the result following a conversion in 12-bit mode when the compare function is enabled.

Address: 10h base + 6h offset = 16h

Bit	7	6	5	4	3	2	1	0
Read	0				CV			
Write								
Reset	0	0	0	0	0	0	0	0

ADC_CVH field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CV	Conversion Result[11:8]

19.3.8 Compare Value Low Register (ADC_CVL)

This register holds the lower 8 bits of the 12-bit compare value. Bits CV7:CV0 are compared to the lower 8 bits of the result following a conversion in 12-bit mode.

Address: 10h base + 7h offset = 17h

Bit	7	6	5	4	3	2	1	0
Read Write	CV							
Reset	0	0	0	0	0	0	0	0

ADC_CVL field descriptions

Field	Description
CV	Conversion Result[7:0]

19.3.9 Pin Control 1 Register (ADC_APCTL1)

The pin control registers disable the I/O port control of MCU pins used as analog inputs. APCTL1 is used to control the pins associated with channels 0-7 of the ADC module.

Address: 10h base + 309Ch offset = 30ACh

Bit	7	6	5	4	3	2	1	0
Read Write	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0
Reset	0	0	0	0	0	0	0	0

ADC_APCTL1 field descriptions

Field	Description
7 ADPC7	ADC Pin Control 7 ADPC7 controls the pin associated with channel AD7. 0 AD7 pin I/O control enabled. 1 AD7 pin I/O control disabled.
6 ADPC6	ADC Pin Control 6 ADPC6 controls the pin associated with channel AD6. 0 AD6 pin I/O control enabled. 1 AD6 pin I/O control disabled.
5 ADPC5	ADC Pin Control 5 ADPC5 controls the pin associated with channel AD5. 0 AD5 pin I/O control enabled. 1 AD5 pin I/O control disabled.
4 ADPC4	ADC Pin Control 4 ADPC4 controls the pin associated with channel AD4. 0 AD4 pin I/O control enabled. 1 AD4 pin I/O control disabled.
3 ADPC3	ADC Pin Control 3 ADPC3 controls the pin associated with channel AD3. 0 AD3 pin I/O control enabled. 1 AD3 pin I/O control disabled.
2 ADPC2	ADC Pin Control 2 ADPC2 controls the pin associated with channel AD2. 0 AD2 pin I/O control enabled. 1 AD2 pin I/O control disabled.

Table continues on the next page...

ADC_APCTL1 field descriptions (continued)

Field	Description
1 ADPC1	ADC Pin Control 1 ADPC1 controls the pin associated with channel AD1. 0 AD1 pin I/O control enabled. 1 AD1 pin I/O control disabled.
0 ADPC0	ADC Pin Control 0 ADPC0 controls the pin associated with channel AD0. 0 AD0 pin I/O control enabled. 1 AD0 pin I/O control disabled.

19.3.10 Pin Control 2 Register (ADC_APCTL2)

APCTL2 controls channels 8-15 of the ADC module.

Address: 10h base + 309Dh offset = 30ADh

Bit	7	6	5	4	3	2	1	0
Read Write	ADPC15	ADPC14	ADPC13	ADPC12	ADPC11	ADPC10	ADPC9	ADPC8
Reset	0	0	0	0	0	0	0	0

ADC_APCTL2 field descriptions

Field	Description
7 ADPC15	ADC Pin Control 15 ADPC15 controls the pin associated with channel AD15. 0 AD15 pin I/O control enabled. 1 AD15 pin I/O control disabled.
6 ADPC14	ADC Pin Control 14 ADPC14 controls the pin associated with channel AD14. 0 AD14 pin I/O control enabled. 1 AD14 pin I/O control disabled.
5 ADPC13	ADC Pin Control 13 ADPC13 controls the pin associated with channel AD13. 0 AD13 pin I/O control enabled. 1 AD13 pin I/O control disabled.
4 ADPC12	ADC Pin Control 12 ADPC12 controls the pin associated with channel AD12.

Table continues on the next page...

ADC_APCTL2 field descriptions (continued)

Field	Description
	0 AD12 pin I/O control enabled. 1 AD12 pin I/O control disabled.
3 ADPC11	ADC Pin Control 11 ADPC11 controls the pin associated with channel AD11. 0 AD11 pin I/O control enabled. 1 AD11 pin I/O control disabled.
2 ADPC10	ADC Pin Control 10 ADPC10 controls the pin associated with channel AD10. 0 AD10 pin I/O control enabled. 1 AD10 pin I/O control disabled.
1 ADPC9	ADC Pin Control 9 ADPC9 controls the pin associated with channel AD1. 0 AD9 pin I/O control enabled. 1 AD9 pin I/O control disabled.
0 ADPC8	ADC Pin Control 8 ADPC8 controls the pin associated with channel AD8. 0 AD8 pin I/O control enabled. 1 AD8 pin I/O control disabled.

19.4 Functional description

The ADC module is disabled during reset or when the ADC_SC1[ADCH] bits are all high. The module is idle when a conversion has completed and another conversion has not been initiated. When idle, the module is in its lowest power state.

The ADC can perform an analog-to-digital conversion on any of the software selectable channels. In 12-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 12-bit digital result. In 10-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 10-bit digital result. In 8-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 8-bit digital result.

When the conversion is completed, the result is placed in the data registers (ADC_RH and ADC_RL). In 10-bit mode, the result is rounded to 10 bits and placed in the data registers (ADC_RH and ADC_RL). In 8-bit mode, the result is rounded to 8 bits and

placed in ADC_RL. The conversion complete flag (ADC_SC1[COCO]) is then set and an interrupt is generated if the conversion complete interrupt has been enabled (ADC_SC1[AIEN] = 1).

The ADC module has the capability of automatically comparing the result of a conversion with the contents of its compare registers. The compare function is enabled by setting the ADC_SC2[ACFE] bit and operates with any of the conversion modes and configurations.

19.4.1 Clock select and divide control

One of four clock sources can be selected as the clock source for the ADC module. This clock source is then divided by a configurable value to generate the input clock to the converter (ADCK). The clock is selected from one of the following sources by means of the ADC_SC3[ADICLK] bits.

- The bus clock, which is equal to the frequency at which software is executed. This is the default selection following reset.
- The bus clock divided by 2: For higher bus clock rates, this allows a maximum divide by 16 of the bus clock.
- ALTCLK, that is, alternate clock which is OSCOUT
- The asynchronous clock (ADACK): This clock is generated from a clock source within the ADC module. When selected as the clock source, this clock remains active while the MCU is in Wait or Stop3 mode and allows conversions in these modes for lower noise operation.

Whichever clock is selected, its frequency must fall within the specified frequency range for ADCK. If the available clocks are too slow, the ADC does not perform according to specifications. If the available clocks are too fast, the clock must be divided to the appropriate frequency. This divider is specified by the ADC_SC3[ADIV] bits and can be divide-by 1, 2, 4, or 8.

19.4.2 Input select and pin control

The Pin Control registers (ADC_APCTL2 and ADC_APCTL1) disables the I/O port control of the pins used as analog inputs. When a pin control register bit is set, the following conditions are forced for the associated MCU pin:

- The output buffer is forced to its high impedance state.

- The input buffer is disabled. A read of the I/O port returns a zero for any pin with its input buffer disabled.
- The pullup is disabled.

19.4.3 Hardware trigger

The ADC module has a selectable asynchronous hardware conversion trigger, ADHWT, that is enabled when the ADC_SC2[ADTRG] bit is set. This source is not available on all MCUs. See the module introduction for information on the ADHWT source specific to this MCU.

When ADHWT source is available and hardware trigger is enabled (ADC_SC2[ADTRG] = 1), a conversion is initiated on the rising edge of ADHWT. If a conversion is in progress when a rising edge occurs, the rising edge is ignored. In continuous convert configuration, only the initial rising edge to launch continuous conversions is observed. The hardware trigger function operates in conjunction with any of the conversion modes and configurations.

19.4.4 Conversion control

Conversions can be performed in 12-bit mode, 10-bit mode, or 8-bit mode as determined by the ADC_SC3[MODE] bits. Conversions can be initiated by a software or hardware trigger. In addition, the ADC module can be configured for low power operation, long sample time, continuous conversion, and an automatic compare of the conversion result to a software determined compare value.

19.4.4.1 Initiating conversions

A conversion initiates under the following conditions:

- A write to ADC_SC1 or a set of write to ADC_SC1 in FIFO mode (with ADCH bits not all 1s) if software triggered operation is selected.
- A hardware trigger (ADHWT) event if hardware triggered operation is selected.
- The transfer of the result to the data registers when continuous conversion is enabled.

If continuous conversions are enabled, a new conversion is automatically initiated after the completion of the current conversion. In software triggered operation, continuous conversions begin after ADC_SC1 is written and continue until aborted. In hardware triggered operation, continuous conversions begin after a hardware trigger event and continue until aborted.

19.4.4.2 Completing conversions

A conversion is completed when the result of the conversion is transferred into the data result registers, ADC_RH and ADC_RL. This is indicated by the setting of ADC_SC1[COCO]. An interrupt is generated if ADC_SC1[AIEN] is high at the time that ADC_SC1[COCO] is set.

A blocking mechanism prevents a new result from overwriting previous data in ADC_RH and ADC_RL if the previous data is in the process of being read while in 12-bit or 10-bit MODE (the ADC_RH register has been read but the ADC_RL register has not). When blocking is active, the data transfer is blocked, ADC_SC1[COCO] is not set, and the new result is lost. In the case of single conversions with the compare function enabled and the compare condition false, blocking has no effect and ADC operation is terminated. In all other cases of operation, when a data transfer is blocked, another conversion is initiated regardless of the state of ADC_SC1[ADCO] whether single or continuous conversions are enabled.

If single conversions are enabled, the blocking mechanism could result in several discarded conversions and excess power consumption. To avoid this issue, the data registers must not be read after initiating a single conversion until the conversion completes.

In fifo mode, a blocking mechanism will keep current channel conversion and no channel fifo and result fifo switching until a block mechanism is released.

19.4.4.3 Aborting conversions

Any conversion in progress is aborted in the following cases:

- A write to ADC_SC1 occurs.
  - The current conversion will be aborted and a new conversion will be initiated, if ADC_SC1[ADCH] are not all 1s and ADC_SC4[AFDEP] are all 0s.
  - The current conversion and the rest of conversions will be aborted and no new conversion will be initialed, if ADC_SC4[AFDEP] are not all 0s.
  - A new conversion will be initiated when the FIFO is re-fulfilled upon the levels indicated by the ADC_SC4[AFDEP] bits).

- A write to ADC_SC2, ADC_SC3, ADC_SC4, ADC_CVH, or ADC_CVL occurs. This indicates a mode of operation change has occurred and the current and rest of conversions (when ADC_SC4[AFDEP] are not all 0s) are therefore invalid.
- The MCU is reset.
- The MCU enters Stop mode with ADACK not enabled.

When a conversion is aborted, the contents of the data registers, ADC_RH and ADC_RL, are not altered. However, they continue to be the values transferred after the completion of the last successful conversion. If the conversion was aborted by a reset, ADC_RH and ADC_RL return to their reset states.

19.4.4.4 Power control

The ADC module remains in its idle state until a conversion is initiated. If ADACK is selected as the conversion clock source, the ADACK clock generator is also enabled.

Power consumption when active can be reduced by setting ADC_SC3[ADLPC]. This results in a lower maximum value for f_{ADCK} (see the data sheet).

19.4.4.5 Sample time and total conversion time

The total conversion time depends on the sample time (as determined by ADC_SC3[ADLSMP]), the MCU bus frequency, the conversion mode (8-bit, 10-bit or 12-bit), and the frequency of the conversion clock (f_{ADCK}). After the module becomes active, sampling of the input begins.ADC_SC3[ADLSMP] selects between short (3.5 ADCK cycles) and long (23.5 ADCK cycles) sample times. When sampling is complete, the converter is isolated from the input channel and a successive approximation algorithm is performed to determine the digital value of the analog signal. The result of the conversion is transferred to ADC_RH and ADC_RL upon completion of the conversion algorithm.

If the bus frequency is less than the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when short sample is enabled (ADC_SC3[ADLSMP] = 0). If the bus frequency is less than 1/11th of the f_{ADCK} frequency, precise sample time for continuous conversions cannot be guaranteed when long sample is enabled (ADC_SC3[ADLSMP] = 1).

The maximum total conversion time for different conditions is summarized in the table below.

Table 19-2. Total conversion time vs. control conditions

Conversion type	ADICLK	ADLSMP	Max total conversion time
Single or first continuous 8-bit	0x, 10	0	20 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	0x, 10	0	23 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	0x, 10	1	40 ADCK cycles + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	0x, 10	1	43 ADCK cycles + 5 bus clock cycles
Single or first continuous 8-bit	11	0	5 µs + 20 ADCK + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	11	0	5 µs + 23 ADCK + 5 bus clock cycles
Single or first continuous 8-bit	11	1	5 µs + 40 ADCK + 5 bus clock cycles
Single or first continuous 10-bit or 12-bit	11	1	5 µs + 43 ADCK + 5 bus clock cycles
Subsequent continuous 8-bit; $f_{BUS} > f_{ADCK}$	xx	0	17 ADCK cycles
Subsequent continuous 10-bit or 12-bit; $f_{BUS} > f_{ADCK}$	xx	0	20 ADCK cycles
Subsequent continuous 8-bit; $f_{BUS} > f_{ADCK}/11$	xx	1	37 ADCK cycles
Subsequent continuous 10-bit or 12-bit; $f_{BUS} > f_{ADCK}/11$	xx	1	40 ADCK cycles

The maximum total conversion time is determined by the selected clock source and the divide ratio. The clock source is selectable by the ADC_SC3[ADICLK] bits, and the divide ratio is specified by the ADC_SC3[ADIV] bits. For example, in 10-bit mode, with the bus clock selected as the input clock source, the input clock divide-by-1 ratio selected, and a bus frequency of 8 MHz, then the conversion time for a single conversion as given below:

$$\text{Conversion time} = \frac{23\,\text{ADCK Cyc}}{8\,\text{MHz}/1} + \frac{5\,\text{bus Cyc}}{8\,\text{MHz}} = 3.5\,\mu\text{s}$$

The number of bus cycles at 8 MHz is:

$$\text{Bus cycles} = 3.5\mu\text{s} \times 8\text{MHz} = 28$$

Note

The ADCK frequency must be between f_{ADCK} minimum and f_{ADCK} maximum to meet ADC specifications.

19.4.5 Automatic compare function

The compare function can be configured to check for an upper or lower limit. After the input is sampled and converted, the result is added to the two's complement of the compare value (ADC_CVH and ADC_CVL). When comparing to an upper limit (ADC_SC2[ACFGT] = 1), if the result is greater-than or equal-to the compare value, ADC_SC1[COCO] is set. When comparing to a lower limit (ADC_SC2[ACFGT] = 0), if the result is less than the compare value, ADC_SC1[COCO] is set. The value generated by the addition of the conversion result and the two's complement of the compare value is transferred to ADC_RH and ADC_RL.

On completion of a conversion while the compare function is enabled, if the compare condition is not true, ADC_SC1[COCO] is not set and no data is transferred to the result registers. An ADC interrupt is generated on the setting of ADC_SC1[COCO] if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1).

On completion of all conversions while the compare function is enabled and FIFO enabled, if none of the compare conditions are true when ADC_SC4[ACFSEL] is low or if not all of compare conditions are true when ADC_SC4[ACFSEL] is high, ADC_SC1[COCO] is not set. The compare data are transferred to the result registers regardless of compare condition true or false when FIFO enabled.

Note

The compare function can monitor the voltage on a channel while the MCU is in Wait or Stop3 mode. The ADC interrupt wakes the MCU when the compare condition is met.

Note

The compare function can not work in continuous conversion mode when FIFO enabled.

19.4.6 FIFO operation

The ADC module supports FIFO operation to minimize the interrupts to CPU in order to reduce CPU loading in ADC interrupt service routines. This module contains two FIFOs to buffer analog input channels and analog results respectively.

The FIFO function is enabled when the ADC_SC4[AFDEP] bits are set non-zero. The FIFO depth is indicated by these bits. The FIFO supports up to eight level buffer.

The analog input channel FIFO is accessed by ADC_SC1[ADCH] bits, when FIFO function is enabled. The analog channel must be written to this FIFO in order. The ADC will not start the conversion if the channel FIFO is fulfilled below the level indicated by

the ADC_SC4[AFDEP] bits, no matter whether software or hardware trigger is set. Read ADC_SC1[ADCH] will read the current active channel value. Write to ADC_SC1[ADCH] will re-fill channel FIFO to initial new conversion. It will abort current conversion and any other conversions that did not start. Write to the ADC_SC1 after all the conversions are completed or ADC is in idle state.

The result of the FIFO is accessed by ADC_RH:ADC_RL registers, when FIFO function is enabled. The result must be read via these two registers by the same order of analog input channel FIFO to get the proper results. Don't read ADC_RH:ADC_RL until all of the conversions are completed in FIFO mode. The ADC_SC1[COCO] bit will be set only when all conversions indicated by the analog input channel FIFO complete whatever software or hardware trigger is set. An interrupt request will be submitted to CPU if the ADC_SC1[AIEN] is set when the FIFO conversion completes and the ADC_SC1[COCO] bit is set.

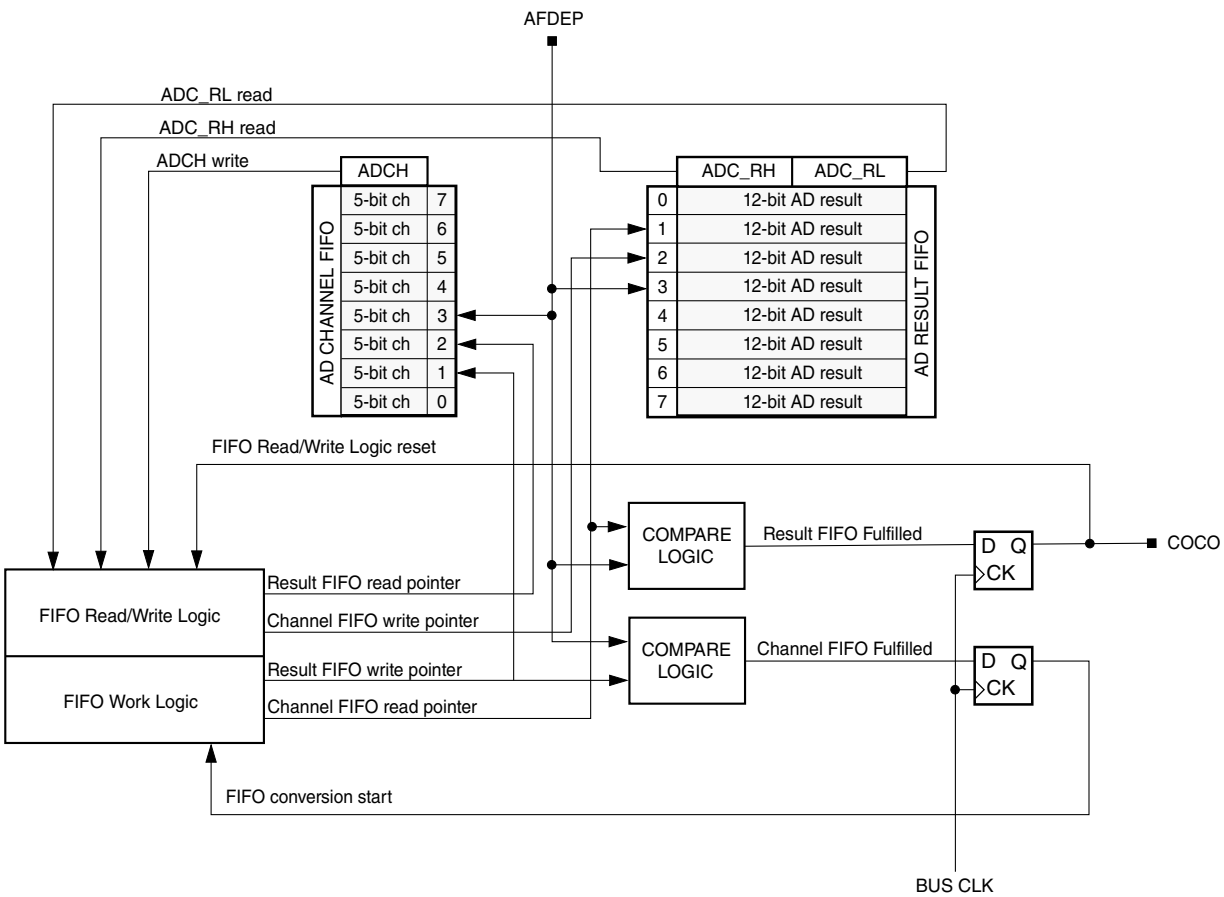


Figure 19-2. FADC FIFO structure

If software trigger is enabled, the next analog channel is fetched from analog input channel FIFO as soon as a conversion completes and its result is stored in the result FIFO. When all conversions set in the analog input channel FIFO completes, the ADC_SC1[COCO] bit is set and an interrupt request will be submitted to CPU if the ADC_SC1[AIEN] bit is set.

If hardware trigger mode is enabled, the next analog is fetched from analog input channel FIFO only when this conversion completes, its result is stored in the result FIFO, and the next hardware trigger is fed to ADC module. When all conversions set in the analog input channel FIFO completes, the ADC_SC1[COCO] bit is set and an interrupt request will be submitted to CPU if the ADC_SC1[AIEN] bit is set.

In single conversion in which ADC_SC1[ADCO] bit is clear, the ADC stops conversions when ADC_SC1[COCO] bit is set until the channel FIFO is fulfilled again or new hardware trigger occur.

The FIFO also provides scan mode to simplify the dummy work of input channel FIFO. When the ADC_SC4[ASCANE] bit is set in FIFO mode, the FIFO will always use the first dummied channel in spite of the value in the input channel FIFO. The ADC conversion start to work in FIFO mode as soon as the first channel is dummied. The following write operation to the input channel FIFO will cover the first channel element in this FIFO. In scan FIFO mode, the ADC_SC1[COCO] bit is set when the result FIFO is fulfilled according to the depth indicated by the ADC_SC4[AFDEP] bits.

In continuous conversion in which the ADC_SC1[ADCO] bit is set, the ADC starts next conversion immediately when all conversions are completed. ADC module will fetch the analog input channel from the beginning of analog input channel FIFO.

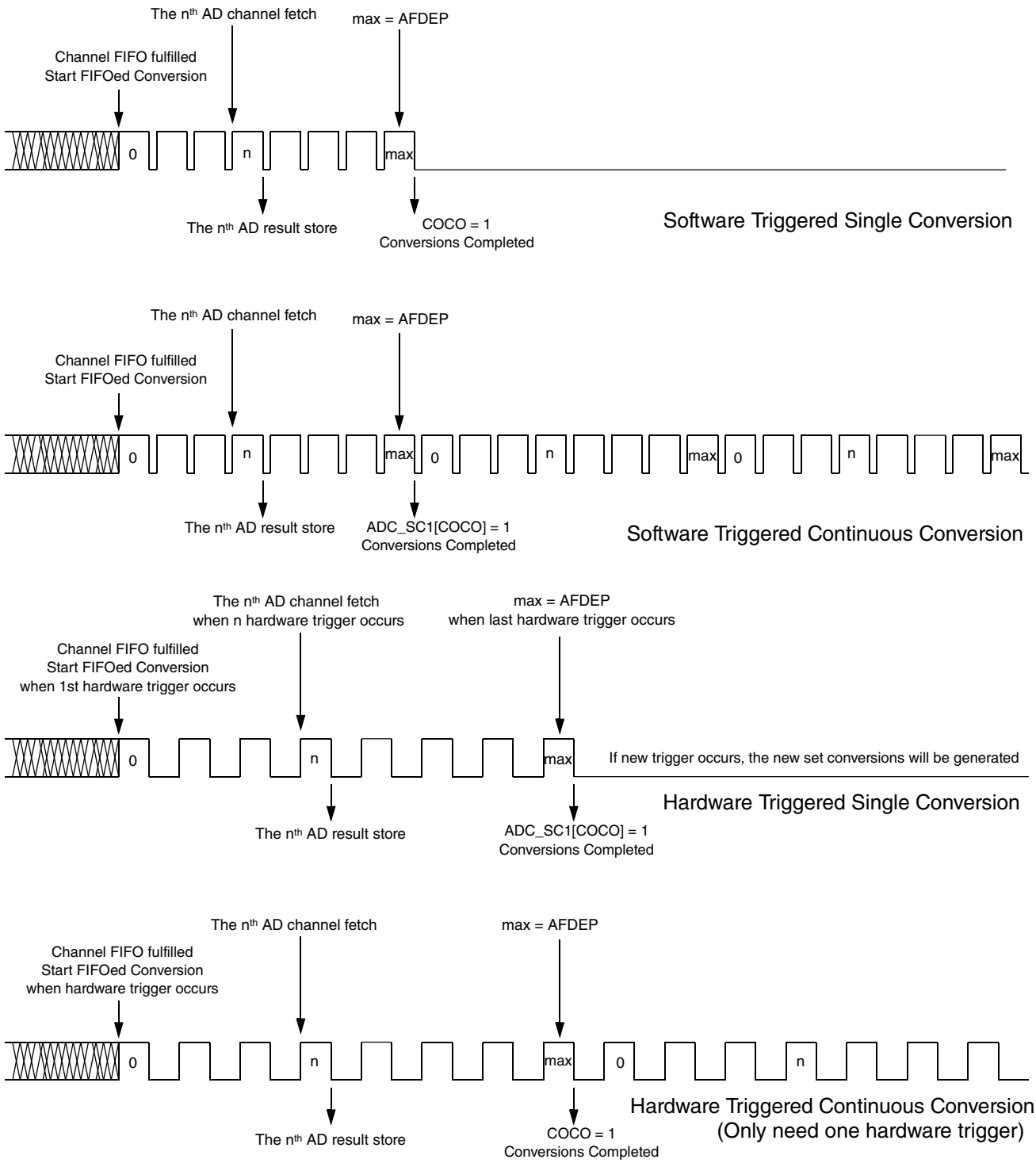


Figure 19-3. ADC FIFO conversion sequence

19.4.7 MCU wait mode operation

Wait mode is a low-power consumption standby mode from which recovery is fast because the clock sources remain active. If a conversion is in progress when the MCU enters wait mode, it continues until completion. Conversions can be initiated while the MCU is in wait mode by means of the hardware trigger or if continuous conversions are enabled.

The bus clock, bus clock divided by two, ALTCLK and ADACK are available as conversion clock sources while in wait mode.

ADC_SC1[COCO] is set by a conversion complete event that generates an ADC interrupt to wake the MCU from wait mode if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1).

19.4.8 MCU Stop3 mode operation

Stop3 mode is a low-power consumption standby mode during which most or all clock sources on the MCU are disabled.

19.4.8.1 Stop3 mode with ADACK disabled

If the asynchronous clock, ADACK, is not selected as the conversion clock, executing a STOP instruction aborts the current conversion and places the ADC in its idle state. The contents of ADC_RH and ADC_RL are unaffected by Stop3 mode. After exiting from Stop3 mode, a software or hardware trigger is required to resume conversions.

19.4.8.2 Stop3 mode with ADACK enabled

If ADACK is selected as the conversion clock, the ADC continues operation during Stop3 mode. For guaranteed ADC operation, the MCU's voltage regulator must remain active during Stop3 mode. See the module introduction for configuration information for this MCU.

If a conversion is in progress when the MCU enters Stop3 mode, it continues until completion. Conversions can be initiated while the MCU is in Stop3 mode by means of the hardware trigger or if continuous conversions are enabled.

A conversion complete event sets the ADC_SC1[COCO] and generates an ADC interrupt to wake the MCU from Stop3 mode if the ADC interrupt is enabled (ADC_SC1[AIEN] = 1). In fifo mode, ADC cannot complete the conversion operation fully or wake the MCU from Stop3 mode.

Note

The ADC module can wake the system from low-power stop and cause the MCU to begin consuming run-level currents without generating a system level interrupt. To prevent this scenario, the data transfer blocking mechanism must be cleared when entering Stop3 and continuing ADC conversions.

19.5 Initialization information

This section gives an example that provides some basic direction on how to initialize and configure the ADC module. You can configure the module for 8-, 10-, or 12-bit resolution, single or continuous conversion, and a polled or interrupt approach, among many other options. Refer to ADC_SC3 register for information used in this example.

Note

Hexadecimal values prefixed by a 0x, binary values prefixed by a %, and decimal values have no preceding character.

19.5.1 ADC module initialization example

Before the ADC module can be used to complete conversions, it must be initialized. Given below is a method to initialize ADC module.

19.5.1.1 Initialization sequence

A typical initialization sequence is as follows:

1. Update the configuration register (ADC_SC3) to select the input clock source and the divide ratio used to generate the internal clock, ADCK. This register is also used for selecting sample time and low-power configuration.
2. Update status and control register 2 (ADC_SC2) to select the hardware or software conversion trigger and compare function options, if enabled.

3. Update status and control register 1 (ADC_SC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

19.5.1.2 Pseudo-code example

In this example, the ADC module is set up with interrupts enabled to perform a single 10-bit conversion at low power with a long sample time on input channel 1, where the internal ADCK clock is derived from the bus clock divided by 1.

Example: 19.5.1.2.1 General ADC initialization routine

```
void ADC_init(void)
{
      /* The following code segment demonstrates how to initialize ADC by low-power mode,
long
      sample time, bus frequency, software triggered from AD1 external pin without FIFO
enabled
      */
 ADC_APCTL1 = ADC_APCTL1_ADPC1_MASK;
      ADC_SC3 = ADC_SC3_ADLPC_MASK | ADC_SC3_ADLSMP_MASK | ADC_SC3_MODE0_MASK;
      ADC_SC2 = 0x00;
      ADC_SC1 = ADC_SC1_AIEN_MASK | ADC_SC1_ADCH0_MASK;
}
```

19.5.2 ADC FIFO module initialization example

Before the ADC module can be used to start FIFOed conversions, an initialization procedure must be performed. A typical sequence is as follows:

1. Update the configuration register (ADC_SC3) to select the input clock source and the divide ratio used to generate the internal clock, ADCK. This register is also used to select sample time and low-power configuration.
2. Update the configuration register (ADC_SC4) to select the FIFO scan mode, FIFO compare function selection (OR or AND function) and FIFO depth.
3. Update status and control register 2 (ADC_SC2) to select the hardware or software conversion trigger, compare function options if enabled.
4. Update status and control register 1 (ADC_SC1) to select whether conversions will be continuous or completed only once, and to enable or disable conversion complete interrupts. The input channel on which conversions will be performed is also selected here.

19.5.2.1 Pseudo-code example

In this example, the ADC module is set up with interrupts enabled to perform a single hardware triggered 10-bit 4-level-FIFO conversion at low power with a long sample time on input channels of 1, 3, 5, and 7. Here the internal ADCK clock is derived from the bus clock divided by 1.

Example: 19.5.2.1.1 FIFO ADC initialization routine

```
void ADC_init(void)
{
/* The following code segment demonstrates how to initialize ADC by low-power mode, long
sample time, bus frequency, hardware triggered from AD1, AD3, AD5, and AD7 external pins
with 4-level FIFO enabled */

ADC_APCTL1 = ADC_APCTL1_ADPC6_MASK | ADC_APCTL1_ADPC5_MASK | ADC_APCTL1_ADPC3_MASK |
ADC_APCTL1_ADPC1_MASK; ADC_SC3 = ADC_SC3_ADLPC_MASK | ADC_SC3_ADLSMP_MASK |
ADC_SC3_MODE1_MASK;


// setting hardware trigger
ADC_SC2 = ADC_SC2_ADTRG_MASK ;

//4-Level FIFO
ADC_SC4 = ADC_SC4_AFDEP1_MASK | ADC_SC4_AFDEP0_MASK;

// dummy the 1st channel
ADC_SC1 = ADC_SC1_ADCH0_MASK;

// dummy the 2nd channel
ADC_SC1 = ADC_SC1_ADCH1_MASK | ADC_SC1_ADCH0_MASK;

// dummy the 3rd channel
ADC_SC1 = ADC_SC1_ADCH2_MASK | ADC_SC1_ADCH0_MASK;

// dummy the 4th channel and ADC starts conversion
ADC_SC1 = ADC_SC1_AIEN_MASK | ADC_SC1_ADCH2_MASK | ADC_SC1_ADCH1_MASK | ADC_SC1_ADCH0_MASK;

}
```

Example: 19.5.2.1.2 FIFO ADC interrupt service routine

```
unsigned short buffer[4];
interrupt VectorNumber_Vadc void ADC_isr(void)
{
      /* The following code segment demonstrates read AD result FIFO */
      // read conversion result of channel 1 and COCO bit is cleared
      buffer[0] = ADC_R;
      // read conversion result of channel 3
      buffer[1] = ADC_R;
      // read conversion result of channel 5
      buffer[2] = ADC_R;
      // read conversion result of channel 7
      buffer[3] = ADC_R;
}
```

NOTE

ADC_R is 16-bit ADC result register, combined from ADC_RH and ADC_RL

19.6 Application information

This section contains information for using the ADC module in applications. The ADC has been designed to be integrated into a microcontroller for use in embedded control applications requiring an A/D converter.

19.6.1 External pins and routing

The following sections discuss the external pins associated with the ADC module and how they are used for best results.

19.6.1.1 Analog supply pins

The ADC module has analog power and ground supplies (V_{DDA} and V_{SSA}) available as separate pins on some devices. V_{SSA} is shared on the same pin as the MCU digital V_{SS} on some devices. On other devices, V_{SSA} and V_{DDA} are shared with the MCU digital supply pins. In these cases, there are separate pads for the analog supplies bonded to the same pin as the corresponding digital supply so that some degree of isolation between the supplies is maintained.

When available on a separate pin, both V_{DDA} and V_{SSA} must be connected to the same voltage potential as their corresponding MCU digital supply (V_{DD} and V_{SS}) and must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

If separate power supplies are used for analog and digital power, the ground connection between these supplies must be at the V_{SSA} pin. This should be the only ground connection between these supplies if possible. The V_{SSA} pin makes a good single point ground location.

19.6.1.2 Analog reference pins

In addition to the analog supplies, the ADC module has connections for two reference voltage inputs. The high reference is V_{REFH}, which may be shared on the same pin as V_{DDA} on some devices. The low reference is V_{REFL}, which may be shared on the same pin as V_{SSA} on some devices.

When available on a separate pin, V_{REFH} may be connected to the same potential as V_{DDA}, or may be driven by an external source between the minimum V_{DDA} spec and the V_{DDA} potential (V_{REFH} must never exceed V_{DDA}). When available on a separate pin, V_{REFL} must be connected to the same voltage potential as V_{SSA}. V_{REFH} and V_{REFL} must be routed carefully for maximum noise immunity and bypass capacitors placed as near as possible to the package.

AC current in the form of current spikes required to supply charge to the capacitor array at each successive approximation step is drawn through the V_{REFH} and V_{REFL} loop. The best external component to meet this current demand is a 0.1 μF capacitor with good high frequency characteristics. This capacitor is connected between V_{REFH} and V_{REFL} and must be placed as near as possible to the package pins. Resistance in the path is not recommended because the current causes a voltage drop that could result in conversion errors. Inductance in this path must be minimum (parasitic only).

19.6.1.3 Analog input pins

The external analog inputs are typically shared with digital I/O pins on MCU devices. The pin I/O control is disabled by setting the appropriate control bit in one of the pin control registers. Conversions can be performed on inputs without the associated pin control register bit set. It is recommended that the pin control register bit always be set when using a pin as an analog input. This avoids problems with contention because the output buffer is in its high impedance state and the pullup is disabled. Also, the input buffer draws DC current when its input is not at V_{DD} or V_{SS}. Setting the pin control register bits for all pins used as analog inputs should be done to achieve lowest operating current.

Empirical data shows that capacitors on the analog inputs improve performance in the presence of noise or when the source impedance is high. Use of 0.01 μF capacitors with good high-frequency characteristics is sufficient. These capacitors are not necessary in all cases, but when used they must be placed as near as possible to the package pins and be referenced to V_{SSA}.

For proper conversion, the input voltage must fall between V_{REFH} and V_{REFL}. If the input is equal to or exceeds V_{REFH}, the converter circuit converts the signal to 0xFFF (full scale 12-bit representation), 0x3FF (full scale 10-bit representation) or 0xFF (full scale 8-bit

representation). If the input is equal to or less than V_{REFL}, the converter circuit converts it to 0x000. Input voltages between V_{REFH} and V_{REFL} are straight-line linear conversions. There is a brief current associated with V_{REFL} when the sampling capacitor is charging. The input is sampled for 3.5 cycles of the ADCK source when ADC_SC3[ADLSMP] is low, or 23.5 cycles when ADC_SC3[ADLSMP] is high.

For minimal loss of accuracy due to current injection, pins adjacent to the analog input pins should not be transitioning during conversions.

19.6.2 Sources of error

Several sources of error exist for A/D conversions. These are discussed in the following sections.

19.6.2.1 Sampling error

For proper conversions, the input must be sampled long enough to achieve the proper accuracy. Given the maximum input resistance of approximately 7 kΩ and input capacitance of approximately 5.5 pF, sampling to within 1/4 LSB (at 12-bit resolution) can be achieved within the minimum sample window (3.5 cycles at 8 MHz maximum ADCK frequency) provided the resistance of the external analog source (R_{AS}) is kept below 2 kΩ.

Higher source resistances or higher-accuracy sampling is possible by setting ADC_SC3[ADLSMP] (to increase the sample window to 23.5 cycles) or decreasing ADCK frequency to increase sample time.

19.6.2.2 Pin leakage error

Leakage on the I/O pins can cause conversion error if the external analog source resistance (R_{AS}) is high. If this error cannot be tolerated by the application, keep R_{AS} lower than $V_{DDA} / (2^N * I_{LEAK})$ for less than 1/4 LSB leakage error (N = 8 in 8-bit, 10 in 10-bit or 12 in 12-bit mode).

19.6.2.3 Noise-induced errors

System noise that occurs during the sample or conversion process can affect the accuracy of the conversion. The ADC accuracy numbers are guaranteed as specified only if the following conditions are met:

- There is a 0.1 µF low-ESR capacitor from V_{REFH} to V_{REFL}.
- There is a 0.1 µF low-ESR capacitor from V_{DDA} to V_{SSA}.
- If inductive isolation is used from the primary supply, an additional 1 µF capacitor is placed from V_{DDA} to V_{SSA}.
- V_{SSA} (and V_{REFL}, if connected) is connected to V_{SS} at a quiet point in the ground plane.
- Operate the MCU in wait or Stop3 mode before initiating (hardware triggered conversions) or immediately after initiating (hardware or software triggered conversions) the ADC conversion.
  - For software triggered conversions, immediately follow the write to ADC_SC1 with a wait instruction or stop instruction.
  - For Stop3 mode operation, select ADACK as the clock source. Operation in Stop3 reduces V_{DD} noise but increases effective conversion time due to stop recovery.
- There is no I/O switching, input or output, on the MCU during the conversion.

There are some situations where external system activity causes radiated or conducted noise emissions or excessive V_{DD} noise is coupled into the ADC. In these situations, or when the MCU cannot be placed in wait or Stop3 or I/O activity cannot be halted, these recommended actions may reduce the effect of noise on the accuracy:

- Place a 0.01 µF capacitor (C_{AS}) on the selected input channel to V_{REFL} or V_{SSA} (this improves noise issues, but affects the sample rate based on the external analog source resistance).
- Average the result by converting the analog input many times in succession and dividing the sum of the results. Four samples are required to eliminate the effect of a 1LSB, one-time error.
- Reduce the effect of synchronous noise by operating off the asynchronous clock (ADACK) and averaging. Noise that is synchronous to ADCK cannot be averaged out.

19.6.2.4 Code width and quantization error

The ADC quantizes the ideal straight-line transfer function into 4096 steps (in 12-bit mode). Each step ideally has the same height (1 code) and width. The width is defined as the delta between the transition points to one code and the next. The ideal code width for an N bit converter (in this case N can be 8, 10 or 12), defined as 1LSB, is:

$$1\,\text{lsb} = \left(V_{\text{REFH}} - V_{\text{REFL}}\right) / \ 2^N$$

There is an inherent quantization error due to the digitization of the result. For 8-bit or 10-bit conversions the code transitions when the voltage is at the midpoint between the points where the straight line transfer function is exactly represented by the actual transfer function. Therefore, the quantization error will be ± 1/2 lsb in 8- or 10-bit mode. As a consequence, however, the code width of the first (0x000) conversion is only 1/2 lsb and the code width of the last (0xFF or 0x3FF) is 1.5 lsb.

For 12-bit conversions the code transitions only after the full code width is present, so the quantization error is -1 lsb to 0 lsb and the code width of each step is 1 lsb.

19.6.2.5 Linearity errors

The ADC may also exhibit non-linearity of several forms. Every effort has been made to reduce these errors but the system must be aware of them because they affect overall accuracy. These errors are:

- Zero-scale error (E_{ZS}) (sometimes called offset) — This error is defined as the difference between the actual code width of the first conversion and the ideal code width (1/2 lsb in 8-bit or 10-bit modes and 1 lsb in 12-bit mode). If the first conversion is 0x001, the difference between the actual 0x001 code width and its ideal (1 lsb) is used.
- Full-scale error (E_{FS}) — This error is defined as the difference between the actual code width of the last conversion and the ideal code width (1.5 lsb in 8-bit or 10-bit modes and 1LSB in 12-bit mode). If the last conversion is 0x3FE, the difference between the actual 0x3FE code width and its ideal (1 lsb) is used.
- Differential non-linearity (DNL) — This error is defined as the worst-case difference between the actual code width and the ideal code width for all conversions.

- Integral non-linearity (INL) — This error is defined as the highest-value that the absolute value of the running sum of DNL achieves. More simply, this is the worst-case difference of the actual transition voltage to a given code and its corresponding ideal transition voltage, for all codes.
- Total unadjusted error (TUE) — This error is defined as the difference between the actual transfer function and the ideal straight-line transfer function and includes all forms of error.

19.6.2.6 Code jitter, non-monotonicity, and missing codes

Analog-to-digital converters are susceptible to three special forms of error. These are code jitter, non-monotonicity, and missing codes.

Code jitter occurs when, at certain points, a given input voltage converts to one of two values when sampled repeatedly. Ideally, when the input voltage is infinitesimally smaller than the transition voltage, the converter yields the lower code (and vice-versa). However, even small amounts of system noise can cause the converter to be indeterminate, between two codes, for a range of input voltages around the transition voltage. This range is normally around ±1/2 lsb in 8-bit or 10-bit mode, or around 2 lsb in 12-bit mode, and increases with noise.

This error may be reduced by repeatedly sampling the input and averaging the result. Additionally the techniques discussed in Noise-induced errors reduces this error.

Non-monotonicity is defined when, except for code jitter, the converter converts to a lower code for a higher input voltage. Missing codes are those values that are never converted for any input value.

In 8-bit or 10-bit mode, the ADC is guaranteed to be monotonic and have no missing codes.

Chapter 20
Analog comparator (ACMP)

20.1 Introduction

The analog comparator module (ACMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).

The analog mux provides a circuit for selecting an analog input signal from eight channels. One signal provided by the 6-bit DAC. The mux circuit is designed to operate across the full range of the supply voltage. The 6-bit DAC is 64-tap resistor ladder network which provides a selectable voltage reference for applications where voltage reference is needed. The 64-tap resistor ladder network divides the supply reference V_{in} into 64 voltage level. A 6-bit digital signal input selects output voltage level, which varies from V_{in} to $V_{in}/64$. V_{in} can be selected from two voltage sources.

20.1.1 Features

ACMP features include:

- Operational over the whole supply range of 2.7 V to 5.5 V
- On-chip 6-bit resolution DAC with selectable reference voltage from V_{DD} or internal bandgap
- Configurable hysteresis
- Selectable interrupt on rising edge, falling edge, or both rising or falling edges of comparator output
- Selectable inversion on comparator output
- Up to four selectable comparator inputs
- Operational in Stop3 mode

20.1.2 Modes of operation

This section defines the ACMP operation in Wait, Stop3, and Background Debug modes.

20.1.2.1 Operation in Wait mode

The ACMP continues to operate in Wait mode, if enabled. The interrupt can wake the MCU if enabled.

20.1.2.2 Operation in Stop3 mode

The ACMP (including DAC and CMP) continues to operate in Stop3 mode if enabled. If ACMP_CS[ACIE] is set, a ACMP interrupt can be generated to wake the MCU up from Stop3 mode.

If the Stop3 is exited by an interrupt, the ACMP setting remains before entering the Stop mode. If Stop3 is exited with a reset, the ACMP goes into its reset.

The user must turn off the DAC if the output is not used as a reference input of ACMP to save power, because the DAC consumes additional power.

20.1.2.3 Operation in Debug mode

When the MCU is in Debug mode, the ACMP continues operating normally.

20.1.3 Block diagram

The block diagram of the ACMP module is shown in the following figure.

Figure 20-1. ACMP block diagram

20.2 External signal description

The output of ACMP can also be mapped to an external pin. When the output is mapped to an external pin, ACMP_CS[ACOPE] controls the pin to enable/disable the ACMP output function.

20.3 Memory map and register definition

ACMP memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
2C	ACMP Control and Status Register (ACMP_CS)	8	R/W	00h	20.3.1/573
2D	ACMP Control Register 0 (ACMP_C0)	8	R/W	00h	20.3.2/574
2E	ACMP Control Register 1 (ACMP_C1)	8	R/W	00h	20.3.3/575
2F	ACMP Control Register 2 (ACMP_C2)	8	R/W	00h	20.3.4/575

20.3.1 ACMP Control and Status Register (ACMP_CS)

Address: 2Ch base + 0h offset = 2Ch

Bit	7	6	5	4	3	2	1	0
Read	ACE	HYST	ACF	ACIE	ACO	ACOPE	ACMOD	
Write								
Reset	0	0	0	0	0	0	0	0

ACMP_CS field descriptions

Field	Description
7 ACE	Analog Comparator Enable Enables the ACMP module. 0 The ACMP is disabled. 1 The ACMP is enabled.
6 HYST	Analog Comparator Hysterisis Selection Selects ACMP hysterisis. 0 20 mV. 1 30 mV.
5 ACF	ACMP Interrupt Flag Bit Synchronously set by hardware when ACMP output has a valid edge defined by ACMOD. The setting of this bit lags the ACMPO to bus clocks. Clear ACF bit by writing a 0 to this bit. Writing a 1 to this bit has no effect.
4 ACIE	ACMP Interrupt Enable Enables an ACMP CPU interrupt. 0 Disable the ACMP Interrupt. 1 Enable the ACMP Interrupt.

Table continues on the next page...

ACMP_CS field descriptions (continued)

Field	Description
3 ACO	ACMP Output Reading ACO will return the current value of the analog comparator output. ACO is reset to a 0 and will read as a 0 when the ACMP is disabled (ACE = 0)
2 ACOPE	ACMP Output Pin Enable ACOPE enables the pad logic so that the output can be placed onto an external pin. 0 ACMP output cannot be placed onto external pin. 1 ACMP output can be placed onto external pin.
ACMOD	ACMP MOD Determines the sensitivity modes of the interrupt trigger. 00 ACMP interrupt on output falling edge. 01 ACMP interrupt on output rising edge. 10 ACMP interrupt on output falling edge. 11 ACMP interrupt on output falling or rising edge.

20.3.2 ACMP Control Register 0 (ACMP_C0)

Address: 2Ch base + 1h offset = 2Dh

Bit	7	6	5	4	3	2	1	0
Read	0		ACPSEL		0		ACNSEL	
Write								
Reset	0	0	0	0	0	0	0	0

ACMP_C0 field descriptions

Field	Description
7–6 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
5–4 ACPSEL	ACMP Positive Input Select 00 External reference 0 01 External reference 1 10 Reserved 11 DAC output
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ACNSEL	ACMP Negative Input Select 00 External reference 0 01 External reference 1 10 Reserved 11 DAC output

20.3.3 ACMP Control Register 1 (ACMP_C1)

Address: 2Ch base + 2h offset = 2Eh

Bit	7	6	5	4	3	2	1	0
Read Write	DACEN	DACREF	DACVAL					
Reset	0	0	0	0	0	0	0	0

ACMP_C1 field descriptions

Field	Description
7 DACEN	DAC Enable Enables the output of 6-bit DAC. 0 The DAC is disabled. 1 The DAC is enabled.
6 DACREF	DAC Reference Select 0 The DAC selects Bandgap as the reference. 1 The DAC selects V_{DDA} as the reference.
DACVAL	DAC Output Level Selection Selects the output voltage using the given formula: V_{output}= (V_{in}/64)x(DACVAL[5:0]+1) The V_{output} range is from V_{in}/64 to V_{in}, the step is V_{in}/64

20.3.4 ACMP Control Register 2 (ACMP_C2)

Address: 2Ch base + 3h offset = 2Fh

Bit	7	6	5	4	3	2	1	0
Read	0					ACIPE		
Write								
Reset	0	0	0	0	0	0	0	0

ACMP_C2 field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
ACIPE	ACMP Input Pin Enable This 3-bit field controls if the corresponding ACMP external pin can be driven by an analog input. 0 The corresponding external analog input is not allowed. 1 The corresponding external analog input is allowed.

20.4 Functional description

The ACMP module is functionally composed of two parts: digital-to-analog (DAC) and comparator (CMP).

The DAC includes a 64-level DAC (digital to analog converter) and relevant control logic. DAC can select one of two reference inputs, V_{DD} or on-chip bandgap, as the DAC input V_{in} by setting ACMP_C1[DACREF]. After the DAC is enabled, it converts the data set in ACMP_C1[DACVAL] to a stepped analog output, which is fed into ACMP as an internal reference input. This stepped analog output is also mapped out of the module. The output voltage range is from $V_{in}/64$ to V_{in}. The step size is $V_{in}/64$.

The ACMP can achieve the analog comparison between positive input and negative input, and then give out a digital output and relevant interrupt. Both the positive and negative input of ACMP can be selected from the four common inputs: three external reference inputs and one internal reference input from the DAC output. The positive input of ACMP is selected by ACMP_C0[ACPSEL] and the negative input is selected by ACMP_C0[ACNSEL]. Any pair of the eight inputs can be compared by configuring the ACMPC0 with the appropriate value.

After the ACMP is enabled by setting ACMP_CS[ACE], the comparison result appears as a digital output. Whenever a valid edge defined in ACMP_CS[ACMOD] occurs, ACMP_CS[ACF] is asserted. If ACMP_CS[ACIE] is set, a ACMP CPU interrupt occurs. The valid edge is defined by ACMP_CS[ACMOD]. When ACMP_CS[ACMOD] = 00b or 10b, only the falling-edge on ACMP output is valid. When ACMP_CS[ACMOD] = 01b, only rising-edge on ACMP output is valid. When ACMP_CS[ACMOD] = 11b, both the rising-edge and falling-edge on the ACMP output are valid.

The ACMP output is synchronized by the bus clock to generate ACMP_CS[ACO] so that the CPU can read the comparison. In stop3 mode, if the output of ACMP is changed, ACMPO cannot be updated in time. The output can be synchronized and ACMP_CS[ACO] can be updated upon the waking up of the CPU because of the availability of the bus clock. ACMP_CS[ACO] changes following the comparison result, so it can serve as a tracking flag that continuously indicates the voltage delta on the inputs.

If a reference input external to the chip is selected as an input of ACMP, the corresponding ACMP_C2[ACIPE] bit must be set to enable the input from pad interface. If the output of the ACMP needs to be put onto the external pin, the ACMP_CS[ACOPE] bit must enable the ACMP pin function of pad logic.

20.5 Setup and operation of ACMP

The two parts of ACMP (DAC and CMP) can be set up and operated independently. But if the DAC works as an input of the CMP, the DAC must be configured before the ACMP is enabled.

Because the input-switching can cause problems on the ACMP inputs, the user should complete the input selection before enabling the ACMP and must not change the input selection setting when the ACMP is enabled to avoid unexpected output. Similarly, because the DAC experiences a setup delay after ACMP_C1[DACVAL] is changed, the user should complete the setting of ACMP_C1[DACVAL] before DAC is enabled.

20.6 Resets

During a reset the ACMP is configured in the default mode. Both CMP and DAC are disabled.

20.7 Interrupts

If the bus clock is available when a valid edge defined in ACMP_CS[ACMOD] occurs, the ACMP_CS[ACF] is asserted. If ACMP_CS[ACIE] is set, a ACMP interrupt event occurs. The ACMP_CS[ACF] bit remains asserted until the ACMP interrupt is cleared by software. When in stop3 mode, a valid edge on ACMP output generates an asynchronous interrupt that can wake the MCU from stop3. The interrupt can be cleared by writing a 0 to the ACMP_CS[ACF] bit.

Chapter 21
Cyclic redundancy check (CRC)

21.1 Introduction

Cyclic redundancy check (CRC) generates 16/32-bit CRC code for error detection. The CRC can be configured to work as a standard CRC. It provides the user with programmable polynomial, SEED and other parameters required to implement a 16-bit or 32-bit CRC standard. These parameters are detailed in further sections.

21.2 Features

Features of the CRC module are:

- Hardware 16/32-bit CRC generator
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Optional feature to reverse input and output data by bit
- Optional final complement output of result
- High-speed CRC calculation

21.3 Block diagram

The following figure is the CRC block diagram.

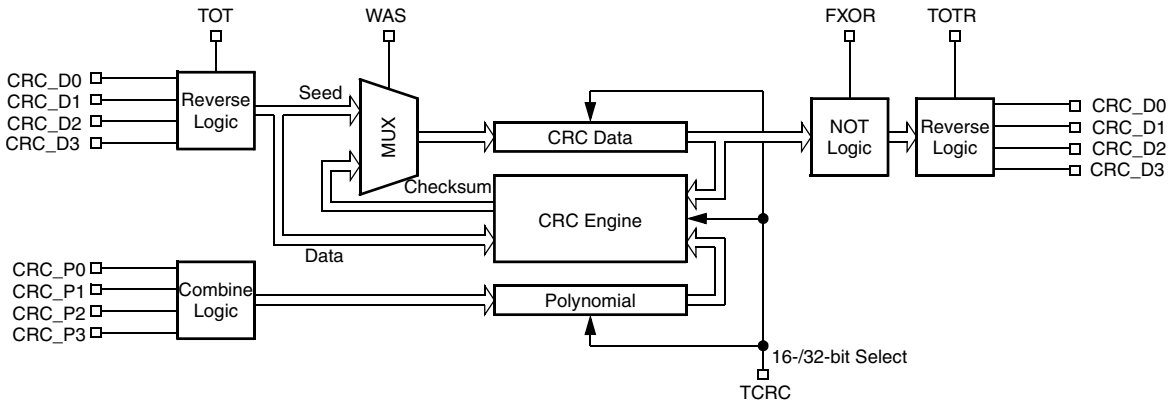


Figure 21-1. Cyclic redundancy check (S08CRC) block diagram

21.4 Modes of operation

This section defines the CRC operation in run, wait, and stop modes.

- Run mode - This is the basic mode of operation in which CRC is full functional.
- Wait mode - The CRC module is optional functional
- Stop3 mode - The CRC module is not functional in this low-power standby state. CRC calculations in progress stop and will resume after the CPU goes into run mode.

21.5 Register definition

CRC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3060	CRC Data 0 Register (CRC_D0)	8	R/W	FFh	21.5.1/581
3061	CRC Data 1 Register (CRC_D1)	8	R/W	FFh	21.5.2/581
3062	CRC Data 2 Register (CRC_D2)	8	R/W	FFh	21.5.3/582
3063	CRC Data 3 Register (CRC_D3)	8	R/W	FFh	21.5.4/583
3064	CRC Polynomial 0 Register (CRC_P0)	8	R/W	00h	21.5.5/583
3065	CRC Polynomial 1 Register (CRC_P1)	8	R/W	00h	21.5.6/584
3066	CRC Polynomial 2 Register (CRC_P2)	8	R/W	10h	21.5.7/584
3067	CRC Polynomial 3 Register (CRC_P3)	8	R/W	21h	21.5.8/585
3068	CRC Control Register (CRC_CTRL)	8	R/W	00h	21.5.9/585

21.5.1 CRC Data 0 Register (CRC_D0)

D0 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 0h offset = 3060h

Bit	7	6	5	4	3	2	1	0
Read Write	DH0							
Reset	1	1	1	1	1	1	1	1

CRC_D0 field descriptions

Field	Description
DH0	CRC Data Bit 31:24

21.5.2 CRC Data 1 Register (CRC_D1)

D1 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 1h offset = 3061h

Bit	7	6	5	4	3	2	1	0
Read Write	D1							
Reset	1	1	1	1	1	1	1	1

CRC_D1 field descriptions

Field	Description
D1	CRC Data Bit 23:16

21.5.3 CRC Data 2 Register (CRC_D2)

D2 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 2h offset = 3062h

Bit	7	6	5	4	3	2	1	0
Read Write	D2							
Reset	1	1	1	1	1	1	1	1

CRC_D2 field descriptions

Field	Description
D2	CRC Data Bit 15:8

21.5.4 CRC Data 3 Register (CRC_D3)

D3 is one of the CRC data registers (D0:D3). The set of CRC data registers contains the value of seed, data, and checksum. When CRC_CTRL[WAS] bit is set, any write to the data registers is regarded as seed for CRC module. When CRC_CTRL[WAS] bit is clear, any write to the data registers is regarded as data for general CRC computation, in which D0:D2 does not accept any data and D3 accept 8-bit write upon the polynomial configuration. When final data are written, the final result can be read from the data register. The registers of D0:D1 contain the MSB 16-bit of CRC data, which is used only in CRC 32-bit mode. Only D3 is used to dummy data to CRC. Writing D2 will be ignored when WAS = 0.

Address: 3060h base + 3h offset = 3063h

Bit	7	6	5	4	3	2	1	0
Read Write	D3							
Reset	1	1	1	1	1	1	1	1

CRC_D3 field descriptions

Field	Description
D3	CRC Data Bit 7:0

21.5.5 CRC Polynomial 0 Register (CRC_P0)

P0 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 4h offset = 3064h

Bit	7	6	5	4	3	2	1	0
Read Write	P0							
Reset	0	0	0	0	0	0	0	0

CRC_P0 field descriptions

Field	Description
P0	CRC Polynominal Bit 31:24

21.5.6 CRC Polynomial 1 Register (CRC_P1)

P1 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 5h offset = 3065h

Bit	7	6	5	4	3	2	1	0
Read Write	P1							
Reset	0	0	0	0	0	0	0	0

CRC_P1 field descriptions

Field	Description
P1	CRC Polynominal Bit 23:16

21.5.7 CRC Polynomial 2 Register (CRC_P2)

P2 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 6h offset = 3066h

Bit	7	6	5	4	3	2	1	0
Read Write	P2							
Reset	0	0	0	1	0	0	0	0

CRC_P2 field descriptions

Field	Description
P2	CRC Polynominal Bit 15:8

21.5.8 CRC Polynomial 3 Register (CRC_P3)

P3 is one of the CRC polynomial registers (P0:P3). The set of CRC polynominal registers contains the value of polynomial. The registers of P0:P1 contain the MSB 16-bit of CRC polynomial, which is used only in CRC 32-bit mode. The registers of P2:P3 contain the LSB 16-bit of CRC polynomial, which is used in both CRC 16- and 32-bit modes.

Address: 3060h base + 7h offset = 3067h

Bit	7	6	5	4	3	2	1	0
Read Write	P3							
Reset	0	0	1	0	0	0	0	1

CRC_P3 field descriptions

Field	Description
P3	CRC Polynominal Bit 7:0

21.5.9 CRC Control Register (CRC_CTRL)

Address: 3060h base + 8h offset = 3068h

Bit	7	6	5	4	3	2	1	0
Read	TOT		TOTR		0	FXOR	WAS	TCRC
Write								
Reset	0	0	0	0	0	0	0	0

CRC_CTRL field descriptions

Field	Description
7–6 TOT	Reverse of Write These bits identify the reverse of the input data. 00 No reverse. 01 Bit is reversed in byte; No byte is reversed. 10 Reserved. 11 Reserved.
5–4 TOTR	Reverse of Read These bits identify the reverse of the output data. 00 No reverse. 01 Bit is reversed in byte; No byte is reversed. 10 Reserved. 11 Reserved.

Table continues on the next page...

CRC_CTRL field descriptions (continued)

Field	Description
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 FXOR	Complement of Read This bit allows CRC module to output the complement of the final CRC checksum. 0 Normal checksum output. 1 Complement of checksum output.
1 WAS	Write CRC data register as seed This bit indicates the data written to the CRC data register (D0:D3) is seed or data. 0 Data is written in data registers. 1 Seed is written in data registers.
0 TCRC	Width of Polynomial Generator This bit indicates the bit width of the polynomial generator. 0 16-bit CRC Polynomial Generator. 1 32-bit CRC Polynomial Generator.

21.6 Functional description

21.6.1 16-bit CRC calculation

The following steps show how to start a general 16-bit CRC calculation:

1. Clear CRC_CTRL[TCRC] bit to enable 16-bit CRC mode.
2. Optional to enable reverse and complement function. Please see Bit reverse and Result complement for details.
3. Write 16-bit polynomial to CRC_P2:CRC_P3.
4. Set CRC_CTRL[WAS] bit to allow CRC_D2:CRC_D3 to be written by seed.
5. Write 16-bit seed to CRC_D2:CRC_D3.
6. Clear CRC_CTRL[WAS] bit to start 16-bit CRC calculation.
7. Dummy CRC_D3 with 8-bit CRC raw data.
8. Get the checksum from CRC_D2:CRC_D3 when all CRC raw data dummied.

21.6.2 32-bit CRC calculation

The following steps show how to start a general 32-bit CRC calculation:

1. Set CRC_CTRL[TCRC] bit to enable 32-bit CRC mode.

2. Optional to enable reverse and complement function. Please see Bit reverse and Result complement for details.
3. Write 32-bit polynomial to CRC_P0:CRC_P3.
4. Set CRC_CTRL[WAS] bit to allow CRC_D0:CRC_D3 written by seed.
5. Write 32-bit seed to CRC_D0:CRC_D3.
6. Clear CRC_CTRL[WAS] bit to start 32-bit CRC calculation.
7. Dummy CRC_D3 with 8-bit CRC raw data.
8. Get the checksum from CRC_D0:CRC_D3 when all CRC raw data dummied.

21.6.3 Bit reverse

The bit reverse function allows the input and output data reversed by bit for different CRC standard and endian systems. The CRC_CTRL[TOT] bits control the reverse of input data and the CRC_CTRL[TOTR] bits control the reverse of output data. The following table shows how the CRC_CTRL[TOT] and CRC_CTRL[TOTR] bits work.

Table 21-1. TOT and TOTR bit and byte reverse function

TOT ROW	D0	D1	D2	D3
00	b31b30b29b28b27b26b25b24	b23b22b21b20b19b18b17b16	b15b14b13b12b11b10b9b8	b7b6b5b4b3b2b1b0
01	b24b25b26b27b28b29b30b31	b16b17b18b19b20b21b22b23	b8b9b10b11b12b13b14b15	b0b1b2b3b4b5b6b7

NOTE

00 is the default case that no bit is reversed.

21.6.4 Result complement

The result complement function allows to output the complement of the checksum in CRC data registers. When CRC_CTRL[FXOR] bit is set, the checksum is read by its complement. Otherwise, the raw checksum is accessed.

21.6.5 CCITT compliant CRC example

The following code segment shows CCITT CRC-16 compliant example.

Example: 21.6.5.1 CCITT CRC-16 compliant example

```
CRC_CTRL = CRC_CTRL_WAS_MASK; // 16-bit CRC, ready to dummy seed
CRC_P2P3 = 0x1021; // Standard CCITT polynomail of (x^16 + x^12 + x^5 + 1)
CRC_D2D3 = 0xFFFF; // Set seed by 0xFFFF
CRC_CTRL = 0x00;

for ( i = 0 ; i < 128 ; i++ )
{
CRC_D3 = 'A'; // Dummy 256 'A'
CRC_D3 = 'A';
}

// Get 0xea0b in CRC_D2:CRC_D3 here
```

Chapter 22
Watchdog (WDOG)

22.1 Introduction

The Watchdog Timer (WDOG) module is an independent timer that is available for system use. It provides a safety feature to ensure that software is executing as planned and that the CPU is not stuck in an infinite loop or executing unintended code. If the WDOG module is not serviced (refreshed) within a certain period, it resets the MCU.

22.1.1 Features

Features of the WDOG module include:

- Configurable clock source inputs independent from the:
  - bus clock
  - Internal 32 kHz RC oscillator
  - Internal 1 kHz RC oscillator
  - External clock source
- Programmable timeout period
  - Programmable 16-bit timeout value
  - Optional fixed 256 clock prescaler when longer timeout periods are needed
- Robust write sequence for counter refresh
  - Refresh sequence of writing 0xA602 and then 0xB480 within 16 bus clocks
- Window mode option for the refresh mechanism
  - Programmable 16-bit window value

- Provides robust check that program flow is faster than expected
- Early refresh attempts trigger a reset.

- Optional timeout interrupt to allow post-processing diagnostics
  - Interrupt request to CPU with interrupt vector for an interrupt service routine (ISR)
  - Forced reset occurs 128 bus clocks after the interrupt vector fetch.
- Configuration bits are write-once-after-reset to ensure watchdog configuration cannot be mistakenly altered.
- Robust write sequence for unlocking write-once configuration bits
  - Unlock sequence of writing 0xC520 and then 0xD928 within 16 bus clocks for allowing updates to write-once configuration bits
  - Software must make updates within 128 bus clocks after unlocking and before WDOG closing unlock window.

22.1.2 Block diagram

The following figure provides a block diagram of the WDOG module.

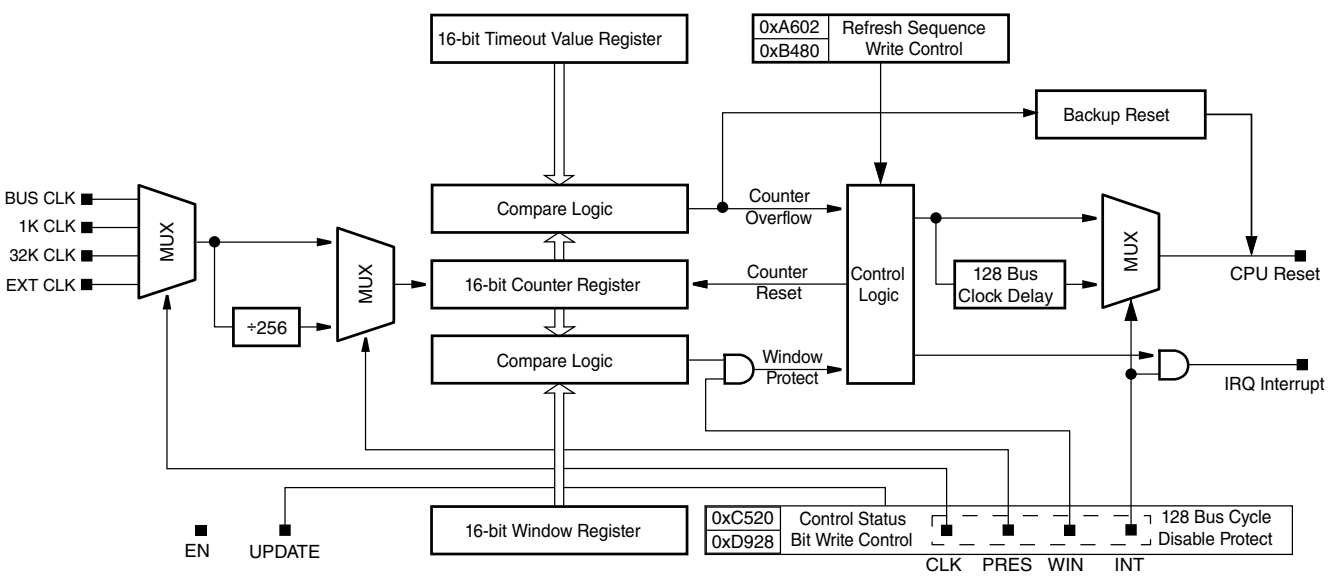


Figure 22-1. WDOG block diagram

22.2 Memory map and register definition

WDOG memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3030	Watchdog Control and Status Register 1 (WDOG_CS1)	8	R/W	80h	22.2.1/591
3031	Watchdog Control and Status Register 2 (WDOG_CS2)	8	R/W	01h	22.2.2/593
3032	Watchdog Counter Register: High (WDOG_CNTH)	8	R/W	00h	22.2.3/594
3033	Watchdog Counter Register: Low (WDOG_CNTL)	8	R/W	00h	22.2.4/594
3034	Watchdog Timeout Value Register: High (WDOG_TOVALH)	8	R/W	00h	22.2.5/595
3035	Watchdog Timeout Value Register: Low (WDOG_TOVALL)	8	R/W	04h	22.2.6/595
3036	Watchdog Window Register: High (WDOG_WINH)	8	R/W	00h	22.2.7/596
3037	Watchdog Window Register: Low (WDOG_WINL)	8	R/W	00h	22.2.8/596

22.2.1 Watchdog Control and Status Register 1 (WDOG_CS1)

This section describes the function of Watchdog Control and Status Register 1.

NOTE

TST is cleared (0:0) on POR only. Any other reset does not affect the value of this field.

Address: 3030h base + 0h offset = 3030h

Bit	7	6	5	4	3	2	1	0
Read Write	EN	INT	UPDATE	TST		DBG	WAIT	STOP
Reset	1	0	0	0	0	0	0	0

WDOG_CS1 field descriptions

Field	Description
7 EN	Watchdog Enable This write-once bit enables the watchdog counter to start counting. 0 Watchdog disabled. 1 Watchdog enabled.
6 INT	Watchdog Interrupt This write-once bit configures the watchdog to generate an interrupt request upon a reset-triggering event (timeout or illegal write to the watchdog), prior to forcing a reset. After the interrupt vector fetch, the reset occurs after a delay of 128 bus clocks.

Table continues on the next page...

WDOG_CS1 field descriptions (continued)

Field	Description
	0 Watchdog interrupts are disabled. Watchdog resets are not delayed. 1 Watchdog interrupts are enabled. Watchdog resets are delayed by 128 bus clocks.
5 UPDATE	Allow updates This write-once bit allows software to reconfigure the watchdog without a reset. 0 Updates not allowed. After the initial configuration, the watchdog cannot be later modified without forcing a reset. 1 Updates allowed. Software can modify the watchdog configuration registers within 128 bus clocks after performing the unlock write sequence.
4–3 TST	Watchdog Test Enables the fast test mode. The test mode allows software to exercise all bits of the counter to demonstrate that the watchdog is functioning properly. See the Fast testing of the watchdog section. This write-once field is cleared (0:0) on POR only. Any other reset does not affect the value of this field. 00 Watchdog test mode disabled. 01 Watchdog user mode enabled. (Watchdog test mode disabled.) After testing the watchdog, software should use this setting to indicate that the watchdog is functioning normally in user mode. 10 Watchdog test mode enabled, only the low byte is used. WDOG_CNTL is compared with WDOG_TOVALL. 11 Watchdog test mode enabled, only the high byte is used. WDOG_CNTH is compared with WDOG_TOVALH.
2 DBG	Debug Enable This write-once bit enables the watchdog to operate when the chip is in debug mode. 0 Watchdog disabled in chip debug mode. 1 Watchdog enabled in chip debug mode.
1 WAIT	Wait Enable This write-once bit enables the watchdog to operate when the chip is in wait mode. 0 Watchdog disabled in chip wait mode. 1 Watchdog enabled in chip wait mode.
0 STOP	Stop Enable This write-once bit enables the watchdog to operate when the chip is in stop mode. 0 Watchdog disabled in chip stop mode. 1 Watchdog enabled in chip stop mode.

22.2.2 Watchdog Control and Status Register 2 (WDOG_CS2)

This section describes the function of the watchdog control and status register 2.

Address: 3030h base + 1h offset = 3031h

Bit	7	6	5	4	3	2	1	0
Read	WIN	FLG	0	PRES	0		CLK	
Write		w1c						
Reset	0	0	0	0	0	0	0	1

WDOG_CS2 field descriptions

Field	Description
7 WIN	Watchdog Window This write-once bit enables window mode. See the Window mode section. 0 Window mode disabled. 1 Window mode enabled.
6 FLG	Watchdog Interrupt Flag This bit is an interrupt indicator when INT is set in control and status register 1. Write 1 to clear it. 0 No interrupt occurred. 1 An interrupt occurred.
5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4 PRES	Watchdog Prescalar This write-once bit enables a fixed 256 pre-scaling of watchdog counter reference clock. (The block diagram shows this clock divider option.) 0 256 prescalar disabled. 1 256 prescalar enabled.
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CLK	Watchdog Clock This write-once field indicates the clock source that feeds the watchdog counter. See the Clock source section. 00 Bus clock. 01 1 kHz internal low-power oscillator (LPOCLK). 10 32 kHz internal oscillator (ICSIRCLK). 11 External clock source.

22.2.3 Watchdog Counter Register: High (WDOG_CNTH)

This section describes the watchdog counter registers: high (CNTH) and low (CNTL) combined.

The watchdog counter registers CNTH and CNTL provide access to the value of the free-running watchdog counter. Software can read the counter registers at any time.

Software cannot write directly to the watchdog counter; however, two write sequences to these registers have special functions:

1. The *refresh sequence* resets the watchdog counter to 0x0000. See the Refreshing the Watchdog section.
2. The *unlock sequence* allows the watchdog to be reconfigured without forcing a reset (when WDOG_CS1[UPDATE] = 1). See the Example code: Reconfiguring the Watchdog section.

NOTE

All other writes to these registers are illegal and force a reset.

Address: 3030h base + 2h offset = 3032h

Bit	7	6	5	4	3	2	1	0
Read Write	CNTHIGH							
Reset	0	0	0	0	0	0	0	0

WDOG_CNTH field descriptions

Field	Description
CNTHIGH	High byte of the Watchdog Counter

22.2.4 Watchdog Counter Register: Low (WDOG_CNTL)

See the description of the WDOG_CNTH register.

Address: 3030h base + 3h offset = 3033h

Bit	7	6	5	4	3	2	1	0
Read Write	CNTLOW							
Reset	0	0	0	0	0	0	0	0

WDOG_CNTL field descriptions

Field	Description
CNTLOW	Low byte of the Watchdog Counter

22.2.5 Watchdog Timeout Value Register: High (WDOG_TOVALH)

This section describes the watchdog timeout value registers: high (WDOG_TOVALH) and low (WDOG_TOVALL) combined. WDOG_TOVALH and WDOG_TOVALL contains the 16-bit value used to set the timeout period of the watchdog.

The watchdog counter (WDOG_CNTH and WDOG_CNTL) is continuously compared with the timeout value (WDOG_TOVALH and WDOG_TOVALL). If the counter reaches the timeout value, the watchdog forces a reset.

NOTE

Do not write 0 to the Watchdog Timeout Value Register, otherwise, the watchdog always generates a reset.

Address: 3030h base + 4h offset = 3034h

Bit	7	6	5	4	3	2	1	0
Read Write	TOVALHIGH							
Reset	0	0	0	0	0	0	0	0

WDOG_TOVALH field descriptions

Field	Description
TOVALHIGH	High byte of the timeout value

22.2.6 Watchdog Timeout Value Register: Low (WDOG_TOVALL)

See the description of the WDOG_TOVALH register.

NOTE

All the bits reset to 0 in read.

Address: 3030h base + 5h offset = 3035h

Bit	7	6	5	4	3	2	1	0
Read Write	TOVALLOW							
Reset	0	0	0	0	0	1	0	0

WDOG_TOVALL field descriptions

Field	Description
TOVALLOW	Low byte of the timeout value

22.2.7 Watchdog Window Register: High (WDOG_WINH)

This section describes the watchdog window registers: high (WDOG_WINH) and low (WDOG_WINL) combined. When window mode is enabled (WDOG_CS2[WIN] is set), WDOG_WINH and WDOG_WINL determine the earliest time that a refresh sequence is considered valid. See the Watchdog refresh mechanism section.

WDOG_WINH and WDOG_WINL must be less than WDOG_TOVALH and WDOG_TOVALL.

Address: 3030h base + 6h offset = 3036h

Bit	7	6	5	4	3	2	1	0
Read Write	WINHIGH							
Reset	0	0	0	0	0	0	0	0

WDOG_WINH field descriptions

Field	Description
WINHIGH	High byte of Watchdog Window

22.2.8 Watchdog Window Register: Low (WDOG_WINL)

See the description of the WDOG_WINH register.

Address: 3030h base + 7h offset = 3037h

Bit	7	6	5	4	3	2	1	0
Read Write	WINLOW							
Reset	0	0	0	0	0	0	0	0

WDOG_WINL field descriptions

Field	Description
WINLOW	Low byte of Watchdog Window

22.3 Functional description

The WDOG module provides a fail safe mechanism to ensure the system can be reset to a known state of operation in case of system failure, such as the CPU clock stopping or there being a run away condition in the software code. The watchdog counter runs continuously off a selectable clock source and expects to be serviced (refreshed) periodically. If it is not, it resets the system.

The timeout period, window mode, and clock source are all programmable but must be configured within 128 bus clocks after a reset.

22.3.1 Watchdog refresh mechanism

The watchdog resets the MCU if the watchdog counter is not refreshed. A robust refresh mechanism makes it very unlikely that the watchdog can be refreshed by runaway code.

To refresh the watchdog counter, software must execute a refresh write sequence before the timeout period expires. In addition, if window mode is used, software must not start the refresh sequence until after the time value set in the WDOG_WINH and WDOG_WINL registers. See the following figure.

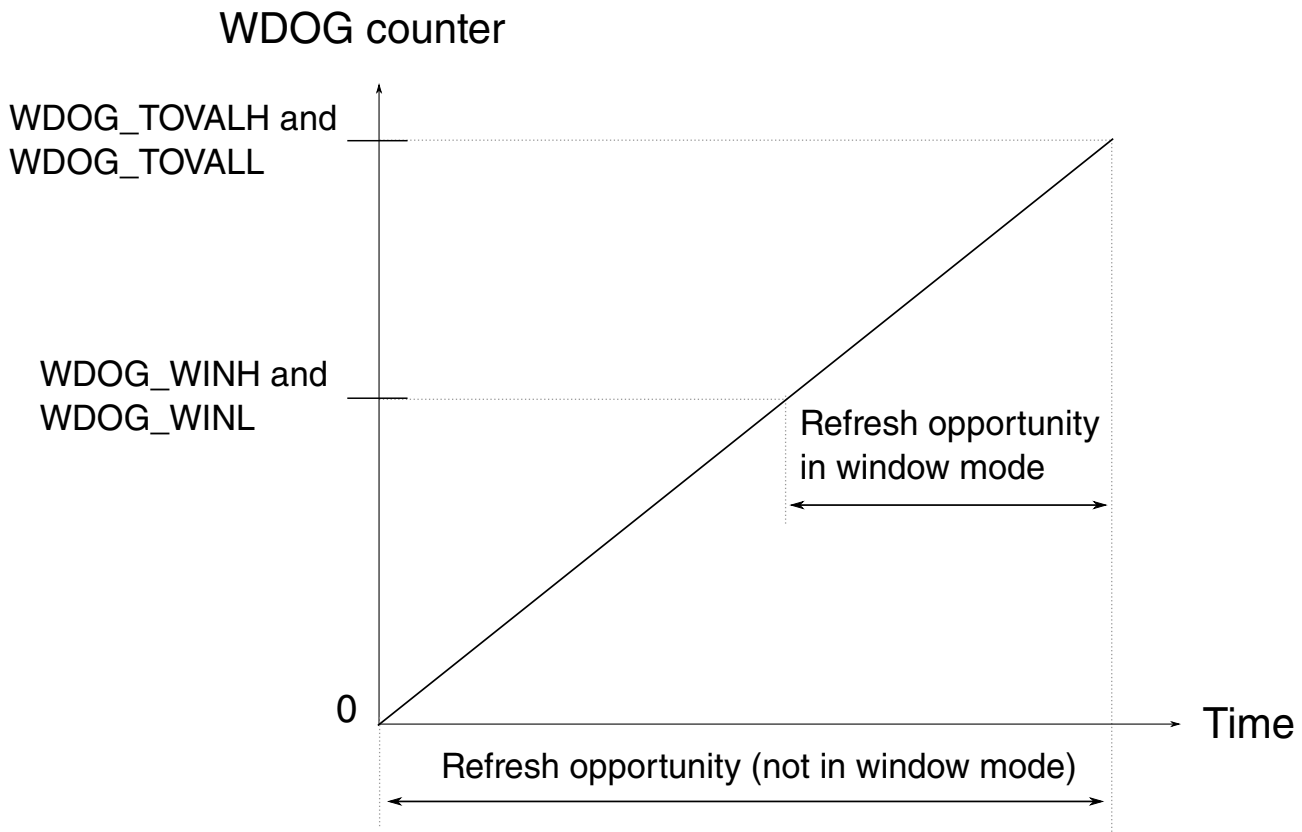


Figure 22-2. Refresh opportunity for the Watchdog counter

22.3.1.1 Window mode

Software finishing its main control loop faster than expected could be an indication of a problem. Depending on the requirements of the application, the WDOG can be programmed to force a reset when refresh attempts are early.

When Window mode is enabled, the watchdog must be refreshed after the counter has reached a minimum expected time value; otherwise, the watchdog resets the MCU. The minimum expected time value is specified in the WDOG_WINH:L registers. Setting CS1[WIN] enables Window mode.

22.3.1.2 Refreshing the Watchdog

The refresh write sequence is a write of 0xA602 followed by a write of 0xB480 to the WDOG_CNTH and WDOG_CNTL registers. The write of the 0xB480 must occur within 16 bus clocks after the write of 0xA602; otherwise, the watchdog resets the MCU.

Note

Before starting the refresh sequence, disable global interrupts. Otherwise, an interrupt could effectively invalidate the refresh sequence if writing the four bytes takes more than 16 bus clocks. Re-enable interrupts when the sequence is finished.

22.3.1.3 Example code: Refreshing the Watchdog

The following code segment shows the refresh write sequence of the WDOG module.

```
/* Refresh watchdog */

for (;;) // main loop
{
   ...

   DisableInterrupts; // disable global interrupt

   WDOG_CNT = 0xA602; // write the 1st refresh word

   WDOG_CNT = 0xB480; // write the 2nd refresh word to refresh counter

   EnableInterrupts; // enable global interrupt

   ...
}
```

22.3.2 Configuring the Watchdog

All watchdog control bits, timeout value, and window value are write-once after reset. This means that after a write has occurred they cannot be changed unless a reset occurs. This provides a robust mechanism to configure the watchdog and ensure that a runaway condition cannot mistakenly disable or modify the watchdog configuration after configured.

This is guaranteed by the user configuring the window and timeout value first, followed by the other control bits, and ensuring that CS1[UPDATE] is also set to 0. The new configuration takes effect only after all registers except WDOG_CNTH:L are written once after reset. Otherwise, the WDOG uses the reset values by default. If window mode is not used (CS2[WIN] is 0), writing to WDOG_WINH:L is not required to make the new configuration take effect.

22.3.2.1 Reconfiguring the Watchdog

In some cases (such as when supporting a bootloader function), users may want to reconfigure or disable the watchdog without forcing a reset first. By setting CS1[UPDATE] to a 1 on the initial configuration of the watchdog after a reset, users can reconfigure the watchdog at any time by executing an unlock sequence. (Conversely, if CS1[UPDATE] remains 0, the only way to reconfigure the watchdog is by initiating a reset.) The unlock sequence is similar to the refresh sequence but uses different values.

22.3.2.2 Unlocking the Watchdog

The unlock sequence is a write to the WDOG_CNTH:L registers of 0xC520 followed by 0xD928 within 16 bus clocks at any time after the watchdog has been configured. On completing the unlock sequence, the user must reconfigure the watchdog within 128 bus clocks; otherwise, the watchdog forces a reset to the MCU.

NOTE

Due to 128 bus clocks requirement for reconfiguring the watchdog, some delays must be inserted before executing STOP or WAIT instructions after reconfiguring the watchdog. This ensures that the watchdog's new configuration takes effect before MCU enters low power mode. Otherwise, the MCU may not be waken up from low power mode.

22.3.2.3 Example code: Reconfiguring the Watchdog

The following code segment shows an example reconfiguration of the WDOG module.

```
/* Initialize watchdog with ~1-kHz clock source, ~1s time-out */

DisableInterrupts; // disable global interrupt

WDOG_CNT = 0xC520; // write the 1st unlock word

WDOG_CNT = 0xD928; // write the 2nd unlock word

WDOG_TOVAL = 1000; // setting timeout value

WDOG_CS2 = WDOG_CS2_CLK_MASK; // setting 1-kHz clock source

WDOG_CS1 = WDOG_CS1_EN_MASK; // enable counter running

EnableInterrupts; // enable global interrupt
```

22.3.3 Clock source

The watchdog counter has four clock source options selected by programming CS2[CLK]:

- bus clock
- internal Low-Power Oscillator (LPO) running at approximately 1 kHz (This is the default source.)
- internal 32 kHz clock
- external clock

The options allow software to select a clock source independent of the bus clock for applications that need to meet more robust safety requirements. Using a clock source other than the bus clock ensures that the watchdog counter continues to run if the bus clock is somehow halted; see Backup reset.

An optional fixed prescaler for all clock sources allows for longer timeout periods. When CS2[PRES] is set, the clock source is prescaled by 256 before clocking the watchdog counter.

The following table summarizes the different watchdog timeout periods available.

Table 22-1. Watchdog timeout availability

Reference clock	Prescaler	Watchdog time-out availability
Internal ~1 kHz (LPO)	Pass through	~1 ms–65.5 s[1]
	÷256	~256 ms–16,777 s
Internal ~32 kHz	Pass through	~31.25 µs–2.048 s
	÷256	~8 ms–524.3 s
1 MHz (from bus or external)	Pass through	1 µs–65.54 ms
	÷256	256 µs–16.777 s
20 MHz (from bus or external)	Pass through	50 ns–3.277 ms
	÷256	12.8 µs–838.8 ms

1. The default timeout value after reset is approximately 4 ms.

NOTE

When the programmer switches clock sources during reconfiguration, the watchdog hardware holds the counter at zero for 2.5 periods of the previous clock source and 2.5 periods of the new clock source after the configuration time period (128 bus clocks) ends. This delay ensures a smooth transition before restarting the counter with the new configuration.

22.3.4 Using interrupts to delay resets

When interrupts are enabled (CS1[INT] = 1), the watchdog first generates an interrupt request upon a reset triggering event (such as a counter timeout or invalid refresh attempt). The watchdog delays forcing a reset for 128 bus clocks to allow the interrupt service routine (ISR) to perform tasks, such as analyzing the stack to debug code.

When interrupts are disabled (CS1[INT] = 0), the watchdog does not delay forcing a reset.

22.3.5 Backup reset

NOTE

A clock source other than the bus clock must be used as the reference clock for the counter; otherwise, the backup reset function is not available.

The backup reset function is a safeguard feature that independently generates a reset in case the main WDOG logic loses its clock (the bus clock) and can no longer monitor the counter. If the watchdog counter overflows twice in succession (without an intervening reset), the backup reset function takes effect and generates a reset.

22.3.6 Functionality in debug and low-power modes

By default, the watchdog is not functional in Active Background mode, Wait mode, or Stop3 mode. However, the watchdog can remain functional in these modes as follows:

- For Active Background mode, set CS1[DBG]. (This way the watchdog is functional in Active Background mode even when the CPU is held by the Debug module.)
- For Wait mode, set CS1[WAIT].
- For Stop3 mode, set CS1[STOP].

NOTE

The watchdog can not generate interrupt in Stop3 mode even if CS1[STOP] is set and will not wake the MCU from Stop3 mode. It can generate reset during Stop3 mode.

For Active Background mode and Stop3 mode, in addition to the above configurations, a clock source other than the bus clock must be used as the reference clock for the counter; otherwise, the watchdog cannot function.

22.3.7 Fast testing of the watchdog

Before executing application code in safety critical applications, users are required to test that the watchdog works as expected and resets the MCU. Testing every bit of a 16-bit counter by letting it run to the overflow value takes a relatively long time (64 kHz clocks).

To help minimize the startup delay for application code after reset, the watchdog has a feature to test the watchdog more quickly by splitting the counter into its constituent byte-wide stages. The low and high bytes are run independently and tested for timeout against the corresponding byte of the timeout value register. (For complete coverage when testing the high byte of the counter, the test feature feeds the input clock via the 8th bit of the low byte, thus ensuring that the overflow connection from the low byte to the high byte is tested.)

Using this test feature reduces the test time to 512 clocks (not including overhead, such as user configuration and reset vector fetches). To further speed testing, use a faster clock (such as the bus clock) for the counter reference.

On a power-on reset, the POR bit in the system reset register is set, indicating the user should perform the WDOG fast test.

22.3.7.1 Testing each byte of the counter

The test procedure follows these steps:

1. Program the preferred watchdog timeout value in the WDOG_TOVALH and WDOG_TOVALL registers during the watchdog configuration time period.
2. Select a byte of the counter to test using the WDOG_CS1[TST] = 10b for the low byte; WDOG_CS1[TST] = 11b for the high byte.
3. Wait for the watchdog to timeout. Optionally, in the idle loop, increment RAM locations as a parallel software counter for later comparison. Because the RAM is not affected by a watchdog reset, the timeout period of the watchdog counter can be compared with the software counter to verify the timeout period has occurred as expected.
4. The watchdog counter times out and forces a reset.

5. Confirm the WDOG flag in the system reset register is set, indicating that the watchdog caused the reset. (The POR flag remains clear.)
6. Confirm that WDOG_CS1[TST] shows a test (10b or 11b) was performed.

If confirmed, the count and compare functions work for the selected byte. Repeat the procedure, selecting the other byte in step 2.

NOTE

WDOG_CS1[TST] is cleared by a POR only and not affected by other resets.

22.3.7.2 Entering user mode

After successfully testing the low and high bytes of the watchdog counter, the user can configure WDOG_CS1[TST] to 01b to indicate the watchdog is ready for use in application user mode. Thus if a reset occurs again, software can recognize the reset trigger as a real watchdog reset caused by runaway or faulty application code.

As an ongoing test when using the default 1 kHz clock source, software can periodically read the WDOG_CNTH and WDOG_CNTL registers to ensure the counter is being incremented.

Chapter 23
Development support

23.1 Introduction

This chapter describes the single-wire background debug mode (BDM), which uses the on-chip background debug controller (BDC) module, and the independent on-chip real-time in-circuit emulation (ICE) system, which uses the on-chip debug (DBG) module.

23.1.1 Forcing active background

The method for forcing active background mode depends on the specific HCS08 derivative. For the 9S08xxxx, you can force active background after a power-on reset by holding the BKGD pin low as the device exits the reset condition. You can also force active background by driving BKGD low immediately after a serial background command that writes a one to the BDFR bit in the SBDFR register. Other causes of reset including an external pin reset or an internally generated error reset ignore the state of the BKGD pin and reset into normal user mode. If no debug pod is connected to the BKGD pin, the MCU will always reset into normal operating mode.

23.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC

- BDC clock runs in stop mode, if BDC enabled
- Watchdog disabled by default while in active background mode. It can also be enabled by proper configuration

Features of the ICE system include:

- Two trigger comparators: Two address + read/write (R/W) or one full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
  - Change-of-flow addresses or
  - Event-only data
- Two types of breakpoints:
  - Tag breakpoints for instruction opcodes
  - Force breakpoints for any address access
- Nine trigger modes:
  - Basic: A-only, A OR B
  - Sequence: A then B
  - Full: A AND B data, A AND NOT B data
  - Event (store data): Event-only B, A then event-only B
  - Range: Inside range (A ≤ address ≤ B), outside range (address < A or address > B)

23.2 Background debug controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

- Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be read or written, and allow the user to trace one user instruction at a time, or GO to the user program from active background mode.
- Non-intrusive commands can be executed at any time even while the user's program is running. Non-intrusive commands allow a user to read or write MCU memory locations or access status and control registers within the background debug controller.

Typically, a relatively simple interface pod is used to translate commands from a host computer into commands for the custom serial interface to the single-wire background debug system. Depending on the development tool vendor, this interface pod may use a standard RS-232 serial port, a parallel printer port, or some other type of communications such as a universal serial bus (USB) to communicate between the host PC and the pod. The pod typically connects to the target system with ground, the BKGD pin, RESET, and sometimes V_{DD}. An open-drain connection to reset allows the host to force a target system reset, which is useful to regain control of a lost target system or to control startup of a target system before the on-chip nonvolatile memory has been programmed. Sometimes V_{DD} can be used to allow the pod to use power from the target system to avoid the need for a separate power supply. However, if the pod is powered separately, it can be connected to a running target system without forcing a target system reset or otherwise disturbing the running application program.

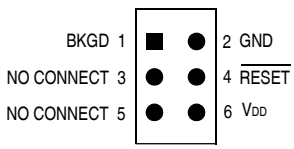


Figure 23-1. BDM tool connector

23.2.1 BKGD pin description

BKGD is the single-wire background debug interface pin. The primary function of this pin is for bidirectional serial communication of active background mode commands and data. During reset, this pin is used to select between starting in active background mode or starting the user's application program. This pin is also used to request a timed sync response pulse to allow a host development tool to determine the correct clock frequency for background debug serial communications.

BDC serial communications use a custom serial protocol first introduced on the M68HC12 Family of microcontrollers. This protocol assumes the host knows the communication clock rate that is determined by the target BDC clock rate. All communication is initiated and controlled by the host that drives a high-to-low edge to signal the beginning of each bit time. Commands and data are sent most significant bit first (MSB first). For a detailed description of the communications protocol, refer to Communication details.

If a host is attempting to communicate with a target MCU that has an unknown BDC clock rate, a SYNC command may be sent to the target MCU to request a timed sync response signal from which the host can determine the correct communication speed.

BKGD is a pseudo-open-drain pin and there is an on-chip pullup so no external pullup resistor is required. Unlike typical open-drain pins, the external RC time constant on this pin, which is influenced by external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speedup pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to Communication details for more detail.

When no debugger pod is connected to the 6-pin BDM interface connector, the internal pullup on BKGD chooses normal operating mode. When a debug pod is connected to BKGD it is possible to force the MCU into active background mode after reset. The specific conditions for forcing active background depend upon the HCS08 derivative (refer to the introduction to this Development Support section). It is not necessary to reset the target MCU to communicate with it through the background debug interface.

23.2.2 Communication details

The BDC serial interface requires the external controller to generate a falling edge on the BKGD pin to indicate the start of each bit time. The external controller provides this falling edge whether data is transmitted or received.

BKGD is a pseudo-open-drain pin that can be driven either by an external controller or by the MCU. Data is transferred MSB first at 16 BDC clock cycles per bit (nominal speed). The interface times out if 512 BDC clock cycles occur between falling edges from the host. Any BDC command that was in progress when this timeout occurs is aborted without affecting the memory or operating mode of the target MCU system.

The custom serial protocol requires the debug pod to know the target BDC communication clock speed.

The clock switch (CLKSW) control bit in the BDC status and control register allows the user to select the BDC clock source. The BDC clock source can either be the bus or the alternate BDC clock source.

The BKGD pin can receive a high or low level or transmit a high or low level. The following diagrams show timing for each of these cases. Interface timing is synchronous to clocks in the target BDC, but asynchronous to the external host. The internal BDC clock signal is shown for reference in counting cycles.

The following figure shows an external host transmitting a logic 1 or 0 to the BKGD pin of a target HCS08 MCU. The host is asynchronous to the target so there is a 0-to-1 cycle delay from the host-generated falling edge to where the target perceives the beginning of the bit time. Ten target BDC clock cycles later, the target senses the bit level on the BKGD pin. Typically, the host actively drives the pseudo-open-drain BKGD pin during

host-to-target transmissions to speed up rising edges. Because the target does not drive the BKGD pin during the host-to-target transmission period, there is no need to treat the line as an open-drain signal during this period.

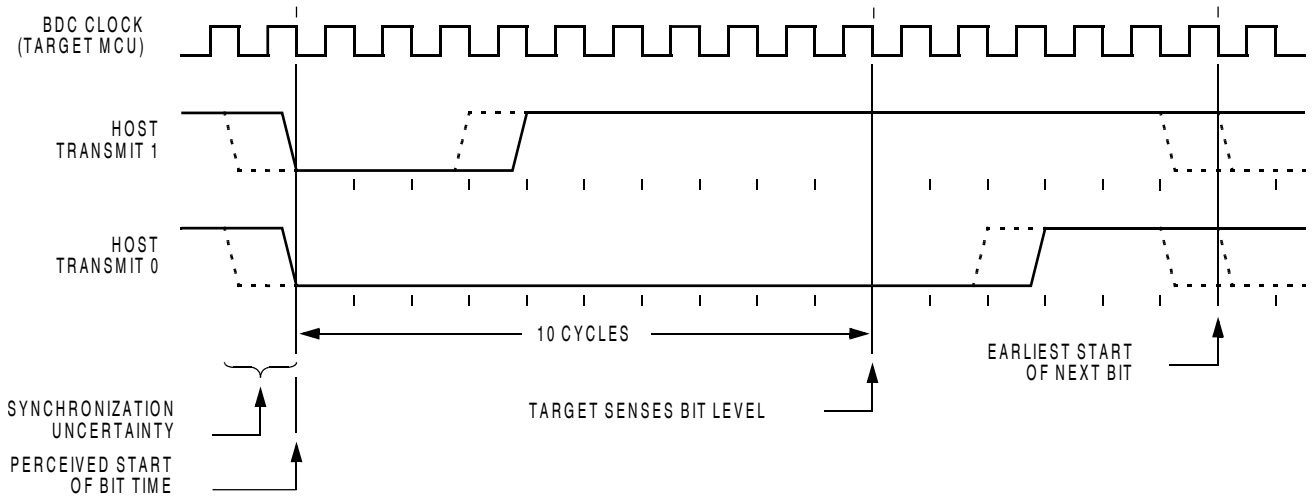


Figure 23-2. BDC host-to-target serial bit timing

The next figure shows the host receiving a logic 1 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target MCU. The host holds the BKGD pin low long enough for the target to recognize it (at least two target BDC cycles). The host must release the low drive before the target MCU drives a brief active-high speedup pulse seven cycles after the perceived start of the bit time. The host should sample the bit level about 10 cycles after it started the bit time.

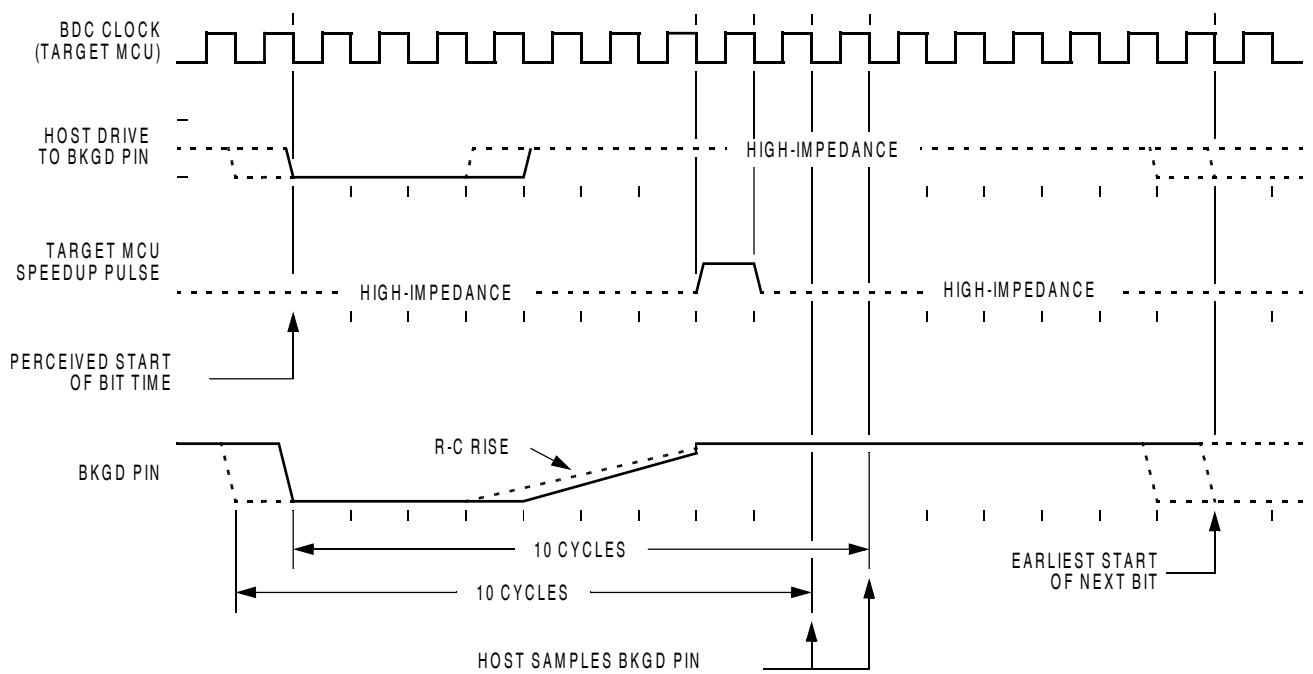


Figure 23-3. BDC target-to-host serial bit timing (logic 1)

The following figure shows the host receiving a logic 0 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target MCU. The host initiates the bit time but the target HCS08 finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 BDC clock cycles, then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 cycles after starting the bit time.

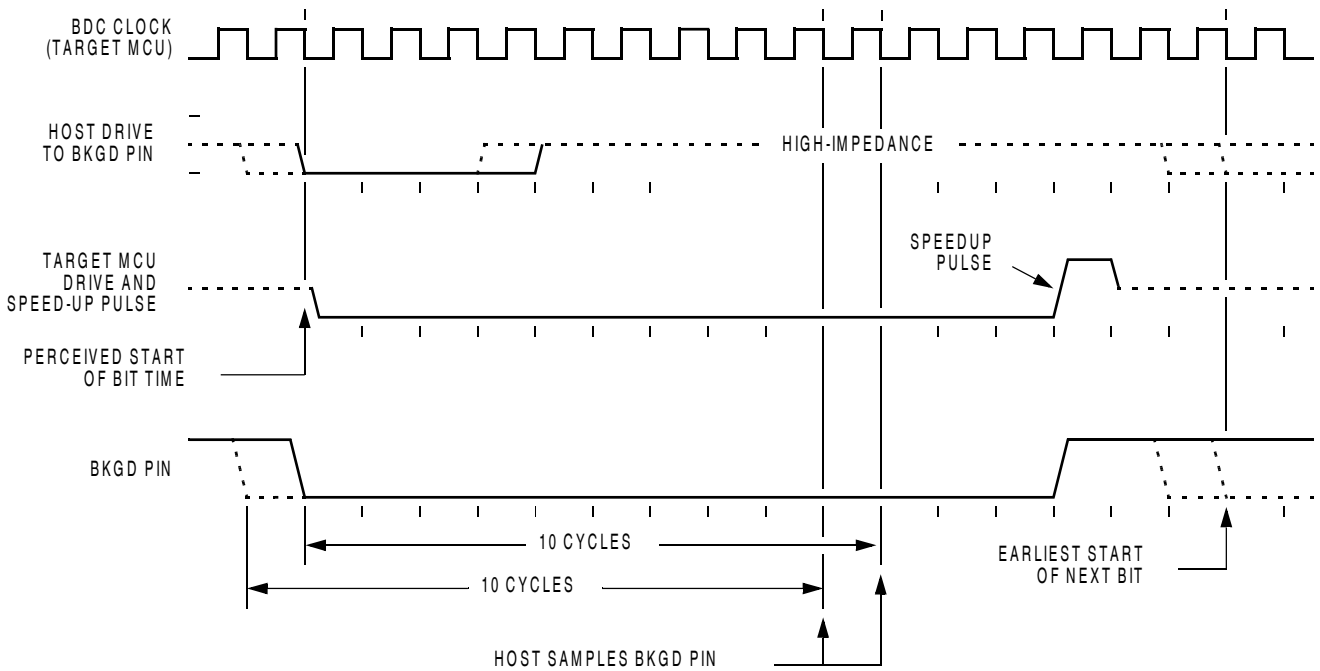


Figure 23-4. BDM target-to-host serial bit timing (logic 0)

23.2.3 BDC commands

BDC commands are sent serially from a host computer to the BKGD pin of the target HCS08 MCU. All commands and data are sent MSB-first using a custom BDC communications protocol. Active background mode commands require that the target MCU is currently in the active background mode while non-intrusive commands may be issued at any time whether the target MCU is in active background mode or running a user application program.

The following table shows all HCS08 BDC commands, a shorthand description of their coding structure, and the meaning of each command.

Coding Structure Nomenclature

This nomenclature is used in the following table to describe the coding structure of the BDC commands.

```
Commands begin with an 8-bit hexadecimal command code in the host-to-target direction (most
significant bit first)
/ =separates parts of the command
d=delay 16 target BDC clock cycles
AAAA = a 16-bit address in the host-to-target direction
RD   = 8 bits of read data in the target-to-host direction
WD   = 8 bits of write data in the host-to-target direction
RD16 = 16 bits of read data in the target-to-host direction
WD16 = 16 bits of write data in the host-to-target direction
SS   = the contents of BDCSCR in the target-to-host direction (STATUS)
CC   = 8 bits of write data for BDCSCR in the host-to-target direction (CONTROL)
RBKP = 16 bits of read data in the target-to-host direction (from BDCBKPT breakpoint
register)
WBKP = 16 bits of write data in the host-to-target direction (for BDCBKPT breakpoint
register)
```

Table 23-1. BDC command summary

Command mnemonic	Active BDM/ non-intrusive	Coding structure	Description
SYNC	Non-intrusive	N/A[1]	Request a timed reference pulse to determine target BDC communication speed
ACK_ENABLE	Non-intrusive	D5/d	Enable acknowledge protocol. Refer to NXP document order no. HCS08RMv1/D.
ACK_DISABLE	Non-intrusive	D6/d	Disable acknowledge protocol. Refer to NXP document order no. HCS08RMv1/D.
BACKGROUND	Non-intrusive	90/d	Enter active background mode if enabled (ignore if ENBDM bit equals 0)
READ_STATUS	Non-intrusive	E4/SS	Read BDC status from BDCSCR
WRITE_CONTROL	Non-intrusive	C4/CC	Write BDC controls in BDCSCR
READ_BYTE	Non-intrusive	E0/AAAA/d/RD	Read a byte from target memory
READ_BYTE_WS	Non-intrusive	E1/AAAA/d/SS/RD	Read a byte and report status
READ_LAST	Non-intrusive	E8/SS/RD	Re-read byte from address just read and report status
WRITE_BYTE	Non-intrusive	C0/AAAA/WD/d	Write a byte to target memory
WRITE_BYTE_WS	Non-intrusive	C1/AAAA/WD/d/SS	Write a byte and report status
READ_BKPT	Non-intrusive	E2/RBKP	Read BDCBKPT breakpoint register
WRITE_BKPT	Non-intrusive	C2/WBKP	Write BDCBKPT breakpoint register
GO	Active BDM	08/d	Go to execute the user application program starting at the address currently in the PC
TRACE1	Active BDM	10/d	Trace 1 user instruction at the address in the PC, then return to active background mode

Table continues on the next page...

Table 23-1. BDC command summary (continued)

Command mnemonic	Active BDM/ non-intrusive	Coding structure	Description
TAGGO	Active BDM	18/d	Same as GO but enable external tagging (HCS08 devices have no external tagging pin)
READ_A	Active BDM	68/d/RD	Read accumulator (A)
READ_CCR	Active BDM	69/d/RD	Read condition code register (CCR)
READ_PC	Active BDM	6B/d/RD16	Read program counter (PC)
READ_HX	Active BDM	6C/d/RD16	Read H and X register pair (H:X)
READ_SP	Active BDM	6F/d/RD16	Read stack pointer (SP)
READ_NEXT	Active BDM	70/d/RD	Increment H:X by one then read memory byte located at H:X
READ_NEXT_WS	Active BDM	71/d/SS/RD	Increment H:X by one then read memory byte located at H:X. Report status and data.
WRITE_A	Active BDM	48/WD/d	Write accumulator (A)
WRITE_CCR	Active BDM	49/WD/d	Write condition code register (CCR)
WRITE_PC	Active BDM	4B/WD16/d	Write program counter (PC)
WRITE_HX	Active BDM	4C/WD16/d	Write H and X register pair (H:X)
WRITE_SP	Active BDM	4F/WD16/d	Write stack pointer (SP)
WRITE_NEXT	Active BDM	50/WD/d	Increment H:X by one, then write memory byte located at H:X
WRITE_NEXT_WS	Active BDM	51/WD/d/SS	Increment H:X by one, then write memory byte located at H:X. Also report status.

1. The SYNC command is a special operation that does not have a command code.

The SYNC command is unlike other BDC commands because the host does not necessarily know the correct communications speed to use for BDC communications until after it has analyzed the response to the SYNC command.

To issue a SYNC command, the host:

- Drives the BKGD pin low for at least 128 cycles of the slowest possible BDC clock (The slowest clock is normally the reference oscillator/64 or the self-clocked rate/ 64.)
- Drives BKGD high for a brief speedup pulse to get a fast rise time (This speedup pulse is typically one cycle of the fastest clock in the system.)
- Removes all drive to the BKGD pin so it reverts to high impedance
- Monitors the BKGD pin for the sync response pulse

The target, upon detecting the SYNC request from the host (which is a much longer low time than would ever occur during normal BDC communications):

- Waits for BKGD to return to a logic high
- Delays 16 cycles to allow the host to stop driving the high speedup pulse
- Drives BKGD low for 128 BDC clock cycles
- Drives a 1-cycle high speedup pulse to force a fast rise time on BKGD
- Removes all drive to the BKGD pin so it reverts to high impedance

The host measures the low time of this 128-cycle sync response pulse and determines the correct speed for subsequent BDC communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

23.2.4 BDC hardware breakpoint

The BDC includes one relatively simple hardware breakpoint that compares the CPU address bus to a 16-bit match value in the BDCBKPT register. This breakpoint can generate a forced breakpoint or a tagged breakpoint. A forced breakpoint causes the CPU to enter active background mode at the first instruction boundary following any access to the breakpoint address. The tagged breakpoint causes the instruction opcode at the breakpoint address to be tagged so that the CPU will enter active background mode rather than executing that instruction if and when it reaches the end of the instruction queue. This implies that tagged breakpoints can be placed only at the address of an instruction opcode while forced breakpoints can be set at any address.

The breakpoint enable (BKPTEN) control bit in the BDC status and control register (BDCSCR) is used to enable the breakpoint logic (BKPTEN = 1). When BKPTEN = 0, its default value after reset, the breakpoint logic is disabled and no BDC breakpoints are requested regardless of the values in other BDC breakpoint registers and control bits. The force/tag select (FTS) control bit in BDCSCR is used to select forced (FTS = 1) or tagged (FTS = 0) type breakpoints.

The on-chip debug module (DBG) includes circuitry for two additional hardware breakpoints that are more flexible than the simple breakpoint in the BDC module.

23.3 On-chip debug system (DBG)

Because HCS08 devices do not have external address and data buses, the most important functions of an in-circuit emulator have been built onto the chip with the MCU. The debug system consists of an 8-stage FIFO that can store address or data bus information,

and a flexible trigger system to decide when to capture bus information and what information to capture. The system relies on the single-wire background debug system to access debug control registers and to read results out of the eight stage FIFO.

The debug module includes control and status registers that are accessible in the user's memory map. These registers are located in the high register space to avoid using valuable direct page memory space.

Most of the debug module's functions are used during development, and user programs rarely access any of the control and status registers for the debug module. The one exception is that the debug system can provide the means to implement a form of ROM patching. This topic is discussed in greater detail in Hardware breakpoints.

23.3.1 Comparators A and B

Two 16-bit comparators (A and B) can optionally be qualified with the R/W signal and an opcode tracking circuit. Separate control bits allow you to ignore R/W for each comparator. The opcode tracking circuitry optionally allows you to specify that a trigger will occur only if the opcode at the specified address is actually executed as opposed to only being read from memory into the instruction queue. The comparators are also capable of magnitude comparisons to support the inside range and outside range trigger modes. Comparators are disabled temporarily during all BDC accesses.

The A comparator is always associated with the 16-bit CPU address. The B comparator compares to the CPU address or the 8-bit CPU data bus, depending on the trigger mode selected. Because the CPU data bus is separated into a read data bus and a write data bus, the RWAEN and RWA control bits have an additional purpose, in full address plus data comparisons they are used to decide which of these buses to use in the comparator B data bus comparisons. If RWAEN = 1 (enabled) and RWA = 0 (write), the CPU's write data bus is used. Otherwise, the CPU's read data bus is used.

The currently selected trigger mode determines what the debugger logic does when a comparator detects a qualified match condition. A match can cause:

- Generation of a breakpoint to the CPU
- Storage of data bus values into the FIFO
- Starting to store change-of-flow addresses into the FIFO (begin type trace)
- Stopping the storage of change-of-flow addresses into the FIFO (end type trace)

23.3.2 Bus capture information and FIFO operation

The usual way to use the FIFO is to setup the trigger mode and other control options, then arm the debugger. When the FIFO has filled or the debugger has stopped storing data into the FIFO, you would read the information out of it in the order it was stored into the FIFO. Status bits indicate the number of words of valid information that are in the FIFO as data is stored into it. If a trace run is manually halted by writing 0 to ARM before the FIFO is full (CNT = 1:0:0:0), the information is shifted by one position and the host must perform ((8 - CNT) - 1) dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see Trigger modes), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When ARM = 0, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

23.3.3 Change-of-flow information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

23.3.4 Tag vs. force breakpoints and triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.

A force-type breakpoint waits for the current instruction to finish and then acts upon the breakpoint request. The usual action in response to a breakpoint is to go to active background mode rather than continuing to the next instruction in the user application program.

The tag vs. force terminology is used in two contexts within the debug module. The first context refers to breakpoint requests from the debug module to the CPU. The second refers to match signals from the comparators to the debugger control logic. When a tag-type break request is sent to the CPU, a signal is entered into the instruction queue along with the opcode so that if/when this opcode ever executes, the CPU will effectively replace the tagged opcode with a BGND opcode so the CPU goes to active background mode rather than executing the tagged instruction. When the TRGSEL control bit in the DBGT register is set to select tag-type operation, the output from comparator A or B is qualified by a block of logic in the debug module that tracks opcodes and produces only a trigger to the debugger if the opcode at the compare address is actually executed. There is separate opcode tracking logic for each comparator so more than one compare event can be tracked through the instruction queue at a time.

23.3.5 Trigger modes

The trigger mode controls the overall behavior of a debug run. The 4-bit TRG field in the DBGT register selects one of nine trigger modes. When TRGSEL = 1 in the DBGT register, the output of the comparator must propagate through an opcode tracking circuit before triggering FIFO actions. The BEGIN bit in DBGT chooses whether the FIFO begins storing data when the qualified trigger is detected (begin trace), or the FIFO stores data in a circular fashion from the time it is armed until the qualified trigger is detected (end trigger).

A debug run is started by writing a 1 to the ARM bit in the DBGC register, which sets the ARMF flag and clears the AF and BF flags and the CNT bits in DBGS. A begin-trace debug run ends when the FIFO gets full. An end-trace run ends when the selected trigger event occurs. Any debug run can be stopped manually by writing a 0 to ARM or DBGEN in DBGC.

In all trigger modes except event-only modes, the FIFO stores change-of-flow addresses. In event-only trigger modes, the FIFO stores data in the low-order eight bits of the FIFO.

The BEGIN control bit is ignored in event-only trigger modes and all such debug runs are begin type traces. When TRGSEL = 1 to select opcode fetch triggers, it is not necessary to use R/W in comparisons because opcode tags would apply only to opcode fetches that are always read cycles. It would also be unusual to specify TRGSEL = 1 while using a full mode trigger because the opcode value is normally known at a particular address.

The following trigger mode descriptions state only the primary comparator conditions that lead to a trigger. Either comparator can usually be further qualified with R/W by setting RWAEN (RWBEN) and the corresponding RWA (RWB) value to be matched against R/W. The signal from the comparator with optional R/W qualification is used to request a CPU breakpoint if BRKEN = 1 and TAG determines whether the CPU request will be a tag request or a force request.

A-Only – Trigger when the address matches the value in comparator A

A OR B – Trigger when the address matches either the value in comparator A or the value in comparator B

A Then B – Trigger when the address matches the value in comparator B but only after the address for another cycle matched the value in comparator A. There can be any number of cycles after the A match and before the B match.

A AND B Data (Full Mode)— This is called a full mode because address, data, and R/W (optionally) must match within the same bus cycle to cause a trigger event. Comparator A checks address, the low byte of comparator B checks data, and R/W is checked against RWA if RWAEN = 1. The high-order half of comparator B is not used.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

A AND NOT B Data (Full Mode)— Address must match comparator A, data must not match the low half of comparator B, and R/W must match RWA if RWAEN = 1. All three conditions must be met within the same bus cycle to cause a trigger.

In full trigger modes it is not useful to specify a tag-type CPU breakpoint (BRKEN = TAG = 1), but if you do, the comparator B data match is ignored for the purpose of issuing the tag request to the CPU and the CPU breakpoint is issued when the comparator A address matches.

Event-Only B (Store Data)— Trigger events occur each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

A Then Event-Only B (Store Data)— After the address has matched the value in comparator A, a trigger event occurs each time the address matches the value in comparator B. Trigger events cause the data to be captured into the FIFO. The debug run ends when the FIFO becomes full.

Inside Range (A ≤ Address ≤ B)— A trigger occurs when the address is greater than or equal to the value in comparator A and less than or equal to the value in comparator B at the same time.

Outside Range (Address < A or Address > B)— A trigger occurs when the address is either less than the value in comparator A or greater than the value in comparator B.

23.3.6 Hardware breakpoints

The BRKEN control bit in the DBGC register may be set to 1 to allow any of the trigger conditions described in Trigger modes to be used to generate a hardware breakpoint request to the CPU. TAG in DBGC controls whether the breakpoint request will be treated as a tag-type breakpoint or a force-type breakpoint. A tag breakpoint causes the current opcode to be marked as it enters the instruction queue. If a tagged opcode reaches

the end of the pipe, the CPU executes a BGND instruction to go to active background mode rather than executing the tagged opcode. A force-type breakpoint causes the CPU to finish the current instruction and then go to active background mode.

If the background mode has not been enabled (ENBDM = 1) by a serial WRITE_CONTROL command through the BKGD pin, the CPU will execute an SWI instruction instead of going to active background mode.

23.4 Memory map and register description

This section contains the descriptions of the BDCand DBG registers and control bits. Refer to the high-page register summary in the device overview chapter of this data sheet for the absolute address assignments for all DBG registers. This section refers to registers and control bits only by their names. An NXP-provided equate or header file is used to translate these names into the appropriate absolute addresses.

BDC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	BDC Status and Control Register (BDC_SCR)	8	R/W	00h	23.4.1/619
1	BDC Breakpoint Match Register: High (BDC_BKPTH)	8	R/W	00h	23.4.2/621
2	BDC Breakpoint Register: Low (BDC_BKPTL)	8	R/W	00h	23.4.3/622
3	System Background Debug Force Reset Register (BDC_SBDFR)	8	W (always reads 0)	00h	23.4.4/622

23.4.1 BDC Status and Control Register (BDC_SCR)

This register can be read or written by serial BDC commands (READ_STATUS and WRITE_CONTROL) but is not accessible to user programs because it is not located in the normal memory map of the MCU.

NOTE

The reset values shown in the register figure are those in the normal reset conditions. If the MCU is reset in BDM, ENBDM, BDMACT, CLKSW will be reset to 1 and others all be to 0.

Address: 0h base + 0h offset = 0h

Bit	7	6	5	4	3	2	1	0
Read	ENBDM	BDMACT	BKPTEN	FTS	CLKSW	WS	WSF	DVF
Write								
Reset	0	0	0	0	0	0	0	0

BDC_SCR field descriptions

Field	Description
7 ENBDM	Enable BDM (Permit Active Background Mode) Typically, this bit is written to 1 by the debug host shortly after the beginning of a debug session or whenever the debug host resets the target and remains 1 until a normal reset clears it. 0 BDM cannot be made active (non-intrusive commands still allowed). 1 BDM can be made active to allow active background mode commands.
6 BDMACT	Background Mode Active Status This is a read-only status bit. 0 BDM not active (user application program running). 1 BDM active and waiting for serial commands.
5 BKPTEN	BDC Breakpoint Enable If this bit is clear, the BDC breakpoint is disabled and the FTS (force tag select) control bit and BDCBKPT match register are ignored. 0 BDC breakpoint disabled. 1 BDC breakpoint enabled.
4 FTS	Force/Tag Select When FTS = 1, a breakpoint is requested whenever the CPU address bus matches the BDCBKPT match register. When FTS = 0, a match between the CPU address bus and the BDCBKPT register causes the fetched opcode to be tagged. If this tagged opcode ever reaches the end of the instruction queue, the CPU enters active background mode rather than executing the tagged opcode. 0 Tag opcode at breakpoint address and enter active background mode if CPU attempts to execute that instruction 1 Breakpoint match forces active background mode at next instruction boundary (address need not be an opcode)
3 CLKSW	Select Source for BDC Communications Clock CLKSW defaults to 0, which selects the alternate BDC clock source. 0 Alternate BDC clock source. 1 MCU bus clock.
2 WS	Wait or Stop Status When the target CPU is in wait or stop mode, most BDC commands cannot function. However, the BACKGROUND command can be used to force the target CPU out of wait or stop and into active background mode where all BDC commands work. Whenever the host forces the target MCU into active background mode, the host should issue a READ_STATUS command to check that BDMACT = 1 before attempting other BDC commands.

Table continues on the next page...

BDC_SCR field descriptions (continued)

Field	Description
	0 Target CPU is running user application code or in active background mode (was not in wait or stop mode when background became active). 1 Target CPU is in wait or stop mode, or a BACKGROUND command was used to change from wait or stop to active background mode.
1 WSF	Wait or Stop Failure Status This status bit is set if a memory access command failed due to the target CPU executing a wait or stop instruction at or about the same time. The usual recovery strategy is to issue a BACKGROUND command to get out of wait or stop mode into active background mode, repeat the command that failed, then return to the user program. (Typically, the host would restore CPU registers and stack values and re-execute the wait or stop instruction.) 0 Memory access did not conflict with a wait or stop instruction. 1 Memory access command failed because the CPU entered wait or stop mode.
0 DVF	Data Valid Failure Status 0 Memory access did not conflict with a slow memory access 1 Memory access command failed because CPU was not finished with a slow memory access.

23.4.2 BDC Breakpoint Match Register: High (BDC_BKPTH)

This register, together with BDC_BKPTL, holds the address for the hardware breakpoint in the BDC. The BKPTEN and FTS control bits in BDCSCR are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDCBKPT register but is not accessible to user programs because it is not located in the normal memory map of the MCU. Breakpoints are normally set while the target MCU is in active background mode before running the user application program.

Address: 0h base + 1h offset = 1h

Bit	7	6	5	4	3	2	1	0
Read Write	A[15:8]							
Reset	0	0	0	0	0	0	0	0

BDC_BKPTH field descriptions

Field	Description
A[15:8]	High 8-bit of hardware breakpoint address.

23.4.3 BDC Breakpoint Register: Low (BDC_BKPTL)

BDC_BKPTH and BDC_BKPTL registers hold the address for the hardware breakpoint in the BDC. The BDC_SCR[FTS] and BDC_SCR[BKPTEN] bits are used to enable and configure the breakpoint logic. Dedicated serial BDC commands (READ_BKPT and WRITE_BKPT) are used to read and write the BDC_BKPTH and BDC_BKPTL register. Breakpoints are normally set while the target MCU is in background debug mode before running the user application program. However, since READ_BKPT and WRITE_BKPT are foreground commands, they could be executed even while the user program is running.

Address: 0h base + 2h offset = 2h

Bit	7	6	5	4	3	2	1	0
Read Write	A[7:0]							
Reset	0	0	0	0	0	0	0	0

BDC_BKPTL field descriptions

Field	Description
A[7:0]	Low 8-bit of hardware breakpoint address.

23.4.4 System Background Debug Force Reset Register (BDC_SBDFR)

This register contains a single write-only control bit. A serial background mode command such as WRITE_BYTE must be used to write to SBDFR. Attempts to write this register from a user program are ignored. Reads always return 0x00.

Address: 0h base + 3h offset = 3h

Bit	7	6	5	4	3	2	1	0
Read	0							0
Write								BDFR
Reset	0	0	0	0	0	0	0	0

BDC_SBDFR field descriptions

Field	Description
7–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 BDFR	Background Debug Force Reset

Table continues on the next page...

BDC_SBDFR field descriptions (continued)

Field	Description
	A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

Chapter 24
Debug module (DBG)

24.1 Introduction

The DBG module implements an on-chip ICE (in-circuit emulation) system and allows non-intrusive debug of application software by providing an on-chip trace buffer with flexible triggering capability. The trigger also can provide extended breakpoint capacity. The on-chip ICE system is optimized for the S08CPUV6 8-bit architecture and supports 2 M bytes of memory space.

24.1.1 Features

The on-chip ICE system includes these distinctive features:

- Three comparators (A, B, and C) with ability to match addresses in 64 KB space
  - Dual mode, Comparators A and B used to compare addresses
  - Full mode, Comparator A compares address and Comparator B compares data
  - Can be used as triggers and/or breakpoints
  - Comparator C can be used as a normal hardware breakpoint
  - Loop1 capture mode, Comparator C is used to track most recent COF event captured into FIFO
- Tag and Force type breakpoints
- Nine trigger modes
  - A
  - A Or B
  - A then B
  - A and B, where B is data (full mode)
  - A and not B, where B is data (full mode)
  - Event only B, store data
  - A then event only B, store data
  - Inside range, A ≤ address ≤ B
  - Outside range, address < A or address > B

- FIFO for storing change of flow information and event only data
  - Source address of conditional branches taken
  - Destination address of indirect JMP and JSR instruction
  - Destination address of interrupts, RTI, RTC, and RTS instruction
  - Data associated with Event B trigger modes
- Ability to End-trace until reset and begin-trace from reset

24.1.2 Modes of operation

The on-chip ICE system can be enabled in all MCU functional modes. The DBG module is disabled if the MCU is secure. The DBG module comparators are disabled when executing a Background Debug Mode (BDM) command.

24.1.3 Block diagram

The following figure shows the structure of the DBG module.

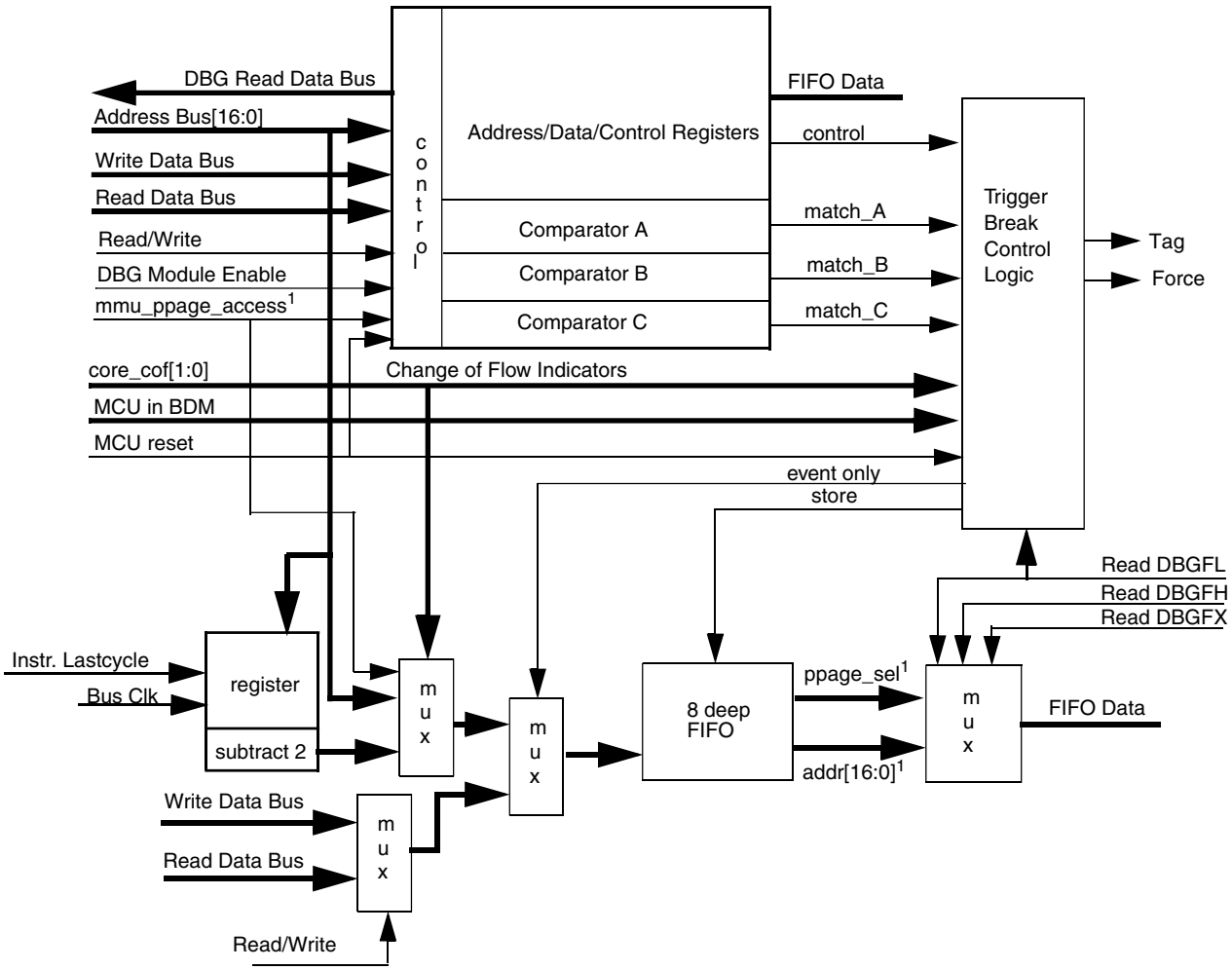


Figure 24-1. DBG block diagram

24.2 Signal description

The DBG module contains no external signals.

24.3 Memory map and registers

This section provides a detailed description of all DBG registers accessible to the end user.

DBG memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
3010	Debug Comparator A High Register (DBG_CAH)	8	R/W	FFh	24.3.1/628
3011	Debug Comparator A Low Register (DBG_CAL)	8	R/W	FEh	24.3.2/629
3012	Debug Comparator B High Register (DBG_CBH)	8	R/W	00h	24.3.3/630
3013	Debug Comparator B Low Register (DBG_CBL)	8	R/W	00h	24.3.4/630
3014	Debug Comparator C High Register (DBG_CCH)	8	R/W	00h	24.3.5/631
3015	Debug Comparator C Low Register (DBG_CCL)	8	R/W	00h	24.3.6/632
3016	Debug FIFO High Register (DBG_FH)	8	R	00h	24.3.7/632
3017	Debug FIFO Low Register (DBG_FL)	8	R	00h	24.3.8/633
3018	Debug Comparator A Extension Register (DBG_CAX)	8	R/W	00h	24.3.9/634
3019	Debug Comparator B Extension Register (DBG_CBX)	8	R/W	00h	24.3.10/ 635
301A	Debug Comparator C Extension Register (DBG_CCX)	8	R/W	00h	24.3.11/ 636
301B	Debug FIFO Extended Information Register (DBG_FX)	8	R	00h	24.3.12/ 637
301C	Debug Control Register (DBG_C)	8	R/W	C0h	24.3.13/ 637
301D	Debug Trigger Register (DBG_T)	8	R/W	40h	24.3.14/ 638
301E	Debug Status Register (DBG_S)	8	R	01h	24.3.15/ 640
301F	Debug Count Status Register (DBG_CNT)	8	R	00h	24.3.16/ 641

24.3.1 Debug Comparator A High Register (DBG_CAH)

NOTE

All the bits in this register reset to 1 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 0h offset = 3010h

Bit	7	6	5	4	3	2	1	0
Read Write	CA[15:8]							
Reset	1	1	1	1	1	1	1	1

DBG_CAH field descriptions

Field	Description
CA[15:8]	Comparator A High Compare Bits The Comparator A High compare bits control whether Comparator A will compare the address bus bits [15:8] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

24.3.2 Debug Comparator A Low Register (DBG_CAL)

NOTE

All the bits in this register reset to 1 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 1h offset = 3011h

Bit	7	6	5	4	3	2	1	0
Read Write	CA[7:0]							
Reset	1	1	1	1	1	1	1	0

DBG_CAL field descriptions

Field	Description
CA[7:0]	Comparator A Low The Comparator A Low compare bits control whether Comparator A will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

24.3.3 Debug Comparator B High Register (DBG_CBH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 2h offset = 3012h

Bit	7	6	5	4	3	2	1	0
Read Write	CB[15:8]							
Reset	0	0	0	0	0	0	0	0

DBG_CBH field descriptions

Field	Description
CB[15:8]	Comparator B High Compare Bits The Comparator B High compare bits control whether Comparator B will compare the address bus bits [15:8] to a logic 1 or logic 0.Not used in full mode. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

24.3.4 Debug Comparator B Low Register (DBG_CBL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 3h offset = 3013h

Bit	7	6	5	4	3	2	1	0
Read Write	CB[7:0]							
Reset	0	0	0	0	0	0	0	0

DBG_CBL field descriptions

Field	Description
CB[7:0]	Comparator B Low The Comparator B Low compare bits control whether Comparator B will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

24.3.5 Debug Comparator C High Register (DBG_CCH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 4h offset = 3014h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[15:8]							
Reset	0	0	0	0	0	0	0	0

DBG_CCH field descriptions

Field	Description
CC[15:8]	Comparator C High Compare Bits The Comparator C High compare bits control whether Comparator C will compare the address bus bits [15:8] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

24.3.6 Debug Comparator C Low Register (DBG_CCL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 5h offset = 3015h

Bit	7	6	5	4	3	2	1	0
Read Write	CC[7:0]							
Reset	0	0	0	0	0	0	0	0

DBG_CCL field descriptions

Field	Description
CC[7:0]	Comparator C Low The Comparator C Low compare bits control whether Comparator C will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0. 1 Compare corresponding address bit to a logic 1.

24.3.7 Debug FIFO High Register (DBG_FH)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 6h offset = 3016h

Bit	7	6	5	4	3	2	1	0
Read	F[15:8]							
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FH field descriptions

Field	Description
F[15:8]	FIFO High Data Bits The FIFO High data bits provide access to bits [15:8] of data in the FIFO. This register is not used in event only modes and will read a $00 for valid FIFO words.

24.3.8 Debug FIFO Low Register (DBG_FL)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 7h offset = 3017h

Bit	7	6	5	4	3	2	1	0
Read	F[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FL field descriptions

Field	Description
F[7:0]	FIFO Low Data Bits The FIFO Low data bits contain the least significant byte of data in the FIFO. When reading FIFO words, read DBGFX and DBGFH before reading DBGFL because reading DBGFL causes the FIFO pointers to advance to the next FIFO location. In event-only modes, there is no useful information in DBGFX and DBGFH so it is not necessary to read them before reading DBGFL.

24.3.9 Debug Comparator A Extension Register (DBG_CAX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 8h offset = 3018h

Bit	7	6	5	4	3	2	1	0
Read	RWAEN	RWA	0					
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CAX field descriptions

Field	Description
7 RWAEN	Read/Write Comparator A Enable Bit The RWAEN bit controls whether read or write comparison is enabled for Comparator A. 0 Read/Write is not used in comparison. 1 Read/Write is used in comparison.
6 RWA	Read/Write Comparator A Value Bit The RWA bit controls whether read or write is used in compare for Comparator A. The RWA bit is not used if RWAEN = 0. 0 Write cycle will be matched. 1 Read cycle will be matched.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

24.3.10 Debug Comparator B Extension Register (DBG_CBX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + 9h offset = 3019h

Bit	7	6	5	4	3	2	1	0
Read	RWBEN	RWB	0					
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CBX field descriptions

Field	Description
7 RWBEN	Read/Write Comparator B Enable Bit The RWBEN bit controls whether read or write comparison is enabled for Comparator B. In full modes, RWAEN and RWA are used to control comparison of R/W and RWBEN is ignored. 0 Read/Write is not used in comparison. 1 Read/Write is used in comparison.
6 RWB	Read/Write Comparator B Value Bit The RWB bit controls whether read or write is used in compare for Comparator B. The RWB bit is not used if RWBEN = 0.In full modes, RWAEN and RWA are used to control comparison of R/W and RWB is ignored. 0 Write cycle will be matched. 1 Read cycle will be matched.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

24.3.11 Debug Comparator C Extension Register (DBG_CCX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + Ah offset = 301Ah

Bit	7	6	5	4	3	2	1	0
Read	RWCEN	RWC	0					
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CCX field descriptions

Field	Description
7 RWCEN	Read/Write Comparator C Enable Bit The RWCEN bit controls whether read or write comparison is enabled for Comparator C. 0 Read/Write is not used in comparison. 1 Read/Write is used in comparison.
6 RWC	Read/Write Comparator C Value Bit The RWC bit controls whether read or write is used in compare for Comparator C. The RWC bit is not used if RWCEN = 0. 0 Write cycle will be matched. 1 Read cycle will be matched.
Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

24.3.12 Debug FIFO Extended Information Register (DBG_FX)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the bits in this register do not change after reset.

Address: 3010h base + Bh offset = 301Bh

Bit	7	6	5	4	3	2	1	0
Read	PPACC	0						Bit16
Write								
Reset	0	0	0	0	0	0	0	0

DBG_FX field descriptions

Field	Description
7 PPACC	PPAGE Access Indicator Bit This bit indicates whether the captured information in the current FIFO word is associated with an extended access through the PPAGE mechanism or not. This is indicated by the internal signal mmu_ppage_sel which is 1 when the access is through the PPAGE mechanism. 0 The information in the corresponding FIFO word is event-only data or an unpaged 17-bit CPU address with bit-16 = 0. 1 The information in the corresponding FIFO word is a 17-bit flash address with PPAGE[2:0] in the three most significant bits and CPU address[13:0] in the 14 least significant bits.
6–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 Bit16	Extended Address Bit 16 This bit is the most significant bit of the 17-bit core address.

24.3.13 Debug Control Register (DBG_C)

Address: 3010h base + Ch offset = 301Ch

Bit	7	6	5	4	3	2	1	0
Read Write	DBGEN	ARM	TAG	BRKEN	0			LOOP1
Reset	1	1	0	0	0	0	0	0

DBG_C field descriptions

Field	Description
7 DBGEN	DBG Module Enable Bit The DBGEN bit enables the DBG module. The DBGEN bit is forced to zero and cannot be set if the MCU is secure. 0 DBG not enabled. 1 DBG enabled.
6 ARM	Arm Bit The ARM bit controls whether the debugger is comparing and storing data in FIFO. 0 Debugger not armed. 1 Debugger armed.
5 TAG	Tag or Force Bit The TAG bit controls whether a debugger or comparator C breakpoint will be requested as a tag or force breakpoint to the CPU. The TAG bit is not used if BRKEN = 0. 0 Force request selected. 1 Tag request selected.
4 BRKEN	Break Enable Bit The BRKEN bit controls whether the debugger will request a breakpoint to the CPU at the end of a trace run, and whether comparator C will request a breakpoint to the CPU. 0 CPU break request not enabled. 1 CPU break request enabled.
3–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 LOOP1	Select LOOP1 Capture Mode This bit selects either normal capture mode or LOOP1 capture mode. LOOP1 is not used in event-only modes. 0 Normal operation - capture COF events into the capture buffer FIFO. 1 LOOP1 capture mode enabled. When the conditions are met to store a COF value into the FIFO, compare the current COF address with the address in comparator C. If these addresses match, override the FIFO capture and do not increment the FIFO count. If the address does not match comparator C, capture the COF address, including the PPACC indicator, into the FIFO and into comparator C..

24.3.14 Debug Trigger Register (DBG_T)

NOTE

The figure shows the values in POR or non-end-run reset. All the bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, the ARM and BRKEN bits are cleared but the remaining control bits in this register do not change after reset.

NOTE

The DBG trigger register (DBGT) can not be changed unless ARM=0.

Address: 3010h base + Dh offset = 301Dh

Bit	7	6	5	4	3	2	1	0
Read	TRGSEL	BEGIN	0		TRG			
Write								
Reset	0	1	0	0	0	0	0	0

DBG_T field descriptions

Field	Description
7 TRGSEL	Trigger Selection Bit The TRGSEL bit controls the triggering condition for the comparators. 0 Trigger on any compare address access. 1 Trigger if opcode at compare address is execute.
6 BEGIN	Begin/End Trigger Bit The BEGIN bit controls whether the trigger begins or ends storing of data in FIFO. 0 Trigger at end of stored data. 1 Trigger before storing data.
5–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
TRG	Trigger Mode Bits The TRG bits select the trigger mode of the DBG module. 0000 A only. 0001 A or B. 0010 A then B. 0011 Event only B. 0100 A then event only B. 0101 A and B (full mode). 0110 A and not B (full mode). 0111 Inside range. 1000 Outside range. 1001-1111 No trigger.

24.3.15 Debug Status Register (DBG_S)

NOTE

The figure shows the values in POR or non-end-run reset. The bits of AF, BF and CF are undefined and ARMF is reset to 0 in end-run reset. In the case of an end-trace to reset where DBGEN=1 and BEGIN=0, ARMF gets cleared by reset but AF, BF, and CF do not change after reset.

Address: 3010h base + Eh offset = 301Eh

Bit	7	6	5	4	3	2	1	0
Read	AF	BF	CF	0				ARMF
Write								
Reset	0	0	0	0	0	0	0	1

DBG_S field descriptions

Field	Description
7 AF	Trigger A Match Bit The AF bit indicates if Trigger A match condition was met since arming. 0 Comparator A did not match. 1 Comparator A match.
6 BF	Trigger B Match Bit The BF bit indicates if Trigger B match condition was met since arming. 0 Comparator B did not match. 1 Comparator B match.
5 CF	Trigger C Match Bit The CF bit indicates if Trigger C match condition was met since arming. 0 Comparator C did not match. 1 Comparator C match.
4–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 ARMF	Arm Flag Bit The ARMF bit indicates whether the debugger is waiting for trigger or waiting for the FIFO to fill. While DBGEN = 1, this status bit is a read-only image of the ARM bit in DBGC. 0 Debugger not armed. 1 Debugger armed.

24.3.16 Debug Count Status Register (DBG_CNT)

NOTE

All the bits in this register reset to 0 in POR or non-end-run reset. The bits are undefined in end-run reset. In the case of an end-trace to reset where DBGEN = 1 and BEGIN = 0, the CNT[3:0] bits do not change after reset.

Address: 3010h base + Fh offset = 301Fh

Bit	7	6	5	4	3	2	1	0
Read	0				CNT			
Write								
Reset	0	0	0	0	0	0	0	0

DBG_CNT field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CNT	FIFO Valid Count Bits The CNT bits indicate the amount of valid data stored in the FIFO. Table 1-20 shows the correlation between the CNT bits and the amount of valid data in FIFO. The CNT will stop after a count to eight even if more data is being stored in the FIFO. The CNT bits are cleared when the DBG module is armed, and the count is incremented each time a new word is captured into the FIFO. The host development system is responsible for checking the value in CNT[3:0] and reading the correct number of words from the FIFO because the count does not decrement as data is read out of the FIFO at the end of a trace run. 0000 No data valid. 0001 1 word valid. 0010 2 words valid. 0011 3 words valid. 0100 4 words valid. 0101 5 words valid. 0110 6 words valid. 0111 7 words valid. 1000 8 words valid.

24.4 Functional description

This section provides a complete functional description of the on-chip ICE system. The DBG module is enabled by setting the DBG_C[DBGEN] bit. Enabling the module allows the arming, triggering and storing of data in the FIFO. The DBG module is made up of three main blocks, the comparators, trigger break control logic and the FIFO.

24.4.1 Comparator

The DBG module contains three comparators, A, B, and C. Comparator A compares the core address bus with the address stored in the DBG_CAH and DBG_CAL registers. Comparator B compares the core address bus with the address stored in the DBG_CBH and DBG_CBL registers except in full mode, where it compares the data buses to the data stored in the DBG_CBL register. Comparator C compares the core address bus with the address stored in the DBG_CCH and DBG_CCL registers. Matches on comparators A, B, and C are signaled to the trigger break control (TBC) block.

24.4.1.1 RWA and RWAEN in full modes

In full modes ("A And B" and "A And Not B") DBG_CAX[RWAEN and DBG_CAX[RWA] are used to select read or write comparisons for both comparators A and B. To select write comparisons and the write data bus in Full Modes set DBG_CAX[RWAEN] = 1 and DBG_CAX[RWA] = 0, otherwise read comparisons and the read data bus will be selected. The DBG_CBX[RWBEN] and DBG_CBX[RWB] bits are not used and will be ignored in full modes.

24.4.1.2 Comparator C in loop1 capture mode

Normally comparator C is used as a third hardware breakpoint and is not involved in the trigger logic for the on-chip ICE system. In this mode, it compares the core address bus with the address stored in the DBG_CCX, DBG_CCH, and DBG_CCL registers. However, in loop1 capture mode, comparator C is managed by logic in the DBG module to track the address of the most recent change-of-flow event that was captured into the FIFO buffer. In loop1 capture mode, comparator C is not available for use as a normal hardware breakpoint.

When the DBG_C[ARM] and DBG_C[DBGEN] bits are set to one in loop1 capture mode, comparator C value registers are cleared to prevent the previous contents of these registers from interfering with the loop1 capture mode operation. When a COF event is detected, the address of the event is compared to the contents of the DBG_CCH and DBG_CCL registers to determine whether it is the same as the previous COF entry in the capture FIFO. If the values match, the capture is inhibited to prevent the FIFO from filling up with duplicate entries. If the values do not match, the COF event is captured into the FIFO and the DBG_CCH and DBG_CCL registers are updated to reflect the address of the captured COF event.

24.4.2 Breakpoints

A breakpoint request to the CPU at the end of a trace run can be created if the DBG_C[BRKEN] bit is set. The value of the DBG_T[BEGIN] bit determines when the breakpoint request to the CPU will occur. If the DBG_T[BEGIN] bit is set, begin-trigger is selected and the breakpoint request will not occur until the FIFO is filled with 8 words. If the DBG_T[BEGIN] bit is cleared, end-trigger is selected and the breakpoint request will occur immediately at the trigger cycle.

When traditional hardware breakpoints from comparators A or B are desired, set DBG_T[BEGIN] = 0 to select an end-trace run and set the trigger mode to either 0x0 (A-only) or 0x1 (A OR B) mode.

There are two types of breakpoint requests supported by the DBG module, tag-type and force-type. Tagged breakpoints are associated with opcode addresses and allow breaking just before a specific instruction executes. Force breakpoints are not associated with opcode addresses. The DBG_C[TAG] bit determines whether CPU breakpoint requests will be a tag-type or force-type breakpoints. When DBG_C[TAG] = 0, a force-type breakpoint is requested and it will take effect at the next instruction boundary after the request. When DBG_C[TAG] = 1, a tag-type breakpoint is registered into the instruction queue and the CPU will break if/when this tag reaches the head of the instruction queue and the tagged instruction is about to be executed.

24.4.2.1 Hardware breakpoints

Comparators A, B, and C can be used as three traditional hardware breakpoints whether the on-chip ICE real-time capture function is required or not. To use any breakpoint or trace run capture functions set DBG_C[DBGEN] = 1. DBG_C[BRKEN] and DBG_C[TAG] affect all three comparators. When DBG_C[BRKEN] = 0, no CPU breakpoints are enabled. When DBG_C[BRKEN] = 1, CPU breakpoints are enabled and the DBG_C[TAG] bit determines whether the breakpoints will be tag-type or force-type

breakpoints. To use comparators A and B as hardware breakpoints, set DBG_T = 0x81 for tag-type breakpoints and 0x01 for force-type breakpoints. This sets up an end-type trace with trigger mode "A OR B".

Comparator C is not involved in the trigger logic for the on-chip ICE system.

24.4.3 Trigger selection

The DBG_T[TRGSEL] bit is used to determine the triggering condition of the on-chip ICE system. DBG_T[TRGSEL] applies to both trigger A and B except in the event only trigger modes. By setting the DBG_T[TRGSEL] bit, the comparators will qualify a match with the output of opcode tracking logic. The opcode tracking logic is internal to each comparator and determines whether the CPU executed the opcode at the compare address. With the DBG_T[TRGSEL] bit cleared a comparator match is all that is necessary for a trigger condition to be met.

NOTE

If the DBG_T[TRGSEL] is set, the address stored in the comparator match address registers must be an opcode address for the trigger to occur.

24.4.4 Trigger break control (TBC)

The TBC is the main controller for the DBG module. Its function is to decide whether data should be stored in the FIFO based on the trigger mode and the match signals from the comparator. The TBC also determines whether a request to break the CPU should occur.

The DBG_C[TAG] bit controls whether CPU breakpoints are treated as tag-type or force-type breakpoints. The DBG_T[TRGSEL] bit controls whether a comparator A or B match is further qualified by opcode tracking logic. Each comparator has a separate circuit to track opcodes because the comparators could correspond to separate instructions that could be propagating through the instruction queue at the same time.

In end-type trace runs (DBG_T[BEGIN] = 0), when the comparator registers match, including the optional R/W match, this signal goes to the CPU break logic where DBG_C[BRKEN] determines whether a CPU break is requested and the DBG_C[TAG] control bit determines whether the CPU break will be a tag-type or force-type breakpoint. When DBG_T[TRGSEL] is set, the R/W qualified comparator match signal also passes through the opcode tracking logic. If/when it propagates through this logic, it will cause a

trigger to the ICE logic to begin or end capturing information into the FIFO. In the case of an end-type (DBG_T[BEGIN] = 0) trace run, the qualified comparator signal stops the FIFO from capturing any more information.

If a CPU breakpoint is also enabled, you would want DBG_C[TAG] and DBG_T[TRGSEL] to agree so that the CPU break occurs at the same place in the application program as the FIFO stopped capturing information. If DBG_T[TRGSEL] was 0 and DBG_C[TAG] was 1 in an end-type trace run, the FIFO would stop capturing as soon as the comparator address matched, but the CPU would continue running until a TAG signal could propagate through the CPUs instruction queue, which could take a long time in the case where changes of flow caused the instruction queue to be flushed. If DBG_T[TRGSEL] was one and DBG_C[TAG] was zero in an end-type trace run, the CPU would break before the comparator match signal could propagate through the opcode tracking logic to end the trace run.

In begin-type trace runs (DBG_T[BEGIN] = 1), the start of FIFO capturing is triggered by the qualified comparator signals, and the CPU breakpoint (if enabled by DBG_C[BRKEN]=1) is triggered when the FIFO becomes full. Since this FIFO full condition does not correspond to the execution of a tagged instruction, it would not make sense to use DBG_C[TAG] = 1 for a begin-type trace run.

24.4.4.1 Begin- and end-trigger

The definition of begin- and end-trigger as used in the DBG module are as follows:

- Begin-trigger: storage in FIFO occurs after the trigger and continues until 8 locations are filled.
- End-trigger: storage in FIFO occurs until the trigger with the least recent data falling out of the FIFO if more than 8 words are collected.

24.4.4.2 Arming the DBG module

Arming occurs by enabling the DBG module by setting the DBG_C[DBGEN] bit and by setting the DBG_C[ARM] bit. The DBG_C[ARM] and DBG_S[ARMF] bits are cleared when the trigger condition is met in end-trigger mode or when the FIFO is filled in begin-trigger mode. In the case of an end-trace where DBG_C[DBGEN] = 1 and DBG_T[BEGIN] = 0, DBG_C[ARM] and DBG_S[ARMF] are cleared by any reset to end the trace run that was in progress. The DBG_S[ARMF] bit is also cleared if DBG_C[ARM] is written to zero or when the DBG_C[DBGEN] bit is low. The TBC logic determines whether a trigger condition has been met based on the trigger mode and the trigger selection.

24.4.4.3 Trigger modes

The on-chip ICE system supports nine trigger modes. The trigger mode is used as a qualifier for either starting or ending the storing of data in the FIFO. When the match condition is met, the appropriate flag AF or BF is set in DBG_S register. Arming the DBG module clears the DBG_S[AF], DBG_S[BF], and DBG_S[CF] flags. In all trigger modes except for the event only modes change of flow addresses are stored in the FIFO. In the event only modes only the value on the data bus at the trigger event B comparator match address will be stored.

24.4.4.3.1 A only

In the A only trigger mode, if the match condition for A is met, the DBG_S[AF] flag is set.

24.4.4.3.2 A or B

In the A or B trigger mode, if the match condition for A or B is met, the corresponding flag(s) in the DBG_S register are set.

24.4.4.3.3 A then B

In the A then B trigger mode, the match condition for A must be met before the match condition for B is compared. When the match condition for A or B is met, the corresponding flag in the DBG_S register is set.

24.4.4.3.4 Event only B

In the event only B trigger mode, if the match condition for B is met, the DBG_S[BF] flag is set. The event only B trigger mode is considered a begin-trigger type and the DBG_T[BEGIN] bit is ignored.

24.4.4.3.5 A then event only B

In the A then event only B trigger mode, the match condition for A must be met before the match condition for B is compared. When the match condition for A or B is met, the corresponding flag in the DBG_S register is set. The A then event only B trigger mode is considered a begin-trigger type and the DBG_T[BEGIN] bit is ignored.

24.4.4.3.6 A and B (full mode)

In the A and B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and B trigger mode, if the match condition for A and B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only B happens, no flags are set.

For breakpoint tagging operation with an end-trigger type trace, only matches from comparator A will be used to determine if the Breakpoint conditions are met and comparator B matches will be ignored.

24.4.4.3.7 A and not B (full mode)

In the A and not B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and not B trigger mode, if the match condition for A and not B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only not B occur no flags are set.

For breakpoint tagging operation with an end-trigger type trace, only matches from comparator A will be used to determine if the breakpoint conditions are met and comparator B matches will be ignored.

24.4.4.3.8 Inside range, A ≤ address ≤ B

In the inside range trigger mode, if the match condition for A and B happen on the same bus cycle, both the DBG_S[AF] and DBG_S[BF] flags are set. If a match condition on only A or only B occur no flags are set.

24.4.4.3.9 Outside range, address < A or address > B

In the outside range trigger mode, if the match condition for A or B is met, the corresponding flag in the DBGS register is set.

The four control bits DBG_T[BEGIN] and DBG_T[TRGSEL], and DBG_C[BRKEN] and DBG_C[TAG], determine the basic type of debug run as shown in the following table. Some of the 16 possible combinations are not used (refer to the notes at the end of the table).

Table 24-1. Basic types of debug runs

BEGIN	TRGSEL	BRKEN	TAG	Type of debug run
0	0	0	x	Fill FIFO until trigger address (no CPU breakpoint - keep running)
0	0	1	0	Fill FIFO until trigger address, then force CPU breakpoint
0	0	1	1	Do not use
0	1	0	x	Fill FIFO until trigger opcode about to execute (no CPU breakpoint - keep running)
0	1	1	0	
0	1	1	1	Fill FIFO until trigger opcode about to execute (trigger causes CPU breakpoint)
1	0	0	x	Start FIFO at trigger address (No CPU breakpoint - keep running)
1	0	1	0	Start FIFO at trigger address, force CPU breakpoint when FIFO full
1	0	1	1	
1	1	0	x	Start FIFO at trigger opcode (No CPU breakpoint - keep running)
1	1	1	0	Start FIFO at trigger opcode, force CPU breakpoint when FIFO full
1	1	1	1	

24.4.5 FIFO

The FIFO is an eight word deep FIFO. In all trigger modes except for event only, the data stored in the FIFO will be change of flow addresses. In the event only trigger modes only the data bus value corresponding to the event is stored. In event only trigger modes, the high byte of the valid data from the FIFO will always read a 0x00.

24.4.5.1 Storing data in FIFO

In all trigger modes except for the event only modes, the address stored in the FIFO will be determined by the change of flow indicators from the core. The signal core_cof[1] indicates the current core address is the destination address of an indirect JSR or JMP instruction, or a RTS or RTI instruction or interrupt vector and the destination address should be stored. The signal core_cof[0] indicates that a conditional branch was taken and that the source address of the conditional branch should be stored.

24.4.5.2 Storing with begin-trigger

Storing with begin-trigger can be used in all trigger modes. Once the DBG module is enabled and armed in the begin-trigger mode, data is not stored in the FIFO until the trigger condition is met. Once the trigger condition is met the DBG module will remain armed until 8 words are stored in the FIFO. If the core_cof[1] signal becomes asserted, the current address is stored in the FIFO. If the core_cof[0] signal becomes asserted, the address registered during the previous last cycle is decremented by two and stored in the FIFO.

24.4.5.3 Storing with end-trigger

Storing with end-trigger cannot be used in event-only trigger modes. After the DBG module is enabled and armed in the end-trigger mode, data is stored in the FIFO until the trigger condition is met. If the core_cof[1] signal becomes asserted, the current address is stored in the FIFO. If the core_cof[0] signal becomes asserted, the address registered during the previous last cycle is decremented by two and stored in the FIFO. When the trigger condition is met, the DBG_C[ARM] and DBG_S[ARMF] will be cleared and no more data will be stored. In non-event only end-trigger modes, if the trigger is at a change of flow address the trigger event will be stored in the FIFO.

24.4.5.4 Reading data from FIFO

The data stored in the FIFO can be read using BDM commands provided the DBG module is enabled and not armed (DBG_C[DBGEN] = 1 and DBG_C[ARM] = 0). The FIFO data is read out first-in-first-out. By reading the DBG_CNT[CNT] bits at the end of a trace run, the number of valid words can be determined. The FIFO data is read by optionally reading the DBG_FH register followed by the DBG_FL register. Each time the DBG_FL register is read, the FIFO is shifted to allow reading of the next word, however, the count does not decrement. In event-only trigger modes where the FIFO will contain only the data bus values stored, to read the FIFO only DBG_FL needs to be accessed.

The FIFO is normally read only while DBG_C[ARM] = 0 and DBG_S[ARMF] = 0, however, reading the FIFO while the DBG module is armed will return the data value in the oldest location of the FIFO and the TBC will not allow the FIFO to shift. This action could cause a valid entry to be lost because the unexpected read blocked the FIFO advance.

If the DBG module is not armed and the DBG_FL register is read, the TBC will store the current opcode address. Through periodic reads of the DBG_FH and DBG_FL registers while the DBG module is not armed, host software can provide a histogram of program execution This is called profile mode.

24.4.6 Interrupt priority

When DBG_T[TRGSEL] is set and the DBG module is armed to trigger on begin- or end-trigger types, a trigger is not detected in the condition where a pending interrupt occurs at the same time that a target address reaches the top of the instruction pipe. In these conditions, the pending interrupt has higher priority and code execution switches to the interrupt service routine.

When DBG_T[TRGSEL] is clear and the DBG module is armed to trigger on end-trigger types, the trigger event is detected on a program fetch of the target address, even when an interrupt becomes pending on the same cycle. In these conditions, the pending interrupt has higher priority, the exception is processed by the core and the interrupt vector is fetched. Code execution is halted before the first instruction of the interrupt service routine is executed. In this scenario, the DBG module will have cleared DBG_C[ARM] without having recorded the change-of-flow that occurred as part of the interrupt exception. Note that the stack will hold the return addresses and can be used to reconstruct execution flow in this scenario.

When DBG_T[TRGSEL] is clear and the DBG module is armed to trigger on begin-trigger types, the trigger event is detected on a program fetch of the target address, even when an interrupt becomes pending on the same cycle. In this scenario, the FIFO captures

the change of flow event. Because the system is configured for begin-trigger, the DBG remains armed and does not break until the FIFO has been filled by subsequent change of flow events.

24.5 Resets

The DBG module cannot cause an MCU reset.

There are two different ways this module will respond to reset depending upon the conditions before the reset event. If the DBG module was setup for an end trace run with DBG_C[DBGEN] = 1 and DBG_T[BEGIN] = 0, DBG_C[ARM], DBG_S[ARMF], and DBG_C[BRKEN] are cleared but the reset function on most DBG control and status bits is overridden so a host development system can read out the results of the trace run after the MCU has been reset. In all other cases including POR, the DBG module controls are initialized to start a begin trace run starting from when the reset vector is fetched. The conditions for the default begin trace run are:

- DBG_CAX = 0x00, DBG_CAH=0xFF, DBG_CAL=0xFE so comparator A is set to match when the 16-bit CPU address 0xFFFE appears during the reset vector fetch
- DBG_C = 0xC0 to enable and arm the DBG module
- DBG_T = 0x40 to select a force-type trigger, a BEGIN trigger, and A-only trigger mode

Appendix A
Revision History

Table A-1. Changes between revision 3 and 2

Chapter	Description
Across the book	• Updated the 1 kHz OSC to 1 kHz LPO in the MCU block diagram. • Changed some OSC to XOSC to make them aligned in the whole book.
Device Overview	• Updated the figure of system clock distribution diagram, added FFCLK descriptions, updated ICSFFCLK descriptions and changed the ICSCLK to ICSOUT (BUSCLK) to make the clock names be aligned in the whole book in the System clock distribution.
Memory Map	• Updated the vector names of IRQ or Watchdog in the Reset and interrupt vector assignments. • In the Register addresses and bit assignments, updated ADC_RH, ADC_CVH in the table of Direct-page register allocation; updated I2C_C2 register in the table of High-page register allocation, added registers of NV_FTRIM and NV_ICSTRM, and changed FPH to FPHS in the table of Reserved flash memory addresses; added more details about ICS trim values and internal reference trim values; updated the conditions to disable security key. • Updated the access to NVM_FPROT and NVM_FOPT to be R/W; updated the note in the NVM_FSEC[SEC]
Chip Configuration	• Added ADC channel assignments. • Added a note to clarify that the TCLK in the chapter of 8-bit modulo timer (MTIM) is the FFCLK in the System clock distribution.
Interrupts	• Updated the vector names to the modules of KBI1, KBI0, FTM2, WDOG and IRQ in the Interrupt vectors, sources, and local masks. • Changed the section titles of Interrupt priority controller (IPC) and External interrupt request (IRQ) . • Removed the note in the Pin configuration options. • Changed the section titles of IRQ and IPC.
System control	• Changed the clock name of ICSCLK to ICSOUT to make it be aligned in the whole book. • Added SYS_SOPT1 register descriptions
Clock management	• Changed the clock name from ICSCLK to ICSOUT to make it be aligned in the whole book. • Updated ICS key features in the Internal clock source (ICS). • Updated Internal reference clock (ICSIRCLK). • Updated the examples in the Initializing FEI mode, Initializing FBI mode, Initializing FEE mode, Initializing FBE mode and Initializing external oscillator for peripherals. • Updated the feedback resistor to be R_F to align with that in the figure above in the External oscillator (XOSC). • Changed the access of ICS_S[LOLS] to be w1c and register to be R/W, updated the reset values of ICS_C3 and ICS_C4[SCFTRIM]; updated ICS_OSCSC[OSCSTEN] descriptions.
FlexTimer Module (FTM)	• Updated FTM_SC[CLKS] descriptions.

Table continues on the next page...

Table A-1. Changes between revision 3 and 2 (continued)

Chapter	Description
8-bit modulo timer (MTIM)	• Corrected the MTIM instances to be MTIM0 and MTIM1 in the Introduction.
Real-time counter (RTC)	• Corrected the annotation in the Initialization/application information. • Updated the figure in the RTC operation example.
8-Bit Serial Peripheral Interface (8-Bit SPI)	• Updated the access of SPI_S to be R/W, updated SPI_S[SPMF] access and descriptions.
16-Bit Serial Peripheral Interface (16-Bit SPI)	• Updated the access of SPI_S to be R/W, updated SPI_S[SPMF] access and descriptions.
Inter-Integrated Circuit (I2C)	• Updated I2C Max. speed in the Introduction. • Updated I2C_C2[4] descriptions. • Updated the note in the I2C divider and hold values.
Analog-to-digital converter (ADC)	• Updated the ADC block diagram. • Updated the External Signal Description. • Updated ADC_SC1[ADCH] descriptions to refer to ADC channel assignments for more details. • Updated ADC_RH and ADC_CVH • Updated the Automatic compare function. • Updated FADC FIFO structure diagram in the FIFO operation.
Touch Sense Input (TSI)	• Updated the TSI module block diagram in the Block diagram. • Updated Noise detection mode.
Watchdog (WDOG)	• Updated the access of WDOG_CNTH and WDOG_CNTL to be R/W.

Table A-2. Changes between revision 2 and 1

Chapter	Description
Memory map	• Corrected the register at 0x309F to SPI0_M
System control	• Corrected the description in $\overline{\text{RESET}}$ pin enable to "The SOPT1[RSTPE] bit must be set to enable the RESET function." • Updated SOPT1[RSTPE] descriptions
Parallel input/output	• Added cross-reference in the Introduction
Clock management	• Updated to clarify the trim value in Internal reference clock (ICSIRCLK) • Updated the examples in the Initializing FEI mode, Initializing FBI mode, Initializing FEE mode and Initializing FBE mode • Corrected ICS_C1[CLKS] • Added a note to the ICS_S[LOCK].
Chip configurations	• Corrected the description of "Convert the temperature sensor channel (AD22)" in the Temperature sensor. • Corrected FTM1 external signals in the FlexTimer module (FTM)
Real-time counter (RTC)	• Corrected to XOSC 32.768 kHz nominal in Features • Added a note to the RTC_CNTH, updated the descriptions of RTC_CNTH[CNTH]and RTC_CNTL[CNTL]. • Updated the example in the Initialization/application information
Serial communications interface (SCI)	• Corrected SCI receiver block diagram in the Block diagram • Added SCI signal descriptions • Added a note to the Transmitter functional description • Added new sections of Baud rate tolerance, Slow data tolerance, and Fast data tolerance • Updated Stop mode operation, Loop mode and Single-wire operation

Table continues on the next page...

Table A-2. Changes between revision 2 and 1 (continued)

Chapter	Description
Inter-Integrated Circuit (I2C)	• Updated the descriptions of I2C_F[ICR], I2C_S[TCF] • Polished Address matching • Updated Programmable input glitch filter • Updated the note in the Address matching wake-up • Updated Initialization/application information
Analog-to-digital converter (ADC)	• Corrected the AHDWT to the ADHWT in Block Diagram • Updated the ADC_SC2[1:0] to write 0 only. • Added a note to the ADC_SC4[AFDEP]. • Corrected all the ADCSC1 to ADC_SC1, ADCRH to ADC_RH, ADCRL to ADC_RL to keep consistent with the registers name. • Updated descriptions in section of Functional description. • Added a note and updated the examples in the Pseudo-code example
Analog comparator (ACMP)	• Corrected ACMPF to ACF in the description of ACMP_CS[ACF]

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