# MC74VHCT08A

# Quad 2-Input AND Gate

The MC74VHCT08A is an advanced high speed CMOS 2−input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT08A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC}$ = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

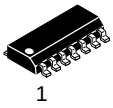
- High Speed: $t_{PD}$ = 4.3 ns (Typ) at $V_{CC}$ = 5 V
- Low Power Dissipation: $I_{CC}$ = 2 μA (Max) at $T_A$ = 25°C
- TTL−Compatible Inputs: $V_{IL}$ = 0.8 V; $V_{IH}$ = 2.0 V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V,
  Machine Model; > 200 V
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

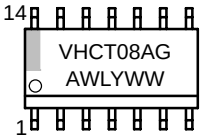
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**MARKING DIAGRAMS**



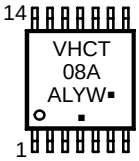

**SOIC−14**
**D SUFFIX**
**CASE 751A**

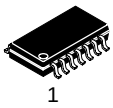




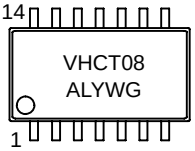


**TSSOP−14**
**DT SUFFIX**
**CASE 948G**




**SOEIAJ−14**
**M SUFFIX**
**CASE 965**




| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y, YY | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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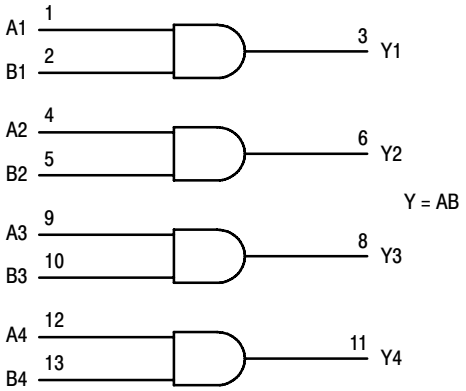



**Figure 1. Logic Diagram**

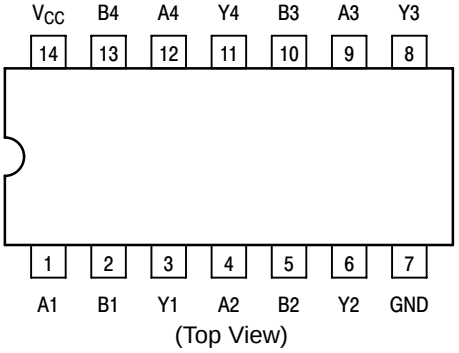



**Figure 2. Pinout: 14−Lead Packages**

**FUNCTION TABLE**

| Inputs | | Output |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

**MAXIMUM RATINGS***

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | –0.5 to +7.0 | V |
| DC Input Voltage | $V_{in}$ | –0.5 to +7.0 | V |
| DC Output Voltage | $V_{out}$ | –0.5 to $V_{CC}$ +0.5 | V |
| Input Diode Current | $I_{IK}$ | −20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current, per Pin | $I_{out}$ | ±25 | mA |
| DC Supply Current, $V_{CC}$ and GND Pins | $I_{CC}$ | ±50 | mA |
| Power Dissipation in Still Air, SOIC Packages† TSSOP Package† | $P_D$ | 500 450 | mW |
| Storage Temperature | $T_{stg}$ | –65 to +150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute−maximum−rated conditions is not implied.

†Derating − SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| DC Input Voltage | $V_{in}$ | 0 | 5.5 | V |
| DC Output Voltage | $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature | $T_A$ | −40 | + 85 | °C |
| Input Rise and Fall Time $V_{CC}$ = 5.0 V ±0.5 V | $t_r$, $t_f$ | 0 | 20 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Parameter | Test Conditions | Symbol | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A \le$ 85°C | | $T_A \le$ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| Minimum High−Level Input Voltage | | $V_{IH}$ | 3.0<br>4.5<br>5.5 | 1.2<br>2.0<br>2.0 | | | 1.2<br>2.0<br>2.0 | | 1.2<br>2.0<br>2.0 | | V |
| Maximum Low−Level Input Voltage | | $V_{IL}$ | 3.0<br>4.5<br>5.5 | | | 0.53<br>0.8<br>0.8 | | 0.53<br>0.8<br>0.8 | | 0.53<br>0.8<br>0.8 | V |
| Minimum High−Level Output Voltage $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = − 50 μA | $V_{OH}$ | 3.0<br>4.5 | 2.9<br>4.4 | 3.0<br>4.5 | | 2.9<br>4.4 | | 2.9<br>4.4 | | V |
| | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA | | 3.0<br>4.5 | 2.58<br>3.94 | | | 2.48<br>3.80 | | 2.34<br>3.66 | | |
| Maximum Low−Level Output Voltage $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | $V_{OL}$ | 3.0<br>4.5 | | 0.0<br>0.0 | 0.1<br>0.1 | | 0.1<br>0.1 | | 0.1<br>0.1 | V |
| | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | | 3.0<br>4.5 | | | 0.36<br>0.36 | | 0.44<br>0.44 | | 0.52<br>0.52 | |
| Maximum Input Leakage Current | $V_{IN}$ = 5.5 V or GND | $I_{IN}$ | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | $I_{CC}$ | 5.5 | | | 2.0 | | 20 | | 40 | μA |
| Quiescent Supply Current | Input: $V_{IN}$ = 3.4 V | $I_{CCT}$ | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| Output Leakage Current | $V_{OUT}$ = 5.5 V | $I_{OPD}$ | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r$ = $t_f$ = 3.0ns)

| Characteristic | Test Conditions | Symbol | $T_A$ = 25°C | | | $T_A \le$ 85°C | | $T_A \le$ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Max | Max | |
| Maximum Propagation Delay, Input A or B to Y | $V_{CC}$ = 3.0 ± 0.3V $C_L$ = 15 pF<br>$C_L$ = 50 pF | $t_{PLH}$,<br>$t_{PHL}$ | | 6.2<br>8.7 | 8.8<br>12.3 | | 10.5<br>14.0 | | 14.0<br>17.5 | ns |
| | $V_{CC}$ = 5.0 ± 0.5V $C_L$ = 15 pF<br>$C_L$ = 50 pF | | | 4.3<br>5.8 | 5.9<br>7.9 | | 7.0<br>9.0 | | 9.0<br>11.0 | |
| Maximum Input Capacitance | | $C_{in}$ | | 4 | 10 | | 10 | | 10 | pF |
| Power Dissipation Capacitance (Note 1) | | $C_{PD}$ | **Typical @ 25°C, $V_{CC}$ = 5.0V** | | | | | | | |
| | | | 20 | | | | | | | pF |

1. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.7

## NOISE CHARACTERISTICS (Input $t_r$ = $t_f$ = 3.0 ns, $C_L$ = 50pF, $V_{CC}$ = 5.0 V)

| Characteristic | Symbol | $T_A$ = 25°C | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| Quiet Output Maximum Dynamic $V_{OL}$ | $V_{OLP}$ | 0.3 | 0.8 | V |
| Quiet Output Minimum Dynamic $V_{OL}$ | $V_{OLV}$ | −0.3 | −0.8 | V |
| Minimum High Level Dynamic Input Voltage | $V_{IHD}$ | | 3.5 | V |
| Maximum Low Level Dynamic Input Voltage | $V_{ILD}$ | | 1.5 | V |

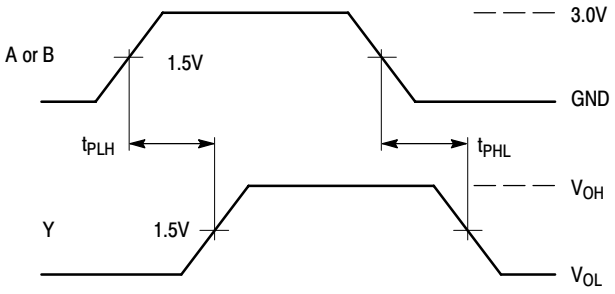
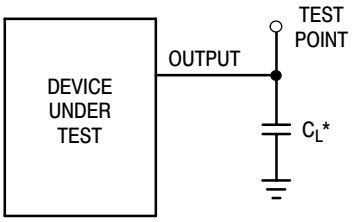



**Figure 3. Switching Waveforms**




*Includes all probe and jig capacitance

**Figure 4. Test Circuit**

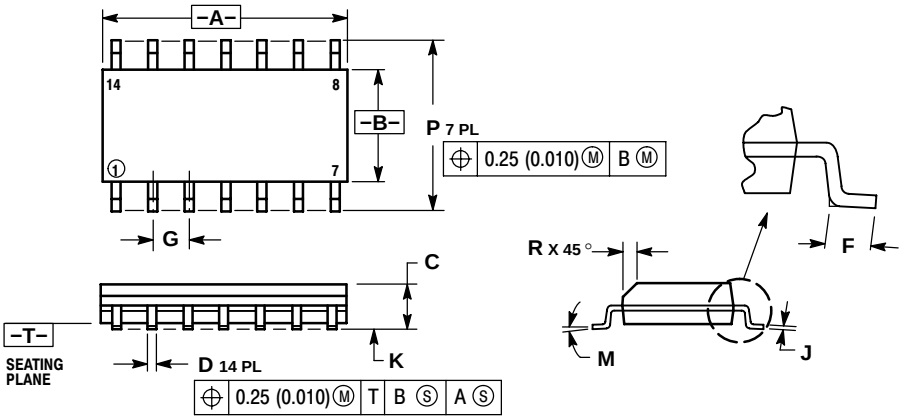
**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74VHCT08ADR2 | SOIC−14 | 2500 Units / Tape & Reel |
| MC74VHCT08ADR2G | SOIC−14 (Pb−Free) | |
| MC74VHCT08ADTR2 | TSSOP−14* | 2500 Units / Tape &Reel |
| MC74VHCT08ADTR2G | TSSOP−14* | |
| MC74VHCT08AM | SOEIAJ−14 | 50 Units / Rail |
| MC74VHCT08AMG | SOEIAJ−14 (Pb−Free) | |
| MC74VHCT08AMEL | SOEIAJ−14 | 2000 Units / Tape & Reel |
| MC74VHCT08AMELG | SOEIAJ−14 (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*These packages are inherently Pb−Free.

## PACKAGE DIMENSIONS

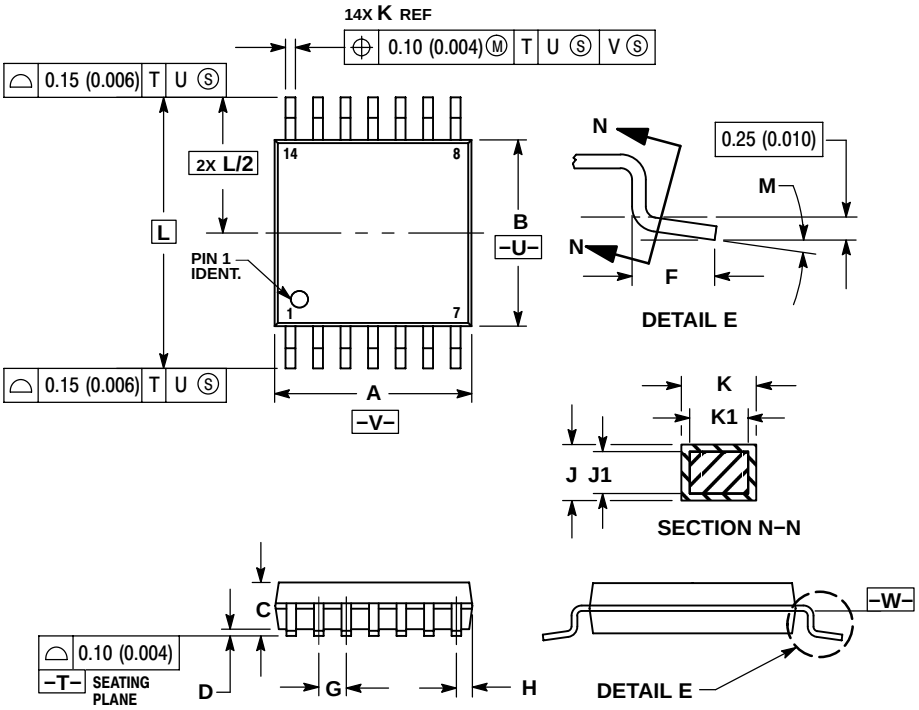
**SOIC−14**
**D SUFFIX**
CASE 751A−03
ISSUE G




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

**TSSOP−14**
CASE 948G−01
ISSUE A

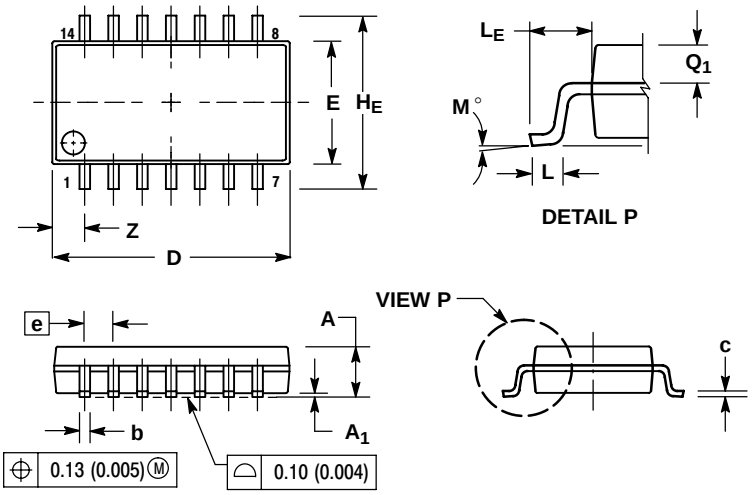



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## PACKAGE DIMENSIONS

**SOEIAJ−14**
CASE 965−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.004 | 0.008 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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