

Advance Information

Low-Voltage CMOS 16-Bit Latching Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16543 is a high performance, non-inverting 16-bit latching transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16543 inputs to be safely driven from 5V devices. The MC74LCX16543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the EAB LOW, the A-to-B Output Enable (OEAB) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal will latch the A latches, and the outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symmetric to that above, but uses the EBA, LEBA, and OEBA inputs.

- Designed for 2.7 to 3.6V V_{CC} Operation
- 5.2ns Maximum t_{pd}
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

MC74LCX16543

LCX

LOW-VOLTAGE CMOS 16-BIT LATCHING TRANSCEIVER



DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202-01

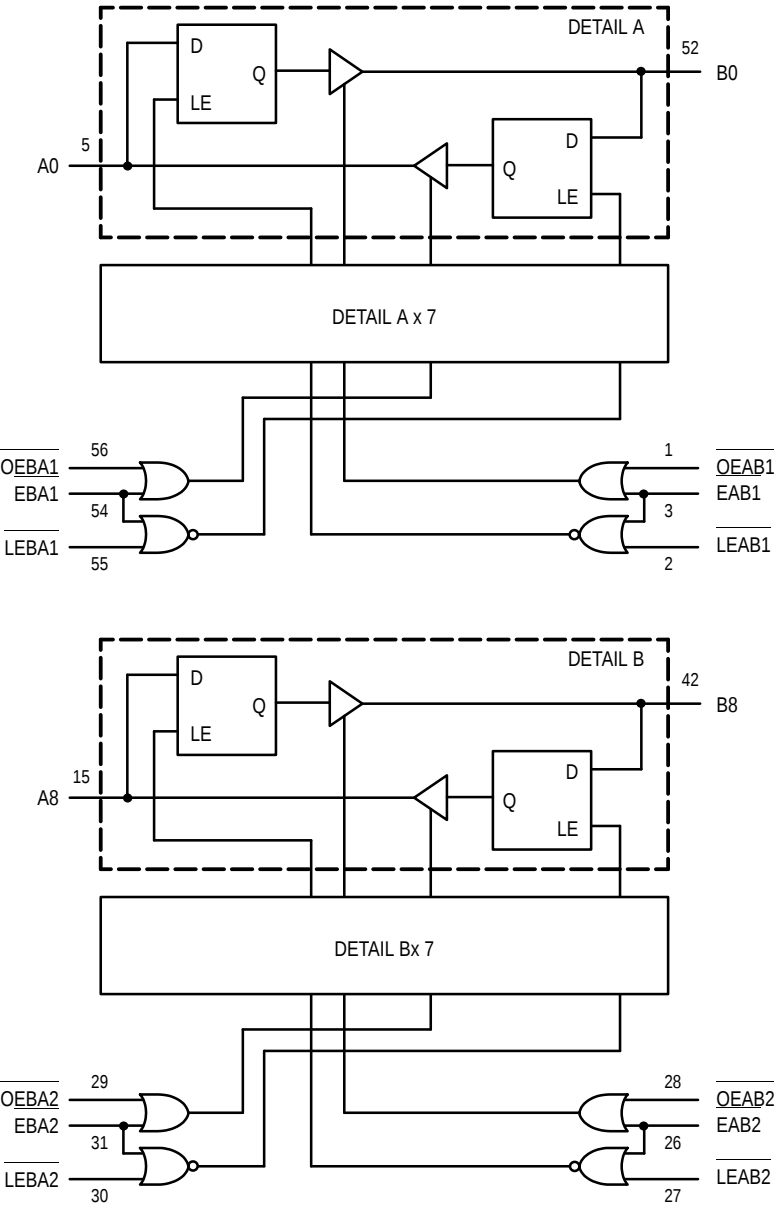
PIN NAMES

Pins	Function
<u>OExxn</u>	Output Enable Inputs
<u>Exxn</u>	Enable Inputs
<u>LExxn</u>	Latch Enable Inputs
A0–A15	3–State Inputs/Outputs
B0–B15	3–State Inputs/Outputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.



LOGIC DIAGRAM



Pinout: 56-Lead TSSOP
(Top View)

OEAB1	1	56	OEBA1
LEAB1	2	55	LEBA1
EAB1	3	54	EBA1
GND	4	53	GND
A0	5	52	B0
A1	6	51	B1
VCC	7	50	VCC
A2	8	49	B2
A3	9	48	B3
A4	10	47	B4
GND	11	46	GND
A5	12	45	B5
A6	13	44	B6
A7	14	43	B7
A8	15	42	B8
A9	16	41	B9
A10	17	40	B10
GND	18	39	GND
A11	19	38	B11
A12	20	37	B12
A13	21	36	B13
VCC	22	35	VCC
A14	23	34	B14
A15	24	33	B15
GND	25	32	GND
EAB2	26	31	EBA2
LEAB2	27	30	LEBA2
OEAB2	28	29	OEBA2

FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OEABn	OEBA n	EABn	EBA n	LEABn	LEBA n	An	Bn	
H	H					Input	Input	
		X	X	X	X	X	X	Disable Outputs
		L	L	L	L	X	X	Transparent Data; Outputs Disabled
				H	H	l h	l h	Latch and Outputs Disabled
L	H					Input	Output	
		H	X*	L	X	l h	Z Z	Load and B Outputs Disabled
				H	X	X	Z	Hold; B Outputs Disabled
		L	X*	L	X	L H	L H	Transparent A to B
				H	X	l h	L H	Latch and Display B Outputs
H	L					Output	Input	
		X*	H	X	L	Z Z	l h	Load and A Outputs Disabled
				X	H	Z	X	Hold; A Outputs Disabled
		X*	L	X	L	L H	L H	Transparent B to A
				X	H	L H	l h	Latch and Display A Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable or Enable Low-to-High Transition; X = Don't Care; * = The latches are not internally gated with the Output Enables. Therefore, data at the A or B ports may enter the latches at any time, provided that the LExx and Exx pins are set accordingly. For I_{CC} reasons, Do Not Float Inputs.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 ≤ V _I ≤ +7.0		V
V _O	DC Output Voltage	−0.5 ≤ V _O ≤ +7.0	Output in 3-State	V
		−0.5 ≤ V _O ≤ V _{CC} + 0.5	Note 1.	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	−65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3-State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, $V_{CC} = 3.0V - 3.6V$			-24	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 3.0V - 3.6V$			24	mA
I_{OH}	HIGH Level Output Current, $V_{CC} = 2.7V - 3.0V$			-12	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 2.7V - 3.0V$			12	mA
T_A	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, $V_{CC} = 3.0V$	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7V \leq V_{CC} \leq 3.6V$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7V \leq V_{CC} \leq 3.6V$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OH} = -100\mu A$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7V$; $I_{OH} = -12mA$	2.2		
		$V_{CC} = 3.0V$; $I_{OH} = -18mA$	2.4		
		$V_{CC} = 3.0V$; $I_{OH} = -24mA$	2.2		
V_{OL}	LOW Level Output Voltage	$2.7V \leq V_{CC} \leq 3.6V$; $I_{OL} = 100\mu A$		0.2	V
		$V_{CC} = 2.7V$; $I_{OL} = 12mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 16mA$		0.4	
		$V_{CC} = 3.0V$; $I_{OL} = 24mA$		0.55	
I_I	Input Leakage Current	$2.7V \leq V_{CC} \leq 3.6V$; $0V \leq V_I \leq 5.5V$		± 5.0	μA
I_{OZ}	3-State Output Current	$2.7 \leq V_{CC} \leq 3.6V$; $0V \leq V_O \leq 5.5V$; $V_I = V_{IH}$ or V_{IL}		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	$V_{CC} = 0V$; V_I or $V_O = 5.5V$		10	μA
I_{CC}	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6V$; $V_I = GND$ or V_{CC}		20	μA
		$2.7 \leq V_{CC} \leq 3.6V$; $3.6 \leq V_I$ or $V_O \leq 5.5V$		± 20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \leq V_{CC} \leq 3.6V$; $V_{IH} = V_{CC} - 0.6V$		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (Note 3.; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			T _A = −40°C to +85°C				
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V		
			Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay An to Bn or Bn to An	1	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns
t _{PLH} t _{PHL}	Propagation Delay LEBAn to An or LEABn to Bn	4	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA _n to An or OEAB _n to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEBA _n to An or OEAB _n to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t _{PZH} t _{PZL}	Output Enable Time EBA _n to An or EAB _n to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time EBA _n to An or EAB _n to Bn	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t _S	Setup Time, HIGH to LOW Data to LExxn	4	2.5		2.5		ns
t _H	Hold Time, HIGH to LOW Data to LExxn	4	1.5		1.5		ns
t _S	Setup Time, HIGH to LOW Data to Exxn	4	2.5		2.5		ns
t _H	Hold Time, HIGH to LOW Data to Exxn	4	1.5		1.5		ns
t _W	Latch Enable or Enable Pulse Width, LOW	4	3.0		3.0		ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 4.)			1.0 1.0			ns

3. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

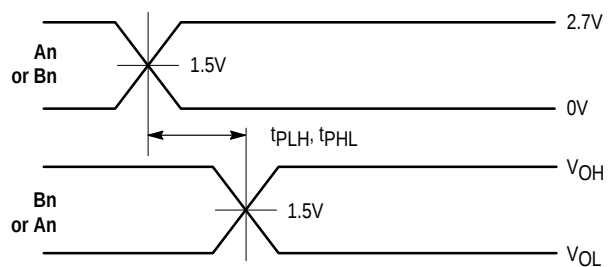
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 5.)	$V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$, $V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 5.)	$V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$, $V_{IH} = 3.3\text{V}$, $V_{IL} = 0\text{V}$		0.8		V

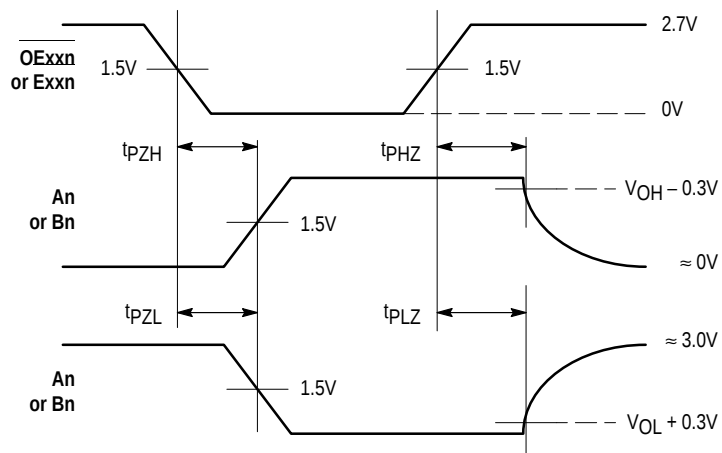
5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}$, $V_I = 0\text{V}$ or V_{CC}	20	pF

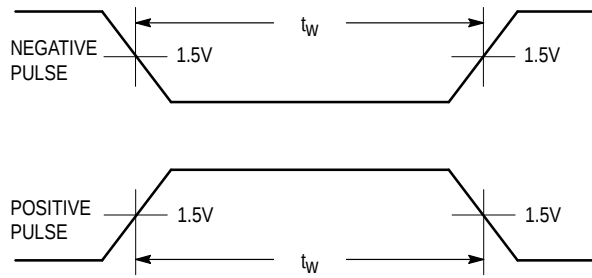


WAVEFORM 1 – A/B to B/A PROPAGATION DELAYS
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

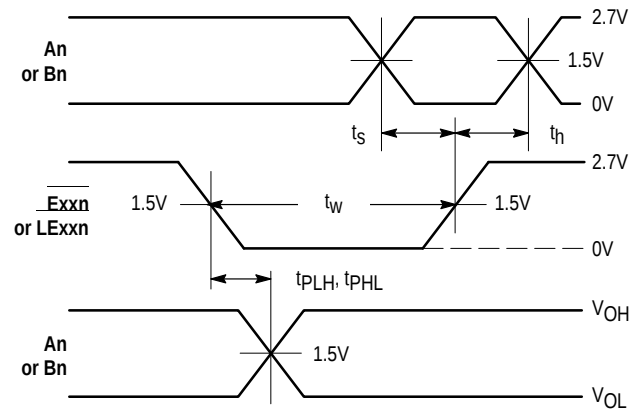


WAVEFORM 2 – OE_{xn}/Exx to A or B OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

Figure 1. AC Waveforms

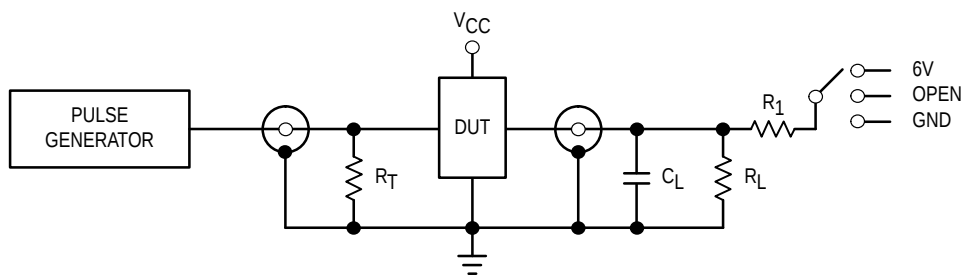


WAVEFORM 3 – INPUT PULSE DEFINITION
 $t_R = t_F = 2.5\text{ns}$, 10% to 90% of 0V to 2.7V



WAVEFORM 4 – Enable to A or B PROPAGATION DELAYS, Enable MINIMUM PULSE WIDTH, A or B to Enable SETUP AND HOLD TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted

Figure 2. AC Waveforms (continued)



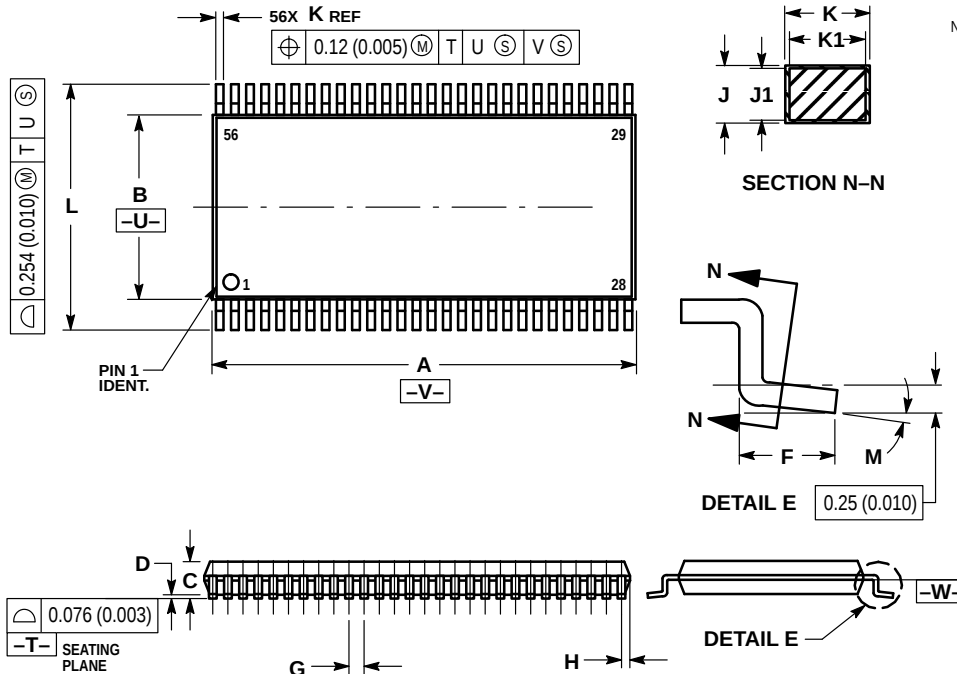
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH} , t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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