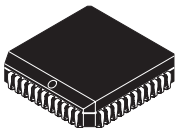
Document Number: MC34920
Rev. 2.0, 1/2007

2.8 Ω (Typ) Quad H-Bridge Motor Driver

34920

H-BRIDGE MOTOR DRIVERS



FN SUFFIX
EI SUFFIX (PB-FREE)
98ASB42598B
44-PIN PLCC

The 34920 is a multifunctional analog ASIC. The 34920 integrates two circuits, four H-bridge drivers, a reset circuit in a single IC, and two DC/DC switching voltage regulators. Input voltage is 21 V to 42 V DC.

Each motor of the two driver blocks can be configured as either a DC motor driver with pulse width modulation (PWM)-control or a single bipolar step motor driver. In step motor mode, both drivers are capable of being operated in the quarter step mode.

In DC motor mode, both bridges in a driver are in parallel, providing 2.4 A of drive current. In step motor mode, each bridge in a driver drives one phase. Each phase is driven with a bipolar current mode drive.

Features

- Individual Thermal Limit Protection
- User-Selectable Motors: 2 DC Motors (2.4 A/Motor), 2 Step Motors (W1-2 Phase Control), 1 DC Motor and 1 Step Motor
- 2 Buck Regulators (Switching @ 200 kHz)
- V_{V2} Output Voltage Is Programmable to 10 V to 15 V DC (Externally Set)
- Low-Voltage Detection Reset (V_{V1} and V_{VB+})
- Pb-Free Packaging Designated by Suffix Code EI

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC34920FN/R2	-40°C to 125°C	44 PLCC
MC34920EI/R2		

ADVANCE INFORMATION*

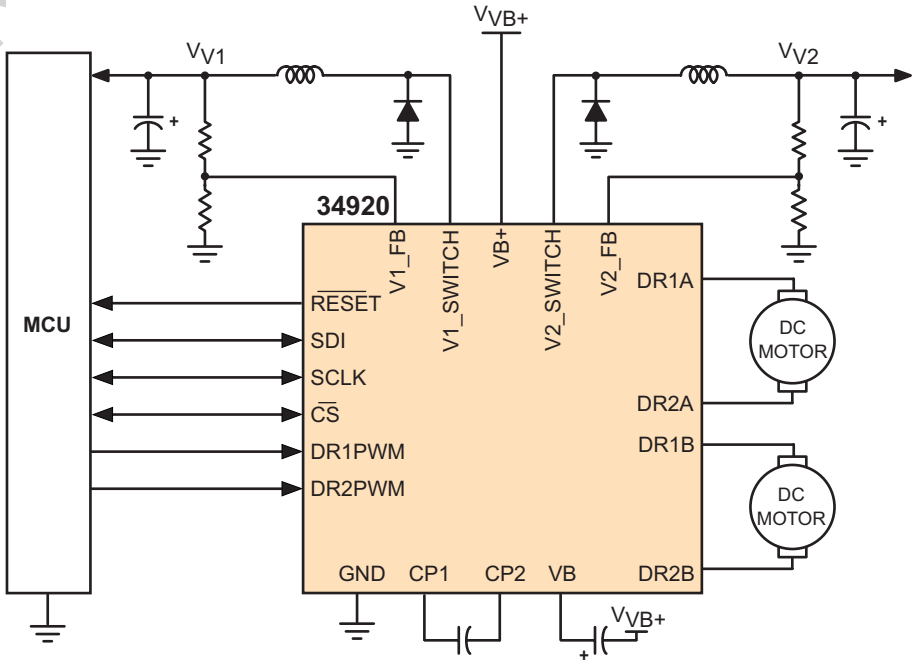


Figure 1. 34920 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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BLOCK DIAGRAM

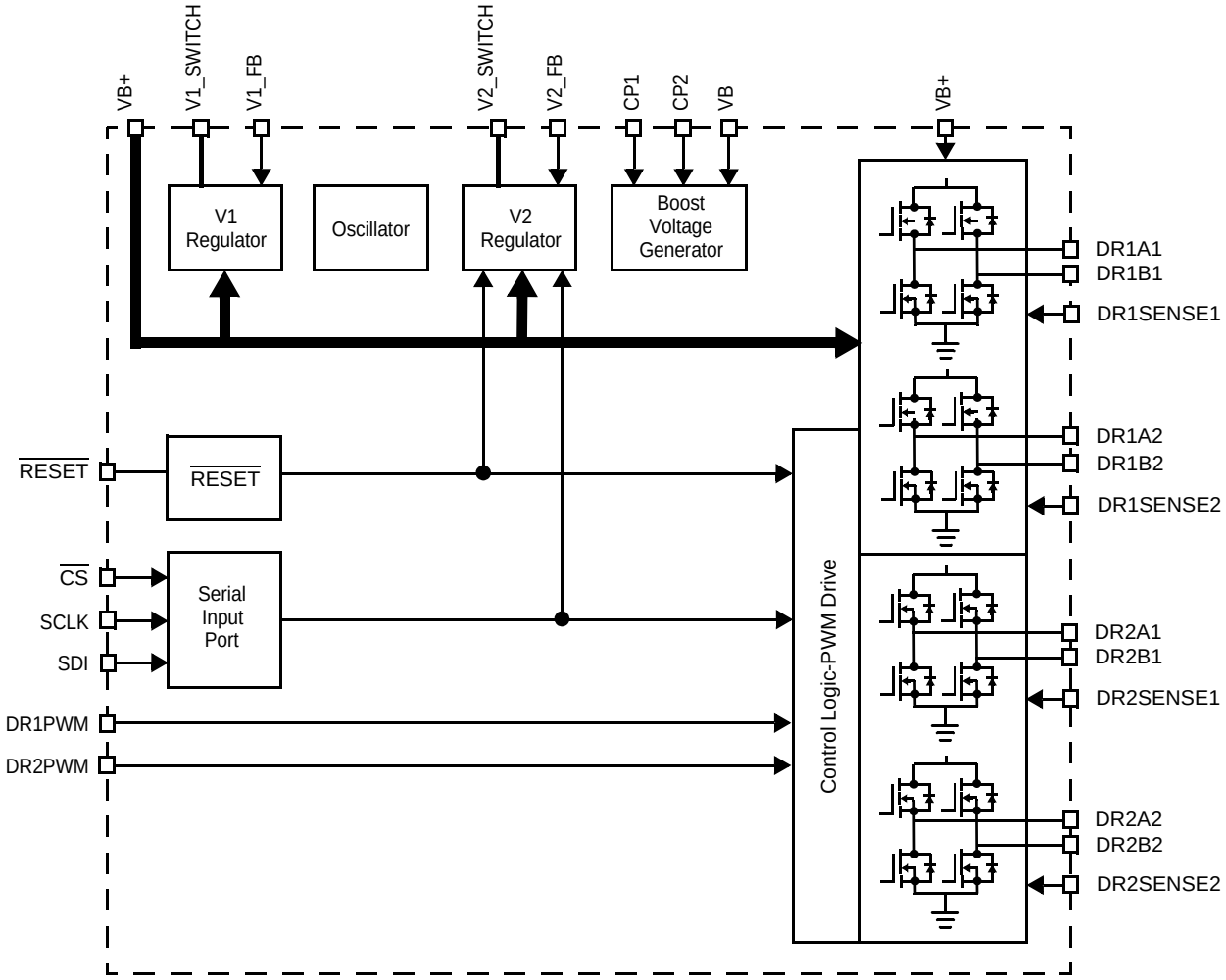


Figure 2. 34920 Simplified Internal Block Diagram

PIN CONNECTIONS

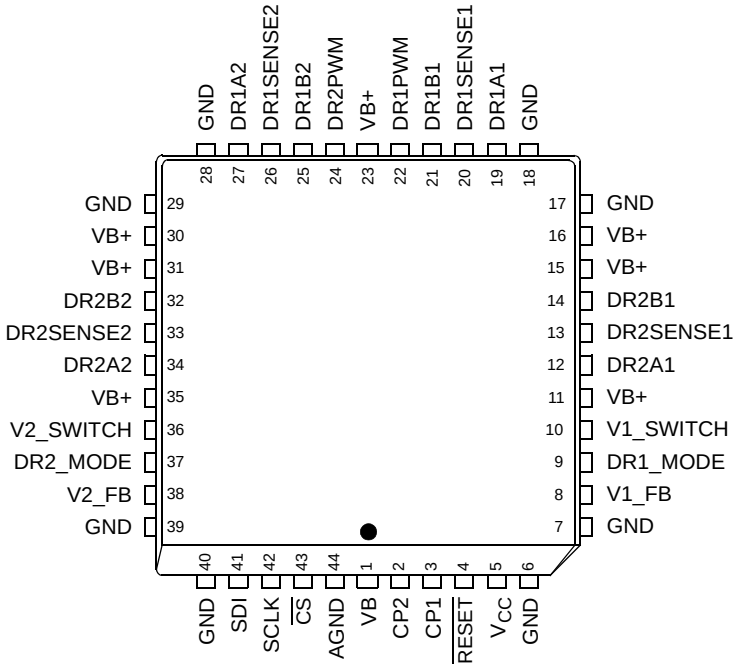


Figure 3. 34920 Pin Connections

Table 1. 34920 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1	VB	Output pin to V_{Vb}	Pin to connect to V_{Vb} capacitor.
2	CP2	Capacitor to CP1	Pin for boost generator switch capacitor.
3	CP1	Capacitor to CP2	Pin for boost generator switch capacitor.
4	RESET	Reset Output	Active low Reset output.
5	VCC	V_{CC} Supply Voltage	V_{CC} power input for internal use. The 34920 accepts either 3.3 V ±10% or 5.0 V ±5% for its logic voltage.
6, 7, 17, 18, 28, 29, 39, 40	GND	Substrate Ground	Ground connections for digital IC circuitry.
8	V1_FB	V1 Regulator Feedback Input	Voltage feedback for the V1 regulator.
9	DR1_MODE	Mode Select for Driver 1	Selects operational mode of Driver 1; Step = 1/DC = 0.
10	V1_SWITCH	Internal MOSFET Source for V1 Regulator	Switching output for V1 regulator.
11, 15, 16, 23, 30, 31, 35	VB+	VB+ (Bulk) Supply Voltage	High-voltage supply for motors and regulators.
12	DR2A1	Driver 2, Bridge 1, Output A	Motor driver output.
13	DR2SENSE1	Driver 2, Bridge 1, I Sense	Current sense for current mode.
14	DR2B1	Driver 2, Bridge 1, Output B	Motor driver output.
19	DR1A1	Driver 1, Bridge 1, Output A	Motor driver output.
20	DR1SENSE1	Driver 1, Bridge 1, I Sense	Current sense for current mode.

Table 1. 34920 Pin Definitions (continued)

Pin Number	Pin Name	Formal Name	Definition
21	DR1B1	Driver 1, Bridge 1, Output B	Motor driver output.
22	DR1PWM	Driver 1 PWM Input	PWM input for Driver 1. Used only when DR1_MODE pin = 0.
24	DR2PWM	Driver 2 PWM Input	PWM input for Driver 2. Used only when DR2_MODE pin = 0.
25	DR1B2	Driver 1, Bridge 2, Output B	Motor driver output.
26	DR1SENSE2	Driver 1, Bridge 2, I Sense	Current sense for current mode.
27	DR1A2	Driver 1, Bridge 2, Output A	Motor driver output.
32	DR2B2	Driver 2, Bridge 2, Output B	Motor driver output.
33	DR2SENSE2	Driver 2, Bridge 2, I Sense	Current sense for current mode.
34	DR2A2	Driver 2, Bridge 2, Output A	Motor driver output.
36	V2_SWITCH	Internal MOSFET Source for V2 Regulator	Switching output for V2 regulator.
37	DR2_MODE	Mode Select for Driver 2	Selects operational mode of Driver 2. Step = 1/ DC = 0.
38	V2_FB	V2 Regulator Feedback Input	Switch output for V2 regulator.
41	SDI	Serial Port Data Input	Serial input register serial data input.
42	SCLK	Serial Data Port Clock	Serial input register clock.
43	CS	Serial Data Port Chip Select	Serial input register chip select input. Active low.
44	AGND	Analog Ground	Ground connection for analog circuitry.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
VB+ Supply Voltage	V_{VB+}	45	V
VCC Voltage	$V_{CC(MAX)}$	7.0	V
Bridge Output Current	I_{OUT}	1.5	A
Maximum Voltage on $\overline{\text{RESET}}$ (1)	V_{MAXRST}	V_{CC} - 0.5	V
ESD Voltage (2) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±1000 ±100	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 175	°C
Operating Ambient Temperature	T_A	0 to 70	°C
Operating Junction Temperature	T_J	135	°C
Power Dissipation (T_A = 25° C) (3)	P_D	2.0	W
Pin Soldering Temperature (4)	T_{SOLDER}	220	°C
Thermal Resistance, Junction to Ambient (5)	$R_{\theta JA}$	37	°C/W

Notes

1. $\overline{\text{RESET}}$ is an open drain (open collector) output with an internal pull-up resistor.
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0pF).
3. Maximum power dissipation at indicated ambient temperature in free air with no heatsink used.
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. $R_{\theta JA}$ is dependent on customer application and PCB layout.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 21 V ≤ V_{VB+} ≤ 42 V, T_A = 10°C to 55°C, T_J max = 135°C, V_{CC} = 5.25 V max unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under typical conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
V_{VB+} Supply Voltage	V_{VB+}	21	–	42	V
V_{VB+} Standby Current V_{VB+} = 42 V, I_{CC} Load = 5.0 mA, No Serial Clock, No Motor Driver, No Load on V_{V2}	I_{VB+}	1.0	14	55	mA
CMOS LOGIC LEVEL (6)					
Input Current, High-Voltage State	I_{IH}	–	0.1	170	µA
Input Current, Low-Voltage State	I_{IL}	-170	-0.1	–	µA
Input Low Input Voltage State	V_{IL}				V
V_{CC} + 3.3 V ±10%		–	–	0.8	
V_{CC} + 5.0 V ±5%		–	–	1.5	
Input High-Voltage State	V_{IH}				V
V_{CC} + 3.3 V ±10%		2.1	–	–	
V_{CC} + 5.0 V ±5%		3.3	–	–	
V1 AND V2 VOLTAGE REGULATORS					
Regulator Output Voltage	V_{OUT}	-4.0%	Nom	+4.0%	V
Regulator Thermal Shutdown Junction Temperature	$T_{J(SHUTDOWN)}$	155	–	175	°C
Regulator Thermal Junction Temperature	$T_{J(ENABLE)}$	135	–	155	°C
Overcurrent Detect Level (Peak) for I_{V1_SWITCH}	I_{OC_V1}	1.5	2.0	2.5	A
Overcurrent Detect Level (Peak) for I_{V2_SWITCH}	I_{OC_V2}	2.5	3.25	4.0	A
Short Circuit Detect Level (Peak) for I_{V1_SWITCH} In Soft Start and Foldback Modes	I_{SC_V1}	0.75	1.25	1.75	A
Short Circuit Detect Level (Peak) for I_{V2_SWITCH} In Soft Start and Foldback Modes	I_{SC_V2}	1.75	2.25	2.75	A
V1 Switching MOSFET on Resistance Full On, Typical Value @ T_J = 25°C	$R_{DS(ON)V1}$	–	2.0	–	Ω
V2 Switching MOSFET on Resistance Full On, Typical Value @ T_J = 25°C	$R_{DS(ON)V2}$	–	0.75	–	Ω
Regulator Feedback Input Internal Reference Value of 2.50 V ±2%	V_{V1_FB}, V_{V2_FB}	–	2.5	–	V
Turn-Off Regulator V_{V1} Output/V_{V2} Output = 0 V	$VOFF_{V1_FB}$, $VOFF_{V2_FB}$	3.0	–	–	V

Notes

6. Applicable to all logic level input signals. Inputs are to be designed to accept 3.3 V logic levels and be +5.0 V tolerant.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 21 V ≤ V_{VB+} ≤ 42 V, T_A = 10°C to 55°C, T_J max = 135°C, V_{CC} = 5.25 V max unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under typical conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Overshoot External V_{CC} Load Current from 0.01 to 0.500 A, t_{RISE} > 100 ns	V_{OVRSHT}	–	5.0%	–	–
Load Ripple 0.5 A maximum	$V_{OUTRIPPLE}$	–	100	–	mV
VBOOST GENERATOR					
Charge Pump Output Voltage I_{LOAD} = 1.0 mA	V_{VB}-V_{VB+}	10	–	14	V
BIPOLAR CURRENT REGULATED STEP MOTOR DRIVE SYSTEM					
Peak Step Motor Current, Phase A or B Motor Not Stalled	$I_{STEPMOTOR\ PEAK}$	–	–	0.6	A
Maximum Allowable Voltage Drop Across Any H-Bridge Switch I_{LOAD} = 0.6 A (from Output to GND) or I_{LOAD} = 0.6 A (from V_{VB+} to Output)	V_{DROP}	–	–	1.6	V
Comparator High Threshold Voltage CURR_I0_PHASEX=0, CURR_I1_PHASEX=0	V_{TH}	450	550	650	mV
Comparator Medium Threshold Voltage CURR_I0_PHASEX=1, CURR_I1_PHASEX=0	V_{TM}	300	–	440	mV
Comparator Low Threshold Voltage CURR_I0_PHASEX=0, CURR_I1_PHASEX=1	V_{TL}	105	–	255	mV
V_OOFF Output Leakage Current for Step Motor Driver Outputs V_OOFF = 5.0 V	I_OOFF	-1.0	0.1	1.0	mA
Step Motor Driver Thermal Shutdown Junction Temperature	$T_{J(SHUTDOWN)}$	155	–	175	°C
Step Motor Driver Thermal Enable Junction Temperature	$T_{J(ENABLE)}$	135	–	155	°C
Single MOSFET Typical Value @ T_J = 25°C	$R_{DS(ON)}$	–	1.43	–	Ω
DC MOTOR DRIVE SYSTEM					
Maximum Allowable Voltage Drop Across Any H-Bridge Switch I_{LOAD} = 0.75 A (from Output to GND) or I_{LOAD} = 0.75 A (from V_{VB+} to Output) (Using 2 H-Bridges in Parallel)	V_{DROP}	–	–	1.3	V
Peak DC Motor Driver Current Motor Not Stalled (Using 2 H-Bridges in Parallel)	$I_{DCMOTOR\ PEAK\ CURRENT}$	–	–	1.2	A
DC Motor Overcurrent Threshold [7] Motor Stalled (Paralleled H-Bridges Used for DC Motor Drive)	$I_{DCMOTOR}$OCT	1.6	2.0	2.5	A
DC Motor Driver Sustaining Current Value Current Allowed to Sustain for a Minimum of 100 ms (OCT delay), Current Ripple 100 mA (Peak-to-Peak or Less)	$I_{DC_SUSTAIN}$	1.6	2.0	2.4	A

Notes

7. Because the current clamp is applied to the top H-bridge transistors only, overcurrent protection applies to motor currents. But note that no short circuit protection exists against shorts from the DC motor outputs (DR1A1, DR1A2, DR1B1, or DR1B2 to substrate ground or to VB+.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 21 V ≤ V_{VB+} ≤ 42 V, T_A = 10°C to 55°C, T_J max = 135°C, V_{CC} = 5.25 V max unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under typical conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Differential DC Motor Driver Output Voltage V_{VB+}+ Rising Monotonically from 0 V to 42 V (1.0 µs < t_R < 10 ms) OR V_{VB+} Falling Monotonically from 42 V to 0 V (1.0 µs < t_F < 10 ms)	V_{DCMD}	–	–	4.0	V
DC Motor Driver Thermal Shutdown Output Voltage I_{OH} = 0.1 V	V_{OH_DCM}	V_{VB+} - 0.5 V	–	–	V
DC Motor Driver Thermal Shutdown Junction Temperature	$T_{J(SHUTDOWN)}$	155	–	175	°C
DC Motor Driver Thermal Enable Junction Temperature	$T_{J(ENABLE)}$	135	–	155	°C
Equivalent Resistance Using 2 H-Bridges in Parallel, Nom Value @ T_J = 25°C	$R_{DS(ON)}$	–	0.73	–	Ω
$\overline{\text{RESET}}$					
$\overline{\text{RESET}}$ High-State Output Voltage I_{OH} = -0.1 mA	V_{OH}	V_{CC} - 0.5 V	–	–	V
$\overline{\text{RESET}}$ Low-State Output Voltage V_{V1_FB} < V_{V1T+}	V_{OL}	–	–	0.2	V
Input Low Voltage State V_{CC} + 3.3 V ±10% V_{CC} + 5.0 V ±5%	V_{IL}	– –	– –	0.8 1.5	V
Input High-Voltage State V_{CC} + 3.3 V ±10% V_{CC} + 5.0 V ±5%	V_{IH}	2.1 3.3	– –	– –	V
$\overline{\text{RESET}}$ V_{V1_FB} Low Threshold Voltage at V1_FB	V_{V1T-}	1.9	2.08	2.2	V
$\overline{\text{RESET}}$ V_{V1_FB} High Threshold Voltage at V1_FB	V_{V1T+}	2.05	2.23	2.35	V
$\overline{\text{RESET}}$ V_{VB+} Low Threshold VB+	V_{VB+T-}	13.5	15.4	16.5	V
$\overline{\text{RESET}}$ V_{VB+} High Threshold VB+	V_{VB+T+}	13.5	16.6	20	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 21 V ≤ V_{VB+} ≤ 42 V, T_A = 10°C to 55°C, T_J max = 135°C, V_{CC} = 5.25 V max unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under typical conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SERIAL INPUT PORT TIMING					
Serial Clock Frequency	f_{CLK}	–	4.0	12	MHz
SCLK High Width	t_{CLH}	41.667	125	–	ns
SCLK Low Width	t_{CLL}	41.667	125	–	ns
Delay $\overline{CS}$ Falling to First SCLK Rising	$t_{\overline{CS}\text{-}SCLK}$	83.333	250	–	ns
Delay Last SCLK Rising Edge to $\overline{CS}$ Rising	$t_{SCLK\text{-}\overline{CS}}$	83.333	250	–	ns
Data Valid to SCLK Set-Up Time	t_{DSU}	41.667	125	–	ns
Data Hold Time	t_{DHD}	41.667	125	–	ns
SDI Rise Time	t_{RD}	5.0	–	10	ns
SDI Fall Time	t_{FD}	5.0	–	10	ns
SCLK Rise/Fall Time	t_{RFC}	5.0	–	10	ns
$\overline{CS}$ Off-Time (t_{DHD} + t_{DSU})	$t_{NCS\text{-}OFF}$	83.333	250	–	ns
V1 AND V2 VOLTAGE REGULATORS					
Clock Frequency Overtemperature	f_{OP}	175	200	225	kHz
V1 Duty Cycle	V1_DC	35	37.5	40	%
V2 Duty Cycle	V2_DC	80	82.5	85	%
BIPOLAR CURRENT REGULATED STEP MOTOR DRIVE SYSTEM					
Shoot-Through Delay	t_{DEAD}	15	200	350	ns
Off-Time	t_{OFF}	20	29	38	µs
Current Blanking Time	t_{BLANK}	300	–	750	ns
DC MOTOR DRIVE SYSTEM					
PWM Frequency T_A = 25°C	f_{PWM}	–	20	21	kHz
Shoot-Through Delay	t_{DEAD}	15	180	350	ns
Overcurrent Off-Time	t_{OC_OFF}	10	40	70	µs

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 21 V ≤ V_{VB+} ≤ 42 V, T_A = 10°C to 55°C, T_J max = 135°C, V_{CC} = 5.25 V max unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under typical conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$					
$\overline{\text{RESET}}$ Delay $V_{V1_FB} \geq V_{V1T+}$	t_{DELAY}	15	33	50	ms
V_{CC} Out-of-Tolerance Persistence Time $\overline{\text{RESET}}$ De-Asserted, $V_{V1_FB} < V_{V1T-}$	$t_{PERSIST}$	10	20	30	µs
$\overline{\text{RESET}}$ Rise Time 10% to 90% (8)	t_R	–	630	750	ns
$\overline{\text{RESET}}$ Fall Time 90% to 10% (8)	t_F	–	11	50	ns

Notes

8. Test circuit is 50 pF capacitor from $\overline{\text{RESET}}$ to GND.

TIMING DIAGRAMS

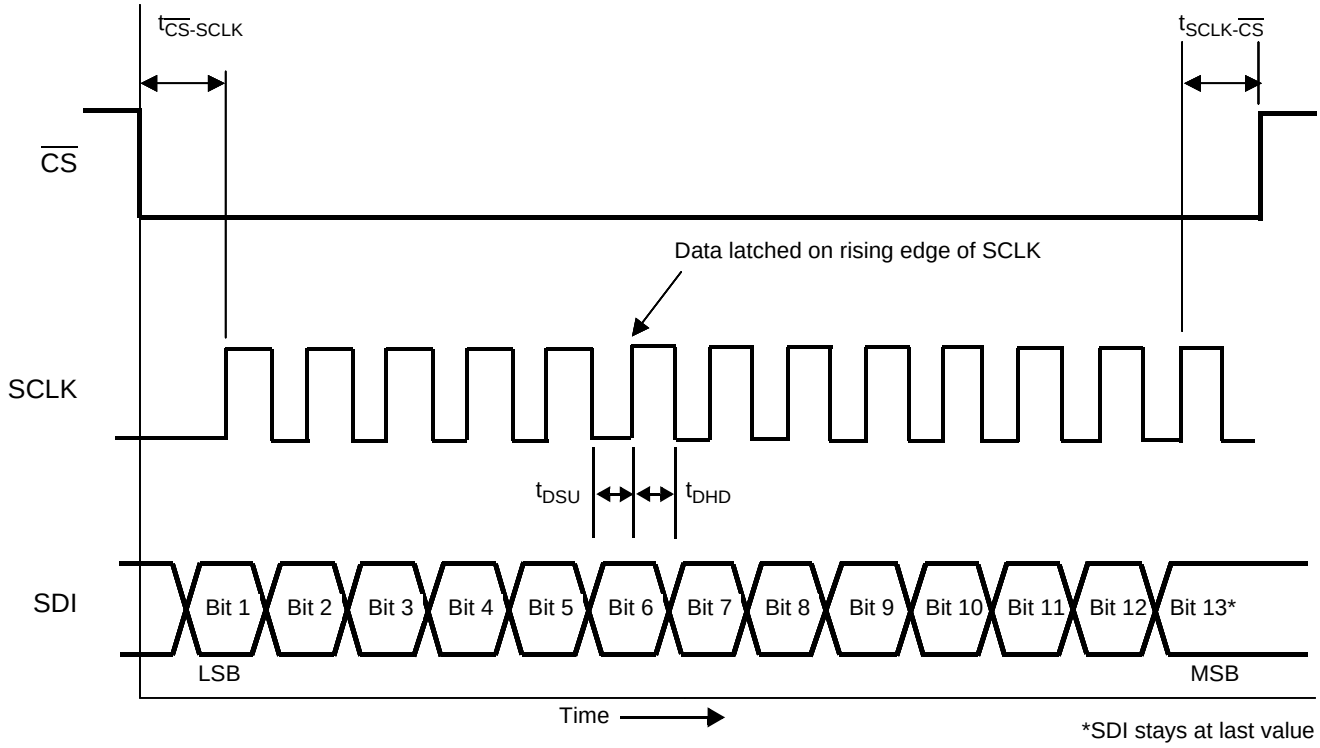


Figure 4. Serial Connectivity Diagram

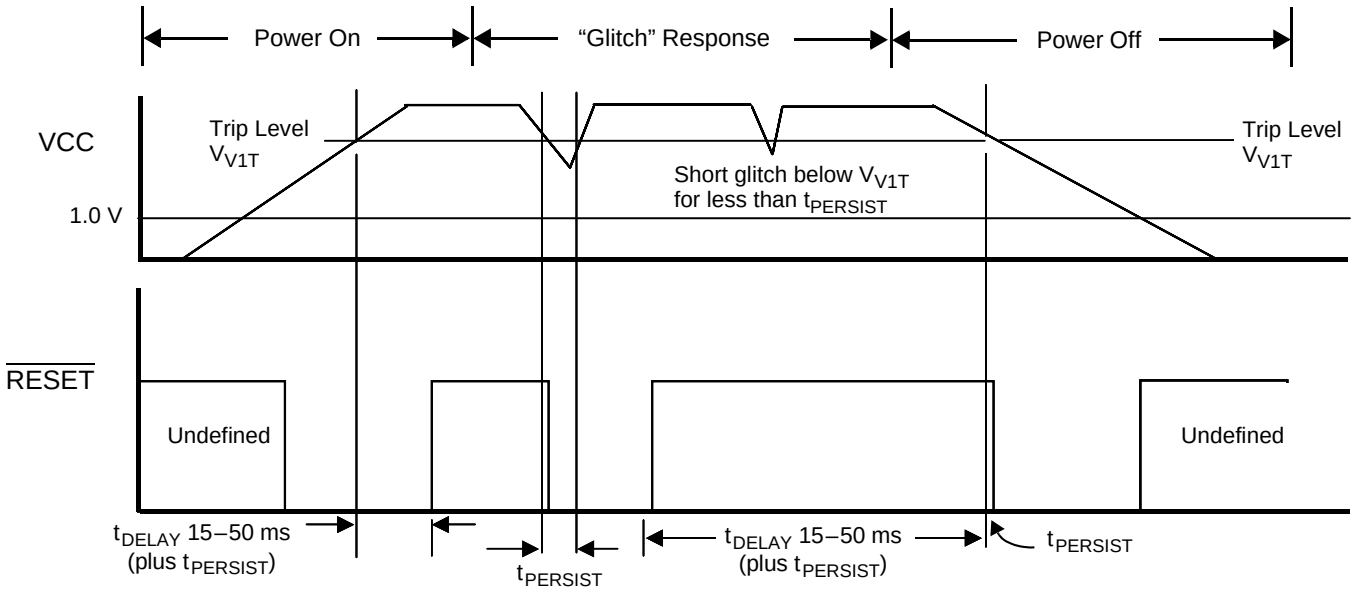


Figure 5. $\overline{\text{RESET}}$ Generation Timing Diagram (Assumes $V_{VB+} > V_{VB+T+}$ During Entire Period)

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34920 is a multifunctional analog IC that can be used in printer and scanner applications. It integrates two switching voltage regulator circuits, four H-bridge drivers, and a reset circuit in a single IC. All 34920 control lines are compatible with CMOS type 3.3 V and 5.0 V logic.

SWITCHING VOLTAGE REGULATOR CIRCUITS

Two switching voltage regulators provide the following voltages from an unregulated input of 21 V to 42 V DC. Both are buck-type switching regulators using a MOSFET (internal to the 34920), current sense resistor (internal to the 34920), Schottky diode (external to the 34920), external inductor, and filter capacitor.

- V1 Voltage Regulator – This regulator is programmable, has a duty cycle of 37%, and provides either 3.3 V (+5%/-4%) or 5.0 V (+5%/-4%) at a current of 10 mA (minimum) to 500 mA (maximum).
- V2 Voltage Regulator – This regulator has a programmable output voltage (by means of an external resistor divider network) in the range of 10 V to 15 V ±2% with a VB+ supply voltage range of 21 V to 42 V.

The V2 voltage regulator is controlled by an Enable bit in the serial register that allows software to turn this regulator on and off. However, the Enable bit does not effect the V1 voltage regulator. The Enable bit will disable the V2 voltage regulator and disable all motor driver circuits.

MOTOR DRIVERS

The two motor drivers can be selectable as either a bi-directional DC motor driver, with PWM control and peak currents of 2.4 A, or a bipolar step motor driver, with average current levels of 183 mA and 550 mA per phase, and quarter step mode capability. In step mode, both drivers are capable of being operated in the quarter step mode.

$\overline{\text{RESET}}$ GENERATION

The 34920 provides an output, $\overline{\text{RESET}}$, that drives an external reset signal to the system microprocessor and/or the system digital logic IC. This signal is an active low logic level signal that is derived by monitoring the level of the VB+ and V1_FB pins.

When $\overline{\text{RESET}}$ is asserted, either internally or from an external source, all 34920 motor driver outputs will be in their inactive states, and the serial input port will be loaded with the reset value.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

INPUT POWER SUPPLY (V_{VB+})

The input voltage for the switching regulators and motor drivers. V_{VB+} has a voltage range of 21 V to 42 V.

CMOS LOGIC LEVEL

CMOS logic level specifications are described on page 6 of the Static Electrical Characteristics table.

34920 INPUT

Table 5, page 13, describes the 34920 input specifications.

SERIAL INPUT PORT

The 34920 provides a serial input port for bit depth of 13 bits of input. This port provides an interface between the 34920 and the digital controller IC. This port is write-only. The interface consists of three signal lines: chip select ($\overline{\text{CS}}$, active low), serial clock (SCLK), and serial data input (SDI).

The digital controller initiates a serial transfer by pulling low the chip select line ($\overline{\text{CS}}$). It then generates 13 clock pulses on the SCLK pin while presenting the serial data on the serial data input (SDI). The 34920 presents the data on SDI one setup time (t_{DSU}) before the rising edge of SCLK. The data is held constant for the data hold time (t_{DHD}) beyond the SCLK rising edge. The data is shifted into the 34920 on the rising edge of SCLK. The least significant bit (LSB) is the first to be shifted out of the 34920 on the rising edge of SCLK, followed by the remaining bits to the last of the 13 bits, which is the most significant bit (MSB). The $\overline{\text{CS}}$ line is then returned to a high state. The low-to-high transition of $\overline{\text{CS}}$ will load the data into the internal 34920 input register, where all the inputs are presented to their appropriate functions in a parallel fashion.

Note The minimum off-time ($\overline{\text{CS}}$ signal equal to logic [1]) for the $\overline{\text{CS}}$ signal needs to be at least 1.0 t_{DSU} delay + 1.0 t_{DHD} delay. This will provide the time for the 34920 to clear the serial input data register (transfer the serial data in parallel to internal latches that use the data) and thereby avoid a data overrun condition and loss of data. See the serial input port timing data in the Dynamic Electrical Characteristics table, page 9.

Table 5. 34920 Input Specifications

Name	Description
V1_FB	Voltage feedback for the V1 regulator.
VCC	VCC power input for internal use. The 34920 accepts either 3.3 V ±10% or 5.0 V ±5% for its logic voltage.
V2_FB	Voltage feedback for the V2 regulator.
$\overline{CS}$	Serial input register chip select input. Active low.
SCLK	Serial input register clock.
SDI	Serial input register serial data input.
DRxPWM	PWM input for the DC motor driver for either Driver 1 or Driver 2.
DRx_MODE	Selects mode of each motor driver. Step = 1/DC = 0.
The following inputs are through the Serial Input Register	
V2_Enable	Enable bit to turn on and off the V2 regulator and the motor drivers. When low (= logic [0]), the V2 regulator and the motor drivers are turned off and the 34920 is placed in its lowest possible power state. V1 is not affected by the Enable bit.
DR1_CURR_I1_PHASEA	Second of two inputs that control the current level in the step motor Phase A winding (Driver 1/Step Mode).
DR1_CURR-I0_PHASEA	First of two inputs that control the current level in the step motor Phase A winding (Driver 1/Step Mode).
DR1_DIR_PH_A	Controls the direction of the current flow through Phase A of the step motor; i.e., logic [1] level causes conventional current flow from DR1A1 to DR1B1 (Driver 1/Step Mode).
DR1_CURR_I1_PHASEB	Second of two inputs that control the current level in the step motor Phase B winding (Driver 1/Step Mode).
DR1_CURR_I0_PHASEB	First of two inputs that control the current level in the step motor Phase B winding (Driver 1/Step Mode).
DR1_DIR_PH_B	Controls the direction of the current flow through Phase B of the step motor. A logic [1] level causes conventional current flow from DR1A2 to DR1B2 (Driver 1/Step Mode).
DR2_CURR_I1_PHASEA	Second of two inputs that control the current level in the step motor Phase A winding (Driver 2/Step Mode).
DR2_CURR_I0_PHASEA	One of two inputs that control the current level in the step motor Phase A winding (Driver 2/Step Mode).
DR2_DIR_PH_A	Controls the direction of the current flow through Phase A of the step motor. A logic [1] level causes conventional current flow from DR2A1 to DR2B1 (Driver 2/Step Mode).
DR2_CURR_I1_PHASEB	Second of two inputs that control the current level in the step motor Phase B winding (Driver 2/Step Mode).
DR2_CURR_I0_PHASEB	One of two inputs that control the current level in the step motor Phase B winding (Driver 2/Step Mode).
DR2_DIR_PH_B	Controls the direction of the current flow through Phase B of the step motor. A logic [1] level causes conventional current flow from DR2A2 to DR2B2 (Driver 2/Step Mode).

SERIAL INPUT PORT BIT DEFINITIONS

Tables 6 through 9 define the bit definitions as they apply to the 13 bits of input that are brought into the 34920 through the serial input port. These signals are listed in bit order from LSB (first bit to be shifted in) to MSB (last bit to be shifted in).

Table 6. Serial Input Port Definition for Step/Step Mode

Name	Bit	Reset Value	Description
V2_Enable	1	1	Enable bit to turn on and off the V2 regulator and the motor drivers and place the 34920 in the minimum power consumption state.
SDR2_CURR_I1_PHASEB	2	1	Second of two inputs that control the current level in the SDR2 step motor Phase B winding.
SDR2_CURR_I0_PHASEB	3	1	One of two inputs that control the current level in the SDR2 step motor Phase B winding.
SDR2_DIR_PH_B	4	0	Controls the direction of the current flow through Phase B of the SDR2 step motor. A logic [1] level causes conventional current flow from PH_B+ (source) to PH_B- (sink).
SDR2_CURR_I1_PHASEA	5	1	Second of two inputs that control the current level in the SDR2 step motor Phase A winding.
SDR2_CURR_I0_PHASEA	6	1	One of two inputs that control the current level in the SDR2 step motor Phase A winding.
SDR2_DIR_PH_A	7	0	Controls the direction of the current flow through Phase A of the SDR2 step motor. A logic [1] level causes conventional current flow from PH_A+ (source) to PH_A- (sink).
SDR1_CURR_I1_PHASEB	8	1	Second of two inputs that control the current level in the SDR1 step motor Phase B winding.
SDR1_CURR_I0_PHASEB	9	1	One of two inputs that control the current level in the SDR1 step motor Phase B winding.
SDR1_DIR_PH_B	10	0	Controls the direction of the current flow through Phase B of the SDR1 step motor. A logic [1] level causes conventional current flow from PH_B+ (source) to PH_B- (sink).
SDR1_CURR_I1_PHASEA	11	1	Second of two inputs that control the current level in the SDR1 step motor Phase A winding.
SDR1_CURR_I0_PHASEA	12	1	One of two inputs that control the current level in the SDR1 step motor Phase A winding.
SDR1_DIR_PH_A	13	0	Controls the direction of the current flow through Phase A of the SDR1 step motor. A logic [1] level causes conventional current flow from PH_A+ (source) to PH_A- (sink).

Table 7. Serial Input Port Definition for DC Motor/DC Motor Mode [9]

Name	Bit	Reset Value	Description
V2_Enable	1	1	Enable bit to turn on and off the V2 regulator and the motor drivers and place the 34920 in the minimum power consumption state.
Not Used	2	X	Not used in this mode.
Not Used	3	X	Not used in this mode.
Not Used	4	X	Not used in this mode.
Not Used	5	X	Not used in this mode.
Not Used	6	X	Not used in this mode.
DR2_DIR_DCM	7	0	Controls the direction of the current flow through the DC motor. A logic [1] level causes conventional current flow from DR2A1 (source)/DR2A2 (source) to DR2B1 (sink)/DR2B2 (sink).
Not Used	8	X	Not used in this mode.
Not Used	9	X	Not used in this mode.
Not Used	10	X	Not used in this mode.
Not Used	11	X	Not used in this mode.
Not Used	12	X	Not used in this mode.
DR1_DIR_DCM	13	0	Controls the direction of the current flow through the DC motor. A logic [1] level causes conventional current flow from DR1A1 (source)/DR1A2 (source) to DR1B1 (sink)/DR1B2 (sink).

Notes

9. DR1_MODE and DR2_MODE pins = logic [0] for DC motor drive for both drivers.

Table 8. Serial Input Port Definition for DR1=Step/DR2=DC Motor Mode

Name	Bit	Reset Value	Description
V2_Enable	1	1	Enable bit to turn on and off the V2 regulator and the motor drivers and place the 34920 in the minimum power consumption state.
Not Used	2	X	Not used in this mode.
Not Used	3	X	Not used in this mode.
Not Used	4	X	Not used in this mode.
Not Used	5	X	Not used in this mode.
Not Used	6	X	Not used in this mode.
DR2_DIR_DCM	7	0	Controls the direction of the current flow through the DC motor. A logic [1] level causes conventional current flow from DR2A1 (source)/DR2A2 (source) to DR2B1 (sink)/DR2B2 (sink).
SDR1_CURR_I1_PHASEB	8	1	Second of two inputs that control the current level in the SDR1DR1 step motor Phase B winding.
SDR1_CURR_I0_PHASEB	9	1	One of two inputs that control the current level in the SDR1 step motor Phase B winding.
SDR1_DIR_PH_B	10	1	Controls the direction of the current flow through Phase B of the SDR1 step motor. A logic [1] level causes conventional current flow from PH_B+ (source) to PH_B- (sink).
SDR1_CURR_I1_PHASEA	11	0	Second of two inputs that control the current level in the SDR1 step motor Phase A winding.
SDR1_CURR_I0_PHASE	12	1	One of two inputs that control the current level in the SDR1 step motor Phase A winding.
SDR1_DIR_PH_A	13	1	Controls the direction of the current flow through Phase A of the SDR1 step motor. A logic [1] level causes conventional current flow from PH_A+ (source) to PH_A- (sink).

Table 9. Serial Input Port Definition for DR1=DC Motor/DR2=Step Mode

Name	Bit	Reset Value	Description
V2_Enable	1	1	Enable bit to turn on and off the V2 regulator and the motor drivers and place the 34920 in the minimum power consumption state.
SDR2_CURR_I1_PHASEB	2	1	Second of two inputs that control the current level in the SDR2 step motor Phase B winding.
SDR2_CURR_I0_PHASEB	3	1	One of two inputs that control the current level in the SDR2 step motor Phase B winding.
SDR2_DIR_PH_B	4	0	Controls the direction of the current flow through Phase B of the SDR2 step motor. A logic [1] level causes conventional current flow from PH_B+ (source) to PH_B+ (sink).
SDR2_CURR_I1_PHASEA	5	1	Second of two inputs that control the current level in the SDR2 step motor Phase A winding.
SDR2_CURR_I0_PHASEA	6	1	One of two inputs that control the current level in the SDR2 step motor Phase A winding.
SDR2_DIR_PH_A	7	0	Controls the direction of the current flow through Phase A of the SDR2 step motor. A logic [1] level causes conventional current flow from PH_A+ (source) to PH_A- (sink).
Not Used	8	X	Not used in this mode.
Not Used	9	X	Not used in this mode.
Not Used	10	X	Not used in this mode.
Not Used	11	X	Not used in this mode.
Not Used	12	X	Not used in this mode.
DR1_DIR_DCM	13	0	Controls the direction of the current flow through the DC motor. A logic [1] level causes conventional current flow from DR1A1 (source)/DR1A2 (source) to DR1B1 (sink)/DR1B2 (sink).

VOLTAGE REGULATORS

The 34920 contains two switching voltage regulators (see Figure 6). Both are buck-type voltage regulators using an internal switching MOSFET. The V1 regulator provides either 3.3 V or 5.0 V at +5%/-4% tolerance. The V2 regulator's output voltage, V_{V2}, is programmable through the use of an external resistor divider network. The voltage tolerance on the V_{V2} output is ±2% of the nominal voltage set point. The switching frequency of the V1 and V2 regulators is approximately 200 kHz.

The V1 and V2 regulators are designed with a dual-mode current limit circuit. The current limit threshold is lowered during the power-on period to allow for a softer start-up, thereby reducing electrical stress in the external components.

V_{VB+}, the input voltage for the switching voltage regulators, ranges from 21 V to 42 V. To minimize the ripple current on V_{VB+}, the V1 regulator and the V2 regulator switch out of phase.

A boost voltage generator (VB generator), which acts as a single-stage charge pump, provides gate drive voltage for the switching regulators. It uses an external capacitor to store the charge.

Output voltages V_{V1} and V_{V2} are set externally with a resistor (1% tolerance) divider network. Input voltages at V1_FB and V2_FB should be chosen to provide a feedback voltage, for the required output regulated voltage, to equal the internal regulator reference voltages of 2.5 V ±2%.

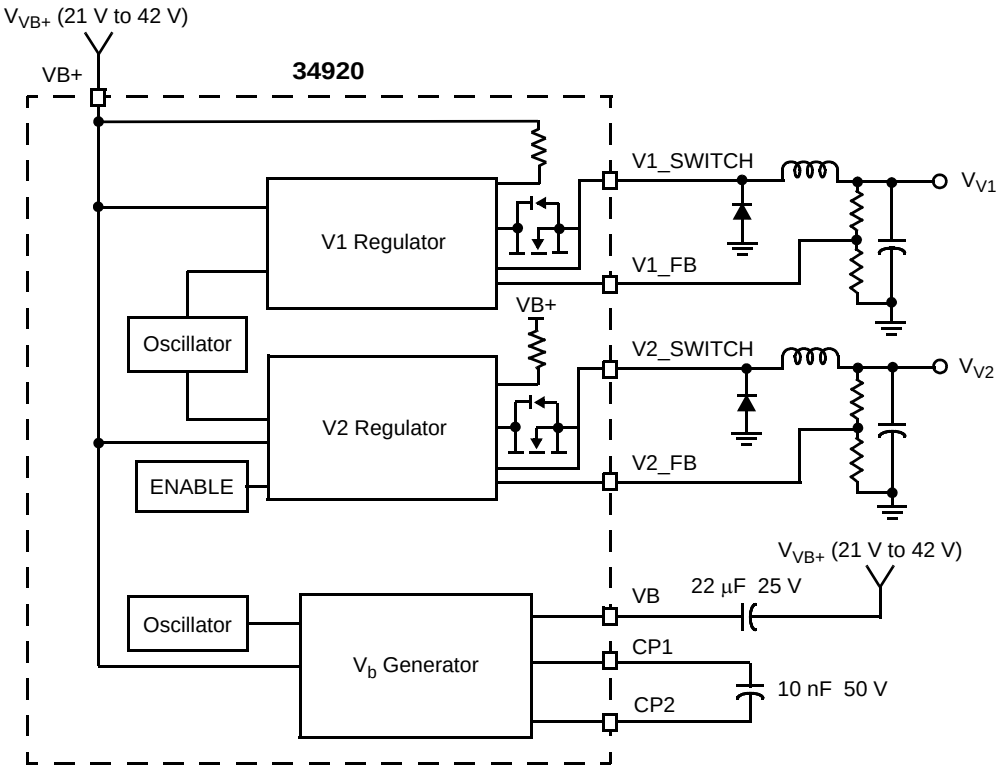


Figure 6. Voltage Regulator Functions

VOLTAGE REGULATOR OUTPUT REQUIREMENTS

Table 10 provides a listing of the output voltages and currents. Both switchmode converters operate at approximately 200 kHz ±25 kHz.

Table 10. Voltage Regulator Output Requirements

Voltage Name	Minimum Voltage	Maximum Voltage	Load Range
V_{V1}	-4.0% of Nominal	+4.0% of Nominal	10 mA Min, 500 mA Max DC
V_{V2} (10)	-2.0% of Nominal	+2.0% of Nominal	10 mA Min, 1.3 A Max DC (11)

Notes
10. This voltage is programmable within a range of 10 V to 15 V via external resistors. The voltage tolerance around any set point is ±2% of the nominal.
11. Maximum peak duration is 400 ms.

The V1 and V2 regulators provide individual internal over-temperature sensing for protection. During an overtemperature event, when the device T_J is at or above $T_{J(SHUTDOWN)}$, the internal thermal protection circuit disables the drive outputs by driving all outputs to the zero current state until the device temperatures have dropped below the lower thermal threshold temperature $T_{J(ENABLE)}$, at which time the driver is re-enabled.

The V1 and V2 voltage regulators may be shut down by applying a voltage in the range of 3.0 V to 6.0 V to the respective V1_FB and V2_FB pins. This will result in the regulator output voltages to be equal to 0 V.

OVERCURRENT PROTECTION

Output voltages V_{V1} and V_{V2} are short circuit protected. The outputs respond to an overcurrent situation by limiting the internal switching duty cycle. This can be reset by removing the main supply to the chip or when the short circuit condition is removed. Refer to the respective I_{OC} and I_{SC}

values for V1 and V2 voltage regulators on page 6 of the Static Electrical Characteristics table.

POWER-SAVING MODE OF OPERATION

The V2 voltage regulator can be disabled via the serial interface by setting the V2_Enable bit (bit 1–LSB) to a value of 0. This provides a reduction in the bias current provided by the V1 supply.

V1 VOLTAGE REGULATOR

Implementation of the V1 switching voltage regulator is accomplished through the use of an internal switch MOSFET, internal MOSFET current sense resistor, external Schottky diode, external inductor, and filter capacitor. The frequency of operation of this regulator is controlled by the internal clock, which is 200 kHz ±25 kHz. The duty cycle (on-time) for this internal regulator clock is a fixed 37.5%. This regulator switches out of phase from the V2 regulator to minimize ripple current on VB+. The line regulation range is 21 V < V_{VB+} < 42 V. The load side regulation is specified on page 6 of the Static Electrical Characteristics table.

This converter is designed so that the current limit threshold is lowered during the power-on period to allow for a “softer” start-up, thereby reducing electrical stress in the external components. This limiting is required for their safe operation.

The voltage is set externally with a resistor (1% tolerance) divider network. The V1_FB input voltage should be chosen, using external voltage divider resistors, so as to provide a regulator feedback voltage, for the required output regulated voltage, to equal the internal regulator reference voltage of 2.50 V ±2%. The V1 regulator is ideal for providing either 3.3 V or 5.0 V with a precision of +5%/-4%.

Output current sensing is implemented by sensing the voltage across an internal sense resistor connected between VB+ and the drain of the internal MOSFET. Current is measured on a cycle-by-cycle basis. The purpose of this current sense is to prevent damage to the 34920 and its associated external components.

V2 VOLTAGE REGULATOR

The V2 switching voltage regulator is implemented as a buck regulator with an internal switch MOSFET, internal MOSFET current sense resistor, external Schottky diode, external inductor, and filter capacitor. The frequency of operation of this regulator is controlled by the internal clock, which is 200 kHz ±25 kHz. This regulator switches out of phase from the V1 regulator to minimize ripple current on VB+.

This converter is designed so that the current limit threshold is lowered during the power-on period to allow for a “softer” start-up, thereby reducing electrical stress in the external components. This limiting is required for their safe operation.

The output voltage is variable with ±2% precision, with a V_{VB+} supply voltage range of 21 V to 42 V. The exact voltage will be set externally with a resistor (1% tolerance) divider network. The V2_FB input voltage should be chosen, using external voltage divider resistors, so as to provide a regulator feedback voltage, for the required output regulated voltage, to equal the internal regulator reference voltages of 2.50 V ±2%.

Output current sensing is implemented by sensing the voltage across an internal sense resistor connected between VB+ and the drain of the internal MOSFET. Current is measured on a cycle-by-cycle basis. The purpose of this current sense is to prevent damage to the 34920 and its associated external components.

Note There is a V2_Enable bit in the Serial Communication Input register (bit 1). When this bit is set to logic [1], the V2 voltage regulator is enabled. When this bit = logic [0], the V2 voltage regulator is disabled. Refer to Tables 5 through 9, pp. 13–17, for a description of this bit. The V2_Enable bit will also disable the motor drivers.

VB GENERATOR

The boost voltage generator circuit is a charge pump circuit using two external capacitors to provide the necessary voltage to drive internal 34920 loads. This circuit is driven at a frequency of 200 kHz ±25 kHz.

The VB generator is utilized exclusively by the 34920. There is no provision for external loading. Also, there is no disable feature for the VB generator.

MOTOR DRIVE SYSTEMS

The 34920 provides two motor drivers. Both drivers are mode selectable to be either a multi-current level bi-directional driver for bipolar step motors or a bi-directional DC motor driver with PWM control. The DR1_MODE (Mode1) and DR2_MODE (Mode2) pins select whether the appropriate motor driver will drive a step motor (pin = 1) or DC motor (pin = 0). Figures 7 and 8 depict the two motor configurations.

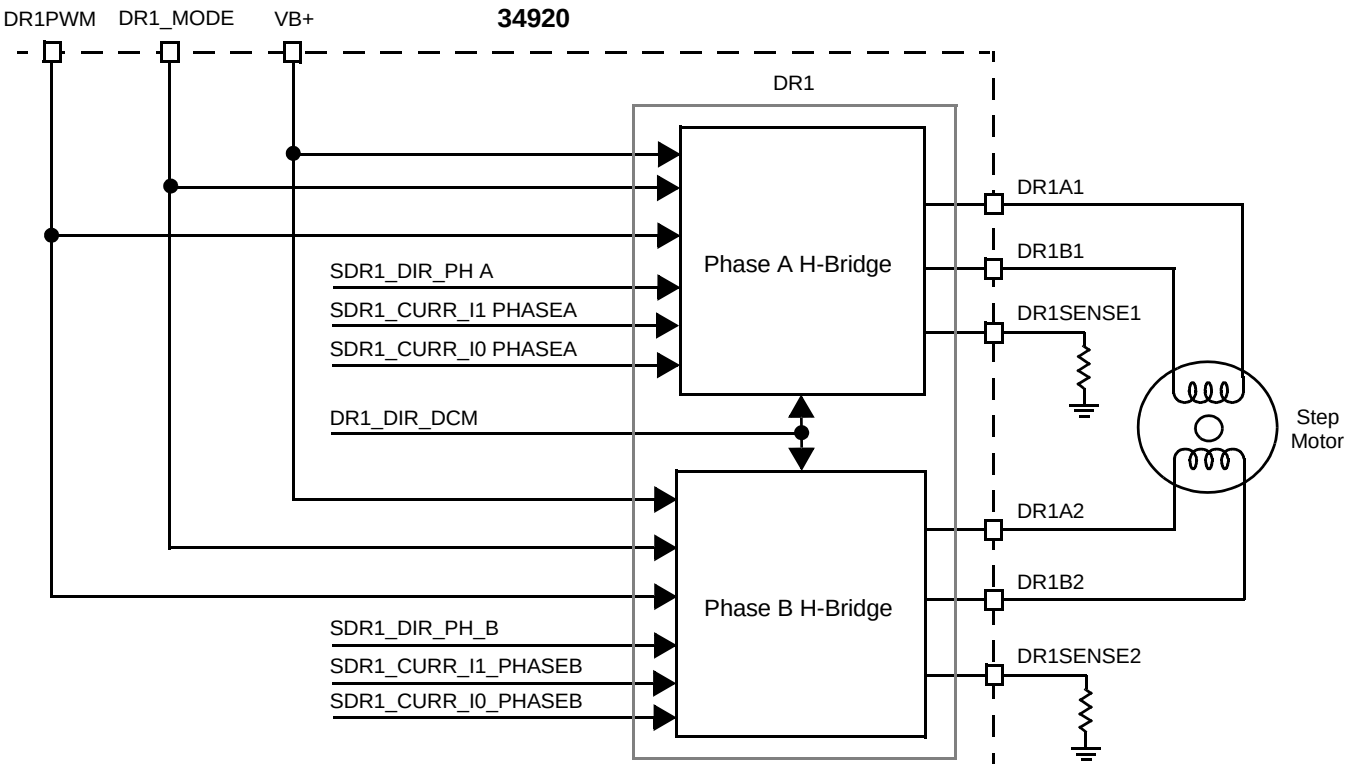


Figure 7. Simplified Step Application Diagram Showing 1 of 2 Step Drive Circuits

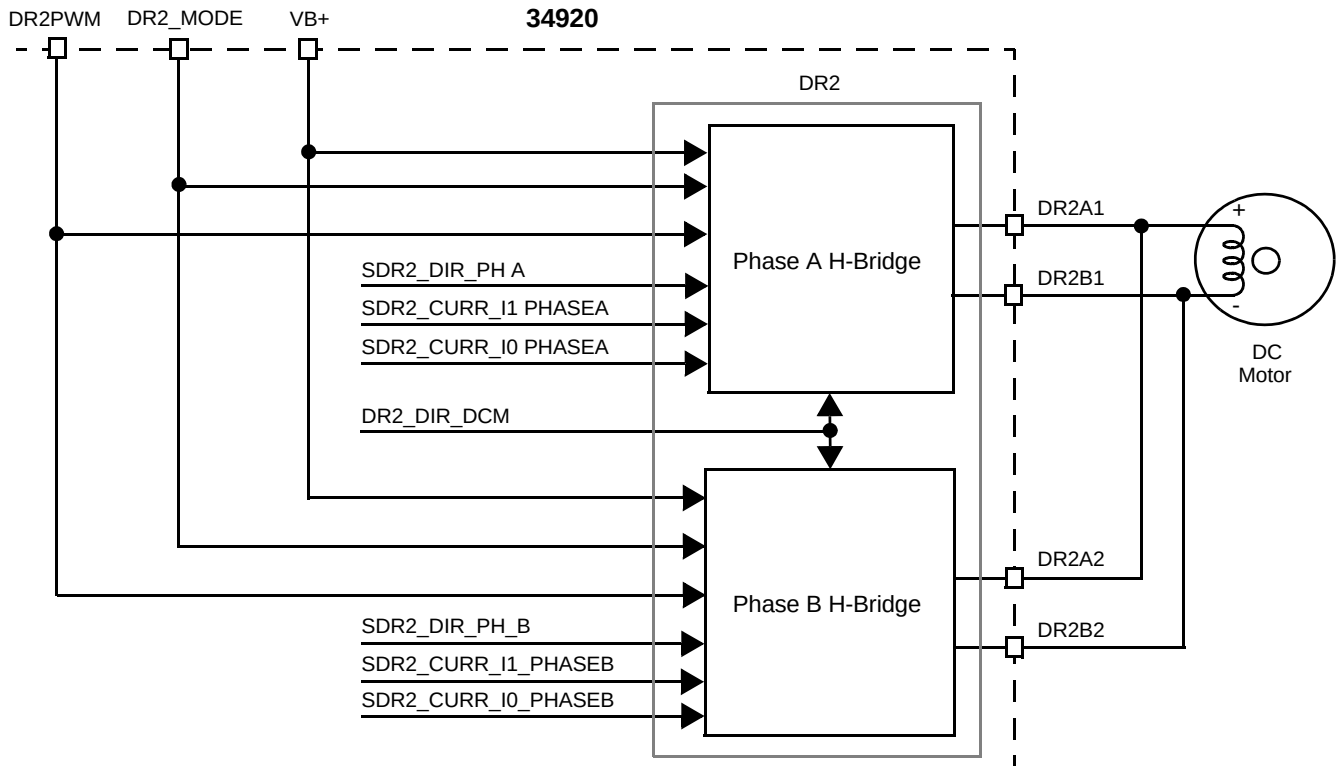


Figure 8. Simplified DC Application Diagram Showing 1 of 2 Motor Drive Circuits

BIPOLAR CURRENT REGULATED STEP MOTOR DRIVE SYSTEM

The drive circuitry is powered by the V_{VB+} supply voltage. For example, with external current sense resistors of 0.910 Ω ±1%, the drive circuitry provides drive for a bipolar step motor at current levels of approximately 183 mA, 367 mA, and 550 mA. Current mode operation supports quarter stepping.

This drive enters the fast current decay mode when both the CURR_I0_PHASEX and CURR_I1_PHASEX inputs are set to the logic [1] level. In fast current decay mode, any residual motor winding current is forced into the V_{VB+} supply rail when going to a zero current state from a non-zero current level. This forces the motor winding current toward zero as quickly as possible.

For each of the two H-bridge drivers, controlled crossover delay, a blanking period, and internal overtemperature sensing are provided. The crossover delay is controlled to provide sufficient time for cross-conduction suppression. At no time will both the upper and lower output device on the same side of the H-bridge be allowed to conduct simultaneously. Also, following a turn-on event a blanking period is included to prevent false turn-offs owing to the initial turn-on current spike, which results from motor circuit capacitance.

This drive has internal overtemperature sensing for protection. During an overtemperature event, when the device T_J is at or above $T_{J(SHUTDOWN)}$, the internal thermal protection circuit disables the drive outputs by driving all outputs to the zero current state until the device temperatures have dropped below the lower thermal threshold temperature $T_{J(ENABLE)}$, at which time the driver is re-enabled.

Note During power-on the step motor driver circuit inhibits its outputs when V_{VB+} is at 4.0 V or greater until $\overline{\text{RESET}}$ is released. Likewise, during power-down the step motor driver circuit inhibits its outputs from the point when $\overline{\text{RESET}}$ goes low until V_{VB+} has dropped below 4.0 V.

DC MOTOR DRIVE SYSTEM

This drive circuitry provides bi-directional drive to a DC motor via two inputs, DCM_PWM (an external pin, CMOS-compatible input) and DRx_DIR_DCM (a bit in the serial input port; refer to Tables 7 through 9, pp. 15–17). This drive is powered from VB+. The DC motor control circuitry uses voltage mode control.

To drive a DC motor the 34920 outputs DR2A1 and DR2A2 must be connected together externally, then connected to the DC motor "+" lead. Likewise, the 34920 outputs DR2B1 and DR2B2 must be connected together externally, then connected to the DC motor "-" lead (see Figure 8).

This drive provides internal overtemperature sensing for protection. During an overtemperature event, when the device T_J is at or above $T_{J(SHUTDOWN)}$, the internal thermal protection circuit disables the drive outputs by driving both outputs to the high state until the device temperatures have dropped below the lower thermal threshold temperature $T_{J(ENABLE)}$, at which time the drive is re-enabled.

The crossover delay must be controlled to provide sufficient time for cross-condition suppression. At no time can both the upper and lower output devices on the same side of the H-bridge be allowed to conduct simultaneously. Also, following a turn-on event a blanking period is included to prevent false turn-offs owing to the initial turn-on current spike, which results from motor circuit capacitance.

Note During power-on the DC Motor Driver circuit inhibits its outputs when V_{VB+} is at 4.0 V or greater until $\overline{\text{RESET}}$ is released. Likewise, during power-down of the machine the DC Motor Driver circuit inhibits its outputs from the point when $\overline{\text{RESET}}$ goes low until V_{VB+} has dropped below 4.0 V.

$\overline{\text{RESET}}$ FUNCTIONALITY

The 34920 provides an output, $\overline{\text{RESET}}$, that drives an external reset signal to the system microprocessor and/or the system digital logic IC. This signal is an active low logic level signal that is derived by monitoring the level of the V_{CC} pin. This output is the equivalent of an open drain- (or open collector-) type output, with an internal 2.5 kΩ pull-up to V_{CC}. This output pin can be driven by other external sources and therefore the state of $\overline{\text{RESET}}$ must be monitored by the 34920.

Note When $\overline{\text{RESET}}$ is asserted either internally or from an external source, all 34920 motor drive outputs will be in their inactive states, and the serial input port will be loaded with the "Reset Value" (refer to Tables 6 through 9). The V2 voltage regulator will be enabled.

During power-up this output asserts a logic low level, and it monitors the V1 regulator output voltage and detects the point that it reaches V_{V1T+}. The output will then remain low for a delay of 15 ms to 50 ms before releasing to a high state. A second case is if V_{V1_FB} is at or above V_{V1T+} for a period longer than the delay period of t_{DELAY} and V_{VB+} is still less than V_{VB+T-}. In this situation $\overline{\text{RESET}}$ will remain low until V_{VB+} is greater than V_{VB+T-}, at which point $\overline{\text{RESET}}$ will be released immediately and there will be no delay period. If V_{VB+} passes through V_{VB+T+} during the t_{DELAY} period, $\overline{\text{RESET}}$ will remain low until the end of the t_{DELAY} period, which started at the time V_{V1_FB} passed through the V_{V1T+} level.

During power-down this output immediately asserts a logic low at the point when V_{V1_FB} drops down to the trip point of V_{V1T-}. Also, if V_{VB+} drops below V_{VB+T-} and V_{V1_FB} is still at or above V_{V1T-}, $\overline{\text{RESET}}$ will be pulled low.

$\overline{\text{RESET}}$ BEHAVIOR

The following conditions describe the behavior of the $\overline{\text{RESET}}$ circuit.

A Note on Terminology Assertion of $\overline{\text{RESET}}$ is defined as the $\overline{\text{RESET}}$ pin outputting a logic low voltage, and de-assertion is when the pin is pulled up to the V_{CC} voltage.

On the power-up condition, $\overline{\text{RESET}}$ behaves as follows:

- If 1.0 V < V_{V1_FB} < V_{V1T+} or V_{VB+} < V_{VB+T+}, $\overline{\text{RESET}}$ will be asserted.
  Important If V_{V1_FB} < 1.0 V, $\overline{\text{RESET}}$ is undefined.
- If $\overline{\text{RESET}}$ is asserted owing to V_{V1_FB} < V_{V1T-}, then when V_{V1_FB} rises monotonically from below V_{V1T-} to above V_{V1T+}, $\overline{\text{RESET}}$ will de-assert after a duration of t_{DELAY}.
- If $\overline{\text{RESET}}$ is asserted owing to V_{VB+} < V_{VB+T+} and $V_{V1_FB} \geq V_{V1T+}$, then when V_{VB+} rises to the V_{VB+T+} level $\overline{\text{RESET}}$ will de-assert with no delay. The only case where a delay would be seen is if the time period from where V_{V1_FB} rises to the V_{V1T+} level to the point where V_{VB+} rises to the V_{VB+T+} level is less than the t_{DELAY} period. Then the delay in de-asserting $\overline{\text{RESET}}$ would be the remaining t_{DELAY} time, thereby maintaining the full t_{DELAY} period, between the time when V_{V1_FB} reaches V_{V1T+} and the de-assertion of $\overline{\text{RESET}}$, that is required for a reliable system reset.

On the power-down condition, $\overline{\text{RESET}}$ behaves as follows:

- If $\overline{\text{RESET}}$ is not asserted, and the V_{V1_FB} voltage monotonically decreases to a value below the negative-going threshold of V_{V1T-} and remains below V_{V1T-} for longer than $t_{PERSIST}$ (10 μs to 30 μs), $\overline{\text{RESET}}$ will be asserted. $\overline{\text{RESET}}$ will remain asserted while 1.0 V < V_{V1_FB} < V_{V1T+}. If V_{V1_FB} falls below 1.0 V, the $\overline{\text{RESET}}$ signal is undefined.
- $\overline{\text{RESET}}$ will also be asserted when V_{VB+} decreases below the V_{VB+T+} level. This will occur even if the V_{V1_FB} level is still above V_{V1T-}.

On the V_{V1_FB} glitch condition, $\overline{\text{RESET}}$ behaves as follows:

- If the V_{V1_FB} supply falls below V_{V1T-} and remains there for less than $t_{PERSIST}$ (10 µs to 30 µs), $\overline{\text{RESET}}$ will not be asserted. However, if the condition lasts longer than $t_{PERSIST}$, $\overline{\text{RESET}}$ will be asserted for a duration of t_{DELAY}. The 10 µs-to-30 µs persistence time specified in $t_{PERSIST}$ is for ESD rejection. The reset trigger will be a retriggerable one-shot, where the delay pulse will be 10 µs to 30 µs for the delay timeout.

ENVIRONMENTAL SPECIFICATIONS

AMBIENT TEMPERATURE AND RELATIVE HUMIDITY

Table 11 lists the temperature and relative humidity for operating and storage conditions for the 34920.

Table 11. Ambient Temperature and Humidity

Condition	Temperature (°C)	% Relative Humidity
Operating	0 to 70	8.0 to 80
Storage	-40 to 150	5.0 to 80

ESD IMMUNITY

Refer to the Maximum Ratings table, page 5.

OVERTEMPERATURE PROTECTION

The 34920 implements overtemperature detection and shutdown functions. The overtemperature circuitry monitors the device's internal temperature and activates thermal shutdown circuitry when the temperature exceeds $T_{J(SHUTDOWN)}$ (155°C minimum, 175°C maximum). The thermal shutdown condition is maintained until the die temperature falls below $T_{J(ENABLE)}$ (135°C minimum, 155°C maximum). Each voltage regulator and motor driver circuit has its own individual shutdown circuit.

FUNCTIONAL DEVICE OPERATION

LOGIC COMMANDS AND REGISTERS

Table 12. Step Motor Truth Table

DIR_PH_A	CURR_I0_ PHASEA	CURR_I1_ PHASEA	IPH_A (mA)	DIR_PH_B	CURR_I0_ PHASEB	CURR_I1_ PHASEB	IPH_B (mA)
0	0	0	550	0	0	0	550
0	1	0	367	0	1	0	367
0	0	1	183	0	0	1	183
X	1	1	Off	X	1	1	Off
1	0	0	-550	1	0	0	-550
1	1	0	-367	1	1	0	-367
1	0	1	-183	1	0	1	-183

Table 13. DC Motor Drive System Truth Table

DRx_DIR_DCM	DRxPWM	High-Side A	Low-Side A	High-Side B	Low-Side B
0	0	On	Off	On	Off
0	1	Off	On	On	Off
1	0	On	Off	On	Off
1	1	On	Off	Off	On

TYPICAL APPLICATIONS

LOGIC VOLTAGE (VCC) AND RESET INTEROPERABILITY

The 3.3 V or 5.0 V V_{V1} output voltage should feed back to the V_{CC} input pin directly (see Figure 9) to ensure that the 34920 can be properly reset during a power-down situation.

If this typology is not the one implemented, the user needs to be aware that the V_{CC} pin is not monitored for undervoltage. Only the V1_FB and VB+ pins are monitored for undervoltage. Thus, it is possible for V_{CC} to be under voltage without the 34920 issuing a reset.

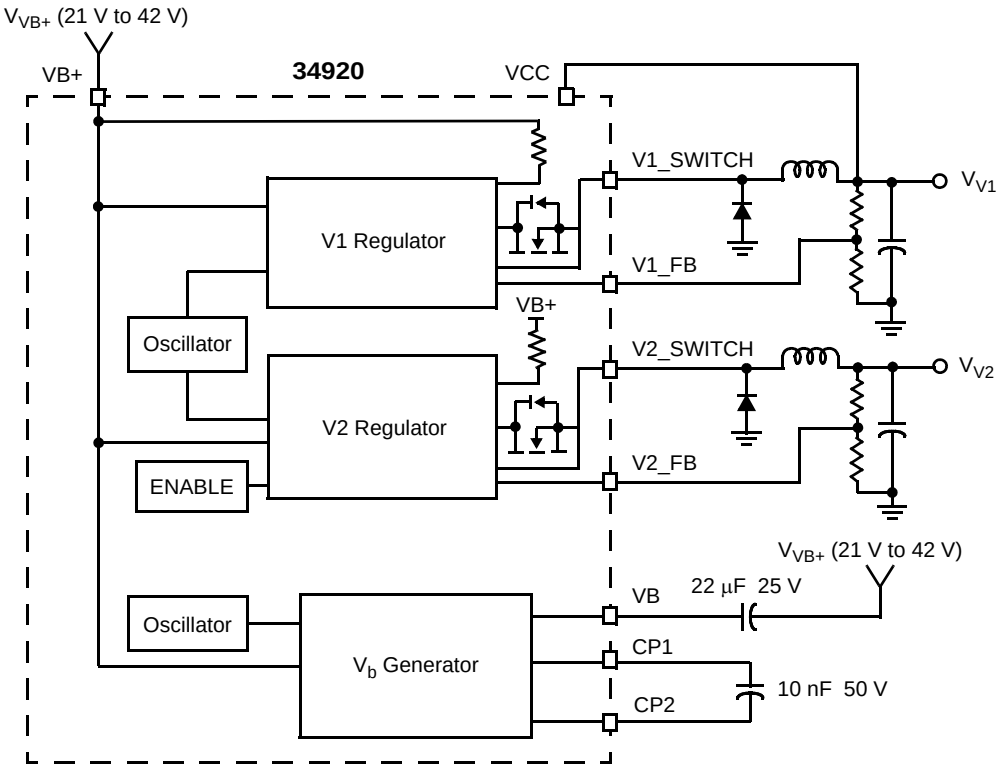
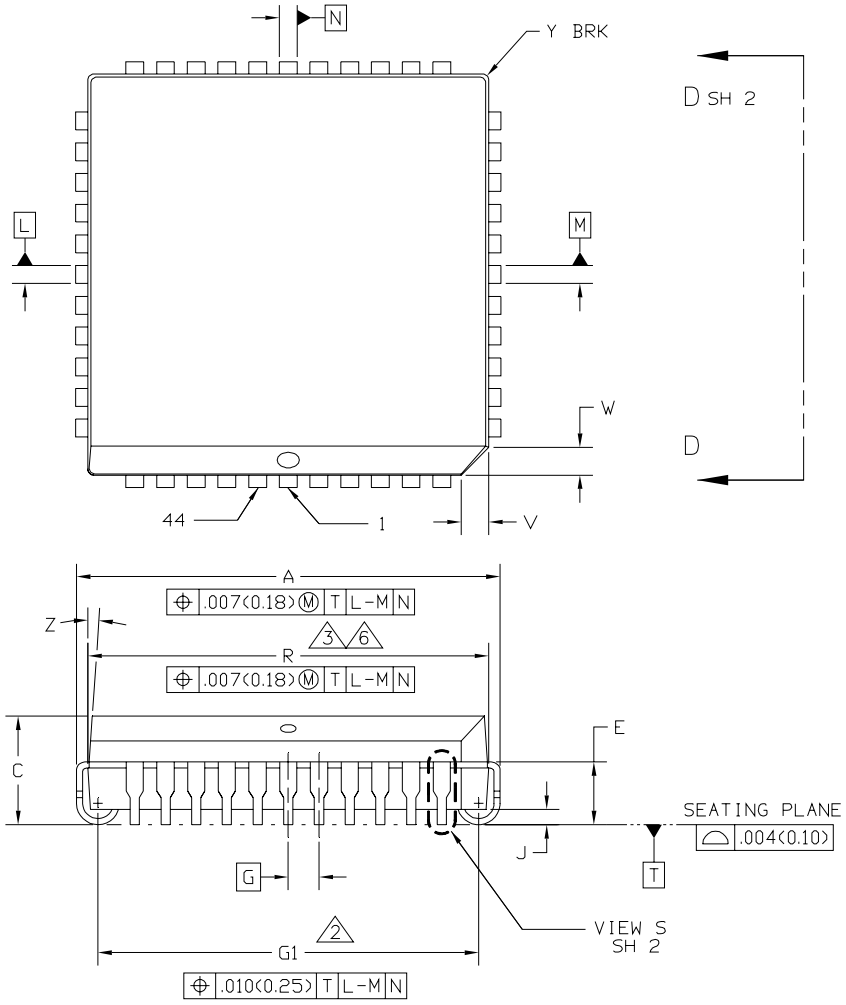


Figure 9. Voltage Regulator Functions

PACKAGING

PACKAGE DIMENSIONS

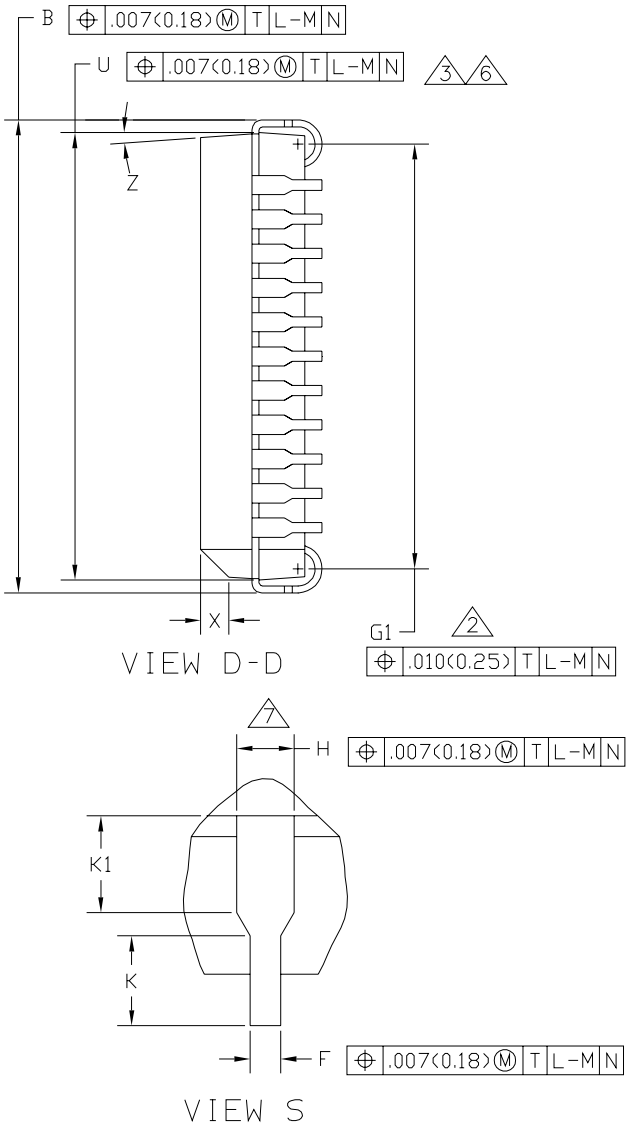
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	STANDARD: NON-JEDEC	

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	8/2006	• Implemented Revision History page • Converted to Freescale format and updated to the prevailing form and style • Added EI Pb-FREE suffix

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