

32 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE
REGISTERED TYPE**Description**

The MC-4532DA727 is a 33,554,432 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 128M SDRAM: μ PD45128441 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 33,554,432 words by 72 bits organization (ECC type)
- Clock frequency and access time from CLK.

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)
MC-4532DA727EF-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6.0 ns
MC-4532DA727PF-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6.0 ns
MC-4532DA727XF-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6.0 ns
MC-4532DA727XFA-A75	CL = 3	133 MHz	5.4 ns
	CL = 2	100 MHz	6.0 ns

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have $10\Omega \pm 10\%$ of series resistor

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Not all devices/types available in every country. Please check with local Elpida Memory, Inc. for availability and additional information.

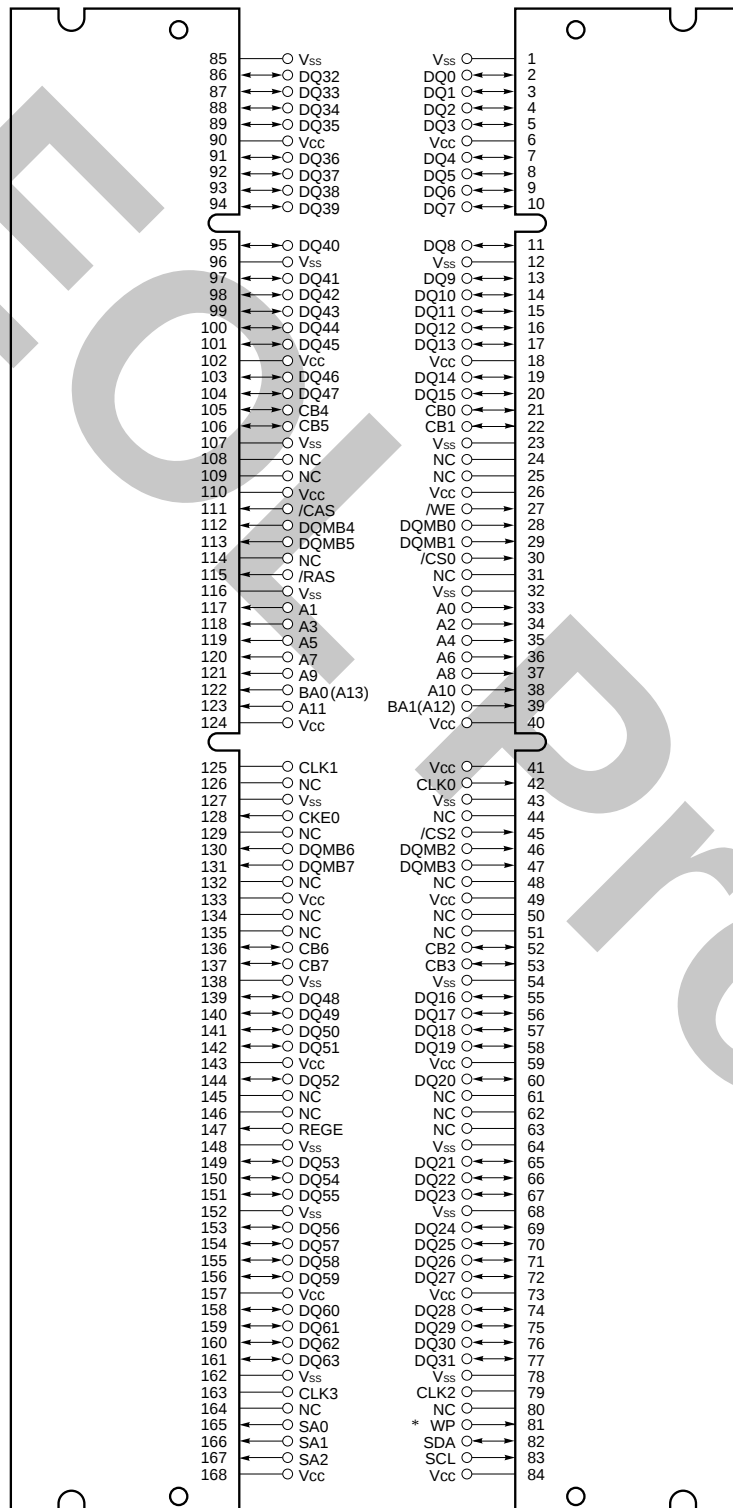
- Single 3.3 V ± 0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD

Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-4532DA727EF-A75	133 MHz	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plated 43.18 mm height	18 pieces of μ PD45128441G5 (Rev. E) (10.16mm (400) TSOP (II))
MC-4532DA727PF-A75			18 pieces of μ PD45128441G5 (Rev. P) (10.16mm (400) TSOP (II))
MC-4532DA727XF-A75			18 pieces of μ PD45128441G5 (Rev. X) (10.16mm (400) TSOP (II))
MC-4532DA727XFA-A75		30.48 mm height	18 pieces of μ PD45128441G5 (Rev. X) (10.16mm (400) TSOP (II))

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

A0 - A11 : Address Inputs

[Row: A0 - A11, Column: A0 - A9, A11]

BA0 (A13), BA1 (A12) : SDRAM Bank Select

DQ0-DQ63, CB0-CB7 : Data Inputs/Outputs

CLK0 - CLK3 : Clock Input

CKE0 : Clock Enable Input

WP* : Write Protect

/CS0, /CS2 : Chip Select Input

/RAS : Row Address Strobe

/CAS : Column Address Strobe

/WE : Write Enable

DQMB0 - DQMB7 : DQ Mask Enable

SA0 - SA2 : Address Input for EEPROM

SDA : Serial Data I/O for PD

SCL : Clock Input for PD

Vcc : Power Supply

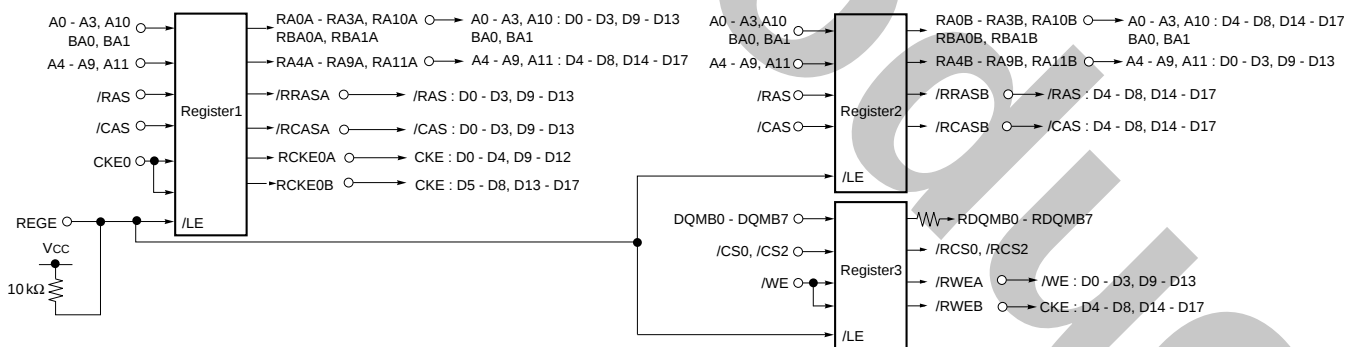
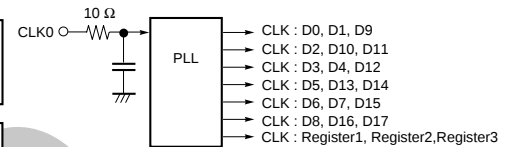
Vss : Ground

REGE : Register / Buffer Enable

NC : No Connection

* : 81 pin of MC-4532DA727XFA is NC pin.

The diagram illustrates the 16-channel 100 Gbps Ethernet PHY architecture, organized into two main sections. Each section contains four data lanes (D0-D3 and D4-D7) and four control lanes (CB0-CB3). The lanes are connected to a 100 Gbps Ethernet PHY block. The diagram is divided into two main sections, each with four data lanes (D0-D3 and D4-D7) and four control lanes (CB0-CB3). Each lane is connected to a 100 Gbps Ethernet PHY block. The PHY blocks are connected to a 100 Gbps Ethernet PHY block.



- Data Sheet E0073N20

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 1 ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		−0.5 to +4.6	V
Voltage on input pin relative to GND	V_I		−0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		22	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	7		20	pF
	C_{I2}	CLK0	15		25	
	C_{I3}	CKE0	7		20	
	C_{I4}	/CS0, /CS2	4		10	
	C_{I5}	DQMB0 - DQMB7	3		12	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63, CB0 - CB7	5		13	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

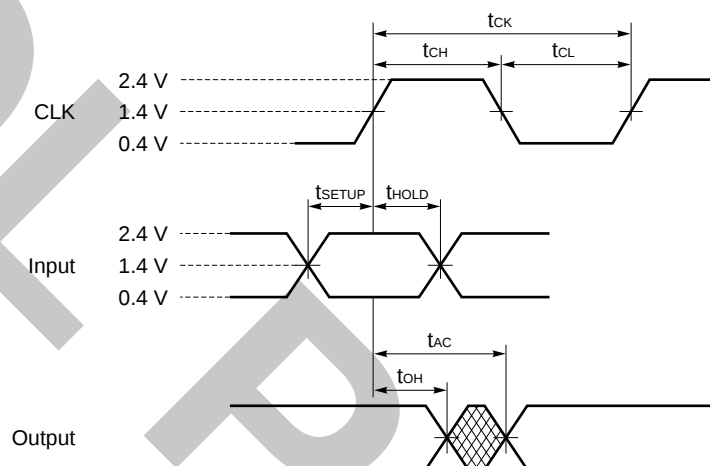
Parameter	Symbol	Test condition		Grade	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC} (MIN.), I _O = 0 mA	/CAS latency = 2	-A75		2,200	mA	1
			/CAS latency = 3	-A75		2,290		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL} (MAX.), t _{CK} = 15 ns				268	mA	
	I _{CC2PS}	CKE ≤ V _{IL} (MAX.), t _{CK} = ∞				98		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH} (MIN.), t _{CK} = 15 ns, /CS ≥ V _{IH} (MIN.), Input signals are changed one time during 30 ns.				610	mA	
	I _{CC2NS}	CKE ≥ V _{IH} (MIN.), t _{CK} = ∞, Input signals are stable.				224		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL} (MAX.), t _{CK} = 15 ns				340	mA	
	I _{CC3PS}	CKE ≤ V _{IL} (MAX.), t _{CK} = ∞				152		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH} (MIN.), t _{CK} = 15 ns, /CS ≥ V _{IH} (MIN.), Input signals are changed one time during 30 ns.				790	mA	
	I _{CC3NS}	CKE ≥ V _{IH} (MIN.), t _{CK} = ∞, Input signals are stable.				440		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK} (MIN.), I _O = 0 mA	/CAS latency = 2	-A75		2,290	mA	2
			/CAS latency = 3	-A75		2,920		
CBR (Auto) Refresh current	I _{CC5}	t _{RC} ≥ t _{RC} (MIN.)	/CAS latency = 2	-A75		4,540	mA	3
			/CAS latency = 3	-A75		4,720		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V				286	mA	
Input leakage current	I _I (L)	V _I = 0 to 3.6 V, All other pins not under test = 0 V			-20	+20	μA	
Output leakage current	I _O (L)	D _{OUT} is disabled, V _O = 0 to 3.6 V			-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA			2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA				0.4	V	

- Notes**
1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK} (MIN.).
 2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK} (MIN.).
 3. I_{CC5} is measured on condition that addresses are changed only one time during t_{CK} (MIN.).

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Test Conditions

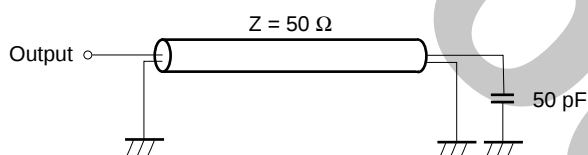
Parameter	Value	Unit
AC high level input voltage / low level input voltage	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Transition time (Input rise and fall time)	1	ns
Output timing measurement reference level	1.4	V



Synchronous Characteristics

Parameter		Symbol	-A75		Unit	Note
			MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	7.5	(133 MHz)	ns	
	/CAS latency = 2	t_{CK2}	10	(100 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		5.4	ns	1
	/CAS latency = 2	t_{AC2}		6.0	ns	1
Input clock frequency			50	133	MHz	
Input CLK duty cycle			45	55	%	
Data-out hold time		t_{OH}	2.7		ns	1
Data-out low-impedance time		t_{LZ}	0		ns	
Data-out high-impedance time	/CAS latency = 3	t_{HZ3}	3.0	5.4	ns	
	/CAS latency = 2	t_{HZ2}	3.0	6.0	ns	
Data-in setup time		t_{DS}	1.5		ns	
Data-in hold time		t_{DH}	0.8		ns	
Address setup time		t_{AS}	1.5		ns	
Address hold time		t_{AH}	0.8		ns	
CKE setup time		t_{CKS}	1.5		ns	
CKE hold time		t_{CKH}	0.8		ns	
CKE setup time (Power down exit)		t_{CKSP}	1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t_{CMS}	1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t_{CMH}	0.8		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics

Parameter	Symbol	-A 75		Unit	Note
		MIN.	MAX.		
ACT to REF/ACT command period (operation)	t _{RC}	67.5		ns	
REF to REF/ACT command period (refresh)	t _{RC1}	67.5		ns	
ACT to PRE command period	t _{RAS}	45	120,000	ns	
PRE to ACT command period	t _{RP}	20		ns	
Delay time ACT to READ/WRITE command	t _{RCD}	20		ns	
ACT(one) to ACT(another) command period	t _{RRD}	15		ns	
Data-in to PRE command period	t _{DPL}	8		ns	
Data-in to ACT(REF) command	/CAS latency = 3 /CAS latency = 2	t _{DAL3} t _{DAL2}	1CLK+22.5 1CLK+20	ns	1
period (Auto precharge)					
Mode register set cycle time	t _{RSC}	2		CLK	
Transition time	t _T	0.5	30	ns	
Refresh time (4,096 refresh cycles)	t _{REF}		64	ms	

Note 1. This device can satisfy the t_{DAL3} spec of 1CLK+20 ns for up to and including 125 MHz operation.

Serial PD

(1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		0BH	0	0	0	0	1	0	1	1	11 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTTL
9	CL = 3 Cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
10	CL = 3 Access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type		02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		04H	0	0	0	0	0	1	0	0	×4
14	Error checking SDRAM width		04H	0	0	0	0	0	1	0	0	×4
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported		06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		1FH	0	0	0	1	1	1	1	1	Registered
22	SDRAM device attributes : General		0EH	0	0	0	0	1	1	1	0	
23	CL = 2 Cycle time	-A75	A0H	1	0	1	0	0	0	0	0	10 ns
24	CL = 2 Access time	-A75	60H	0	1	1	0	0	0	0	0	6 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	t _{RP} (MIN.)	-A75	14H	0	0	0	1	0	1	0	0	20 ns
28	t _{RRD} (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	t _{RCD} (MIN.)	-A75	14H	0	0	0	1	0	1	0	0	20 ns
30	t _{RAS} (MIN.)	-A75	2DH	0	0	1	0	1	1	0	1	45 ns
31	Module bank density		40H	0	1	0	0	0	0	0	0	256M bytes

(2/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal input setup time		15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal input hold time		08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time		15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time		08H	0	0	0	0	1	0	0	0	0.8 ns
36-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		02H	0	0	0	0	0	0	1	0	JEDEC 2
63	Checksum for bytes 0 - 62	-A75	E9H	1	1	1	0	1	0	0	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency		64H	0	1	1	0	0	1	0	0	100 MHz
127	Intel specification /CAS latency support	-A75	85H	1	0	0	0	0	1	0	1	

Timing Chart

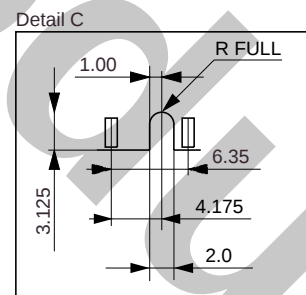
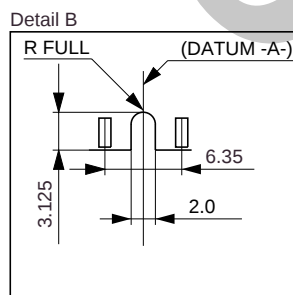
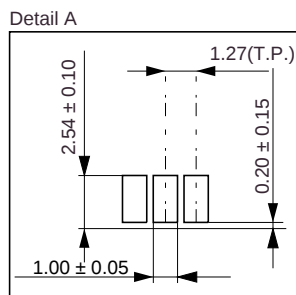
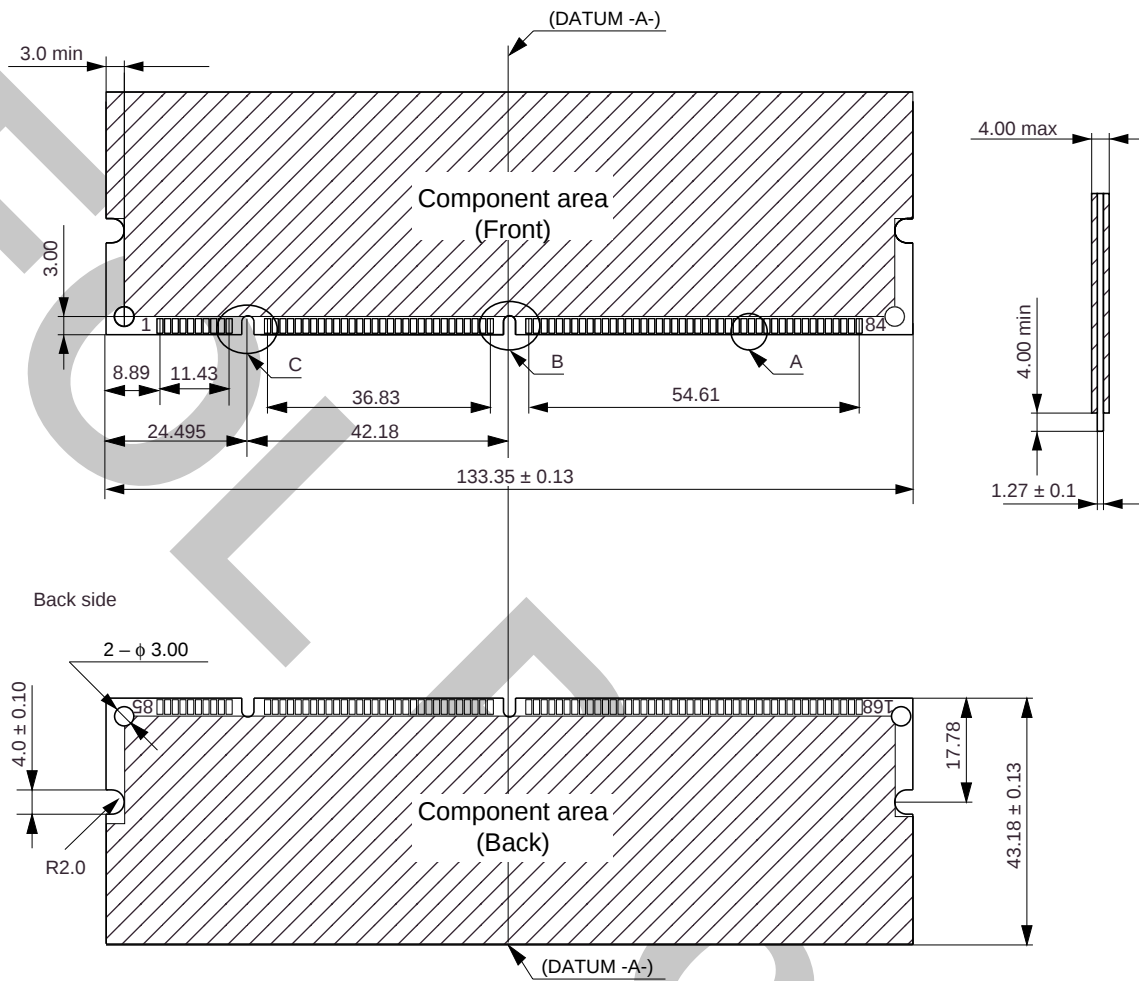
Refer to the **μPD45128441, 45128841, 45128163 Data sheet (E0031N)**.

Package Drawing

MC-4532DA727EF, MC-4532DA727PF, MC-4532DA727XF

Front side

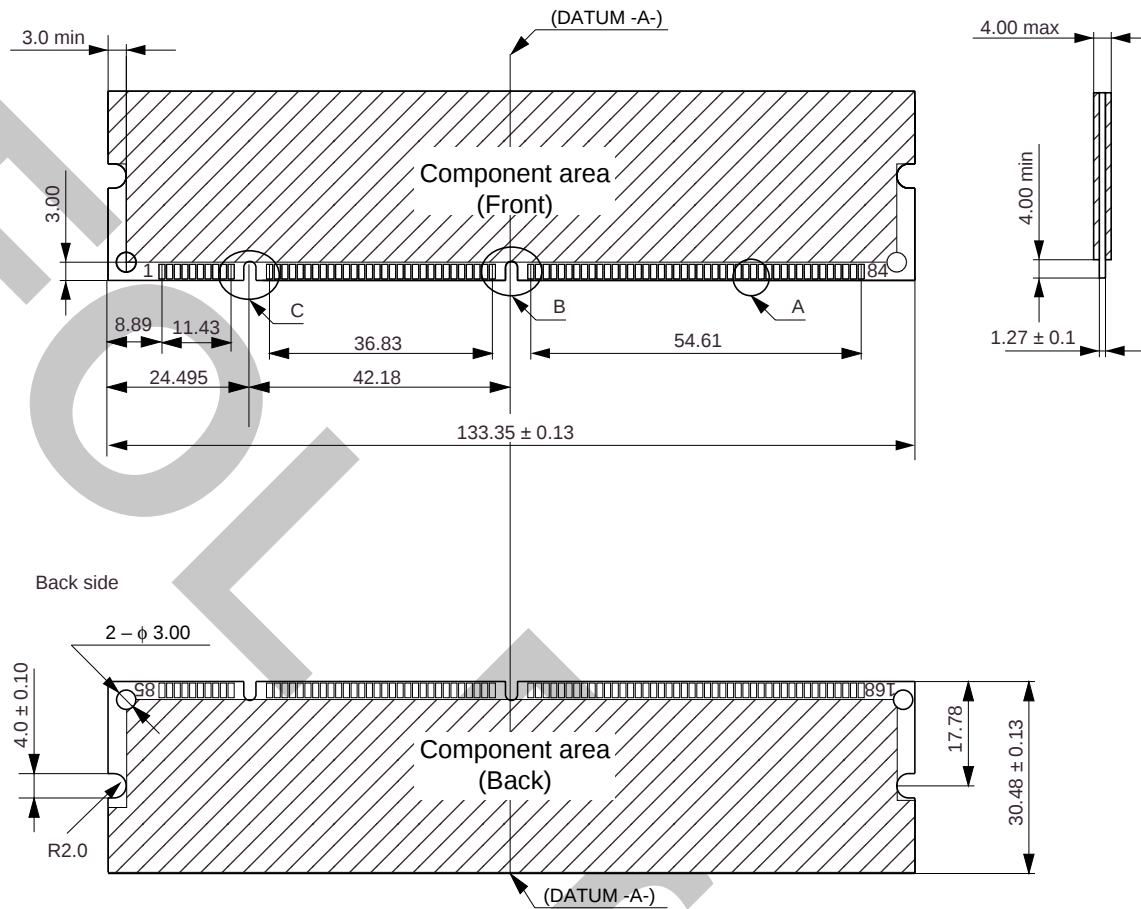
Unit: mm

Note: Tolerance on all dimensions ± 0.15 unless otherwise specified.

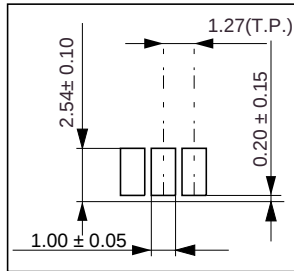
MC-4532DA727XFA

Front side

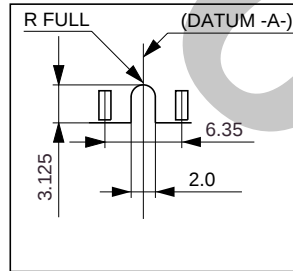
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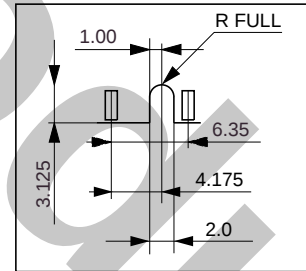
Detail A



Detail B



Detail C



Note: Tolerance on all dimensions ± 0.15 unless otherwise specified.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0107

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Product usage]

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[Usage environment]

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