FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12513-3E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89820 Series

MB89821/823/P825/PV820

■ DESCRIPTION

MB89820 series is a line of single-chip microcontrollers using the F²MC-8L* CPU core which can operate at low voltage but at high speed. In addition to an LCD controller/driver allowing 200-pixel display the microcontrollers contain a variety of peripheral functions such as timers, a UART, a serial interface, and an external interrupt. The configuration of the MB89820 series is therefore best suited to control of LCD display panels.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Minimum execution time: 0.8 µs/5 MHz (V_{CC} = +5.0 V)
- F²MC-8L family CPU core

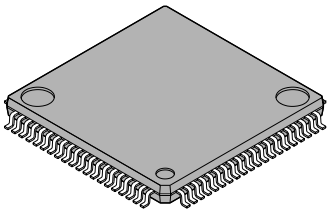
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- LCD controller/driver
  Max. 50 segments × 4 commons
  Divided resistor for LCD power supply

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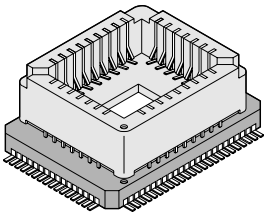
■ PACKAGES

80-pin Plastic QFP



(FPT-80P-M11)

80-pin Ceramic MQFP



(MQP-80C-P01)

(Continued)

- Three types of timers
  8-bit PWM timer (also usable as a reload timer)
  8-bit pulse width count timer (also usable as a reload timer)
  20-bit time-base timer
- Two serial interfaces
  8-bit synchronous serial interface (Switchable transfer direction allows communication with various equipment.)
  UART (5-, 7-, 8-bit transfer capable)
- External interrupt: 2 channels
  Capable of wake-up from low-power consumption modes (with an edge detection function)
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)

■ PRODUCT LINEUP

Part number / Parameter	MB89821	MB89823	MB89P825	MB89PV820
Classification	Mass production product (mask ROM products)		One-time PROM product	Piggyback/evaluation product for evaluation and development
ROM size	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits		1024 × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.8 µs/5 MHz (V_{CC} = 5.0 V) Interrupt processing time: 7.2 µs/5 MHz (V_{CC} = 5.0 V)			
Ports	I/O ports (N-ch open-drain): 16 (All also serve as segment pins.)*1 I/O ports (N-ch open-drain): 6 I/O ports (CMOS): 6 (5 ports also serve as peripheral I/O.) Input ports: 4 (1 port also serves as an external interrupt input.) Total: 32 (max.)			
8-bit PWM timer	8-bit reload timer operation (toggled output capable) 8-bit resolution PWM operation Operating clock (pulse width count timer output: 0.8 µs, 12.8 µs, 51.2 µs/5 MHz)			
8-bit pulse width count timer	8-bit reload timer operation 8-bit pulse width count operation (continuous measurement capable “H” width, “L” width, or single-cycle measurement capable) Operating clock (0.8 µs, 3.2 µs, 25.6 µs/5 MHz)			
8-bit serial I/O	8 bits One clock selectable from four transfer clocks (one external shift clock, three internal shift clock, three internal shift clocks: 1.6 µs, 6.4 µs, 25.6 µs/5 MHz) LSB first/MSB first selectability			

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Part number / Parameter	MB89821	MB89823	MB89P825	MB89PV820
UART	5-, 7-, 8-bit transfer capable Internal baud-rate generator (max. 78125 bps/5 MHz)			
LCD controller/ driver	Common output: 4 Segment output: 50 (max.) Operating mode: 1/2 bias, 1/2 duty; 1/3 bias, 1/3 duty; 1/3 bias, 1/4 duty LCD display RAM size: 50 × 4 bits Dividing resistor for LCD driving: Built-in (An external resistor selectable)			
External interrupt	2 channels (edge selectable) (1 channel also serves as a pulse width count timer input)			
Standby mode	Sleep mode, stop mode			
Process	CMOS			
Operating voltage*2	2.2 V*3 to 6.0 V		2.7 V to 6.0 V	
EPROM for use				MBM27C256A-20TV (LCC package)

*1: The function is selected by the mask option.
*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
*3: The operation at less than 2.2 V is assured separately. Please contact FUJITSU LIMITED.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89821 MB89823 MB89P825	MB89PV820
FPT-80P-M11	○	×
MQP-80C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89821, the register bank address upper than 0140_H cannot be used. On the MB89823 and MB89P825, each register bank addresses upper than 0180_H can be used.
- On the MB89P825, addresses $BFF0_H$ to $BFF6_H$ comprise the option setting area, option settings can be read by reading these addresses.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV820, add the current consumed by the EPROM which is connected to the top socket.
- However, the current consumption in sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics."

3. Mask Options

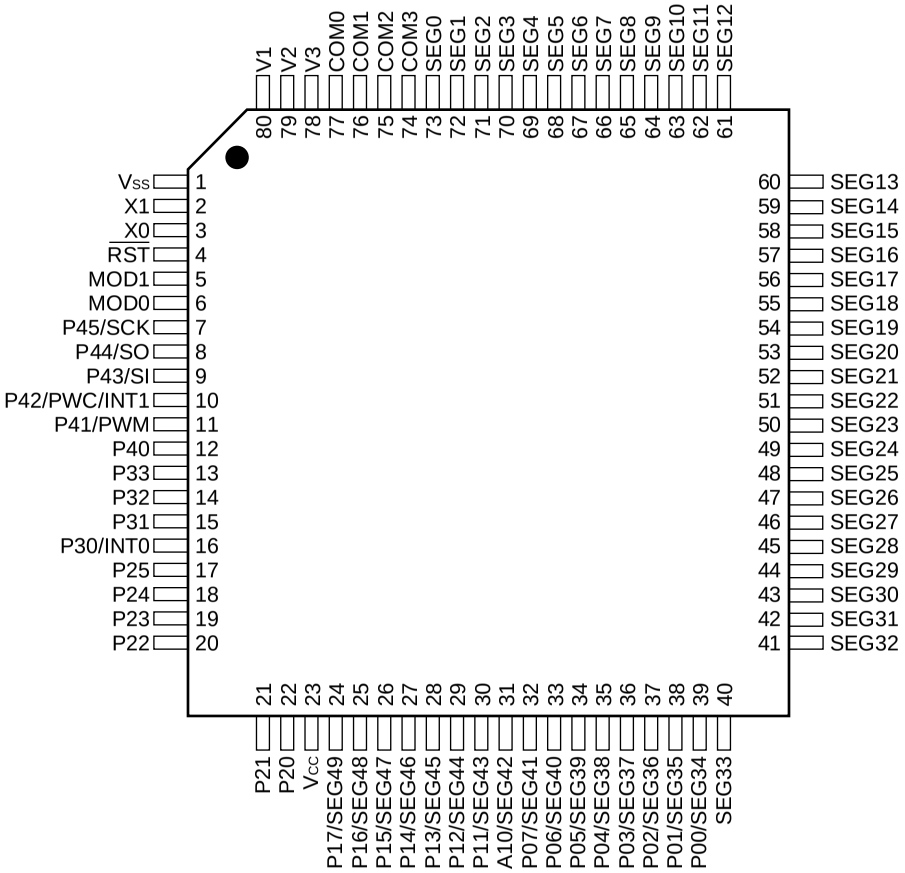
Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following point:

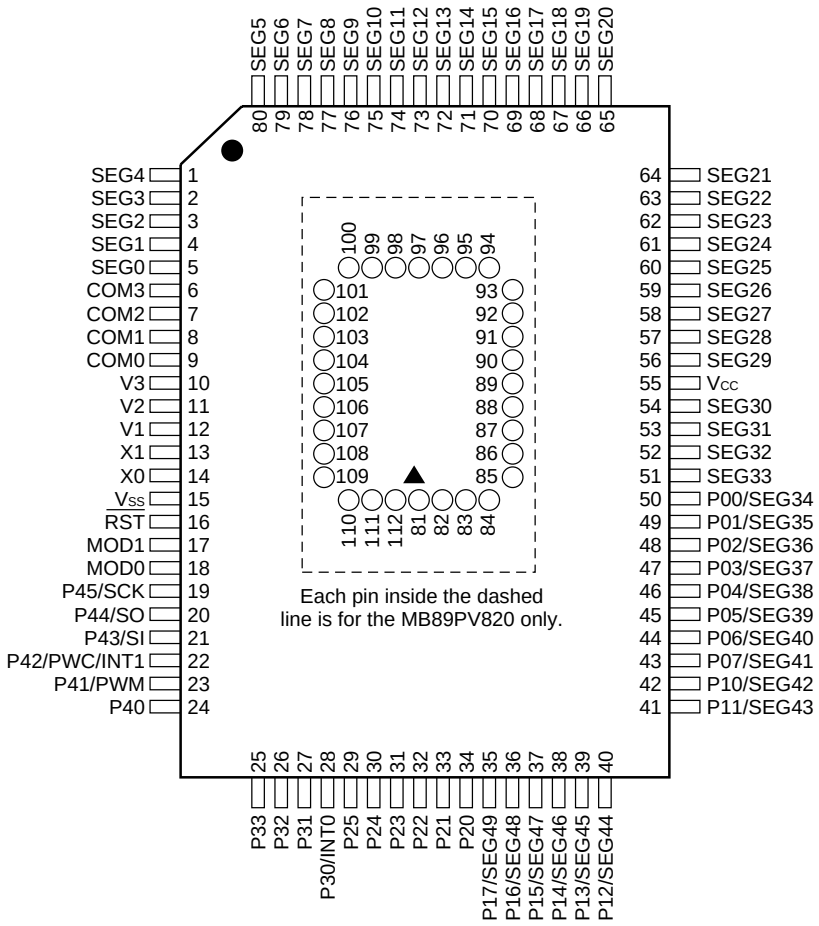
- Options are fixed on the MB89PV820.

■ PIN ASSIGNMENT



(FPT-80P-M11)

(Top view)



(MQP-80C-P01)

- **Pin assignment on package top (MB89PV820 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{OE}$
82	V_{PP}	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	O6	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	$\overline{CE}$	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
3	14	X0	A	Clock crystal oscillator pins
2	13	X1		
6	18	MOD0	B	Operating mode selection pins Connect directly to V_{SS}.
5	17	MOD1		
4	16	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source (optional function). The internal circuit is initialized by the input of “L”.
39 to 32	50 to 43	P00/SEG34 to P07/SEG41	D	General-purpose N-ch open-drain I/O ports Also serve as an LCD controller/driver segment output. The port and segment output are switched by mask option in 8-bit unit.
31 to 24	42 to 35	P10/SEG42 to P17/SEG49	D	General-purpose N-ch open-drain I/O ports Also serve as an LCD controller/driver segment output. The port and segment output are switched by mask option in 4 to 1-bit unit.
22 to 17	34 to 29	P20 to P25	F	General-purpose N-ch open-drain I/O ports A pull-up resistor option is provided.
16	28	P30/INT0	H	General-purpose input port The input is hysteresis input. Also serves as an external interrupt input (INT0). A pull-up resistor option is provided.
15 to 13	27 to 25	P31 to P33	H	General-purpose input ports These pins are a hysteresis input type. A pull-up resistor option is provided.
12	24	P40	E	General-purpose I/O port A pull-up resistor option is provided.
11	23	P41/PWM	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit PWM timer toggle output (PWM).
10	22	P42/PWC/INT1	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit pulse width count timer input (PWC) and an external interrupt input (INT1). The PWC and INT1 input is hysteresis input.
9	21	P43/SI	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit serial I/O and a UART data input (SI). The SI input is hysteresis input.

*1: FPT-80P-M11

*2: MQP-80C-P01

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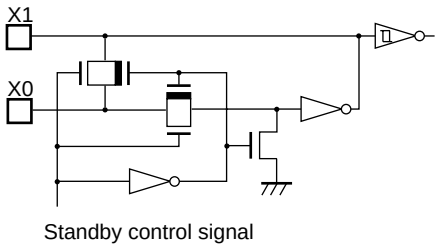
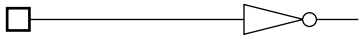
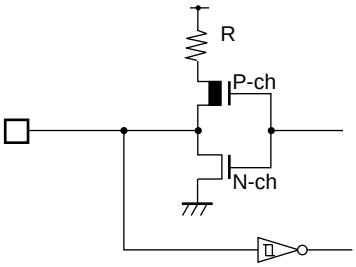
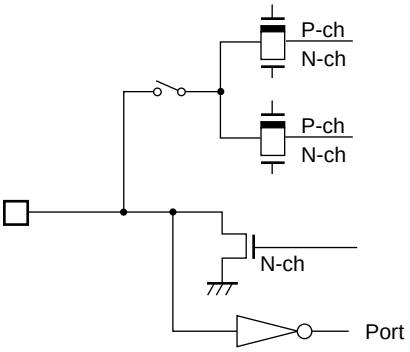
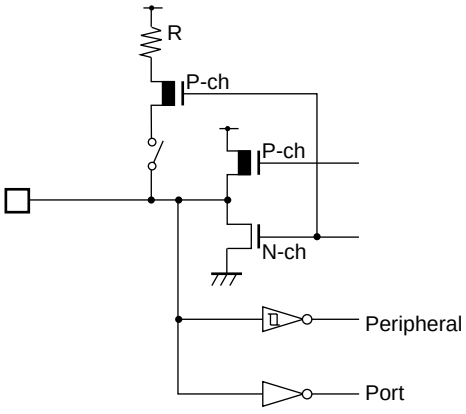
Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
8	20	P44/SO	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a serial I/O and a UART data output (SO).
7	19	P45/SCK	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a serial I/O and a UART clock I/O (SCK). The SCK input is hysteresis input.
73 to 40	5 to 1, 80 to 56, 54 to 51	SEG0 to SEG33	G	LCD controller/driver segment output pins
77 to 74	9 to 6	COM0 to COM3	G	LCD controller/driver common output pins
80 to 78	12 to 10	V1 to V3	—	LCD driving power supply pins
23	55	V_{CC}	—	Power supply pin
1	15	V_{SS}	—	Power supply (GND) pin

*1: FPT-80P-M11
*2: MQP-80C-P01

- **External EPROM pins (MB89PV820 only)**

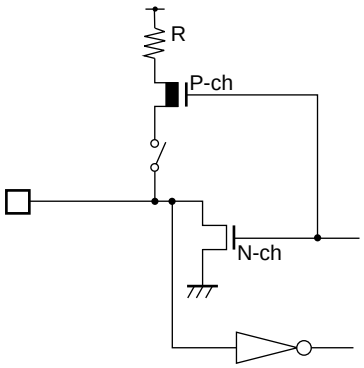
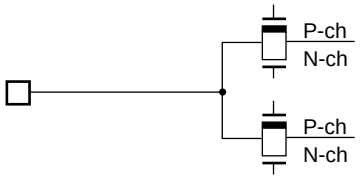
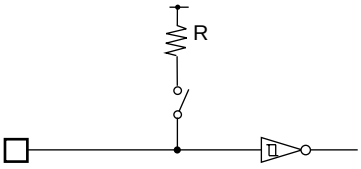
Pin no.	Pin name	I/O	Function
82	V_{PP}	O	“H” level output pin
83 84 85 86 87 88 89 90 91	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V_{CC}	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal oscillator circuit • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• N-ch open-drain output • CMOS input • Segment output optional
E		• CMOS output • CMOS input • Hysteresis input (peripheral input) • Pull-up resistor optional

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Type	Circuit	Remarks
F		• N-ch open-drain output • CMOS input • Pull-up resistor optional
G		• LCD controller/driver
H		• Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P825

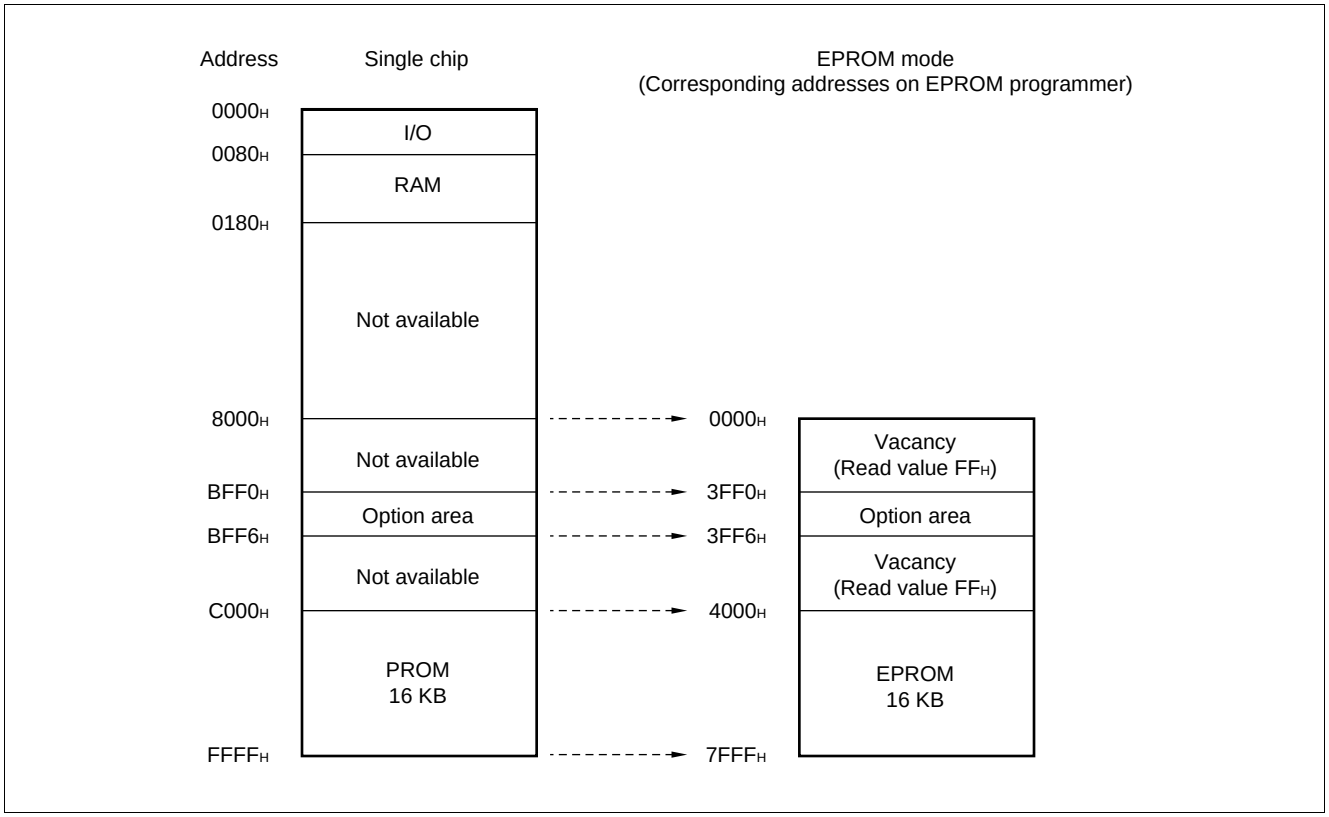
The MB89P825 is an OTPROM (one-time PROM) version for the MB89820 series.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P825 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

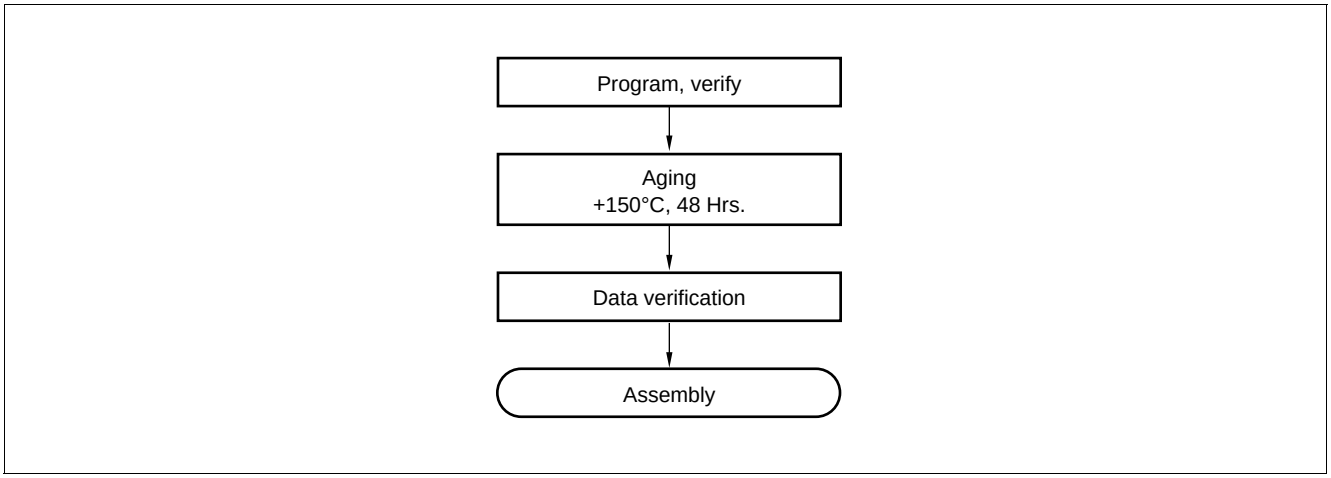
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000H to 7FFFH (note that addresses C000H to FFFFH while operating as a single chip assign to 4000H to 7FFFH in EPROM mode).
Load option data into addresses 3FF0H to 3FF5H of the EPROM programmer. (For information about each corresponding option, see “7. OTPROM Option Bit Map.”

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M11	ROM-80QF2-28DP-8L3

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

7. OTPROM Option Bit Map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$3FF0_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Reset pin output 1: Yes 0: No	Oscillation stabilization time 1: $2^{17}/F_C$ 0: $2^{13}/F_C$	Power-on reset 1: Yes 0: No
$3FF1_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
$3FF2_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
$3FF3_H$	Vacancy Readable	Vacancy Readable	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
$3FF4_H$	Vacancy Readable	Vacancy Readable	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
$3FF5_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes

Notes:
- Set each bit to 1 to erase.
- Do not write 0 to the vacant bit.
  The read value of the vacant bit is 1, unless 0 is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

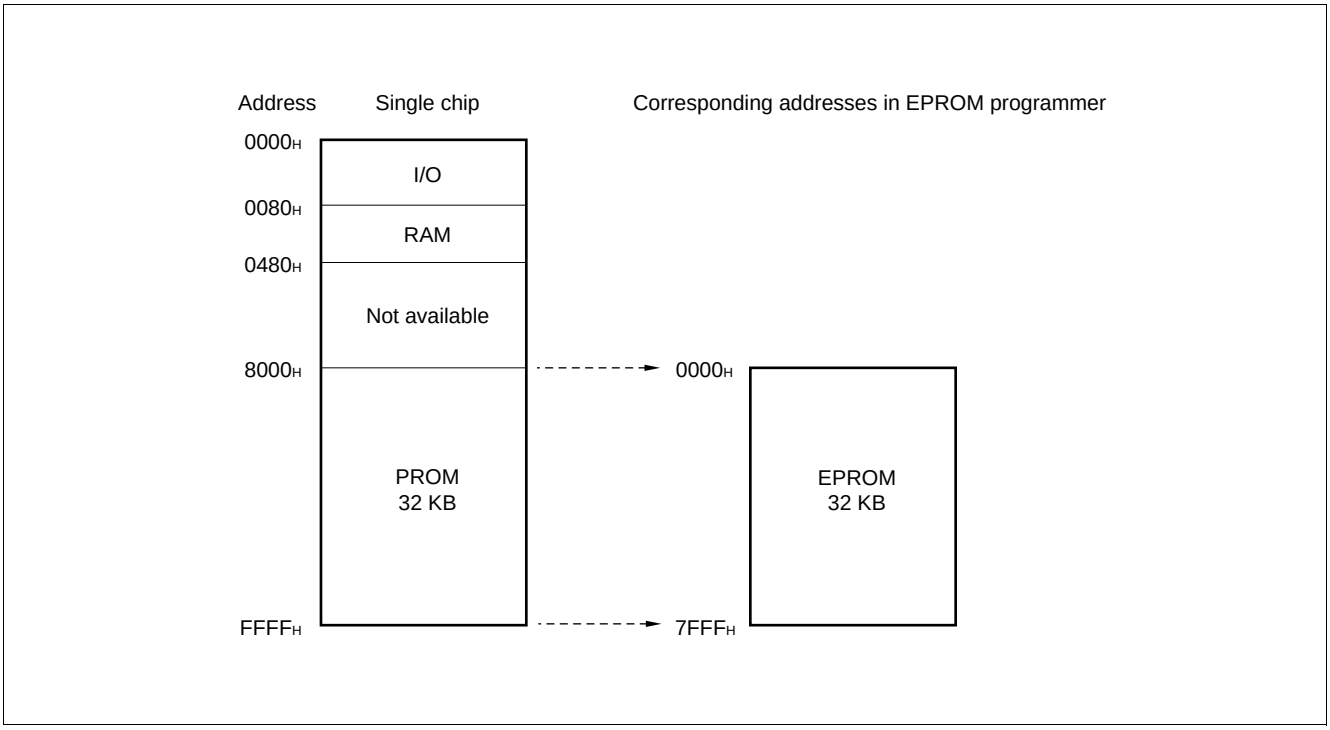
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32 Kbyte PROM, option area is diagrammed below.



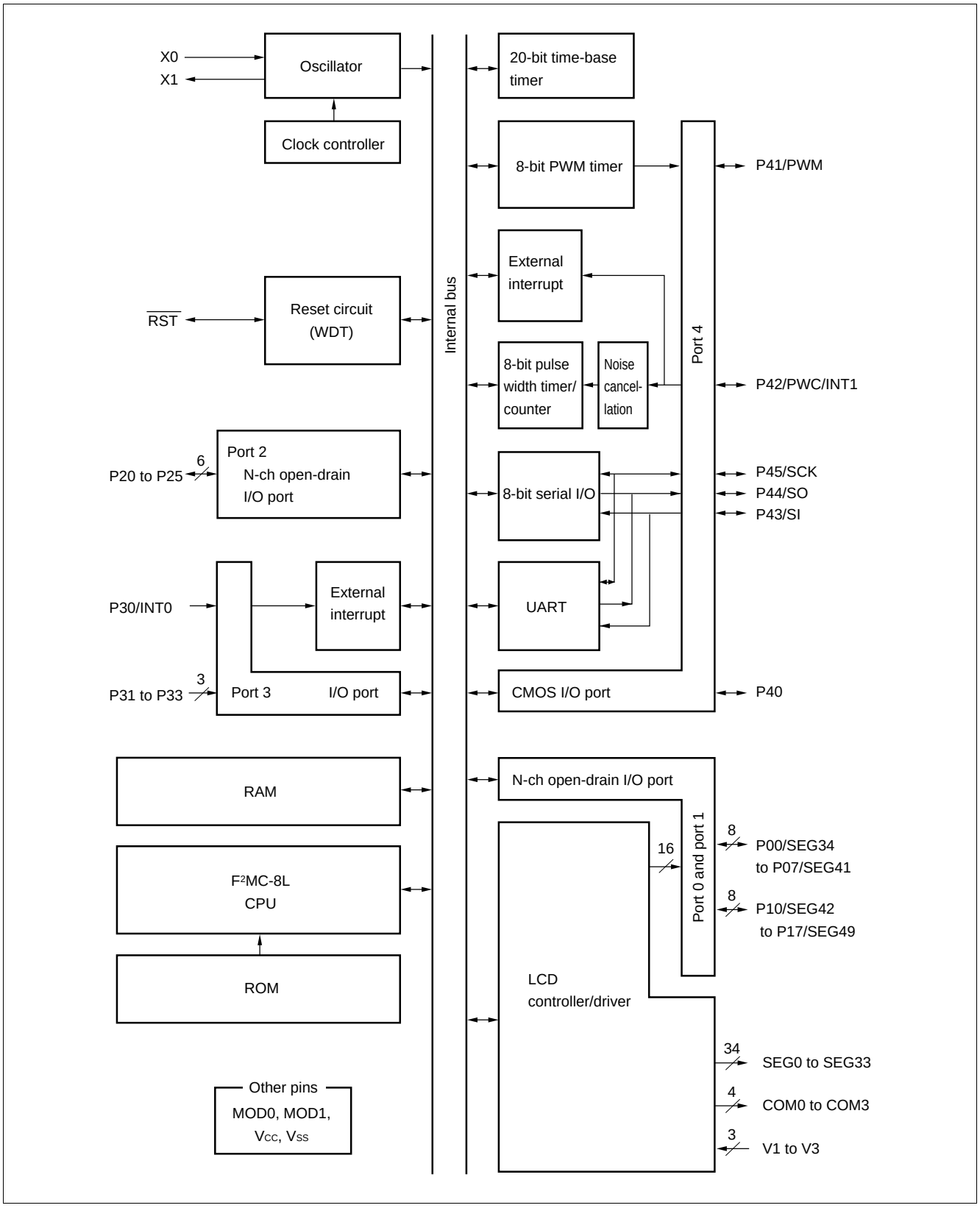
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

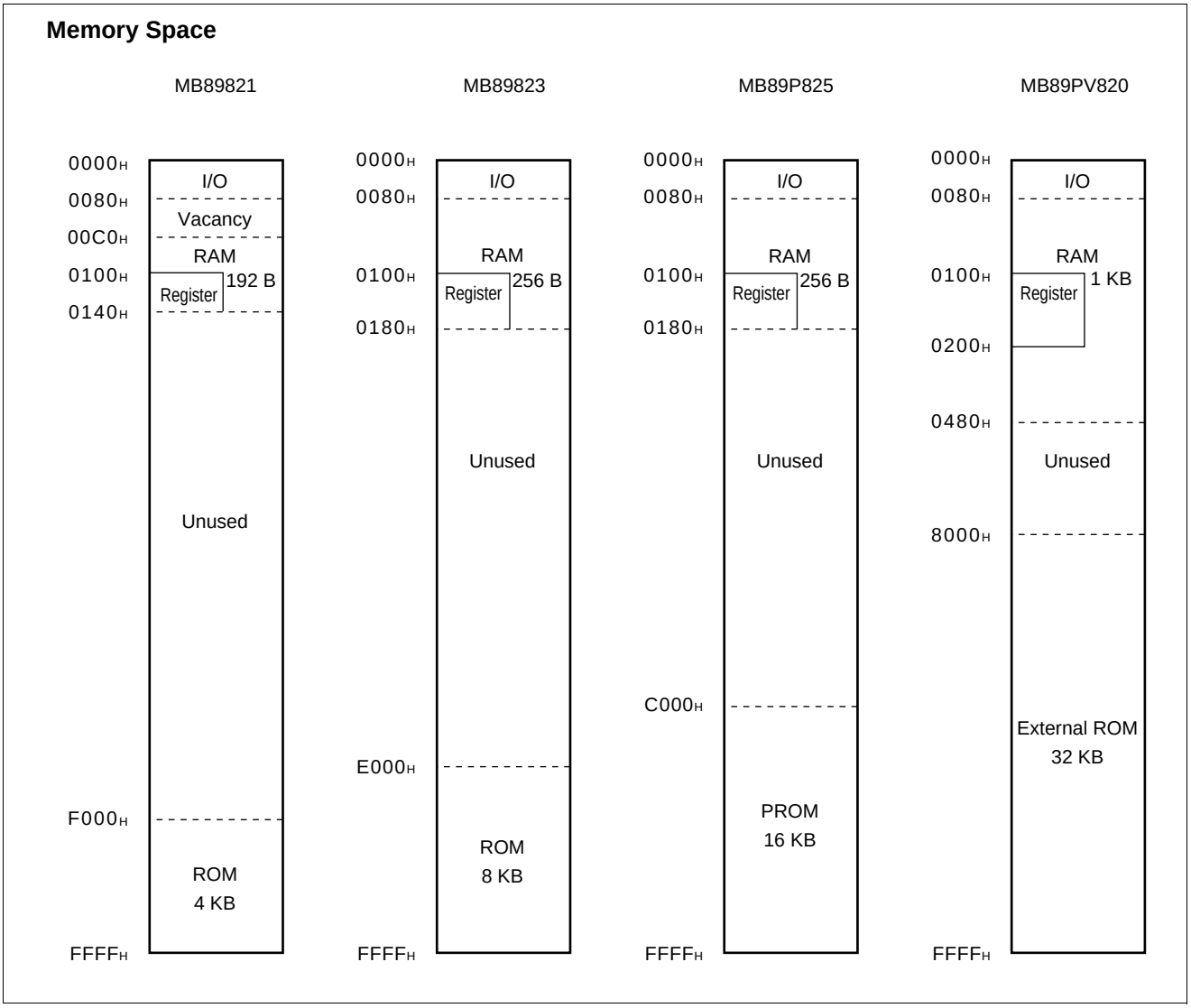


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89820 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89820 series is structured as illustrated below.

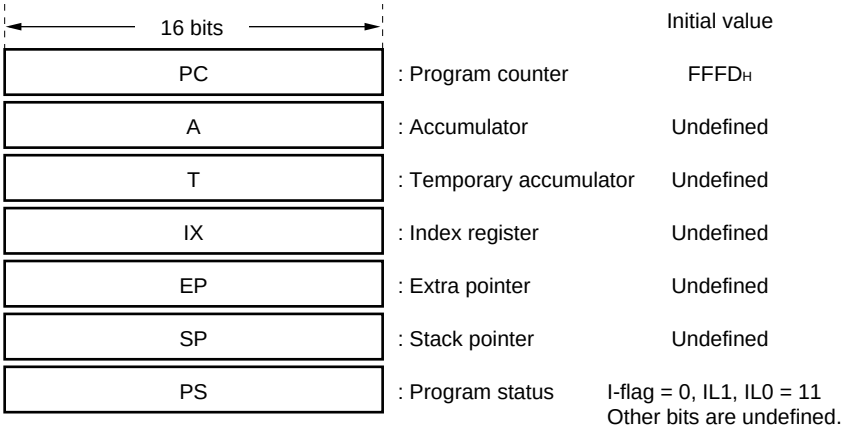
Memory Space



2. Registers

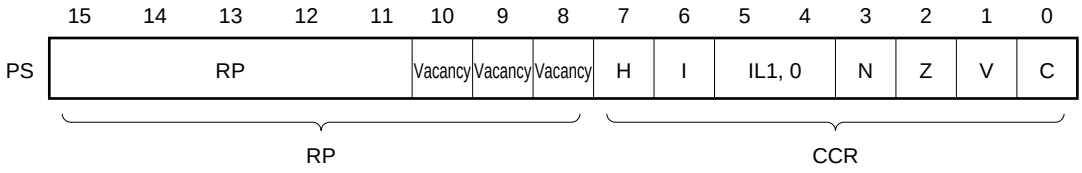
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



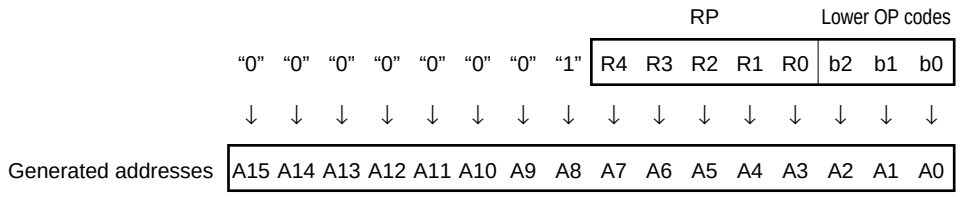
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

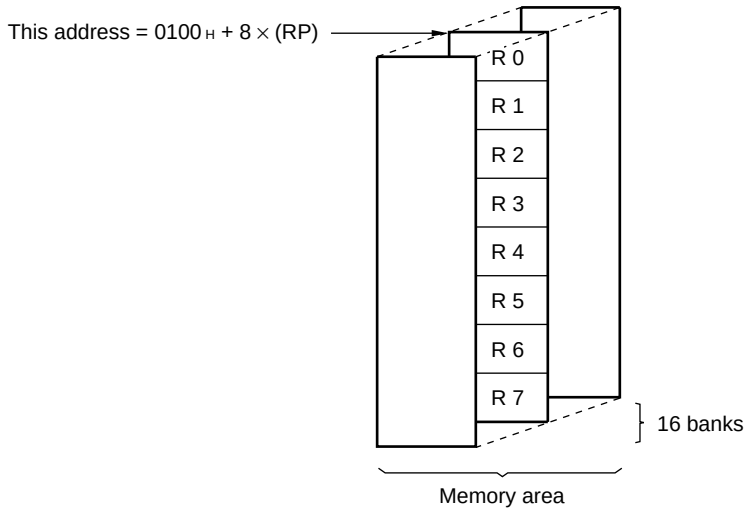
General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89823 (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

MB89821	0100_H to $013F_H$	8 banks
MB89823	0100_H to $017F_H$	16 banks
MB89P825	0100_H to $017F_H$	16 banks
MB89PV820	0100_H to $01FF_H$	32 banks

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H			Vacancy
02H	(R/W)	PDR1	Port 1 data register
03H			Vacancy
04H	(R/W)	PDR2	Port 2 data register
05H			Vacancy
06H			Vacancy
07H			Vacancy
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Time-base timer control register
0BH			Vacancy
0CH	(R)	PDR3	Port 3 data register
0DH			Vacancy
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H			Vacancy
11H			Vacancy
12H	(R/W)	CNTR	PWM timer control register
13H	(W)	COMR	PWM timer compare register
14H	(R/W)	PCR1	PWC pulse width control register 1
15H	(R/W)	PCR2	PWC pulse width control register 2
16H	(R/W)	RLBR	PWC reload buffer register
17H	(R/W)	NCCR	PWC noise cancellation control register
18H			Vacancy
19H			Vacancy
1AH			Vacancy
1BH			Vacancy
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH			Vacancy
1FH			Vacancy

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20H	(R/W)	SMC1	UART serial mode control register 1
21H	(R/W)	SRC	UART serial rate control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register
24H	(R/W)	SMC2	UART serial mode control register 2
25H			Vacancy
26H			Vacancy
27H			Vacancy
28H			Vacancy
29H			Vacancy
2AH			Vacancy
2BH			Vacancy
2CH			Vacancy
2DH			Vacancy
2EH			Vacancy
2FH			Vacancy
30H	(R/W)	EIC1	External interrupt 1 control register
31H to 5FH			Vacancy
60H to 78H	(R/W)	VRAM	Display data RAM
79H	(R/W)	LCR1	LCD controller/driver control register
7AH	(R/W)	SEGR	Segment output selection register
7BH			Vacancy
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
LCD power supply voltage	V3	V_{SS} – 0.3	V_{SS} + 7.0	V	V3 pin
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	V_{I1} must not exceed V_{SS} + 7.0 V. Except P00 to P07 and P10 to P17 for the MB89P825/PV820, and P20 to P25 without a pull-up resistor
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P00 to P07 and P10 to P17 (when selected as ports) for the MB89821/823, and P20 to P25 without a pull-up resistor
	V_{I3}	V_{SS} – 0.3	V3 + 0.3	V	P00 to P07 and P10 to P17 for the MB89P825/PV820
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	V_{O1} must not exceed V_{SS} + 7.0 V. Except P00 to P07 and P10 to P17 for the MB89P825/PV820, and P20 to P25 without a pull-up resistor
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P00 to P07 and P10 to P17 (when selected as ports) for the MB89821/823, and P20 to P25 without a pull-up resistor
	V_{O3}	V_{SS} – 0.3	V3 + 0.3	V	P00 to P07 and P10 to P17 for the MB89P825/PV820
“L” level output current	I_{OL}	—	10	mA	Except power supply pins
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate) Except power supply pins
Total “L” level output current	ΣI_{OL}	—	40	mA	
“H” level output current	I_{OH}	—	–5	mA	Except power supply pins
“H” level average output current	I_{OHAV}	—	–2	mA	Average value (operating current × operating rate) Except power supply pins
Total “H” level output current	ΣI_{OH}	—	–10	mA	
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

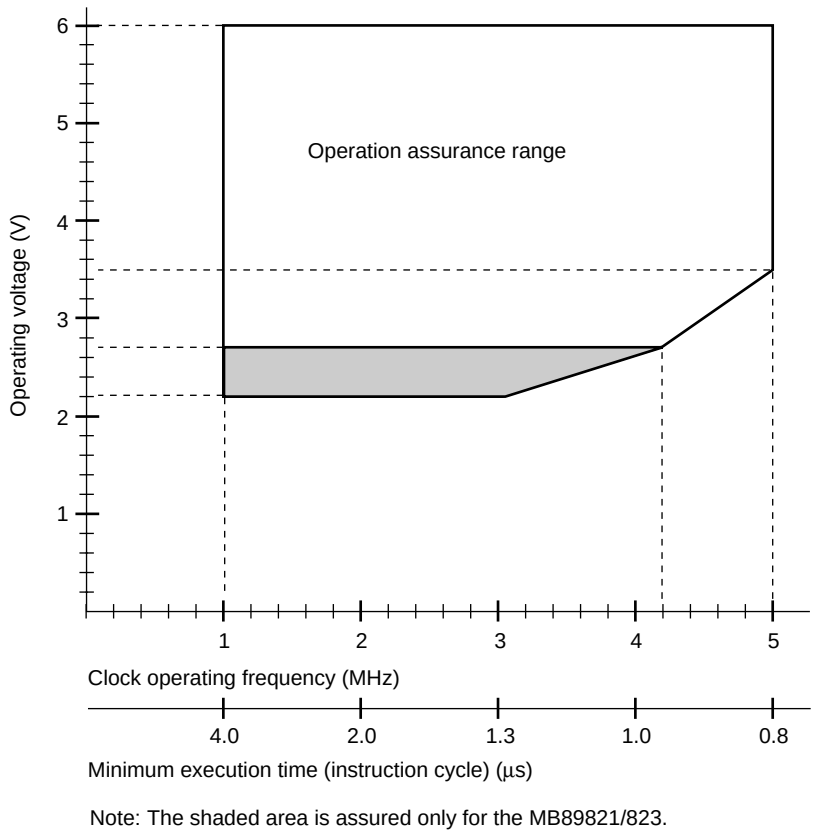
Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range*
		1.5	6.0	V	Retains the RAM state in stop mode
LCD power supply voltage	V3	V_{SS}	6.0	V	V3 pin LCD power supply range. The optimum value is dependent on the element in use.
Operating temperature	T_A	–40	+85	°C	

* : The minimum operating power supply voltage varies with the operating frequency.



Note: The shaded area is assured only for the MB89821/823.

Figure 1 Operating Voltage vs. Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C.

3. DC Characteristics

(V_{CC} = V3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P25, P30 to P33, P40 to P45	—	0.7 V_{CC}*1	—	V_{CC} + 0.3*1	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, INT0, SCK, SI, PWC/INT1	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22 to P25, P30 to P33, P40 to P45	—	V_{CC} – 0.3	—	0.3 V_{CC}*1	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, INT0, SCK, SI, PWC/INT1	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P20 to P25, P00 to P07, P10 to P17	—	V_{SS} – 0.3	—	V_{CC} + 6.0	V	P00 to P07 and P10 to P17 (when selected as ports) for the MB89821/823, and P20 to P25 without pull-up resistor
"H" level output voltage	V_{OH}	P40 to P45	I_{OH} = –2 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P25, P40 to P45	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 4 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	MOD0, MOD1, P30 to P33, P40 to P45	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor for the MB89821/823
		MOD0, MOD1, P00 to P07, P10 to P17, P30 to P33, P40 to P45		—	—	±5	µA	Without pull-up resistor for the MB89P825/PV820
	I_{LI2}	P00 to P07, P10 to P17, P20 to P25	0.0 V < V_I < 6.0 V	—	—	±1	µA	Without pull-up resistor for the MB89821/823
		P20 to P25		—	—	±1	µA	Without pull-up resistor for the MB89P825/PV820

(Continued)

(Continued)

(V_{CC} =V3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R_{PULL}	P20 to P25, P30 to P33, P40 to P45, $\overline{RST}$	V1 = 0.0 V	25	50	100	kΩ	With pull-up resistor
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = +5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG49	V1 to V3 = +5.0 V	—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	Between V3 and V_{SS}	30	60	120	kΩ	
LCD leakage current	I_{LCDL}	V1 to V3, COM0 to COM3, SEG0 to SEG49	—	—	—	±1	µA	
Power supply current*2	I_{CC}	V_{CC}	F_C = 5 MHz t_{inst}*3 = 0.8 µs	—	3.5	5.0	mA	MB89821, MB89823, MB89PV820
				—	4.0	6.5	mA	MB89P825
	I_{CCS}		F_C = 5 MHz t_{inst}*3 = 0.8 µs Sleep mode	—	1.1	1.7	mA	MB89821, MB89823, MB89PV820, MB89P825
	I_{CCH}		T_A = +25°C Stop mode	—	0.1	1	µA	MB89821, MB89823
				—	0.1	10	µA	MB89PV820, MB89P825
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The input voltage to P00 to P07 and P10 to P17 for the MB89P825/PV820 must not exceed the LCD power supply voltage (V3 pin voltage).

*2: The measurement condition of power supply current is as follows: the external clock, open output pins and the external LCD dividing resistor.
In the case of the MB89PV820, the current consumed by the connected EPROM and ICE is not included.

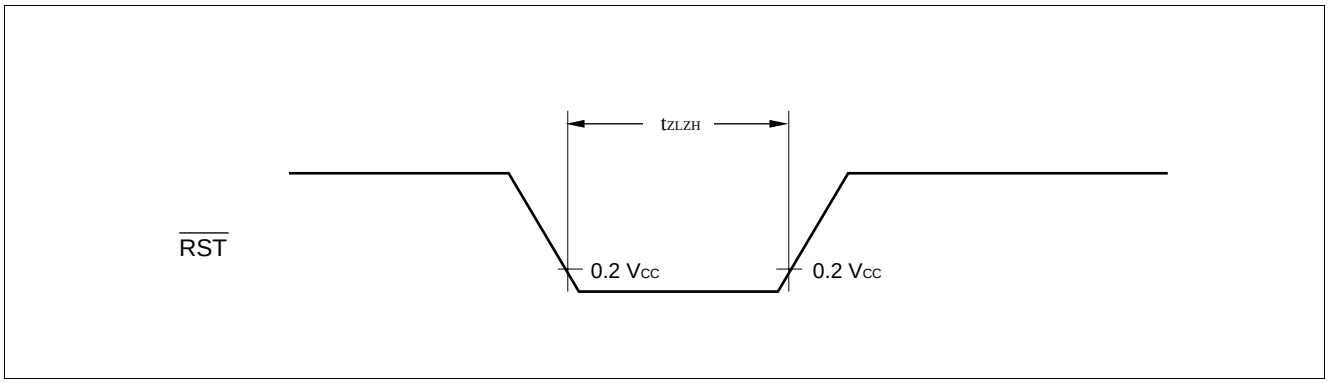
*3: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	ns	

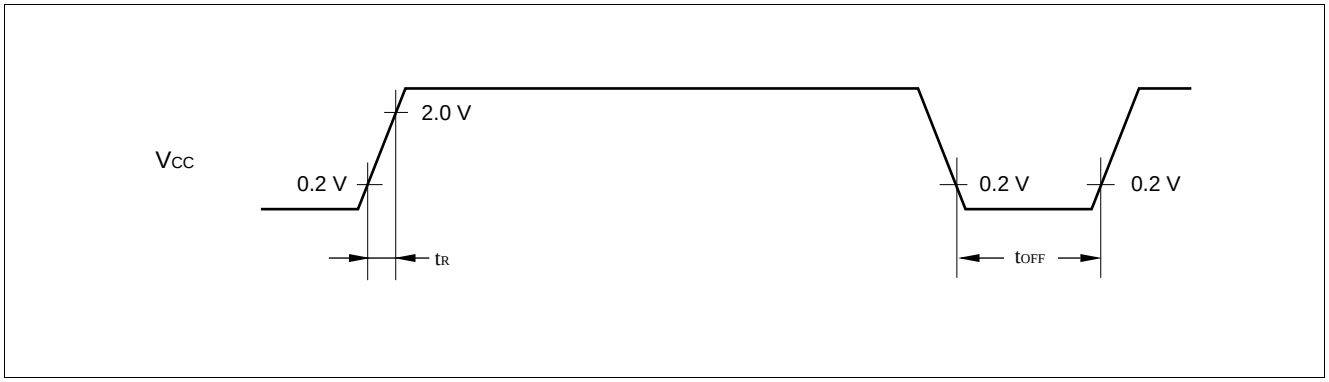


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



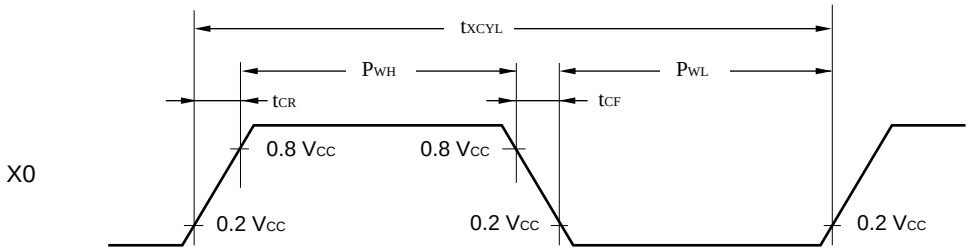
(3) Clock Timing

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

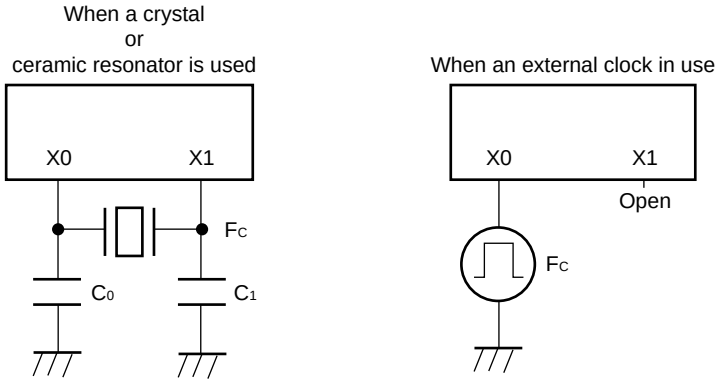
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	1	—	5	MHz	
Clock cycle time	t_{XCYL}			200	—	1000	ns	Crystal or ceramic resonator
Input clock duty ratio*	duty	X0		30	—	70	%	External clock
Input clock rising/ falling time	t_{CR} t_{CF}			—	—	10	ns	External clock

* : duty = P_{WH}/t_{HCYL}, P_{WL}/t_{HCYL}

X0 and X1 Timing and Conditions



Clock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	t_{inst} = 0.8 µs when operating at F_C = 5 MHz

(5) Serial I/O Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

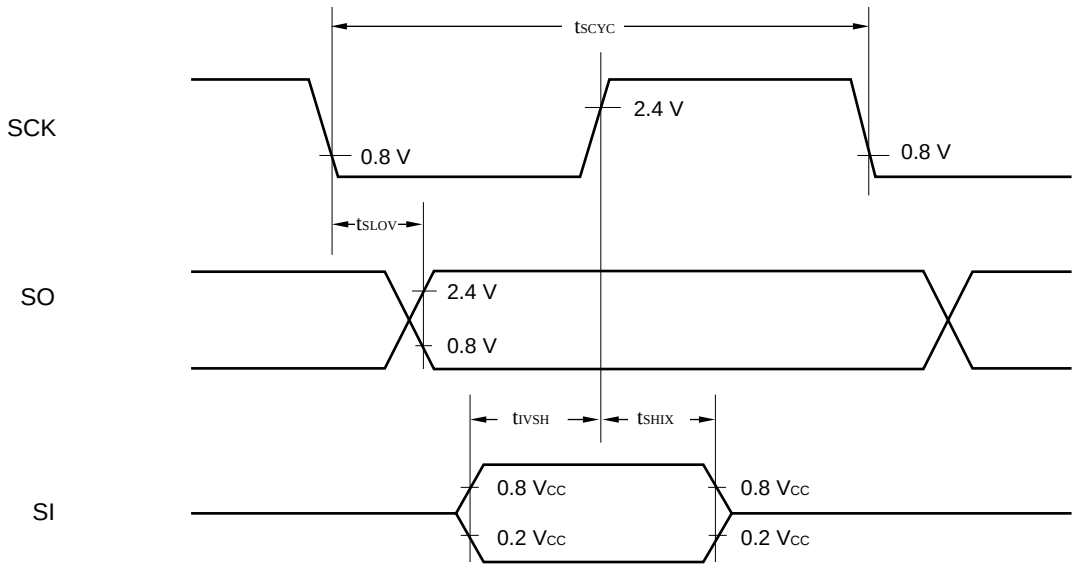
(6) UART Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

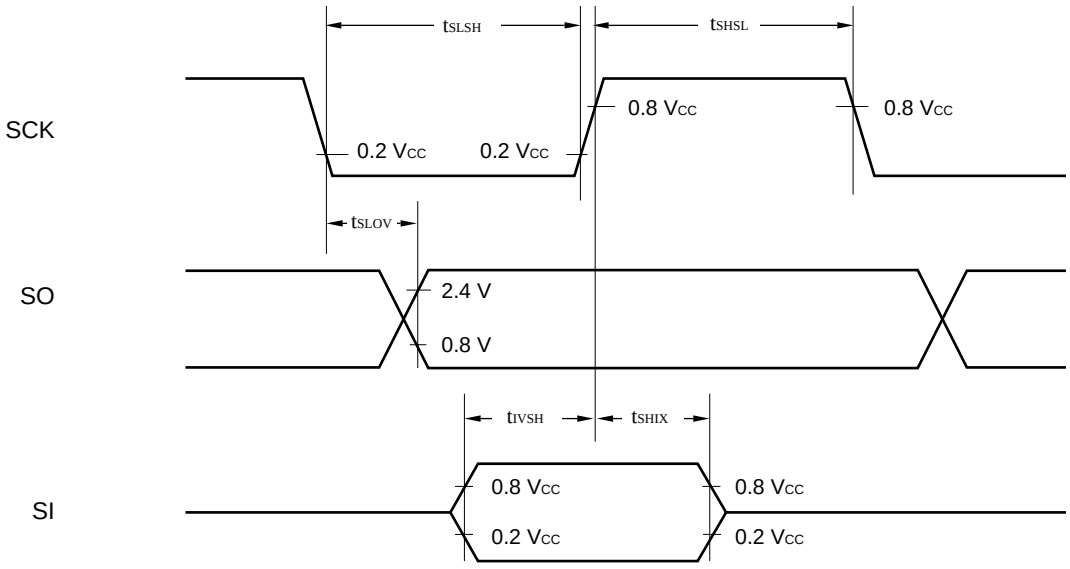
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

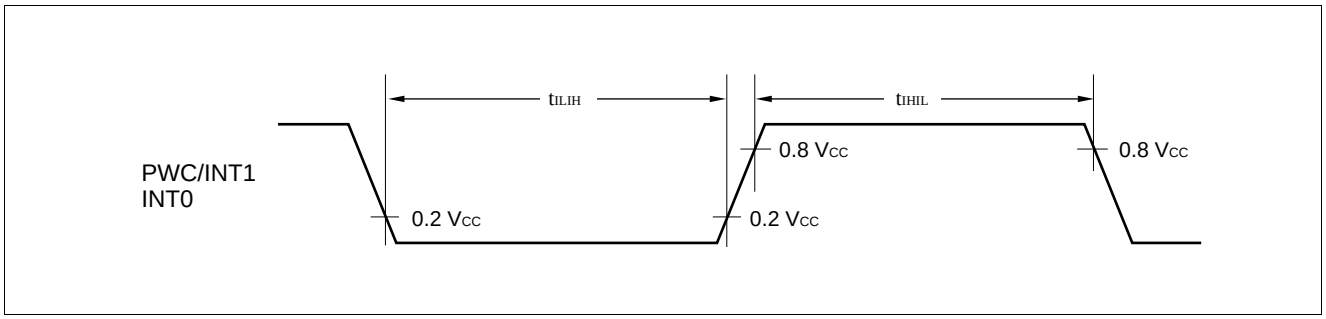


(7) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

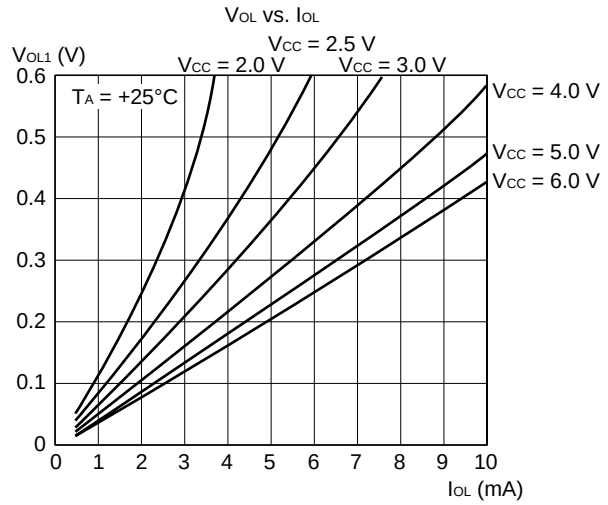
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width	t_{ILIH}	PWC/INT1 INT0	—	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width	t_{IHIL}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

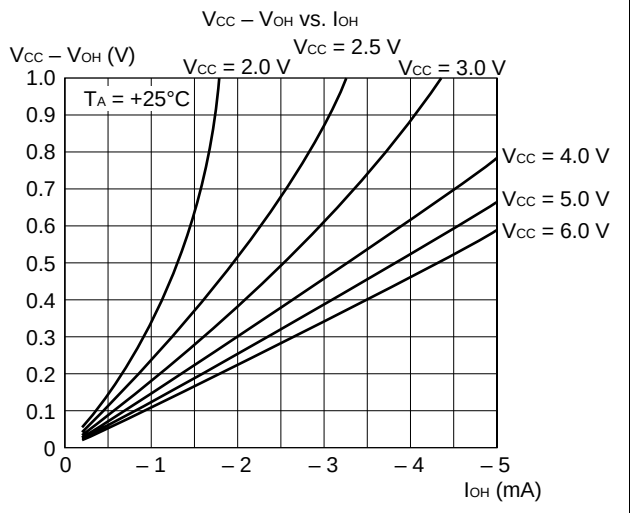


■ EXAMPLE CHARACTERISTICS

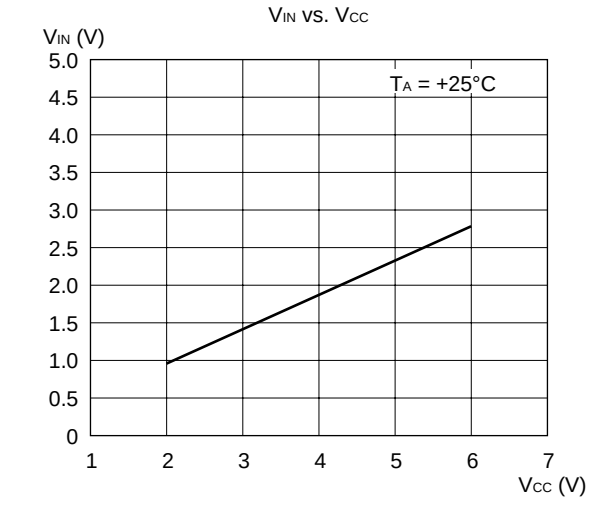
(1) “L” Level Output Voltage



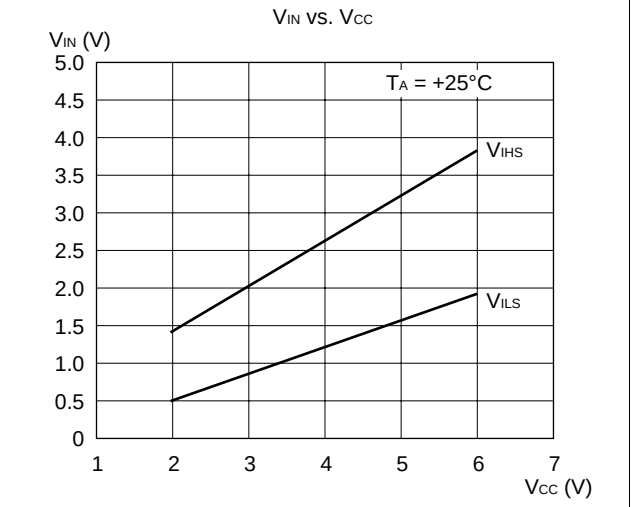
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



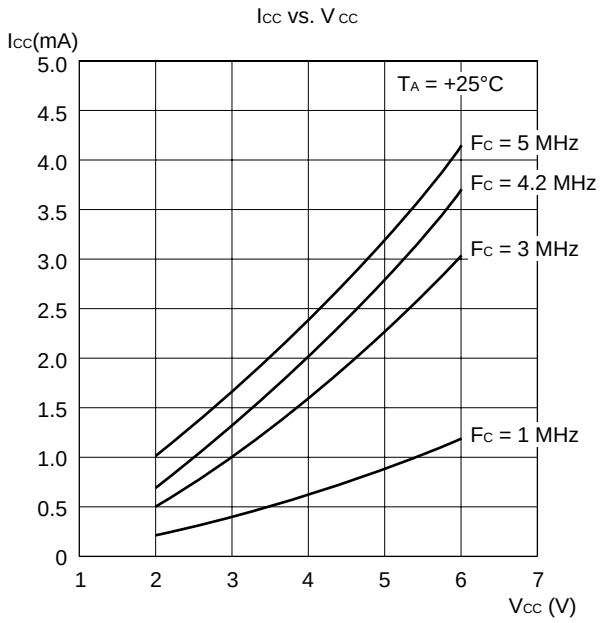
(4) “H” level Input Voltage/“L” Level Input Voltage (CMOS Hysteresis Input)

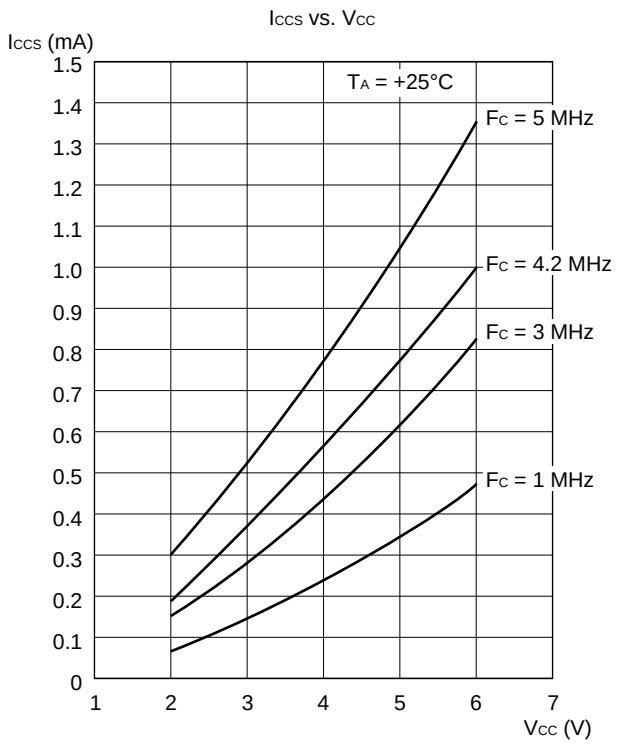


VIHS: Threshold when input voltage in hysteresis characteristics is set to “H” level

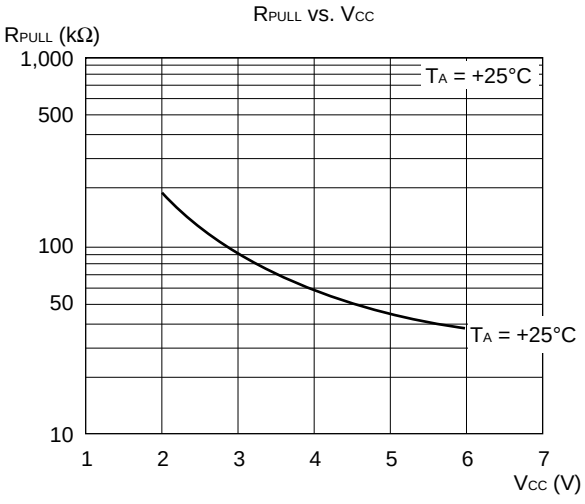
VILS: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)





(6) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

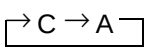
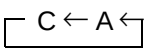
OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes:
- During byte transfer to A, T ← A is restricted to low bytes.
- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 toDF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) +off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89821/823	MB89P825	MB89PV820
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible (Fixed)
1	Pull-up resistors P20 to P25, P30 to P33, P40 to P45	Selectable by pin	Can be set per pin	Without pull-up resistor
2	Power-on reset With power-on reset Without power-on reset	Selectable	Can be set	With power-on reset
3	Oscillation stabilization time selection (F_C = 5 MHz)*1 Approx. $2^{17}/F_C$ (Approx. 26.2 ms) Approx. $2^{13}/F_C$ (Approx. 1.64 ms)	Selectable	Can be set	Oscillation stabilization time Approx. $2^{17}/F_C$ (Approx. 26.2 ms)
4	Reset pin output With reset output Without reset output	Selectable	Can be set	With reset output
5	Segment output switching 50 segments: No port selection 49 segments: Selection of P17 48 segments: Selection of P17 to P16 46 segments: Selection of P17 to P14 42 segments: Selection of P17 to P10 34 segments: Selection of P17 to P10 and P07 to P00	Selectable*2	Can be set*3	Can be set*3

*1: The oscillation settling time is generated by dividing the oscillation clock frequency. Since the oscillation period is not stable immediately after oscillation has been started, therefore, the oscillation settling time in the above list should be regarded as a reference.

*2: Port selection must be same setting of the segment output selection register of LCD controller.

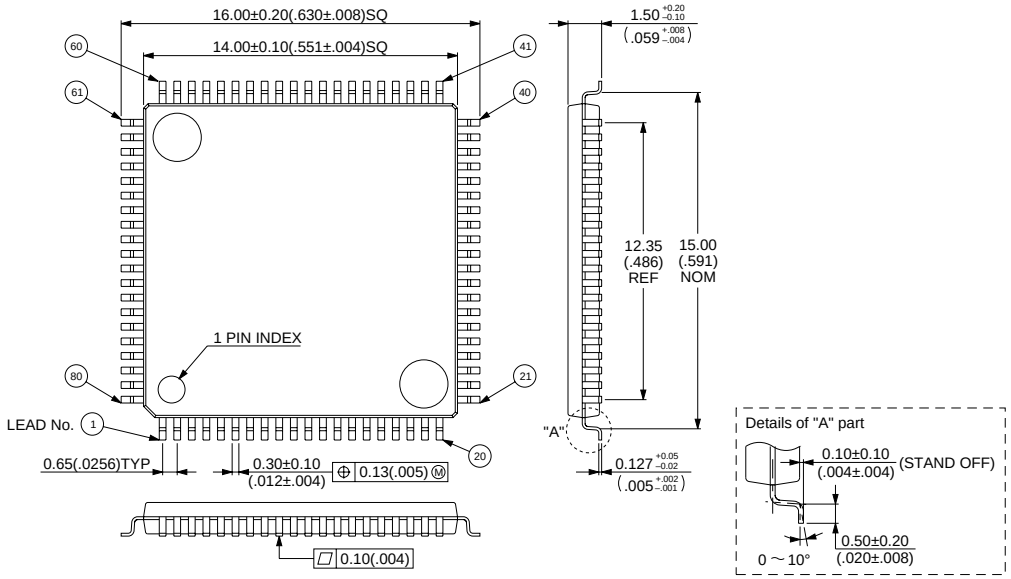
*3: Note that, when ports are set, the input voltage value for the port pins are different from those for mask ROM products.
Ports are set by the register setting of the segment output selection register of LCD controller.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89821PFM MB89823PFM MB89P825PFM	80-pin Plastic QFP (FPT-80P-M11)	
MB89PV820CF	80-pin Ceramic MQFP (MQP-80C-P01)	

■ PACKAGE DIMENSIONS

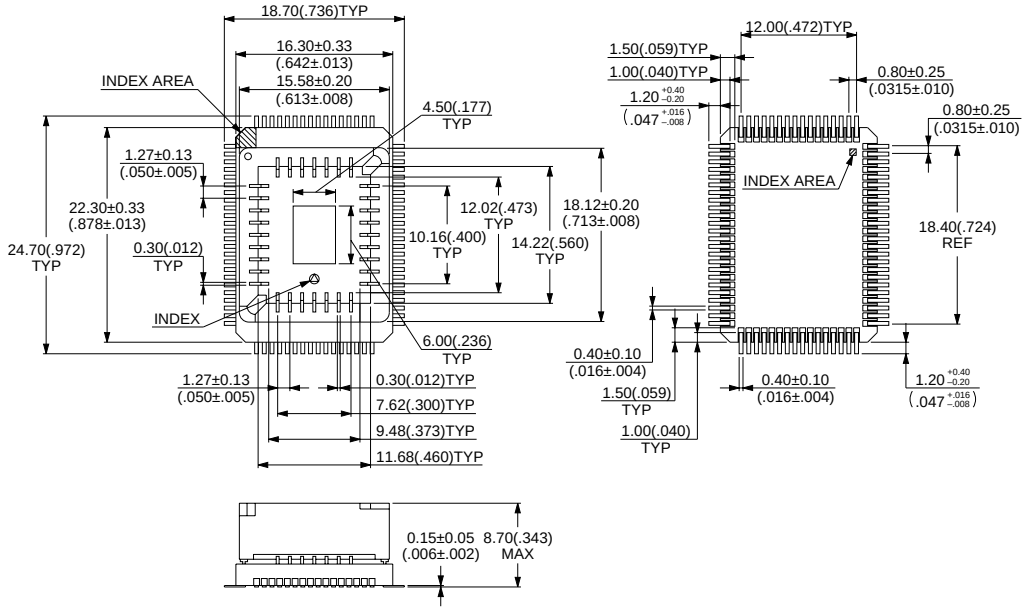
80-pin Plastic QFP
(FPT-80P-M11)



Dimensions in mm (inches)

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80-pin Ceramic MQFP
(MQP-80P-P01)



Dimensions in mm (inches)

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