DS04-21203-4E

FUJITSU

DATA SHEET

MB87076

CMOS PLL FREQUENCY SYNTHESIZER

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER WITH POWER DOWN MODE

The Fujitsu MB87076, fabricated in CMOS technology, is a serial input PLL frequency synthesizer that features a power down mode.

The MB87076 contains an inverter for the oscillator, 14-bit shift register, 18-bit shift register, 1-bit control register, 14-bit latch, 18-bit latch, programmable divider (binary 11-bit programmable counter and binary 7-bit swallow counter), programmable reference divider (binary 14-bit programmable reference counter), phase detector, charge pump, control generator for two modulus prescaler, and power down circuit.

The MB87076 selects either operation mode or power down mode, depending on the PS input signal level. When the device begins operation, phase f_r and f_v are synchronized.

- Single power supply voltage: V_{DD} = 2.7 to 5.5V
- Wide temperature range: T_A = −40 to +85°C
- Low power supply current: 3mA typ, (100μA in power down mode)
- On-chip inverter for oscillator
- Programmable reference divider with input amplifier
  Programmable divider with input amplifier
- 2 Types of phase detector output
  - On-chip charge pump output
  - Output for external charge pump
- On-chip power down circuit
- 16-pin standard dual-in-line package (Suffix: -P)
  16-pin standard flat package (Suffix: -PF)
- Pulse swallow function

  $f_{VCO} = [(N \times M) + A] \times f_{OSC} \div R$
  f_{VCO} : VCO (Voltage Controlled Oscillator) output frequency
  N : Preset divide factor of binary 11-bit programmable counter (16 to 2047)
  M : Preset modulus factor of external two modulus prescaler (64 in 64/65 mode, 128 in 128/129 mode)
  A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
  f_{OSC} : Output frequency of an external oscillator
  R : Preset divide factor of binary 14-bit programmable reference counter (8 to 16383)

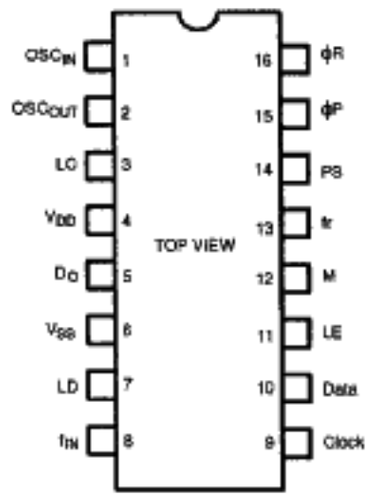


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} −0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} −0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} −0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Open Drain Output	V_{OP}	V_{SS} −0.5 to V_{DD} +3.0	V
Operating Temperature	Ta	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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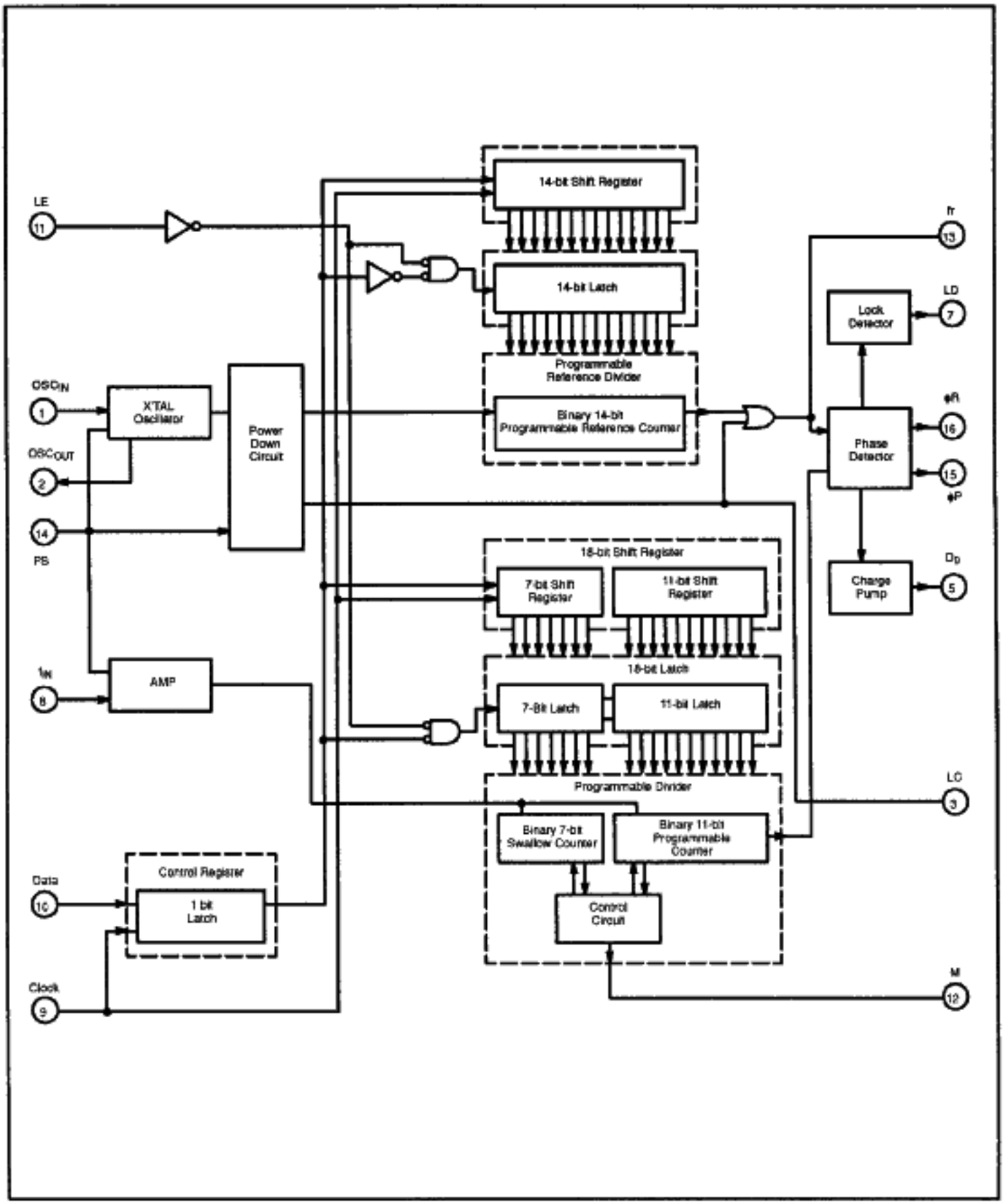
BLOCK DIAGRAM



PIN DESCRIPTION

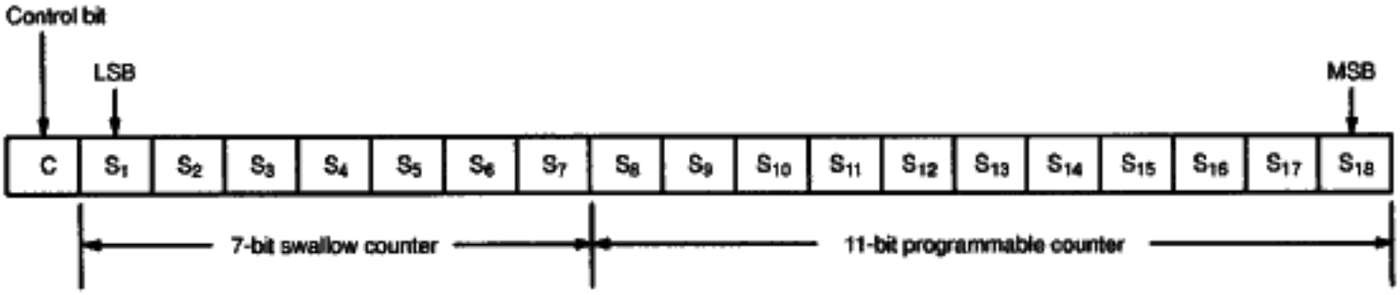
Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Pin for crystal oscillator The input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as an AC coupling when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Pin for crystal oscillator The output of the inverting amplifier. This pin should be connected to ground when an external oscillator is used.
3	LC	O	Output pin for loop control signal This pin is at high level when the operation mode is selected. It is at low level when the power down mode is selected.
4	V_{DD}	-	Power supply voltage
5	D_O	O	Three-state charge pump output The mode of D_O is changed by the combination of the programmable reference divider output frequency (f_r) and the programmable divider output frequency (f_P) as listed below: $f_r > f_P$: D_O = H level $f_r = f_P$: D_O = High-impedance level $f_r < f_P$: D_O = L level
6	V_{SS}	-	Ground
7	LD	O	Output of phase comparator This pin is at low level when f_r and f_P are coherent, and then the loop is locked. Otherwise it outputs high level.
8	f_{IN}	I	Input for binary 7-bit swallow counter and binary 11-bit programmable counter from VCO This input involves the bias circuit and the amplifier. The connection with the dual modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 18-bit shift register and 14-bit shift register Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for shift registers This data is the divide ratio of the divider, which is provided from the corresponding shift register. The last bit of the data is the control bit which specified the destination of the shift register. The data is transferred to the 14-bit shift register when the bit is at high level, and to the 18-bit shift register when it is at low level.
11	LE	I	Load enable input When this pin is at high level, the data latched from the shift register is transferred to the programmable reference divider or the programmable divider, depending on the control bit data.
12	M	O	Control output for external dual modulus prescaler The connection should be a DC connection. Pulse swallow function: (Example) MB501: M = High: Preset modules factor 64 or 128 M = Low: Preset modules factor 65 or 129
13	f_r	O	Monitors output of the phase comparator input Also monitors the output of the reference divider.
14	PS	I	Power down control input When this pin is at high level, the operation mode is selected. When this pin is at low level, the power down mode is selected.
15 16	ϕP ϕR	O O	Output for external charge pump ϕR ϕP $f_r > f_P$: Low Low $f_r = f_P$: Low High-impedance $f_r < f_P$: High High-impedance

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER

Binary serial data is input to the Data pin. Each rising edge of the clock shifts one bit of the data into the shift registers and the control register. Input data consists of 18-bit data and 1-bit of the control bit data. In this case, the control bit is set at low level. S_1 to S_7 is used for setting the divide ratio of the 7-bit swallow counter and S_8 to S_{18} is used for setting the divide ratio of the 11-bit programmable counter.

The data format is shown below.



7-bit Swallow Counter Data Input

Divide Factor A	S_7	S_6	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide factor: 0 to 127

11-bit Programmable Divider Data Input

Divide Factor N	S_{18}	S_{17}	S_{16}	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

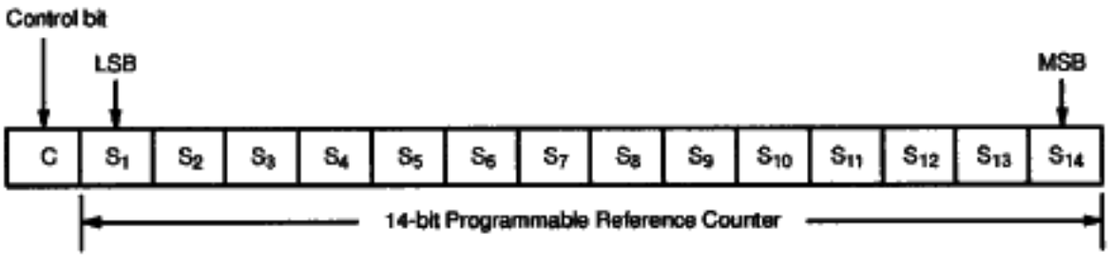
Note: Divide factor less than 5 is prohibited
Divide factor: 5 to 2047

FUNCTIONAL DESCRIPTION (Continued)

SERIAL DATA INPUT FOR PROGRAMMABLE REFERENCE DIVIDER

Binary serial data is input to the Data pin. Each rising edge of the clock shifts one bit of the data into the shift registers and control register. Input data consists of 14-bit data and 1-bit of the control bit data. In this case, the control bit is set at high level.

The data format is shown below.

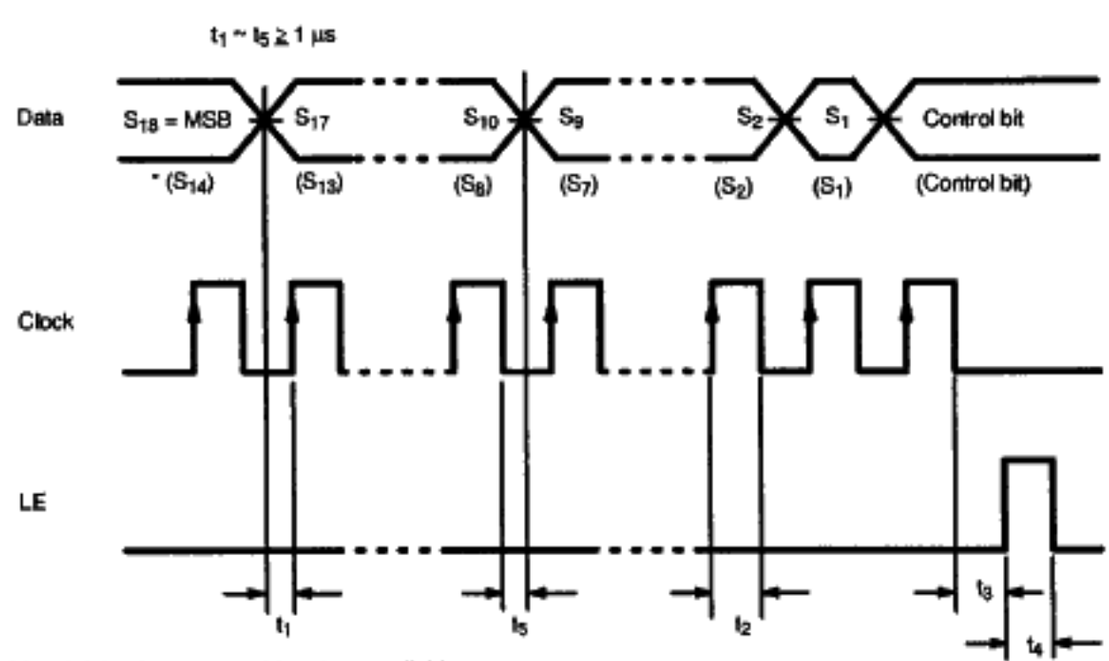


14-bit Programmable Divider Data Input

Divide Factor R	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

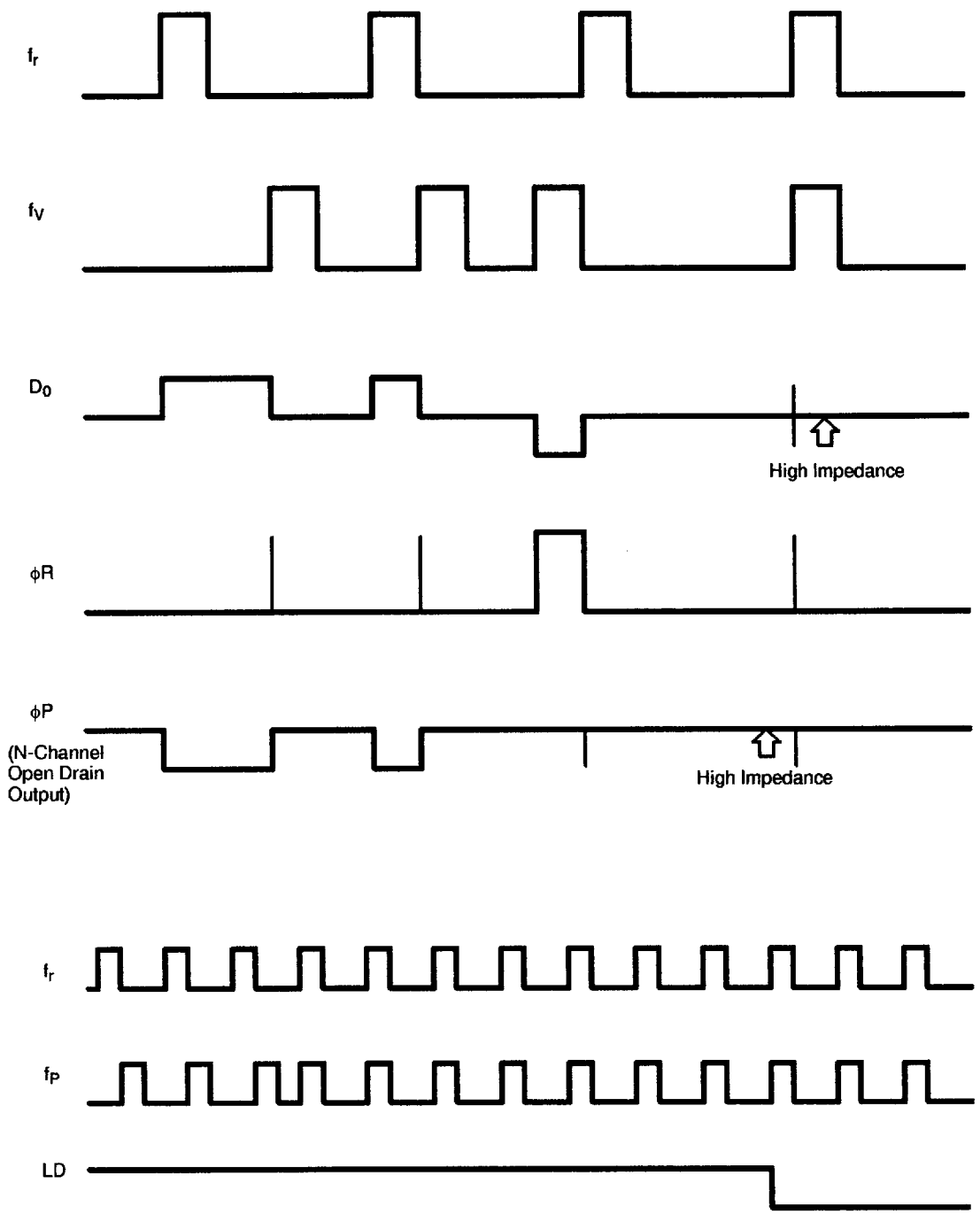
Note: Divide factor less than 8 is prohibited
Divide factor: 8 to 16383

Fig. 1 – SERIAL DATA INPUT TIMING



* Input data of programmable reference divider.

Fig. 2 – PHASE DETECTOR WAVEFORM



Note: LD is set at High level when $f_r \neq f_v$ (unclock condition).
LD is set at Low level when $f_r = f_v$ (lock condition).

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POWER DOWN OPERATION DESCRIPTION

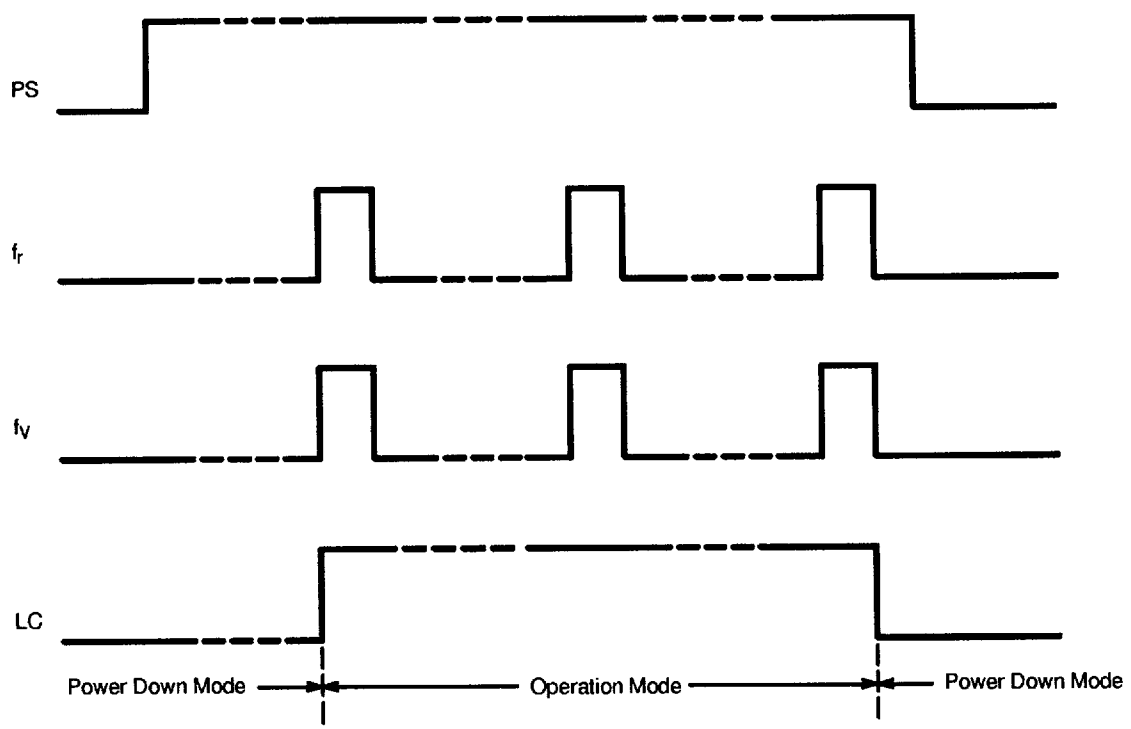
The MB87076 has a power down function which selects the operation mode or power down mode depending on the PS input signal level. When PS is set at low level, the power down mode is selected. During the power down mode, internal dividers stop operation. Thus, very low power supply consumption is achieved and the LC pin is set at Low level.

Then the PS level goes High with the frequency of VCO as almost the same value as that under the condition of phase lock, the following sequence is taken:

1) Programmable divider starts operation
2) f_V is output with some delay
3) Programmable reference divider starts operation when it receives f_V
4) f_r is output
5) LC is forced to set at High level (normal operation mode is selected)

When the f_r outputs immediately after f_P and goes into the phase detector, the phase lock condition is obtained just after the first clock. When PS is set at Low level again, internal dividers stop the operation. The internal condition is then reset.

Fig. 3 – POWER DOWN MODE



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}	—	V_{DD}	V
Output Temperature	T_A	-40	—	+85	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.0V, T_A = -40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	2.1	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	0.9	
Input Sensitivity	f_{IN}	Vf_{PP}	Amplitude in AC coupling, sine wave	0.5	—	—	V_{P-P} Sine
	OCS_{IN}	V_{SIN}		0.5	—	—	
High-level Input Current	Except f_{IN} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	—	-1.0	—	
Input Current	f_{IN}	If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±30	—	µA
	OCS_{IN}	I_{XIN}		—	±30	—	
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95	—	—	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	—	—	0.05	
Low-level Output Voltage	ϕP	V_{OLV}	I_{OL} = 0.8mA	—	—	0.80	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	2.50	—	—	V
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	—	—	0.50	
High-level Output Current	Except ϕP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	-0.5	—	—	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	0.5	—	—	
N-channel Open Drain Cut Off Current		I_{OFF}	$V_O = V_{DD}$ +3.0V	—	1.0	—	µA
Power Supply Current*1		I_{DDOP}	Operation mode	—	2.50	—	mA
		I_{DDPS}	Power down mode	—	—	80	µA
Max. Operating Frequency of Programmable Reference Divider		f_{MAXd}	—	10	20	—	MHz
Max. Operating Frequency of Programmable Divider		f_{MAXp}	—	10	20	—	MHz

Note: *1: f_{IN} = 8.0MHz, 11.5MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
PS is set at high level; all other inputs are set at low level. Outputs are open.

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ELECTRICAL CHARACTERISTICS (Continued)

(V_{SS} = 0V, V_{DD} = 5.0V, T_A = −40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{IN} and OSC_{IN}	V_{IH}	—	3.5	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	1.5	
Input Sensitivity	f_{IN}	Vf_{IN}	Amplitude in AC coupling, sine wave	0.8	—	—	V_{P-P} Sine
	OCS_{IN}	V_{SIN}		1.0	—	—	
High-level Input Current	Except f_{IN} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	—	1.0	—	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	—	−1.0	—	
Input Current	f_{IN}	If_{IN}	$V_{IN} = V_{SS}$ to V_{DD}	—	±50	—	µA
	OCS_{IN}	I_{XIN}		—	±50	—	
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95	—	—	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	—	—	0.05	
Low-level Output Voltage	ϕP	V_{OLV}	I_{OL} = 1mA	—	—	0.50	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	4.50	—	—	V
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	—	—	0.50	
High-level Output Current	Except ϕP and OSC_{OUT}	I_{OH}	V_{OH} = 4.0V	−1.0	—	—	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	1.0	—	—	
N-channel Open Drain Cut Off Current		I_{OFF}	$V_O = V_{DD}$ +3.0V	—	1.0	—	µA
Power Supply Current*1		I_{DDOP}	Operation mode	—	3.0	—	mA
		I_{DDPS}	Power down mode	—	—	100	µA
Max. Operating Frequency of Programmable Reference Divider		$f_{MAX}d$	—	15	25	—	MHz
Max. Operating Frequency of Programmable Divider		$f_{MAX}p$	—	10	25	—	MHz

Note: *1: f_{IN} = 8.0MHz, 11.5MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
PS is set at high level; all other inputs are set at low level. Outputs are open.

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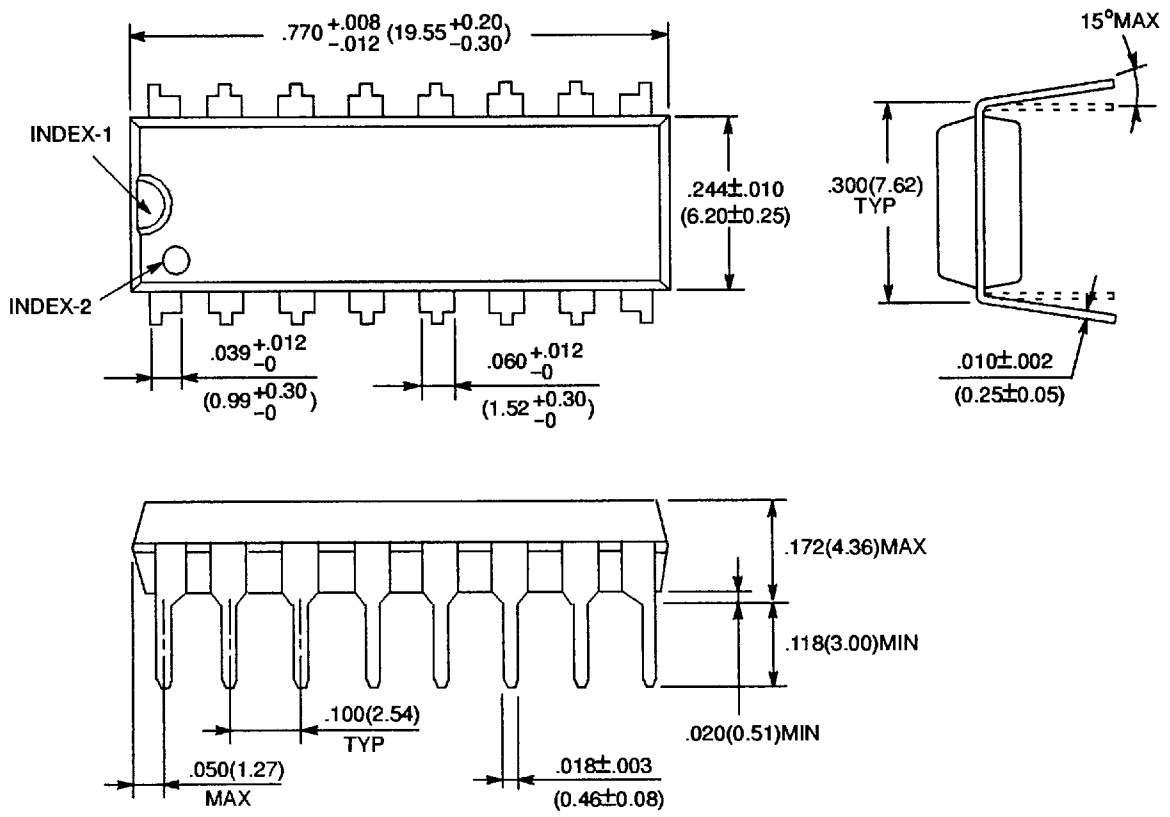
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

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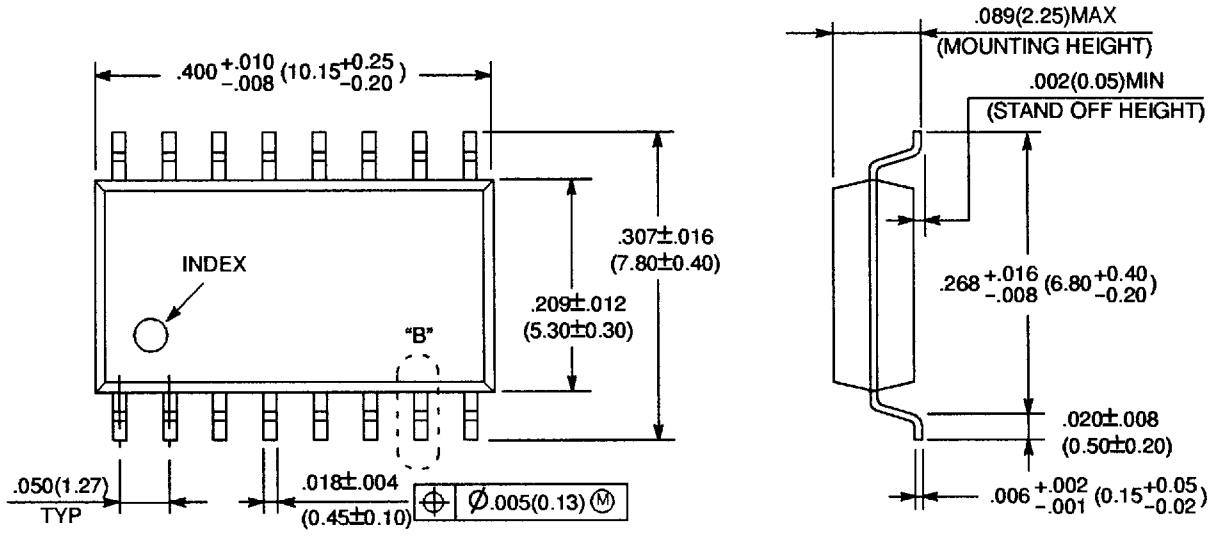
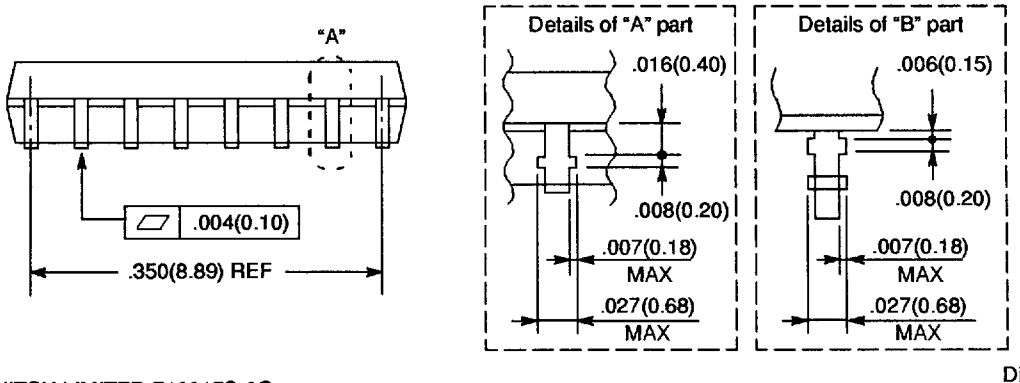
PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)





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Dimensions in
inches (millimeters)

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