Rev 1; 12/08

16-Bit Mixed-Signal Microcontroller with LCD Interface

MAXQ2010

General Description

The MAXQ2010 microcontroller is a low-power, 16-bit device that incorporates a high-performance, 12-bit, multichannel ADC and a liquid-crystal display (LCD) interface. A combination of high performance, low power, and mixed-signal integration makes the MAXQ2010 ideal for a wide variety of applications.

The MAXQ2010 has 64KB of flash memory, 2KB of RAM, three 16-bit timers, and two universal synchronous/asynchronous receiver/transmitters (USARTs). Flash memory aids prototyping and is available for mass production. Mask ROM versions are available for large production volumes when cost is a critical factor. The microcontroller runs from a 2.7V to 3.6V operating supply. For the ultimate in low-power performance, the MAXQ2010 includes a low-power sleep mode, the ability to selectively disable peripherals, and multiple power-saving operating modes.

Applications

- Battery-Powered and Portable Devices
- Portable Medical Equipment
- Blood Glucose Meters
- Electrochemical and Optical Sensors
- Industrial Control
- Data-Acquisition Systems and Data Loggers
- Home Appliances
- Consumer Electronics
- Thermostats/Humidity Sensors
- Security Sensors
- Gas and Chemical Sensors
- HVAC
- Smart Transmitters
- Medical Instrumentation

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXQ2010-RFX+	-40°C to +85°C	100 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Application Circuit, Pin Configuration, and Selector Guide appear at end of data sheet.

Features

- **High-Performance, Low-Power, 16-Bit MAXQ® RISC Core**
- **DC to 10MHz Operation, Approaching 1MIPS per MHz**
- **2.7V to 3.6V Operating Voltage**
- **33 Instructions, Most Single Cycle**
- **Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement**
- **16-Level Hardware Stack**
- **16-Bit Instruction Word, 16-Bit Data Bus**
- **16 x 16-Bit General-Purpose Working Registers**
- **Optimized for C-Compiler (High-Speed/Density Code)**
- **On-Chip FLL Reduces External Clock Frequency**
- **Memory Features**
  - 64KB Flash Memory (In-Application and In-System Programmable)
  - 2KB Internal Data RAM
  - JTAG Bootloader for Programming and Debug
- **Peripheral Features**
  - 12-Bit SAR ADC with Internal Reference and Autoscan
    - Eight Single-Ended or Four Differential Inputs
    - Up to 312.5ksps Sample Rate
  - Supply Voltage Monitor with Adjustable Threshold
  - One-Cycle, 16 x 16 Hardware Multiply/Accumulate with 48-Bit Accumulator
  - Three 16-Bit Programmable Timers/Counters with PWM Outputs
  - 32-Bit Binary Real-Time Clock with Digital Trim Capability
  - Integrated LCD
    - 160 Segments
    - No External Resistors Required
  - Two USARTs, I^2C Master/Slave, and SPI™ Master/Slave Communications Ports
  - On-Chip Power-On Reset/Brownout Reset
  - Programmable Watchdog Timer
- **Low Power Consumption**
  - 1mA (typ) at 1MHz Flash Operation at 2.7V
  - 370nA (typ) in Stop Mode
  - Low-Power Power-Management Mode (PMM)

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

SPI is a trademark of Motorola, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on All Pins (including AVDD, DVDD) Relative to Ground .....-0.5V to +3.6V
Voltage Range on Any Pin Relative to Ground Except AVDD, DVDD .....-0.5V to (V_{DVDD} + 0.5V)
Operating Temperature Range .....-40°C to +85°C
Continuous Output Current
Any Single I/O Pin 20mA
All I/O Pins Combined.....100mA
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	V_{DVDD}		2.7		3.6	V
Digital Supply Voltage Output	V_{REGOUT}	(Note 2)		1.8		V
Analog Supply Voltage	V_{AVDD}	V_{AVDD} = V_{DVDD}	2.7		3.6	V
Ground	GND	AGND = DGND	0		0	V
Digital Power-Fail Reset Voltage	V_{RST}	Monitors V_{DVDD}	2.55	2.6	2.65	V
Active Current, FLL Disabled (Note 3)	I_{DD_HFX1}	f_{CK} = 10MHz, V_{DVDD} = V_{AVDD} = 2.7V, FREQMD = 0		3.1	3.75	mA
	I_{DD_HFX2}	f_{CK} = 10MHz, V_{DVDD} = V_{AVDD} = 3.6V, FREQMD = 0 (Note 4)		3.2	4.0	
Active Current, FLL Enabled (Note 5)	I_{DD1_FLL}	Divide-by-1 mode, FREQMD = 0		3.15	4	mA
	I_{DD2_FLL}	Divide-by-2 mode, FREQMD = 0 (Note 4)		2.9	3.6	
	I_{DD3_FLL}	Divide-by-4 mode, FREQMD = 1 (Note 4)		2.25	3	
	I_{DD4_FLL}	Divide-by-8 mode, FREQMD = 1 (Note 4)		1.4	2	
	I_{DD5_FLL}	PMM mode, FREQMD = 1 (Note 4)		0.5	0.7	
Stop-Mode Current (Note 6)	I_{STOP_1} (Note 7)	T_A = +25°C		0.37	4	µA
		T_A = +85°C		0.68	6.5	
	I_{STOP_2} (Note 8)	T_A = +25°C		0.94	5	
		T_A = +85°C		1.3	6.5	
	I_{STOP_3} (Note 9)	T_A = +25°C		195	295	
		T_A = +85°C		225	335	
Stop-Mode Resume Time (Note 4)	t_{STOP_1}	Internal regulator on		$4t_{CLCL}$		µs
	t_{STOP_2}	Internal regulator off, brownout or SVM on, SVMSTOP = 1		30	160	
	t_{STOP_3}	Internal regulator, brownout, and SVM off		30	320	
Input Low Voltage on HFXIN and 32KIN	V_{IL1}		DGND		0.20 x V_{DVDD}	V
Input Low Voltage on All Other Pins	V_{IL2}		DGND		0.30 x V_{DVDD}	V

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage on HFXIN and 32KIN	V_{IH1}		0.75 x V_{DVDD}		V_{DVDD}	V
Input High Voltage on All Other Pins	V_{IH2}		0.70 V_{DVDD}		V_{DVDD}	V
Input Hysteresis (Schmitt)	V_{IHYS}			0.18		V
Output Low Voltage for All Port Pins (Note 10)	V_{OL}	I_{OL} = +4mA	DGND		0.4	V
Output High Voltage for All Port Pins (Note 10)	V_{OH}	I_{OH} = -4mA	V_{DVDD} - 0.4			V
I/O Pin Capacitance	C_{IO}	Guaranteed by design			15	pF
I/O Pin Capacitance SCL, SDA (Note 11)	C_{IO_I2C}	Guaranteed by design			10	pF
$\overline{RST}$ Pullup Resistance	R_{RST}		30		85	kΩ
Input Low Current for $\overline{RST}$ Pin	I_{IL1}	V_{IN} = 0.4V	-85		-30	µA
Input Low Current for All Other Pins	I_{IL2}	V_{IN} = 0.4V	-85		-30	µA
Input Leakage Current	I_L	Internal pullup disabled	-150		+150	nA
Input Pullup Resistor	R_{PU}		30		85	kΩ
CLOCK SOURCE						
External Clock Frequency	f_{HFIN}		DC		10	MHz
External Clock Period	t_{CLCL}		100			ns
External Clock Duty Cycle	t_{XCLK_DUTY}		40		60	%
System Clock Frequency	f_{CK}		DC		10	MHz
FREQUENCY-LOCKED LOOP (FLL)						
FLL Output Frequency	f_{FLL}	f_{32KIN} = 32.768kHz		8.4		MHz
FLL Output Frequency Delta	Δf_{FLL}	f_{32KIN} = 32.768kHz		1.5	±5	%

Note 1: Specifications to -40°C are guaranteed by design and are not production tested.

Note 2: Typical value presented for reference only. Do not draw current from this pin.

Note 3: FLL disabled. Crystal connected across HFXIN and HFXOUT. Operating in divide-by-1 mode. Measured on the DVDD pin and part executing program code from flash. All inputs are connected to GND or DVDD. Outputs do not source/sink any current. Timer B enabled.

Note 4: This parameter is guaranteed by design and is not production tested.

Note 5: FLL enabled. f_{32KIN} = 32.768kHz, HFXIN = disconnected, FLL = 8.39MHz, measured on the DVDD pin, part executing program code from flash. All inputs are connected to GND or DVDD. Outputs do not source/sink any current. Timer B enabled.

Note 6: I_{STOP} is the total current into the device when the device is in stop mode. This includes both the digital and analog current (current into DVDD and AVDD).

Note 7: Regulator, brownout monitor, LCD, and RTC disabled.

Note 8: Regulator, brownout monitor, and LCD disabled; RTC enabled.

Note 9: Regulator enabled, brownout monitor enabled, and LCD and RTC disabled.

Note 10: $I_{OH(MAX)}$ + $I_{OL(MAX)}$ for all outputs combined should not exceed 35mA to meet the specification.

Note 11: When DVDD is switched off, SDA and SCL may obstruct the line.

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RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLASH PROGRAMMING						
System Clock During Flash Programming/Erase			2			MHz
Flash Erase Time		Mass erase		24		ms
		Page erase		24		
Flash Programming Time per Word (Note 12)				66		µs
Write/Erase Cycles			20,000			Cycles
Data Retention		T_A = +25°C	100			Years
ANALOG-TO-DIGITAL CONVERTER (Note 13)						
Serial Clock Frequency	f_{SCLK}		0.1		5	MHz
Input Voltage Range	V_{AIN}	Unipolar (single-ended)	0		V_{REF}	V
		Bipolar (differential) (Note 14)	$-V_{REF}/2$		$+V_{REF}/2$	
Analog Input Capacitance	C_{AIN}			16		pF
Current Consumption (Note 4)	I_{AVDD1}	f_{SCLK} = 5MHz, internal reference		1.9	2.5	mA
	I_{AVDD2}	f_{SCLK} = 5MHz, external reference (internal reference disabled)		1.1	1.3	
ANALOG-TO-DIGITAL CONVERTER PERFORMANCE (V_{REF} = V_{AVDD}, 0.1µF capacitor on V_{REF}, f_{SCLK} = 5MHz)						
Resolution			12			Bits
Integral Nonlinearity	INL			±1	±2	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error	VOS				±2	LSB
Offset Temperature Coefficient				±0.5		ppm/°C
Gain Error					±1	%
Gain Temperature Coefficient				±0.5		ppm/°C
Signal-to-Noise Plus Distortion	SINAD	f_{IN} = 1kHz	65			dB
Spurious-Free Dynamic Range	SFDR	f_{IN} = 1kHz	68			dB
Throughput		16 SCLK samples			312.5	ksps
Conversion Time	t_{CONV}	Not including t_{ACQ}	2.6			µs
ADC Setup Time	t_{ADC_SETUP} (Note 15)				4	µs
Input Leakage Current	I_{ILA}	Shutdown or conversion stopped, ANx and V_{AEREF}			±1	µA
Autoscan Throughput		All channels active			39	ksps per channel
ANALOG-TO-DIGITAL CONVERTER REFERENCE						
Internal Reference Voltage	V_{AIREF}		1.47	1.5	1.53	V
Internal Reference Voltage Startup Time	t_{AIREF}				50	µs

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Reference Voltage Input	V_{AEREF}		0.9		V_{AVDD} + 0.05	V
Internal Reference Voltage Drift	V_{ADRIFT}	Guaranteed by design			±50	ppm/°C
Reference Settle Time (Switching ADC Reference from Either Internal or External Reference to AVDD) (Note 16)	t_{AAVDD_SETUP} (Note 17)				4	Samples
SUPPLY VOLTAGE MONITOR						
Supply Voltage Set Point	V_{SVM}		2.7		3.5	V
Supply Voltage Increment Resolution (Note 18)	SV_{INC}		0.08	0.1	0.12	V
Supply Voltage Default Set Point				2.7		µA
Supply Voltage Monitor Current Consumption	I_{SVM}			20		µs
Supply Voltage Monitor Setup Time (Time from Supply Voltage Monitor Enabled to SVMRDY Is Set to 1) (Note 18)	t_{SVM_SU}			15	25	µs
REAL-TIME CLOCK						
RTC Input Frequency	f_{32KIN}	32kHz watch crystal		32,768		Hz
RTC Operating Current	I_{RTC}	V_{DVDD} = 2.7V, guaranteed by design		0.45	0.7	µA
		V_{DVDD} = 3.6V		0.5	0.8	
LCD						
LCD Reference Voltage	V_{LCD}		V_{DVDD}		3.6	V
LCD Bias Voltage 1	V_{LCD1}	1/3 bias	V_{ADJ} + 2/3 (V_{LCD} - V_{ADJ})			V
LCD Bias Voltage 2	V_{LCD2}	1/3 bias	V_{ADJ} + 2/3 (V_{LCD} - V_{ADJ})			V
LCD Adjustment Voltage	V_{ADJ}	Guaranteed by design	0		0.4 x V_{LCD}	V
LCD Bias Resistor	R_{LCD}			40		kΩ
LCD Adjustment Resistor	R_{LADJ}	LRA[3:0] = 15		80		kΩ
LCD Segment and COM Voltage (Note 18)	V_{SEGxx}	Pin is driven at V_{LCD} = 3V, I_{SEGxx} = -3µA	V_{LCD} - 0.02		V_{LCD}	V
		Pin is driven at V_{LCD1} = 2V, I_{SEGxx} = -3µA	V_{LCD1} - 0.02		V_{LCD1} + 0.02	
		Pin is driven at V_{LCD2} = 1V, I_{SEGxx} = -3µA	V_{LCD2} - 0.02		V_{LCD2} + 0.02	
		Pin is driven at V_{ADJ} = 0V, I_{SEGxx} = -3µA	-0.1		+0.1	
LCD Output Rise Time	t_{LCD_RISE}	COM output load = 5000pF, SEG output load = 200pF, V_{LCD} = 3.3V			200	µs

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RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI (See Figures 1 and 2)						
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CK}/8$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$(t_{MCK}/2)$ - 25			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}	C_L = 50pF	$(t_{MCK}/2)$ - 25			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$(t_{MCK}/2)$ - 25			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	t_{MIS}		25			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK Inactive to MOSI Inactive	t_{MLH}		$(t_{MCK}/2)$ - 25			ns
$\overline{SSEL}$ Active to First Shift Edge	t_{SSE}		$4t_{CK}$			ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		20			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		t_{CK} + 25			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				$3t_{CK}$ + 25	ns
$\overline{SSEL}$ Inactive	t_{SSH}		t_{CK} + 25			ns
SCLK Inactive to $\overline{SSEL}$ Rising	t_{SD}		t_{CK} + 25			ns
MISO Output Disabled After $\overline{SSEL}$ Edge Rise	t_{SLH}				$2t_{CK}$ + 50	ns

Note 12: Programming time does not include overhead associated with the utility ROM interface.

Note 13: V_{REF} = V_{AVDD}.

Note 14: The operational input voltage range for each individual input of a differentially configured pair is from GND to AVDD. The operational input voltage difference is from $-V_{REF}/2$ to $+V_{REF}/2$.

Note 15: The typical value is applied when a conversion is requested with ADPMO = 0. Under these conditions, the minimum delay is met. If ADPMO = 1, the user is responsible for ensuring the 4µs delay time is met.

Note 16: Switching ADC reference from either internal or external reference to AVDD. Sample accuracy is not guaranteed prior to ADC reference settlement.

Note 17: Total on-board decoupling capacitance on the AVDD pin < 100nF. The output impedance of the regulator driving the AVDD pin < 10Ω.

Note 18: This parameter is guaranteed by design and is not production tested.

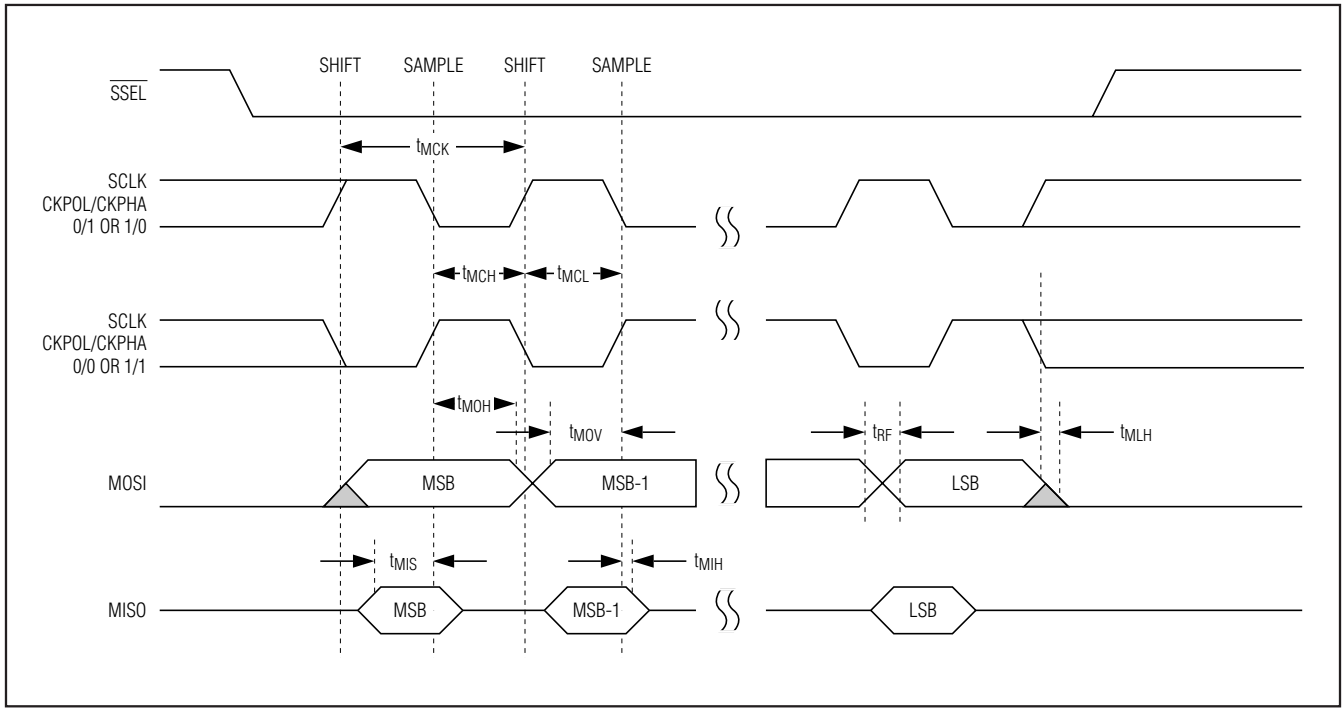


Figure 1. SPI Master Timing

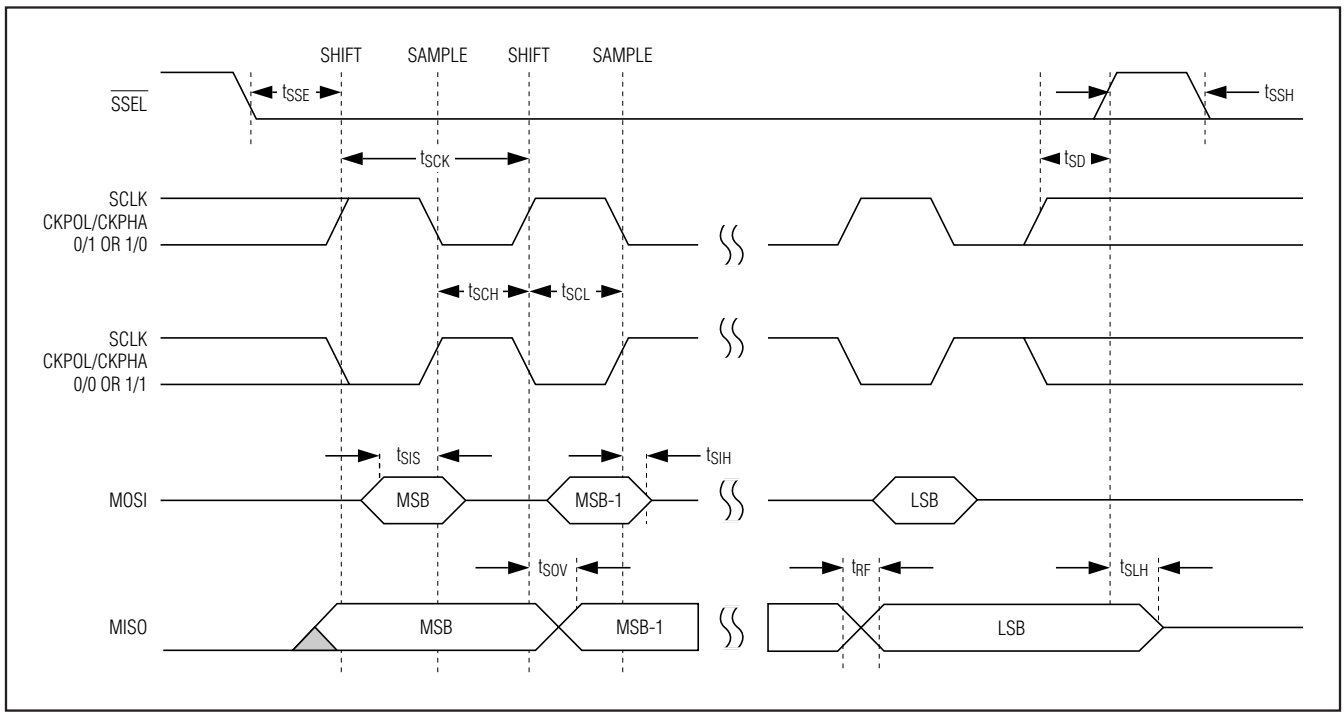


Figure 2. SPI Slave Timing

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I²C ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	TEST CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage (Note 19)	V_{IL_I2C}		-0.5	0.3 x V_{DVDD}	-0.5	0.3 x V_{DVDD}	V
Input High Voltage (Note 19)	V_{IH_I2C}		0.7 x V_{DVDD}		0.7 x V_{DVDD}	V_{DVDD} + 0.5V	V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V_{DVDD} > 2V			0.05 x V_{DVDD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DVDD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Output Fall Time from V_{IH_MIN} to V_{IL_MAX} with Bus Capacitance from 10pF to 400pF (Notes 20, 21)	t_{OF_I2C}			250	20 + 0.1C_B	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t_{SP_I2C}				0	50	ns
Input Current on I/O	I_{IN_I2C}	Input voltage from 0.1 x V_{DVDD} to 0.9 x V_{DVDD}	-10	+10	-10	+10	µA
I/O Capacitance	C_{IO_I2C}			10		10	pF

Note 19: Devices that use nonstandard supply voltages that do not conform to the intended I²C bus system levels must relate their input levels to the voltage to which the pullup resistors R_P are connected. See Figure 3.

Note 20: C_B—Capacitance of one bus line in pF.

Note 21: The maximum fall time of 300ns for the SDA and SCL bus lines shown in the *I²C Bus Controller Timing* table is longer than the specified maximum t_{OF_I2C} of 250ns for the output stages. This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in the *I²C Bus Controller Timing (Acting as I²C Slave)* table without exceeding the maximum specified fall time. See Figure 3.

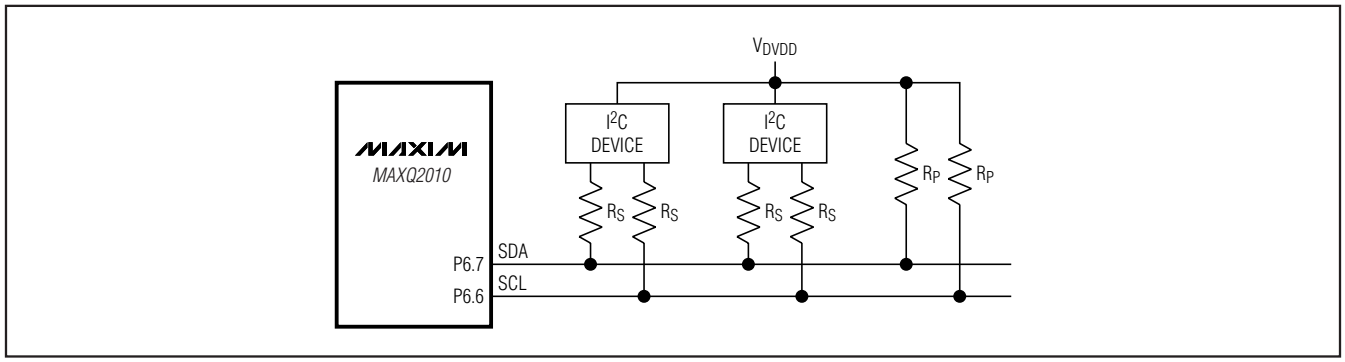


Figure 3. Series Resistors (R_S) for Protecting Against High-Voltage Spikes

I²C BUS CONTROLLER TIMING

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 22) (Figure 4)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
Operating Frequency	f_{I2C}	0	100	0	400	kHz
Hold Time After (Repeated) START	$t_{HD:STA}$	4.0		0.6		µs
Clock Low Period	t_{LOW_I2C}	4.7		1.3		µs
Clock High Period	t_{HIGH_I2C}	4.0		0.6		µs
Setup Time for Repeated START	$t_{SU:STA}$	4.7		0.6		µs
Hold Time for Data	$t_{HD:DAT}$	0 (Note 23)	3.45 (Note 24)	0 (Note 23)	0.9 (Note 24)	µs
Setup Time for Data	$t_{SU:DAT}$	250		100 (Note 25)		ns
SDA/SCL Fall Time	t_{F_I2C}		300	20 + 0.1C_B (Note 26)	300	ns
SDA/SCL Rise Time	t_{R_I2C}		1000	20 + 0.1C_B (Note 26)	300	ns
Setup Time for STOP	$t_{SU:STO}$	4.0		0.6		µs
Bus-Free Time Between STOP and START	t_{BUF}	4.7		1.3		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{NL_I2C}	0.1 x V_{DVDD}		0.1 x V_{DVDD}		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{NH_I2C}	0.2 x V_{DVDD}		0.2 x V_{DVDD}		V

Note 22: All values referenced to $V_{IH_I2C(MIN)}$ and $V_{IL_I2C(MAX)}$.

Note 23: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the $V_{IH_I2C(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 24: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW_I2C}) of the SCL signal.

Note 25: A fast-mode I²C bus device can be used in a standard-mode I²C bus system, but the requirement $t_{SU:DAT} \geq 250$ns must be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R_I2C(MAX)} + t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C specification) before the SCL line is released.

Note 26: C_B—Total capacitance of one bus line in pF.

16-Bit Mixed-Signal Microcontroller with LCD Interface

I²C BUS CONTROLLER TIMING (ACTING AS I²C MASTER)

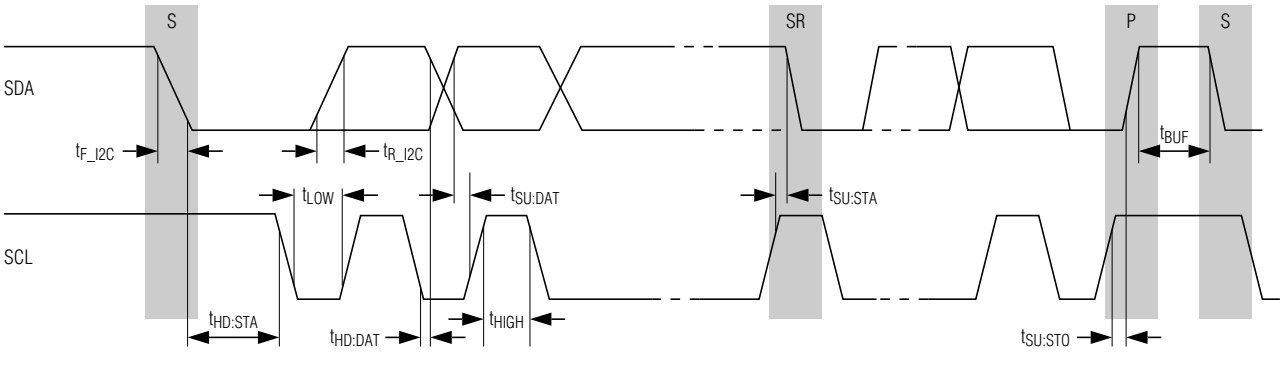
(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Figure 4)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
System Frequency	f_{SYS}	0.90		3.60		MHz
Operating Frequency	f_{I2C}		$f_{SYS}/8$		$f_{SYS}/8$	Hz
Hold Time After (Repeated) START	$t_{HD:STA}$	t_{HIGH_I2C}		t_{HIGH_I2C}		µs
Clock Low Period	t_{LOW_I2C}	$5t_{SYS}$		$5t_{SYS}$		µs
Clock High Period	t_{HIGH_I2C}	$3t_{SYS}$		$3t_{SYS}$		µs
Setup Time for Repeated START	$t_{SU:STA}$	t_{LOW_I2C}		t_{LOW_I2C}		µs
Hold Time for Data	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time	t_{F_I2C}		300	$20+ 0.1C_B$	300	ns
SDA/SCL Rise Time	t_{R_I2C}		1000	$20+ 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	t_{HIGH_I2C}		t_{HIGH_I2C}		µs
Bus-Free Time Between STOP and START	t_{BUF}	t_{LOW_I2C}		t_{LOW_I2C}		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{NL_I2C}	$0.1 \times V_{DVDD}$		$0.1 \times V_{DVDD}$		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{NH_I2C}	$0.2 \times V_{DVDD}$		$0.2 \times V_{DVDD}$		V

I²C BUS CONTROLLER TIMING (ACTING AS I²C SLAVE)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Figure 4)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
System Frequency	f_{SYS}	0.9		3.60		MHz
Operating Frequency	f_{I2C}		$f_{SYS}/8$		$f_{SYS}/8$	Hz
System Clock Period	t_{SYS}	$1/f_{I2C}$			$1/f_{I2C}$	µs
Hold Time After (Repeated) START	$t_{HD:STA}$	$3t_{SYS}$		$3t_{SYS}$		µs
Clock Low Period	t_{LOW_I2C}	$5t_{SYS}$		$5t_{SYS}$		µs
Clock High Period	t_{HIGH_I2C}	$3t_{SYS}$		$3t_{SYS}$		µs
Setup Time for Repeated START	$t_{SU:STA}$	$5t_{SYS}$		$5t_{SYS}$		µs
Hold Time for Data	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time	t_{F_I2C}		300	$20 + 0.1C_B$	300	ns
SDA/SCL Rise Time	t_{R_I2C}		1000	$20 + 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	$3t_{SYS}$		$3t_{SYS}$		µs
Bus-Free Time Between STOP and START	t_{BUF}	$5t_{SYS}$		$5t_{SYS}$		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{NL_I2C}	0.1 x V_{DVDD}		0.1 x V_{DVDD}		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{NH_I2C}	0.2 x V_{DVDD}		0.2 x V_{DVDD}		V



NOTE: TIMING REFERENCED TO $V_{IH_I2C(MIN)}$ AND $V_{IL_I2C(MAX)}$.

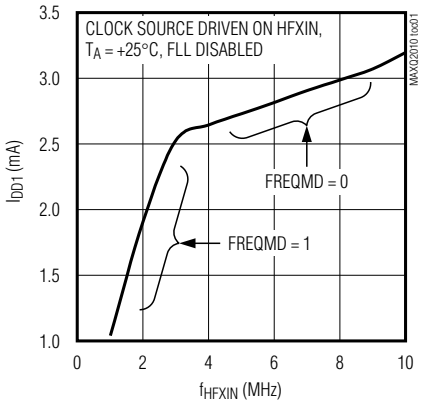
Figure 4. I²C Bus Controller Timing Diagram

16-Bit Mixed-Signal Microcontroller with LCD Interface

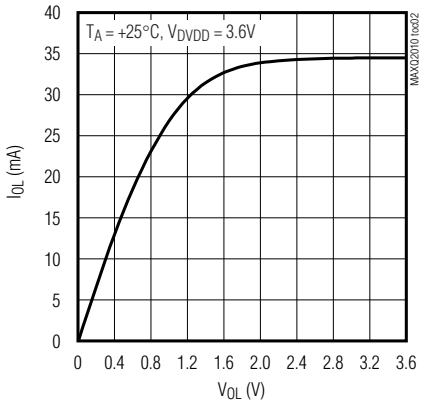
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

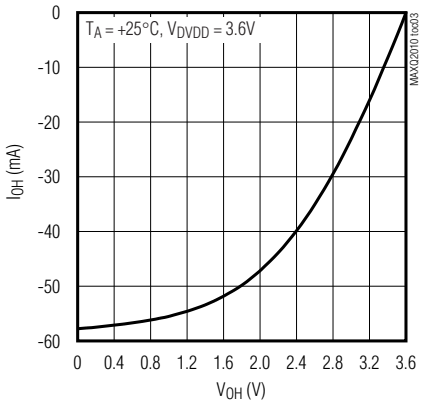
V_{DD} SUPPLY CURRENT vs. CLOCK FREQUENCY



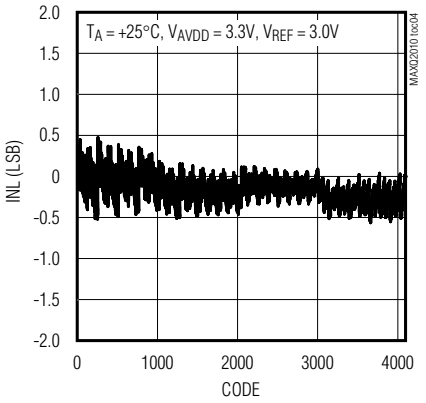
PORT PIN LOW-OUTPUT VOLTAGE vs. SINK CURRENT



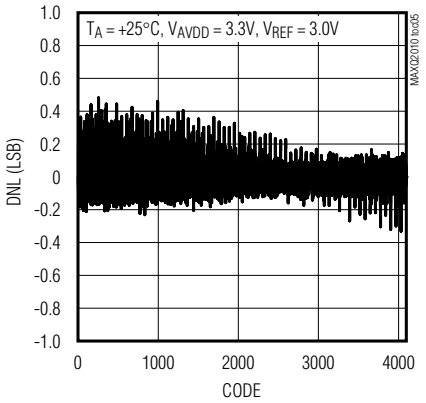
PORT PIN HIGH-OUTPUT VOLTAGE vs. SOURCE CURRENT



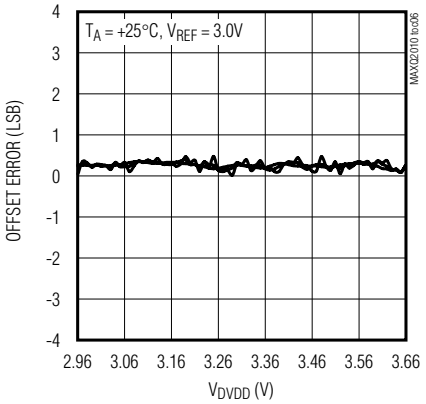
INTEGRAL NONLINEARITY (INL) vs. CODE



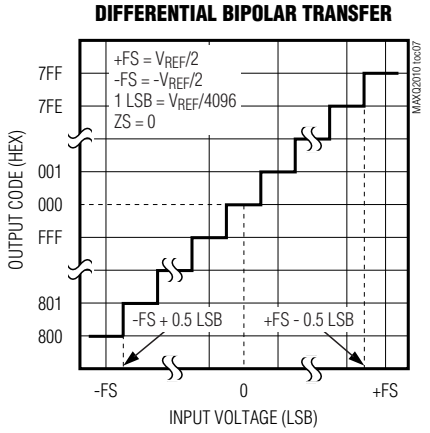
DIFFERENTIAL NONLINEARITY (DNL) vs. CODE



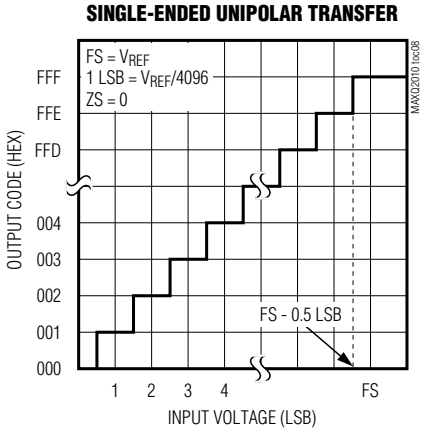
OFFSET ERROR vs. SUPPLY VOLTAGE



DIFFERENTIAL BIPOLAR TRANSFER

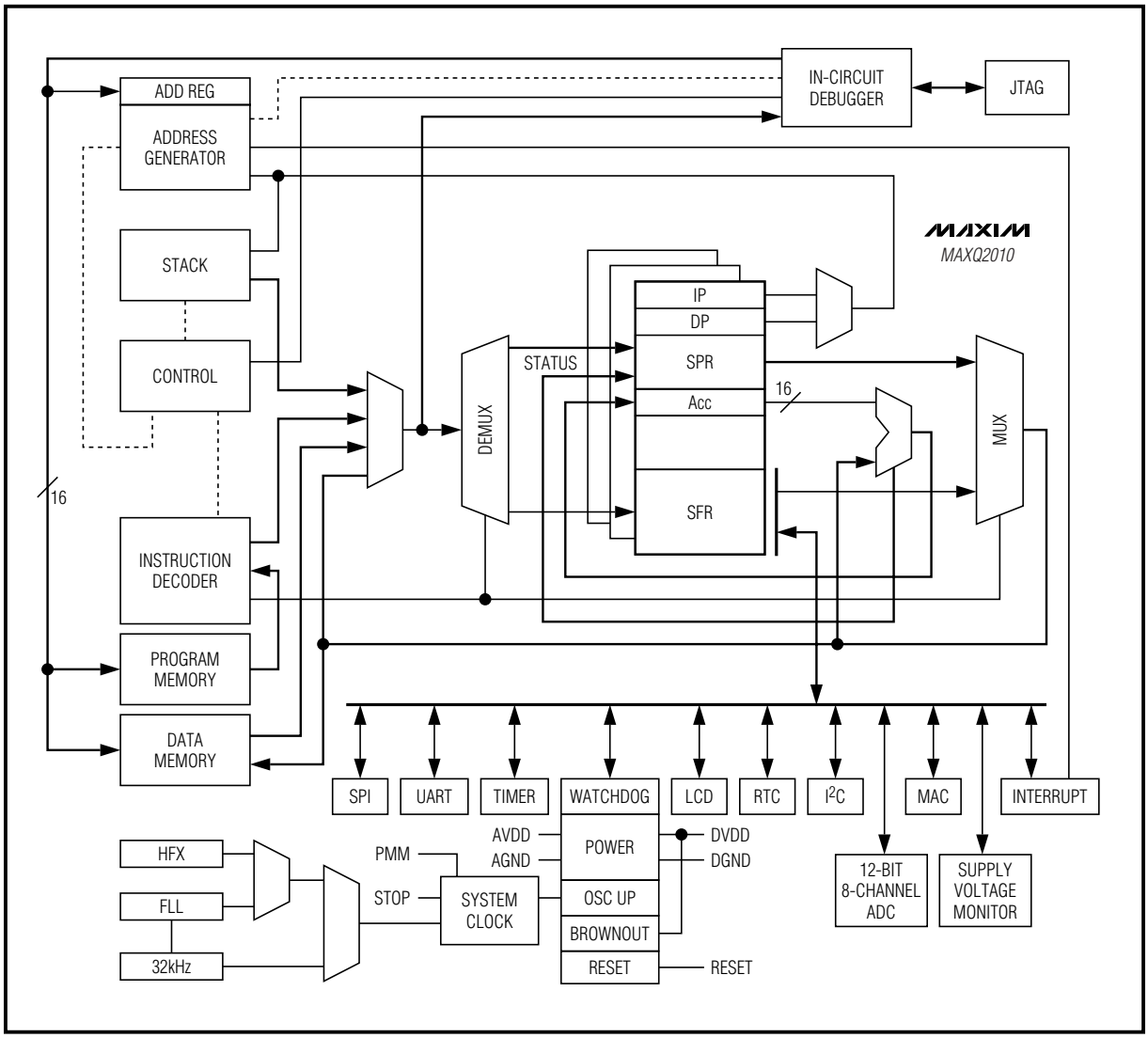


SINGLE-ENDED UNIPOLAR TRANSFER



16-Bit Mixed-Signal Microcontroller with LCD Interface

Block Diagram



16-Bit Mixed-Signal Microcontroller with LCD Interface

Pin Description

PIN	NAME	FUNCTION
		POWER PINS
40, 63, 96	DVDD	**Digital Supply Voltage**
41, 66, 95	DGND	**Digital Ground**
98, 99	REGOUT	**Regulator Capacitor.** These pins must be shorted together at the pins and then connected to ground through a 1.0µF ceramic capacitor.
82	AVDD	**Analog Supply Voltage**
79	AGND	**Analog Ground**
		ANALOG MEASUREMENT PINS
70	AVREF	**Analog Voltage Reference.** When using an external reference source, this pin must be connected to 1µF and 0.01µF filter capacitors in parallel. When using an internal reference source, this pin must be connected to a 0.01µF capacitor.
78, 77	AN0, AN1	**Analog Input 0:1.** This pair of analog inputs can function as two single-ended inputs or one differential pair. When functioning in differential mode, AN0 is the positive input and AN1 is the negative input.
76, 75	AN2, AN3	**Analog Input 2:3.** This pair of analog inputs can function as two single-ended inputs or one differential pair. When functioning in differential mode, AN2 is the positive input and AN3 is the negative input.
74, 73	AN4, AN5	**Analog Input 4:5.** This pair of analog inputs can function as two single-ended inputs or one differential pair. When functioning in differential mode, AN4 is the positive input and AN5 is the negative input.
72, 71	AN6, AN7	**Analog Input 6:7.** This pair of analog inputs can function as two single-ended inputs or one differential pair. When functioning in differential mode, AN6 is the positive input and AN7 is the negative input.
		RESET PIN
92	$\overline{RST}$	**Digital, Active-Low, Reset Input/Output.** The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
		CLOCK PINS
81	32KIN	**32kHz Crystal Input/Output.** Connect an external 6pF, 32kHz watch crystal between 32KIN and 32KOUT to generate the system clock. Alternatively, 32KIN is the input for an external clock source when 32KOUT is disconnected.
80	32KOUT	
64	HFXIN	**High-Frequency Crystal Input**. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is disconnected.
65	HFXOUT	
		LCD PINS
45	V_{LCD}	**LCD Bias Control Voltage**. Highest LCD drive voltage used with static bias. Connected to an external source.
44	V_{LCD1}	**LCD Bias, Voltage 1.** LCD drive voltage used with 1/2 and 1/3 LCD bias. An internal resistor-divider sets the voltage. External resistors and capacitors can be used to change the LCD voltage or drive capability at this pin.

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>43</td><td>V_{LCD2}</td><td>LCD Bias, Voltage 2. LCD drive voltage used with 1/3 LCD bias. An internal resistor-divider sets the voltage. External resistors and capacitors can be used to change LCD voltage or drive capability at this pin.</td></tr>
<tr><td>42</td><td>V_{ADJ}</td><td>LCD Adjustment Voltage. Connect to an external resistor to provide external control of the LCD contrast. Leave disconnected for internal contrast adjustment.</td></tr>
<tr><td colspan="3">GENERAL-PURPOSE I/O, SPECIAL FUNCTION, AND LCD INTERFACE PINS</td></tr>
<tr><td>6–1, 94, 93</td><td>P0.0–P0.7;
SEG0–SEG7;
INT0–INT7</td><td>Digital I/O, Type D Port 0; LCD Segment-Driver Output; External Edge-Selectable Interrupt. This port functions as either bidirectional I/O or alternate LCD segment-drive outputs. The reset condition of the port is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition serves as an input mode. Each port pin can individually be configured to act as an external interrupt. Setting the PCF0 bit switches all pins on this port to LCD segment-drive outputs.

It is possible to mix the LCD and interrupt functions on the same port. To do this, the interrupt enable must be established prior to setting the PCF0 bit. Care must be taken not to enable the external interrupt while the LCD is in normal operational mode, as this could result in potentially harmful contention between the LCD controller output and the external source connected to the interrupt input.
<table>
<tr><th>PIN</th><th>PORT</th><th colspan="2">SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><td>6</td><td>P0.0</td><td>SEG0</td><td>INT0</td></tr>
<tr><td>5</td><td>P0.1</td><td>SEG1</td><td>INT1</td></tr>
<tr><td>4</td><td>P0.2</td><td>SEG2</td><td>INT2</td></tr>
<tr><td>3</td><td>P0.3</td><td>SEG3</td><td>INT3</td></tr>
<tr><td>2</td><td>P0.4</td><td>SEG4</td><td>INT4</td></tr>
<tr><td>1</td><td>P0.5</td><td>SEG5</td><td>INT5</td></tr>
<tr><td>94</td><td>P0.6</td><td>SEG6</td><td>INT6</td></tr>
<tr><td>93</td><td>P0.7</td><td>SEG7</td><td>INT7</td></tr>
</table></td></tr>
<tr><td>91–84</td><td>P1.0–P1.7;
SEG8–SEG15</td><td>Digital I/O, Type C Port 1; LCD Segment-Driver Output. This port functions as either bidirectional I/O or alternate LCD segment-drive outputs. The reset condition of the port is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition serves as an input mode. The port pins also contain a Schmitt voltage input. Setting the PCF1 bit switches all pins on this port to LCD segment-drive outputs.
<table>
<tr><th>PIN</th><th>PORT</th><th>SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><td>91</td><td>P1.0</td><td>SEG8</td></tr>
<tr><td>90</td><td>P1.1</td><td>SEG9</td></tr>
<tr><td>89</td><td>P1.2</td><td>SEG10</td></tr>
<tr><td>88</td><td>P1.3</td><td>SEG11</td></tr>
<tr><td>87</td><td>P1.4</td><td>SEG12</td></tr>
<tr><td>86</td><td>P1.5</td><td>SEG13</td></tr>
<tr><td>85</td><td>P1.6</td><td>SEG14</td></tr>
<tr><td>84</td><td>P1.7</td><td>SEG15</td></tr>
</table></td></tr>
</table>

16-Bit Mixed-Signal Microcontroller with LCD Interface

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="10">56–52,
48–46</td><td rowspan="10">P2.0–P2.7;
SEG16–SEG23</td><td>Digital I/O, Type C Port 2; LCD Segment-Driver Output. This port functions as either bidirectional I/O or alternate LCD segment-drive outputs. The reset condition of the port is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition serves as an input mode. The port pins also contain a Schmitt voltage input. Setting the PCF2 bit switches all pins on this port to LCD segment-drive outputs.</td></tr>
<tr><td>
<table>
<tr><th>PIN</th><th>PORT</th><th>SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><td>56</td><td>P2.0</td><td>SEG16</td></tr>
<tr><td>55</td><td>P2.1</td><td>SEG17</td></tr>
<tr><td>54</td><td>P2.2</td><td>SEG18</td></tr>
<tr><td>53</td><td>P2.3</td><td>SEG19</td></tr>
<tr><td>52</td><td>P2.4</td><td>SEG20</td></tr>
<tr><td>48</td><td>P2.5</td><td>SEG21</td></tr>
<tr><td>47</td><td>P2.6</td><td>SEG22</td></tr>
<tr><td>46</td><td>P2.7</td><td>SEG23</td></tr>
</table>
</td></tr>
<tr><td rowspan="10">36–33, 22–19</td><td rowspan="10">P3.0–P3.7;
SEG24–SEG31</td><td>Digital I/O, Type C Port 3; LCD Segment-Driver Output. This port functions as either bidirectional I/O or alternate LCD segment-drive outputs. The reset condition of the port is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition serves as an input mode. The port pins also contain a Schmitt voltage input. Setting the PCF3 bit switches all pins on this port to LCD segment-drive outputs.</td></tr>
<tr><td>
<table>
<tr><th>PIN</th><th>PORT</th><th>SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><td>36</td><td>P3.0</td><td>SEG24</td></tr>
<tr><td>35</td><td>P3.1</td><td>SEG25</td></tr>
<tr><td>34</td><td>P3.2</td><td>SEG26</td></tr>
<tr><td>33</td><td>P3.3</td><td>SEG27</td></tr>
<tr><td>22</td><td>P3.4</td><td>SEG28</td></tr>
<tr><td>21</td><td>P3.5</td><td>SEG29</td></tr>
<tr><td>20</td><td>P3.6</td><td>SEG30</td></tr>
<tr><td>19</td><td>P3.7</td><td>SEG31</td></tr>
</table>
</td></tr>
<tr><td rowspan="10">18–11</td><td rowspan="10">P4.0–P4.7;
SEG32–SEG39</td><td>Digital I/O, Type-C Port 4; LCD Segment-Driver Output. This port functions as either bidirectional I/O or alternate LCD segment-drive outputs. The reset condition of the port is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition serves as an input mode. The port pins also contain a Schmitt voltage input. Setting the PCF4 bit switches all pins on this port to LCD segment-drive outputs.</td></tr>
<tr><td>
<table>
<tr><th>PIN</th><th>PORT</th><th>SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><td>18</td><td>P4.0</td><td>SEG32</td></tr>
<tr><td>17</td><td>P4.1</td><td>SEG33</td></tr>
<tr><td>16</td><td>P4.2</td><td>SEG34</td></tr>
<tr><td>15</td><td>P4.3</td><td>SEG35</td></tr>
<tr><td>14</td><td>P4.4</td><td>SEG36</td></tr>
<tr><td>13</td><td>P4.5</td><td>SEG37</td></tr>
<tr><td>12</td><td>P4.6</td><td>SEG38</td></tr>
<tr><td>11</td><td>P4.7</td><td>SEG39</td></tr>
</table>
</td></tr>
</table>

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="5">10, 9, 8</td><td rowspan="5">COM3, COM2, COM1; SEG40, SEG41, SEG42</td><td>LCD Segment-Driver Output; LCD Common Drive Output. These pins function as LCD segment or common drive outputs. Configuring a pin as a common drive output disables the segment function for that pin.</td></tr>
<tr><td>
<table>
<tr><th>PIN</th><th colspan="2">SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><td>10</td><td>COM3</td><td>SEG40</td></tr>
<tr><td>9</td><td>COM2</td><td>SEG41</td></tr>
<tr><td>8</td><td>COM1</td><td>SEG42</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>COM0</td><td>LCD Common Drive 0, Output. This pin functions as a LCD common-drive output.</td></tr>
<tr><td>68</td><td>P5.0/INT8/ TB0B/RX0</td><td>Digital I/O, Type D Port 5.0; Timer B0 Pin B; Serial Port 0 Receive; External Edge-Selectable Interrupt 8. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as digital I/O.</td></tr>
<tr><td>67</td><td>P5.1/INT9/ TB0A/TX0</td><td>Digital I/O, Type D Port 5.1; Timer B0 Pin A; Serial Port 0 Transmit; External Edge-Selectable Interrupt 9. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>61</td><td>P5.2/INT10/ SQW</td><td>Digital I/O, Type-D Port 5.2; External Edge-Selectable Interrupt 10; RTC Square-Wave Output. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>60</td><td>P5.3/INT11/ $\overline{SSEL}$</td><td>Digital I/O, Type D Port 5.3; External Edge-Selectable Interrupt 11; Active-Low SPI Slave-Select Input. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>59</td><td>P5.4/INT12/ MOSI</td><td>Digital I/O, Type D Port 5.4; External Edge-Selectable Interrupt 12; SPI Master Out-Slave In. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>58</td><td>P5.5/INT13/ SCLK</td><td>Digital I/O, Type D Port 5.5; External Edge-Selectable Interrupt 13; SPI Clock Output. This pin defaults as an input with a weak pullup after a reset and functions as general-purpose I/O. The port pad contains a Schmitt input circuitry and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>57</td><td>P5.6/INT14/ MISO</td><td>Digital I/O, Type D Port 5.6; External Edge-Selectable Interrupt 14; SPI Master In-Slave Out. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>32</td><td>P6.0/INT15/ TCK</td><td>Digital I/O, Type D Port 6.0; External Edge-Selectable Interrupt 15; JTAG Test Clock Input. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
<tr><td>31</td><td>P6.1/INT16/ TDI</td><td>Digital I/O, Type D Port 6.1; External Edge-Selectable Interrupt 16; JTAG Test Data Input. This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.</td></tr>
</table>

16-Bit Mixed-Signal Microcontroller with LCD Interface

Pin Description (continued)

PIN	NAME	FUNCTION
30	P6.2/INT17/ TMS	**Digital I/O, Type D Port 6.2; External Edge-Selectable Interrupt 17; JTAG Test Mode Select Input.** This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.
29	P6.3/INT18/ TDO	**Digital I/O, Type-D Port 6.3; External Edge-Selectable Interrupt 18; JTAG Test Data Output.** This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.
28	P6.4/INT19/ TB1B/RX1	**Digital I/O, Type D Port 6.4; External Edge-Selectable Interrupt 19; Timer B1 Pin B; Serial Port 1 Receive.** This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.
25	P6.5/INT20/ TB1A/TX1	**Digital I/O, Type D Port 6.5; External Edge-Selectable Interrupt 20; Timer B1 Pin A; Serial Port 1 Transmit.** This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.
24	P6.6/INT21/ TB2B/SCL	**Digital I/O, Type D Port 6.6; External Edge-Selectable Interrupt 21; Timer B2 Pin B; I^2C Clock I/O.** This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general purpose I/O.
23	P6.7/INT22/ TB2A/SDA	**Digital I/O, Type D Port 6.7; External Edge-Selectable Interrupt 22; Timer B2 Pin A; I^2C Data I/O.** This pin defaults to an input with a weak pullup after reset and functions as general-purpose I/O. The port pad contains a Schmitt voltage input and can be configured as an external interrupt. Enabling a special function disables the pin as general-purpose I/O.
NO CONNECTION PINS		
26, 27, 37, 38, 39, 49, 50, 51, 62, 69, 83, 97, 100	N.C.	**No Connection.** Reserved for future use. Leave these pins unconnected.

Detailed Description

The following sections are an introduction to the primary features of the microcontroller. More detailed descriptions of the device features can be found in the errata sheets and user's guides described later in the *Additional Documentation* section.

MAXQ Core Architecture

The MAXQ2010 is a low-cost, high-performance, CMOS, fully static, 16-bit RISC microcontroller with flash memory and an integrated LCD controller. The MAXQ2010 supports up to a 160-segment LCD and supports 8 channels of high-performance measurement using a 12-bit successive approximation register (SAR) ADC with internal reference. The MAXQ2010 is structured on a highly advanced, accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining because the instruction contains both the op code and data. The result is a streamlined microcontroller performing at up to one million instructions-per-second (MIPS) for each MHz of the system operating frequency.

A 16-level hardware stack, enabling fast subroutine calling and task switching, supports the highly efficient core. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement following an operation, eliminating the need for software intervention. As a result, application speed is greatly increased.

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers control the peripherals and are subdivided into register modules. The family architecture is modular so that new devices and modules can reuse code developed for existing products.

The architecture is transport-triggered, which means that writes or reads from certain register locations can also cause side effects to occur. These side effects form the basis for the higher level op codes defined by the assembler, such as ADDC, OR, JUMP, etc. The op codes are actually implemented as MOVE instructions between certain register locations, while the assembler handles the encoding, which need not be a concern to the programmer.

The 16-bit instruction word is designed for efficient execution. Bit 15 indicates the format for the source field of the instruction. Bits 0 to 7 of the instruction represent the source for the transfer. Depending on the value of the format field, this can either be an immediate value or a source register. If this field represents a register, the lower four bits contain the module specifier and the upper four bits contain the register index in that module. Bits 8 to 14 represent the destination for the transfer. This value always represents a destination register, with the lower four bits containing the module specifier and the upper three bits containing the register subindex within that module. Any time that it is necessary to directly select one of the upper 24 registers as a destination, the prefix register (PFX) is needed to supply the extra destination bits. This prefix register write is inserted automatically by the assembler and requires only one additional execution cycle.

Memory Organization

The device incorporates several memory areas, including:

- 4KB utility ROM
- 64KB of flash memory for program storage
- 2KB of SRAM for storage of temporary variables
- 16-level stack memory for storage of program return addresses and general-purpose use

The incorporation of flash memory allows the devices to be reprogrammed multiple times, allowing modifications to user applications post production. Additionally, the flash can be used to store application information including configuration data and log files.

The default memory organization is organized as a Harvard architecture, with separate address spaces for program and data memory. Pseudo-Von Neumann memory organization is supported through the utility ROM for applications that require dynamic program modification and execution from RAM. The pseudo-Von Neumann memory organization places the code, data, and utility ROM memories into a single contiguous memory map. See Figure 5 for the memory map.

Stack Memory

A 16-bit-wide hardware stack provides storage for program return addresses and can also be used as general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

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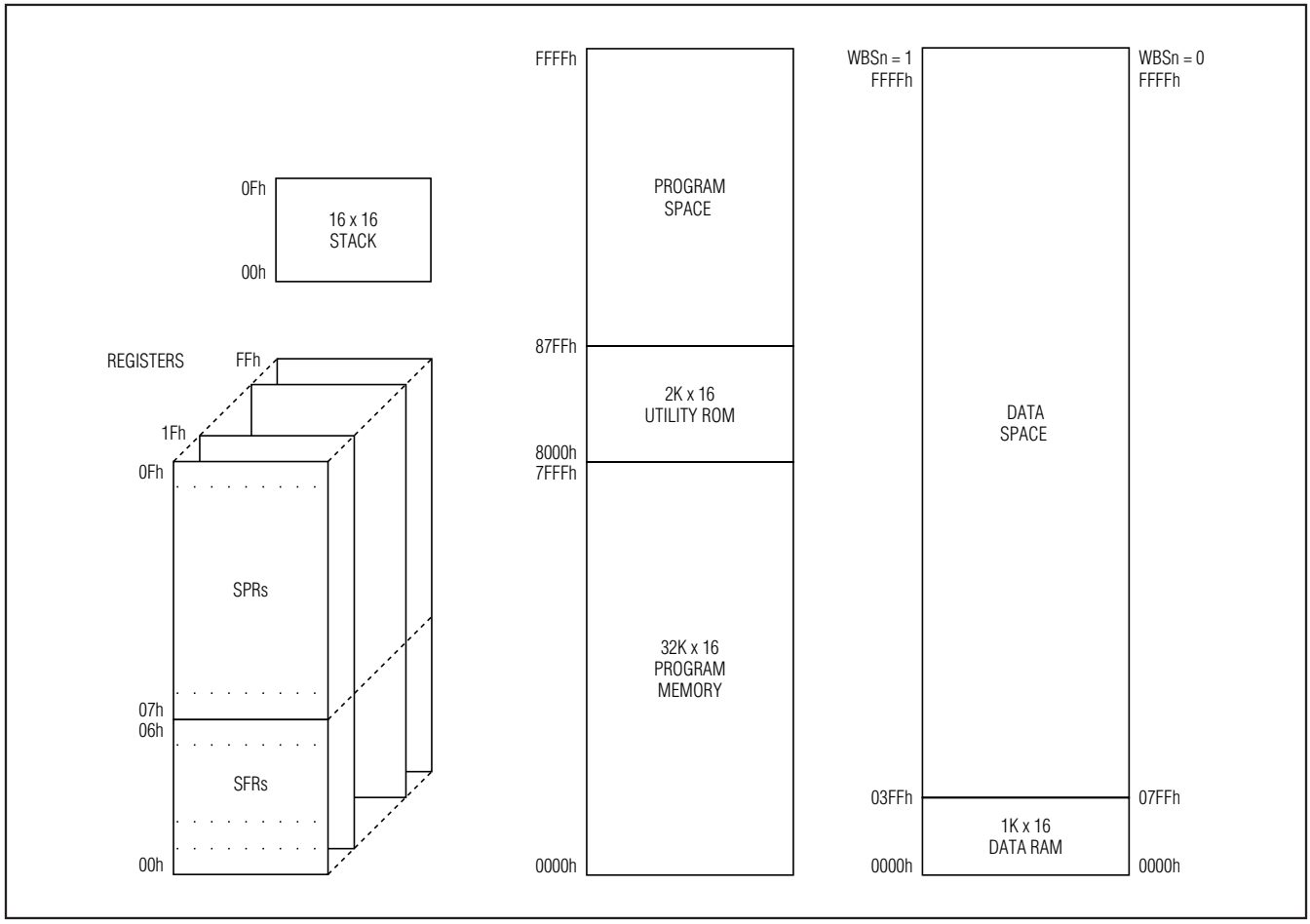


Figure 5. MAXQ2010 Default Memory Map

On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Utility ROM

The utility ROM is a 4KB block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include the following:

- In-system programming (bootstrap loader) using JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash programming and fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of user-application code, or to one of the special routines mentioned. Routines within the utility ROM are user-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the *MAXQ Family User's Guide: MAXQ2010 Supplement*.

Some applications require protection against unauthorized viewing of program code memory. For these

applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

A single password lock (PWL) bit is implemented in the SC register. When the PWL is set to 1 (power-on reset default) and the contents of the memory at addresses 0010h to 001Fh are any value other than all FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to 0, these utilities are fully accessible without the password. The password is automatically set to all 1s following a mass erase.

Programming

The microcontroller's flash memory can be programmed by two different methods: in-system programming and in-application programming. Both methods afford great flexibility in system design and reduce the life-cycle cost of the embedded system. These features can be password protected to prevent unauthorized access to code memory.

(Bootloader) In-System Programming

An internal bootstrap loader allows the device to be reloaded over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software updates enable application updates to physically inaccessible equipment. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a serial-to-JTAG converter such as the MAXQJTAG-001, available from Maxim. If in-system programmability is not required, use a commercial gang programmer for mass programming.

Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to 1 during reset through the JTAG interface executes the bootstrap-loader-mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

The following bootstrap loader functions are supported:

- Load
- Dump
- CRC
- Verify
- Erase

In-Application Programming

The in-application programming feature allows the microcontroller to modify its own flash program memory while simultaneously executing its application software. This allows on-the-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible flash programming functions that erase and program flash memory. These functions are described in detail in the *MAXQ Family User's Guide: MAXQ2010 Supplement*.

Register Set

Most functions of the device are controlled by sets of registers. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers and peripheral registers. The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality that may be included by different products based on the MAXQ architecture. This functionality is broken up into discrete modules so that only the features required for a given product need to be included.

The documentation on the module and register functions is covered fully in the *MAXQ Family User's Guide* and the *MAXQ Family User's Guide: MAXQ2010 Supplement*. This information includes the locations of status and control bits and a detailed description of their function and reset values. Refer to these documents for a complete understanding of the features and operation of the microcontroller.

System Timing

For maximum versatility, the device can generate its internal system clock from several sources:

- External clock source
- Internal oscillator using external crystal or resonator
- FLL using 32kHz clock source (approximately 8MHz)
- FLL with no external crystal (approximately 5MHz)

Operation from an external clock source or internal oscillator using external crystal or resonator is similar to other microcontrollers. The designer must remember that the rated maximum speed of operation applies to the speed of the microcontroller core, not the external

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clock source. The device contains an FLL that is used as a clock source by itself (FLLEN = 0) or as a multiplier for the 32kHz crystal (FLLEN = 1). The 32kHz-mode-based timing is more stable due to the use of the crystal as a time base.

A crystal warmup counter enhances operational reliability. If the user has selected to run from the external crystal or clock source, each time the external crystal oscillation must restart, such as after exiting stop mode, the device initiates a crystal warmup period of 65,536 oscillations. This allows time for the crystal amplitude and frequency to stabilize before using it as a clock source. While in the warmup mode, the device operates from the internal FLL and automatically switches back to the crystal as soon as it is ready.

Programmable clock-divide control bits (CD1 and CD0) and the PMME bit provide the processor with the ability to slow the system clock, resulting in lower power consumption. The CD[1:0] bits default to 00b, selecting a divide-by-1 system clock, but five clock-divisor options allow the selection of different crystals to accommodate specific system needs. In power-management mode (PMM), one system clock is 256 oscillator cycles, significantly reducing power consumption while the microcontroller functions at reduced speed. The switchback feature allows the system to exit PMM in response to an external interrupt or serial port activity, quickly switching from the slower, power-saving mode to full speed. In addition, the lowest power stop mode allows the microcontroller to stop the internal oscillator, halting the system clock.

Interrupts

Multiple interrupt sources are available for quick response to internal and external events. The MAXQ architecture uses a single interrupt vector (IV), single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by the module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the user-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay, and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, the user program must determine whether a jump to 0000h came from a reset or interrupt source.

Once software control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine if a system register or peripheral register was the source of the interrupt. The specified module can then be interrogated for the specific interrupt source and software can take appropriate action. Because the user software evaluates the interrupts, the user can define a unique interrupt priority scheme for each application.

The following interrupt sources are supported:

- Supply Voltage Monitor
- External Interrupts 22 to 0
- Timer 2, 1, 0
- Serial Port 1, 0
- Watchdog Timer
- RTC Time-of-Day or Subsecond Alarm
- SPI
- I^2C
- ADC

When an enabled interrupt is detected, software jumps to the dedicated interrupt vector address reserved for that interrupt. User-application code at this address then routes program execution to a user-defined interrupt routine.

I/O Ports

The microcontroller uses Type C and Type D bidirectional I/O pins as described in the *MAXQ Family User's Guide*. Each port has up to eight independent, general-purpose I/O pins and three configure/control registers. Many pins support alternate functions such as timers or interrupts, which are enabled, controlled, and monitored by dedicated peripheral registers. Using the alternate function automatically converts the pin to that function, overriding the general-purpose I/O functionality.

Type C port pins have Schmitt trigger receivers and full CMOS output drivers, and can support alternate functions. The pin is either high impedance or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register.

Type D port pins have Schmitt trigger receivers and full CMOS output drivers, and can support alternate functions. The pin is either high impedance or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. All Type D pins also have interrupt capability. See Figure 6 for a Type C/D port pin schematic.

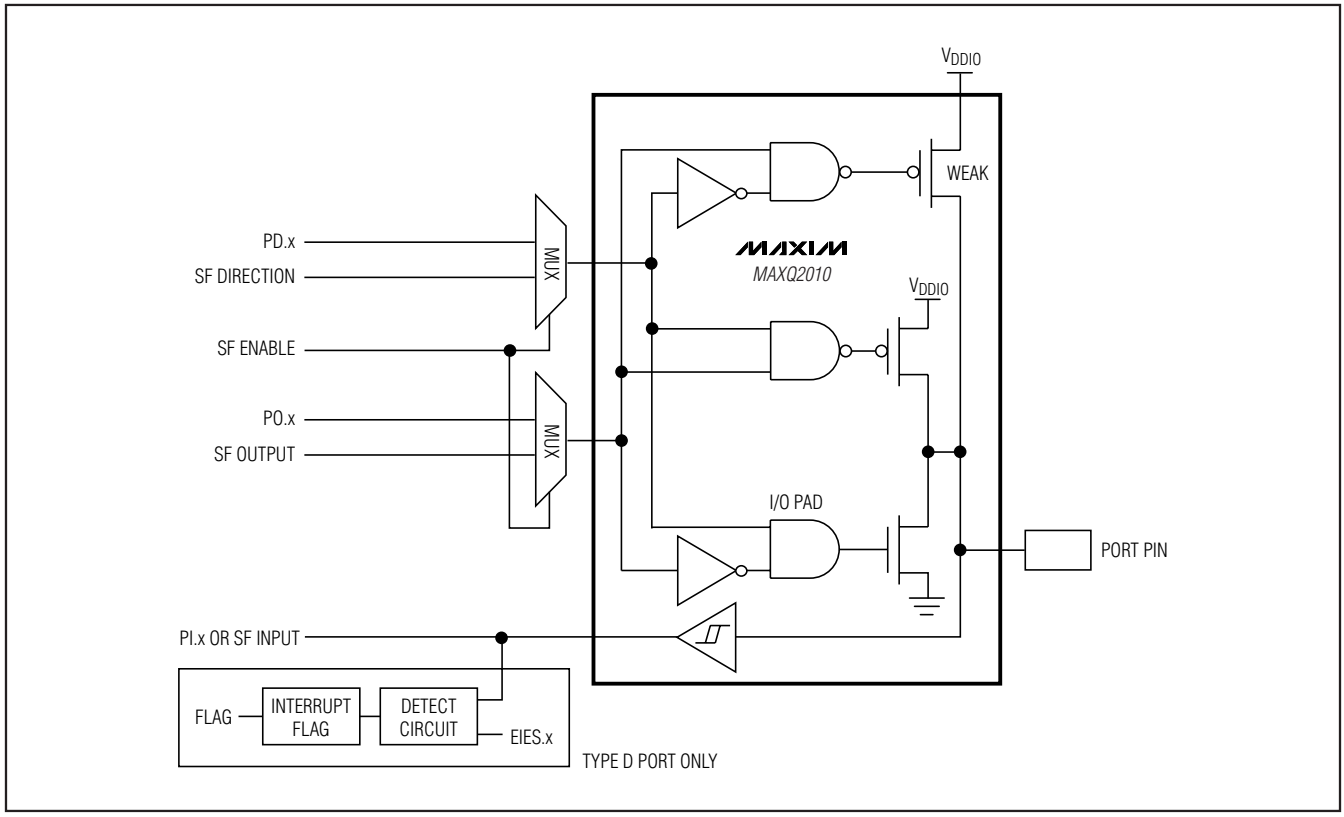


Figure 6. Type C/D Port Pin Schematic

Supply Voltage Monitor

The supply voltage monitor can detect if the supply voltage has fallen below a user-selectable level. If this happens, the microcontroller can be programmed to generate an interrupt to inform the system. The detection level is set using the supply voltage threshold bit (SVTH) and can be adjusted from 2.7V to 3.5V in 0.1V increments. Setting the SVMEN bit to 1 enables the supply voltage monitor. Once the monitoring circuitry is stable and ready for operation, the supply voltage monitor ready (SVMRDY) flag is set to 1. The default set point is 2.7V (SVTH[3:0] = 07h). Care must be taken not to set the set point below 2.7V as SVM interrupts may not occur because the brownout monitor may activate first.

The supply voltage monitor causes a switchback to occur if the supply voltage falls below the threshold value and the supply voltage monitor interrupt is enabled (SVMIE = 1).

The supply voltage monitor remains operational in stop mode if the supply voltage monitor stop mode enable bit (SVMSTOP) is set to 1. Clearing SVMSTOP to 0 disables the supply voltage monitor on entry to stop mode if the SVM peripheral is enabled. If the supply voltage monitor is enabled during stop mode, an SVMI interrupt causes the processor to exit stop mode if enabled (SVMIE = 1).

Serial Peripherals

The microcontroller supports two independent USARTs as well as I^2C master/slave and SPI master communication ports.

USART Serial Ports

The independent USARTs provide transmit and receive signals to communicate with other RS-232 interface-enabled devices, as well as PCs and serial modems when paired with an external RS-232 line driver/receiver. The dual independent USARTs can communicate simultaneously at different baud rates with two separate peripherals. The USART can detect framing errors and indicate the condition through a user-accessible software bit.

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The time base of the serial ports is derived from either a division of the system clock or the dedicated baud-clock generator. Table 1 summarizes the operating characteristics of each mode.

I²C Bus

The microcontroller integrates an internal I²C bus master/slave for communication with a wide variety of other I²C-enabled peripherals. The I²C bus is a 2-wire bidirectional bus using two bus lines, the serial data line (SDA), and the serial clock line (SCL), as well as a ground line. Both the SDA and SCL lines must be driven as open-collector/drain outputs. External resistors are required as shown in Figure 3 to pull the lines to a logic-high state.

The MAXQ2010 is flexible in that it supports both the master and slave protocols. In the master mode, the device has ownership of the I²C bus and drives the clock and generates the START and STOP signals. This allows it to send data to a slave or receive data from a slave as required. In slave mode, the MAXQ2010 relies on an externally generated clock to drive SCL and responds to data and commands only when requested by the I²C master device.

Serial Peripheral Interface (SPI)

The integrated SPI provides an independent serial communication channel that communicates synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time.

The maximum SPI master transfer rate is Sysclk/2. When operating as an SPI slave, the MAXQ2010 can support up to a Sysclk/4 SPI transfer rate. Data is transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of active $\overline{SSEL}$ state through the slave-active select.

Real-Time Clock

A binary real-time clock (RTC) keeps the time of day in absolute seconds with 1/256-second resolution. The 32-bit second counter can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode.

The independent subsecond alarm runs from the same RTC and allows the application to support interrupts with a minimum interval of approximately 3.9ms. This creates an additional timer that can be used to measure long periods of time without performance degradation. Traditionally, long time periods have been measured using multiple interrupts from shorter interrupt intervals. Each timer interrupt required servicing, with each accompanying interruption slowing system operation. By using the RTC subsecond timer as a long-period timer, only one interrupt is needed, eliminating the performance hit associated with using a shorter timer.

An internal crystal oscillator clocks the RTC using integrated 6pF load capacitors, and yields the best performance when mated with a 32.768kHz crystal rated for a 6pF load. No external load capacitors are required. Higher accuracy can be obtained by supplying an external clock source to the RTC.

Programmable Timers

The microcontroller incorporates three instances of the 16-bit programmable Timer/Counter B peripheral, denoted TB0, TB1, and TB2. They can be used in counter/timer/capture/compare/PWM functions, allowing precise control of internal and external events. These timer/counters support clock input prescaling and set/reset/toggle PWM/output control functionality not found on other MAXQ timer implementations. A new register, TBC, supports certain PWM/output control functions in some implementations. A distinguishing characteristic of Timer/Counter B is that its count

Table 1. Serial Port Operating Characteristics

MODE	TYPE	START BITS	DATA BITS	STOP BIT
Mode 0	Synchronous	—	8	—
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

ranges from 0000h to the value stored in the 16-bit capture/reload register (TBR), whereas in other implementations (e.g., Timer 1) the count ranges from the value in the reload register to FFFFh. These timers are fully described in the *MAXQ Family User's Guide*.

Timer B operational modes include the following:

- Autoreload
- Autoreload Using External Pin
- Capture Using External Pin
- Up/Down Count Using External Pin
- Up-Count PWM/Output
- Up/Down PWM/Output
- Clock Output on TBB Pin

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer is controlled through bits in the WDCN register. Its timeout period can be set to one of four programmable intervals ranging from 2^{12} to 2^{21} system clocks in its default mode, allowing flexibility to support different types of applications. The interrupt occurs 512 system clocks before the reset, allowing the system to execute an interrupt and place the system in a known, safe state before the device performs a total system reset. At 8MHz, watchdog timeout periods can be programmed from 512µs to 67s, depending on the system clock mode.

Hardware Multiplier

The internal hardware multiplier supports high-speed multiplications. The multiplier can complete a 16-bit x 16-bit multiply-and-accumulate/subtract operation in a single cycle with the support of a 48-bit accumulator. The multiplier is a fixed-point arithmetic unit. The operands can be either signed or unsigned numbers, but the data type must be defined by the application software prior to loading the operand registers.

Seven different multiply operations can be performed without requiring direct intervention of the microcontroller core. These include the following:

- Unsigned 16-bit multiplication
- Unsigned 16-bit multiplication and accumulation
- Unsigned 16-bit multiplication and subtraction
- Signed 16-bit multiplication
- Signed 16-bit multiplication and negate
- Signed 16-bit multiplication and accumulation
- Signed 16-bit multiplication and subtraction

Each of these operations is controlled and accessed through six SFR registers. The 8-bit multiplier control register (MCNT) selects the operation, data type, operand count, optional hardware-based square function, write option on the MC register, the overflow flag, and the clear control for operand registers and accumulator. Loading and unloading of the data is achieved through five 16-bit SFR registers.

Only one cycle is needed for computation. This means that the result of an operation is ready in the next cycle immediately following the loading of the last operand. Back-to-back operations can be performed without wait states between operations, independent of data type and operand count.

Analog-to-Digital Converter

The MAXQ2010 contains a 12-bit successive approximation analog-to-digital converter (ADC) with an analog mux (Figure 7). The mux selects the ADC input from eight single-ended channels or four differential channels. An internal precision bandgap reference can be used for the ADC reference voltage, or the reference voltage can be externally driven. Additionally, the analog supply voltage (AVDD) can also be used as the voltage reference. The ADC runs off a 2.7V to 3.6V power supply and at a conversion rate up to 300ksps.

The ADC block includes a 12-bit SAR core, ADC controls, a reference generator, and a circular block of sixteen 12-bit data buffers. The ADC is controlled by SFR registers. An autoscan feature allows the user to select up to eight sampling channels for storage in the 16 memory locations.

There are two conversion modes: single-sequence mode and continuous-sequence mode.

The ADC's internal power-management system automatically powers down when the conversion(s) are done (ADCONV = 0). The start conversion bit, ADCONV, is used to start all conversion processes. If the ADC power-management override bit is cleared

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(ADPMO = 0), the ADC waits for 20 ADCCLK before starting the first conversion. This allows the ADC time to set up.

If ADPMO = 1, an ADC conversion is initiated as soon as ADCONV is set to 1. ADC operation is aborted upon entry into PMM or stop mode.

The ADCONV bit is set at the beginning of the conversion process and remains set until the conversion process is finished. In single-sequence mode, this bit remains set until the ADC has finished conversion on the last channel in the sequence. In continuous mode, the ADCONV bit remains set until the continuous mode is stopped. Writing a 0 to the ADCONV bit stops ADC operation at the completion of the current ADC conversion. The new data is written to the data buffer.

An A/D conversion takes 16 ADCCLK cycles to complete. Three of the 16 ADCCLK cycles are used for sample acquisition. The ADCCLK is derived from the system clock with divide ratio defined by the ADC clock divider bits (ADCCLK). Therefore, with 16 ADCCLK to acquire one data, the fastest ADC rate = sysclk/16 (ADCCLK = 0h, ADACQEN = 0h). With a 10MHz system clock, this is theoretically equivalent to 10MHz/16 value Msps. Note, however, that the ADC conversion is limited to 300ksps.

If the ADC data-available interrupt is enabled (ADDAIE = 1), an interrupt is generated to the CPU when ADDAI = 1. Once set, the ADDAI flag can be cleared by software writing a 0 or at the start of a conversion process when ADCONV is set to 1. The data-available interrupt flag (ADDAI) can optionally be set by using the ADC data-available interrupt interval bits (ADDAINV). The ADDAI can be set in 1, 2, 3, 4, 5, 6, 7, 8, 12, or 16 samples intervals. For a sequence that uses only one configuration register, setting ADDAINV = 00 generates an interrupt with the same interval as ADDAINV = 01, both of which set the ADDAI at every ADC sample. When the ADDAI is set, the last memory location written by ADC will also be written to ADDADDR.

LCD Controller

The MAXQ2010 microcontroller incorporates an LCD controller that interfaces to common low-voltage displays. By incorporating the LCD controller into the microcontroller, the design requires only an LCD glass rather than a considerably more expensive LCD module. Every character in an LCD glass is composed of one or more segments, each of which is activated by selecting the appropriate segment and common signal. The microcontroller can multiplex combinations of up to 43 segment outputs (SEG0 to SEG42) and four common signal outputs (COM0 to COM3). Unused segment outputs can be used as general-purpose port pins.

The segments are easily addressed by writing to dedicated display memory. Once the LCD controller settings and display memory have been initialized, the 21-byte display memory is periodically scanned, and the segment and common signals are generated automatically at the selected display frequency. No additional processor overhead is required while the LCD controller is running. Unused display memory can be used for general-purpose storage.

The design is further simplified and cost reduced by the inclusion of software-adjustable internal voltage-

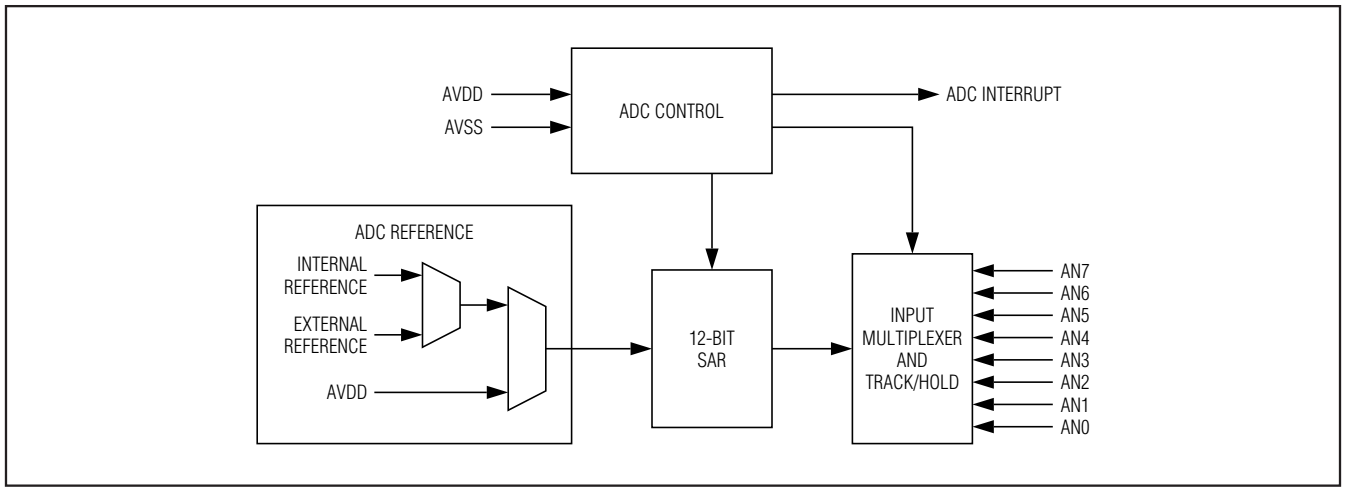


Figure 7. ADC Block Diagram

dividers to control display contrast, using either V_{DDIO} or an external voltage. If desired, contrast can also be controlled with an external resistance. The features of the LCD controller include the following:

- Automatic LCD segment and common-drive signal generation
- Four display modes supported:
  - Static (COM0)
  - 1/2 duty multiplexed with 1/2 bias voltages (COM[0:1])
  - 1/3 duty multiplexed with 1/3 bias voltages (COM[0:2])
  - 1/4 duty multiplexed with 1/3 bias voltages (COM[0:3])
- Up to 43 segment outputs and four common-signal outputs
- 21 bytes (168 bits) of display memory
- Flexible LCD clock source, selectable from 32kHz or HFClk/512
- Adjustable frame frequency
- Internal voltage-divider resistors eliminate requirement for external components
- Internal adjustable resistor allows contrast adjustment without external components

A simple LCD-segmented glass interface example demonstrates the minimal hardware required to interface to a MAXQ2010 microcontroller. A two-character LCD is controlled, with each character containing seven segments plus decimal point. The LCD controller is configured for 1/2 duty-cycle operation, meaning the active segment is controlled using a combination of segment signals and COM0 or COM1 signals are used to select the active display. See Figure 8.

In-Circuit Debug

Embedded debugging capability is available through the JTAG-compatible TAP. Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. Figure 9 shows a block diagram of the in-circuit debugger. The in-circuit debug features include the following:

- A hardware debug engine.
- A set of registers able to set breakpoints on register, code, or data accesses.
- A set of debug service routines stored in the utility ROM.

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

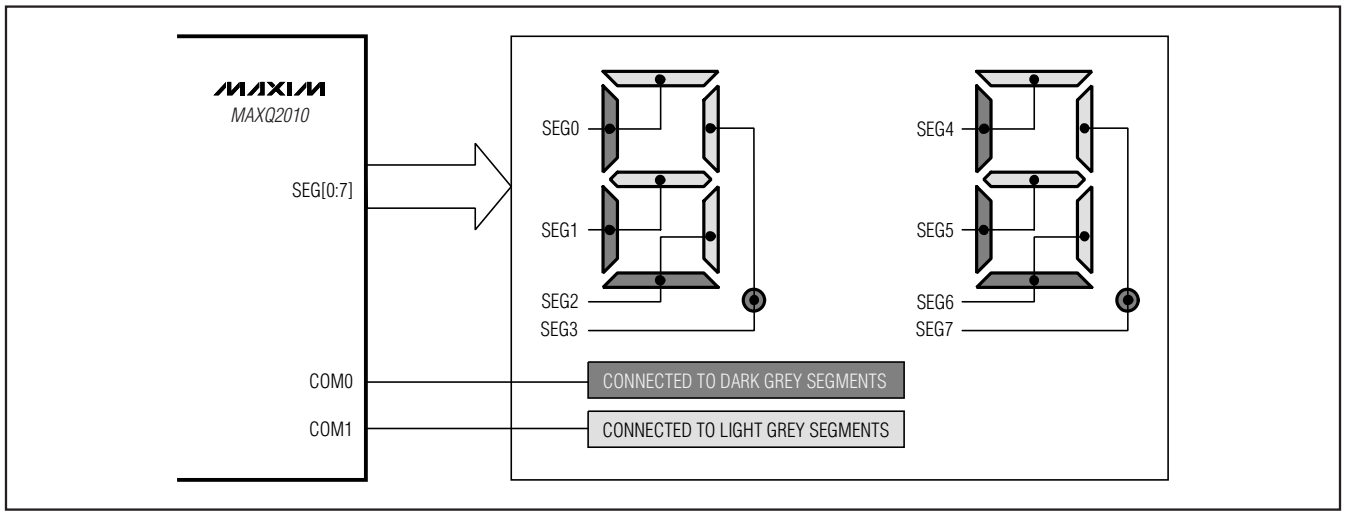


Figure 8. Two-Character, 1/2 Duty, LCD Interface Example

16-Bit Mixed-Signal Microcontroller with LCD Interface

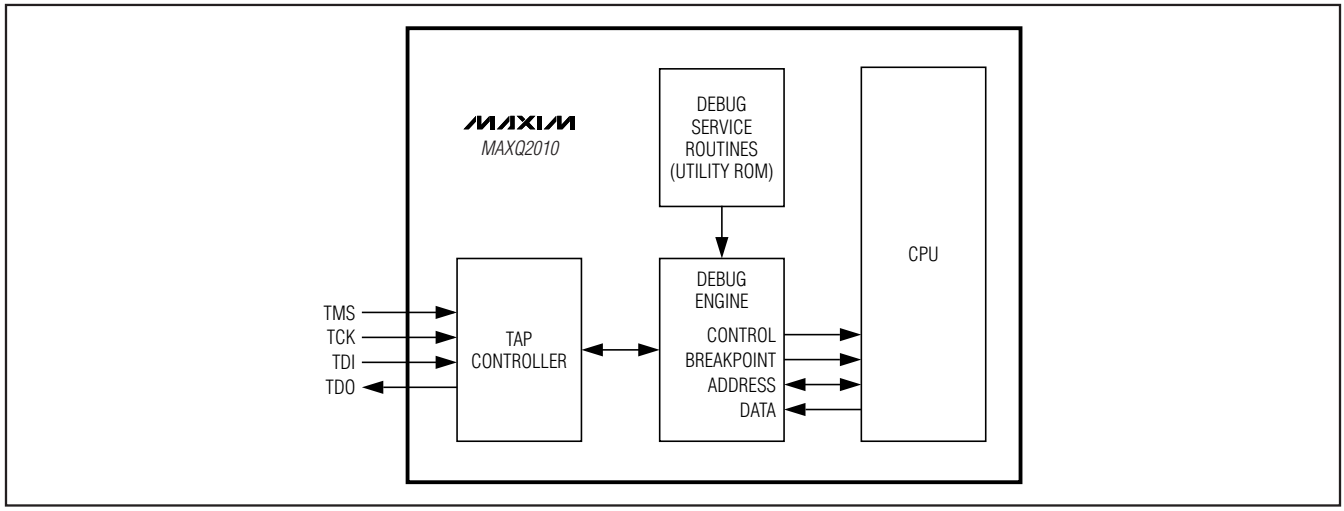


Figure 9. In-Circuit Debugger

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications that require cost-effective computing. The high-throughput core is complemented by a 16-bit hardware multiplier-accumulator, allowing the implementation of sophisticated computational algorithms. Applications benefit from a wide range of peripheral interfaces, allowing the microcontroller to communicate with many external devices. With integrated LCD support of up to 160 segments, applications can support complex user interfaces. Displays are driven directly with no additional external hardware required. Contrast can be adjusted using a built-in, adjustable resistor. The simplified architecture reduces component count and board space, critical factors in the design of portable systems.

The MAXQ2010 is ideally suited for applications such as medical instrumentation, portable blood-glucose equipment, and data-collection devices. For blood-glucose measurement, the microcontroller integrates an SPI interface that directly connects with analog front-ends for measuring test strips.

Grounds and Bypassing

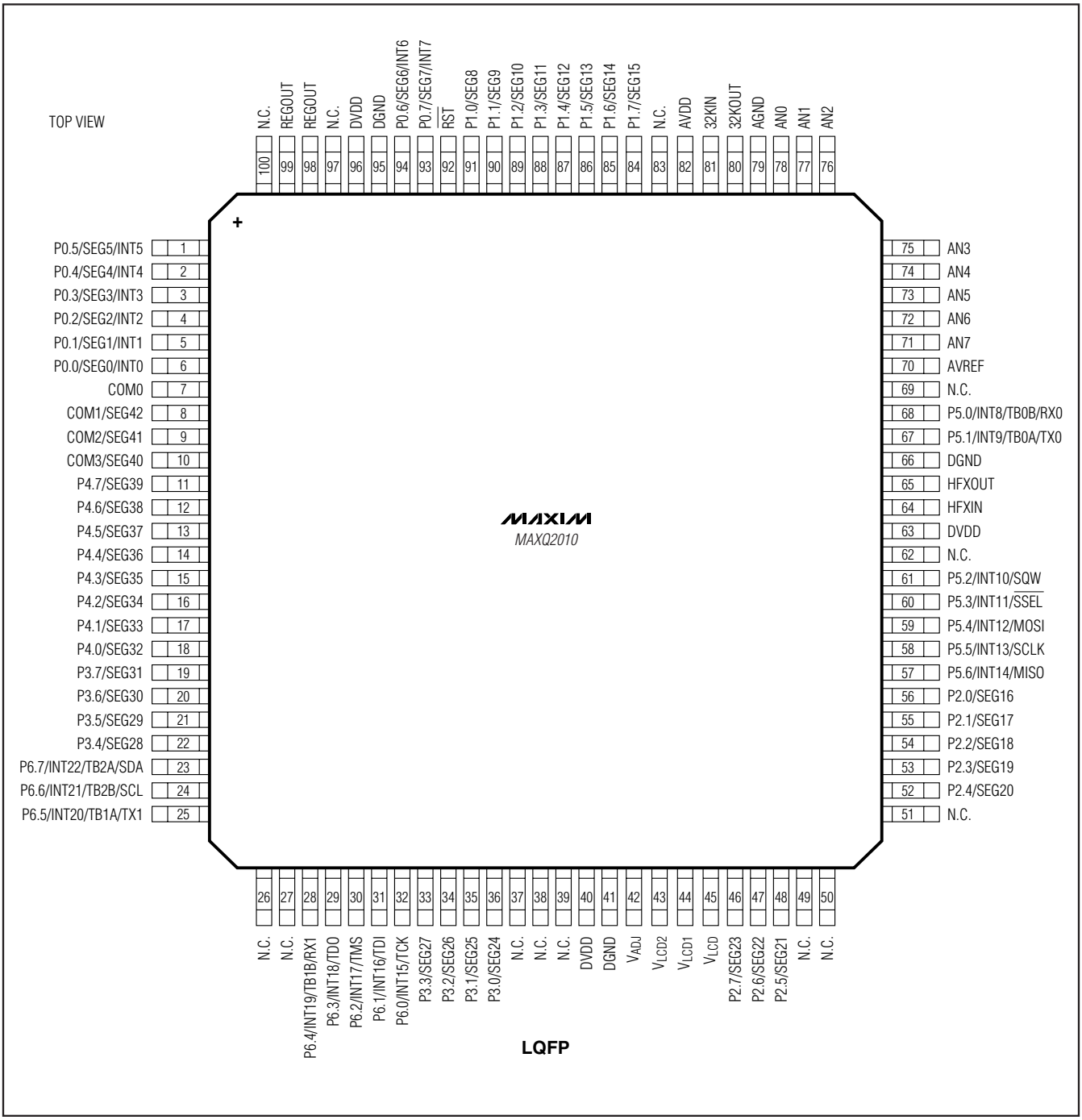
Careful PCB layout significantly minimizes noise on the analog inputs, resulting in less noise on the digital I/O that could cause improper operation. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep any bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

Separate ground areas must be provided for the analog (AGND) and digital (DGND) portions, connected together at a single point.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DVDD} or below DGND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

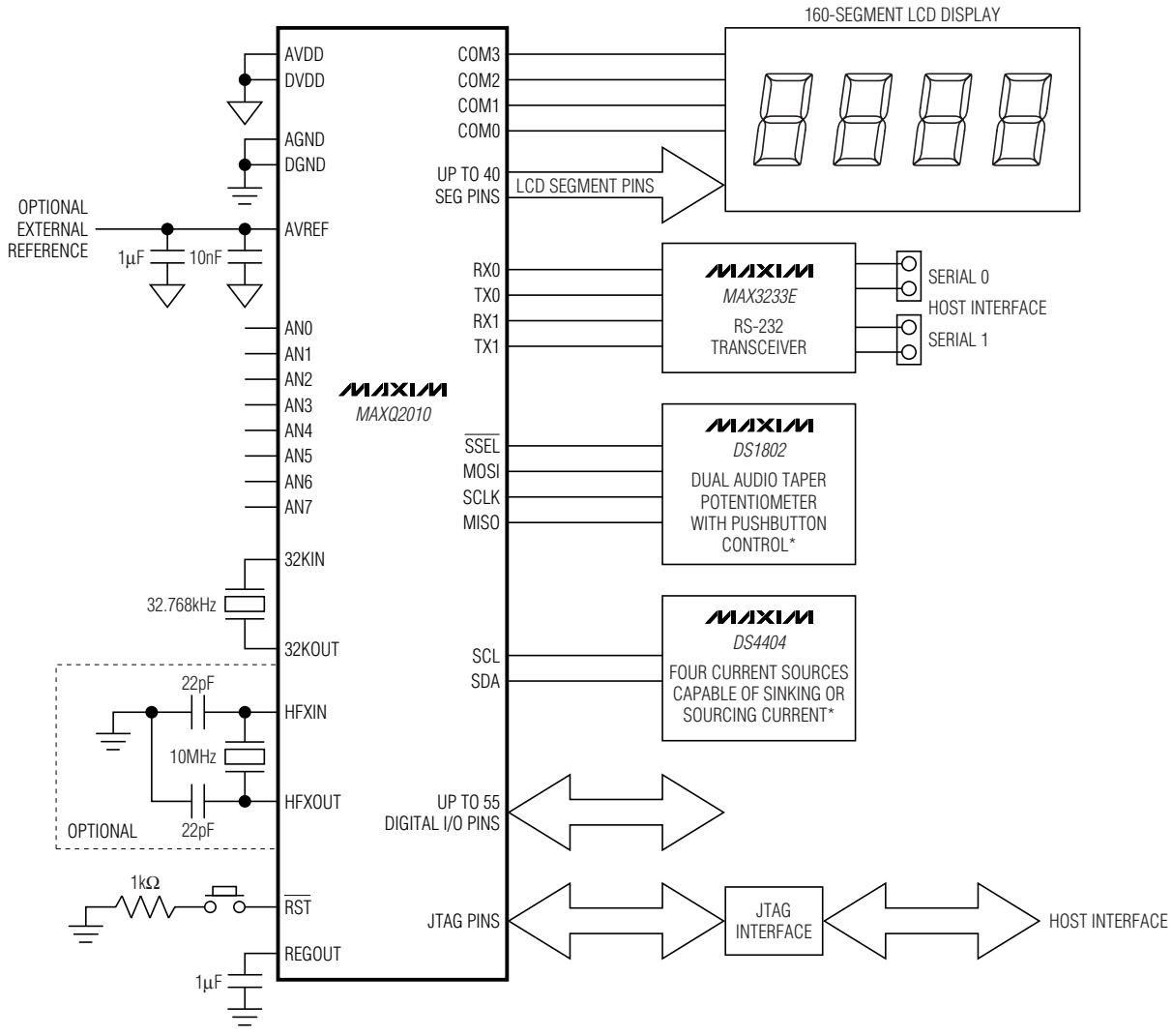
Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Pin Configuration



16-Bit Mixed-Signal Microcontroller with LCD Interface

Typical Application Circuit



*APPLICATION DEPENDENT.

Additional Documentation

Designers must have four documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maxim-ic.com/microcontrollers**.

- This MAXQ2010 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ2010 revision-specific errata sheet (**www.maxim-ic.com/errata**).
- The *MAXQ Family User's Guide*, which contains detailed information on core features and operation, including programming (**www.maxim-ic.com/MAXQUG**).
- The *MAXQ Family User's Guide: MAXQ2010 Supplement*, which contains detailed information on features specific to the MAXQ2010.

Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at **www.maxim-ic.com/MAXQ_tools**.

For technical support, go to **https://support.maxim-ic.com/micro**.

Selector Guide

PART	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	LCD SEGMENTS	ADC CHANNELS	ADC RESOLUTION
MAXQ2010-RFX+	64	2	160	8	12

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
100 LQFP	—	**21-0297**

16-Bit Mixed-Signal Microcontroller with LCD Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release.	—
1	12/08	Updated the title to include “LCD Interface.”	All
		Corrected the axis titles for TOC2 in the *Typical Operating Characteristics* section.	14
		Added the *I^2C Bus* and *Serial Peripheral Interface (SPI)* sections.	26

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