19-4076; Rev 0; 7/08

EVALUATION KIT AVAILABLE

Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

MAX9877

General Description

The MAX9877 combines a high-efficiency Class D audio power amplifier with a stereo Class AB capacitorless DirectDrive® headphone amplifier. Maxim's 3rd generation, filterless Class D amplifier with active emissions limiting technology provides Class AB performance with Class D efficiency.

The MAX9877 delivers up to 725mW from a 3.7V supply into an 8Ω load with 87% efficiency to extend battery life. The filterless modulation scheme combined with active emissions limiting circuitry and spread-spectrum modulation greatly reduces EMI while eliminating the need for output filtering used in traditional Class D devices.

The stereo Class AB headphone amplifier in the MAX9877 uses Maxim's DirectDrive architecture, that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, space, and component height.

The device utilizes a user-defined input architecture, three preamplifier gain settings, an input mixer, volume control, comprehensive click-and-pop suppression, and I²C control. A bypass mode feature disables the integrated Class D amplifier and utilizes an internal DPST switch to allow an external amplifier to drive the speaker that is connected at the outputs of the MAX9877.

The MAX9877 is available in a thermally efficient, space-saving 20-bump WLP package.

Applications

Cell Phones

Portable Multimedia Players

Features

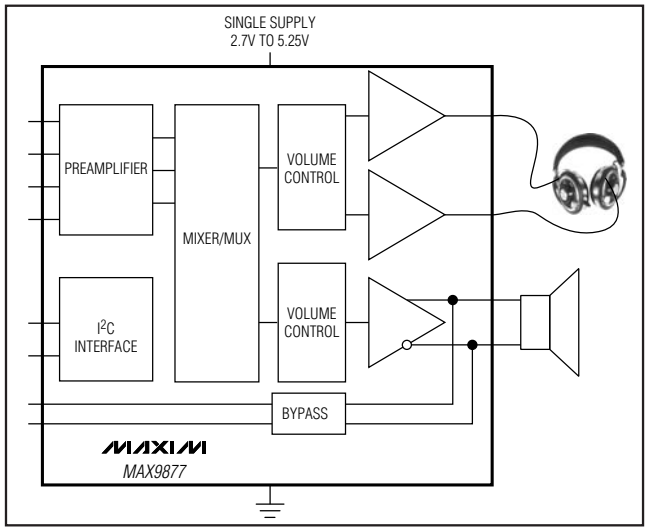
- **Low Emissions, Filterless Class D Amplifier Achieves Better than 10dB Margin Under EN55022 Class B Limits**
- **Low RF Susceptibility Design Rejects TDMA Noise from GSM Radios**
- **Input Mixer with User-Defined Input Mode**
- **725mW Speaker Output (R_{SPK} = 8Ω, PV_{DD} = 3.7V)**
- **53mW Headphone Output (R_{HP} = 16Ω, V_{DD} = 3.7V)**
- **Low 0.05% THD+N at 1kHz (Class D Power Amplifier)**
- **Low 0.016% THD+N at 1kHz (Headphone Amplifier)**
- **87% Efficiency (R_{SPK} = 8Ω, P_{OUT} = 750mW)**
- **1.6Ω Analog Switch for Speaker Amplifier Bypass**
- **High Speaker Amplifier PSRR (72dB at 217Hz)**
- **High Headphone Amplifier PSRR (84dB at 217Hz)**
- **I²C Control**
- **Hardware and Software Shutdown Mode**
- **Click-and-Pop Suppression**
- **Current-Limit and Thermal Protection**
- **Available in a Space-Saving, 2.5mm x 2.0mm WLP Package**

Ordering Information

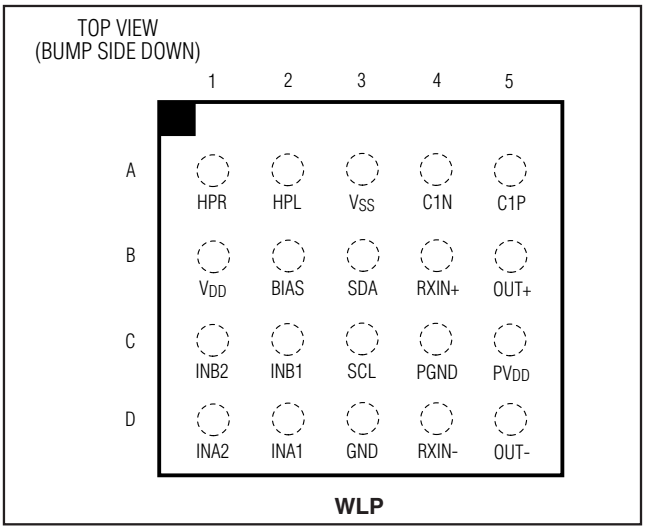
PART	TEMP RANGE	PIN-PACKAGE
MAX9877EWP+TG45	-40°C to +85°C	20 WLP (5x4)

+Denotes a lead-free package.
T = Tape and reel.
G45 indicates protective die coating.

Simplified Block Diagram



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

V_{DD}, PV_{DD} to PGND .....-0.3V to +5.5V
V_{DD} to PV_{DD} .....-0.3V to +0.3V
V_{SS} to PGND .....-5.5V to +0.3V
C1N to PGND .....(V_{SS} - 0.3V) to +0.3V
C1P to PGND .....-0.3V to (PV_{DD} + 0.3V)
HPL, HPR to V_{SS}
(Note 1) .....-0.3V to the lower of (PV_{DD} - (V_{SS} + 0.3V)) or +9V
HPL, HPR to PV_{DD}
(Note 2).....+0.3V to the higher of (V_{SS} - (PV_{DD} - 0.3V)) or -9V
GND to PGND.....±0.3V
INA1, INA2, INB1, INB2, BIAS.....-0.3V to +4V
SDA, SCL.....-0.3V to +5.5V
All Other Pins to GND.....-0.3V to (PV_{DD} + 0.3V)
Continuous Current In/Out of PV_{DD}, PGND, OUT_.....±800mA
Continuous Current In/Out of HPR and HPL.....140mA
Continuous Current In/Out of RXIN+ and RXIN-.....150mA
Continuous Input Current V_{SS}.....100mA
Continuous Input Current (all other pins) .....±20mA
Duration of OUT_ Short Circuit to GND or PV_{DD}.....Continuous
Duration of Short Circuit Between OUT+ and OUT- ..Continuous
Duration of HP_ Short Circuit to GND or PV_{DD} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Bump WLP, 5 x 4, Multilayer Board
(derate 13.0mW/°C above +70°C).....1.04W
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: HPR and HPL should be limited to no more than 9V above V_{SS}, or above PV_{DD} + 0.3V, whichever limits first.
Note 2: HPR and HPL should be limited to no more than 9V below PV_{DD}, or below V_{SS} - 0.3V, whichever limits first.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 3.3V. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}, PV_{DD}	Guaranteed by PSRR test		2.7		5.25	V
Quiescent Current	I_{DD}	HP mode, OUTMODE = 2	OSC = 00		5.6	9.0	mA
			OSC = 10		5.5		
		SPK mode, OUTMODE = 7	OSC = 00		6.6	11.0	
			OSC = 10		5.7		
		SPK + HP mode, OUTMODE = 9	OSC = 00		10.4	16.0	
			OSC = 10		9.3		
Shutdown Current	I_{SHDN}	I_{SHDN} = I_{VDD} + I_{PVDD}; $\overline{SHDN}$ = 0; V_{SDA} = V_{SCL} = logic-high; T_A = +25°C			10	22	µA
Turn-On Time	t_{ON}	Time from shutdown to full operation	OSC = 00		10		ms
			OSC = 01		10		
			OSC = 10		17.5		
BIAS Release Time	t_{BR}	After forcing BIAS low, time from BIAS released to I^2C reset			25	80	ms
Input Resistance	R_{IN}	T_A = +25°C, preamp gain = 0dB or +9dB		11	21	31	kΩ
		T_A = +25°C, preamp gain = +20dB		3	5.5	8	
Maximum Input Signal Swing		Preamp = 0dB			2.30		V_{P-P}
		Preamp = +9dB			0.820		
		Preamp = +20dB			0.230		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 3.3V. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz (differential input mode)	Preamp = 0dB		47		dB
			Preamp = +9dB		49		
			Preamp = +20dB		42		
Input DC Voltage		IN_ inputs		1.22	1.3	1.38	V
Bias Voltage	V_{BIAS}			1.13	1.2	1.27	V
SPEAKER AMPLIFIER (OUTMODE = 1)							
Output Offset Voltage	V_{OS}	T_A = +25°C (volume at mute)			±0.5	±4	mV
		T_A = +25°C (volume at 0dB, OUTMODE = 1, ΔIN_ = 0)			±1.5		
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, volume at mute (Note 4)	Into shutdown		-70		dBV
			Out of shutdown		-70		
Power-Supply Rejection Ratio (Note 4)	PSRR	T_A = +25°C, PV_{DD} = V_{DD}	PV_{DD} = V_{DD} = 2.7V to 5.5V	50	76		dB
			f = 217Hz, 100mV_{P-P} ripple		72		
			f = 1kHz, 100mV_{P-P} ripple		68		
			f = 20kHz, 100mV_{P-P} ripple		55		
Output Power (Note 5)	P_{OUT}	THD+N ≤ 1%	Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		725		mW
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.3V		560		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.0V		465		
			Z_{SPK} = 4Ω + 33µH, V_{DD} = 3.7V		825		
			Z_{SPK} = 4Ω + 33µH, V_{DD} = 3.0V		770		
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, P_{OUT} = 350mW, T_A = +25°C, Z_{SPK} = 8Ω + 68µH			0.05		%
Signal-to-Noise Ratio	SNR	A-weighted, OUTMODE = 1, 3, 4, 6	ΔIN_ = 0 (single-ended)		92		dB
			ΔIN_ = 1 (differential)		94		
		A-weighted, OUTMODE = 7, 9	ΔIN_ = 0 (single-ended)		88		
			ΔIN_ = 1 (differential)		92		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 3.3V. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Frequency		Spread-spectrum modulation mode, OSC = 00			1176 ±60		kHz
		Fixed-frequency mode, OSC = 01			1100		
		Fixed-frequency mode, OSC = 10			700		
Current Limit					1.5		A
Efficiency	η	P_{OUT} = 600mW, f = 1kHz			87		%
Speaker Gain	A_V			11.5	12.0	12.5	dB
Output Noise		A-weighted, OUTMODE = 1, ΔIN_ = 0 (Note 4)			63		$µV_{RMS}$
HEADPHONE AMPLIFIERS (OUTMODE = 2)							
Output Offset Voltage	V_{OS}	T_A = +25°C (volume at mute)			±0.15	±0.6	mV
		T_A = +25°C (volume at 0dB)			±1.6		
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second. volume at mute (Note 4)	Into shutdown		-80		dBV
			Out of shutdown		-80		
Power-Supply Rejection Ratio (Note 4)	PSRR	T_A = +25°C, PV_{DD} = V_{DD}	PV_{DD} = V_{DD} = 2.7V to 5.25V	70	85		dB
			f = 217Hz, V_{RIPPLE} = 100mV_{P-P}		84		
			f = 1kHz, V_{RIPPLE} = 100mV_{P-P}		80		
			f = 20kHz, V_{RIPPLE} = 100mV_{P-P}		62		
Output Power	P_{OUT}	THD+N ≤ 1%	R_{HP} = 16Ω		53		mW
			R_{HP} = 32Ω		27		
Headphone Gain	A_V			-0.4	0	+0.4	dB
Channel-to-Channel Gain Tracking		T_A = +25°C, HPL to HPR, volume at 0dB, OUTMODE = 2, 5; ΔIN_ = 0			±0.3	±2.5	%
Total Harmonic Distortion Plus Noise	THD+N	R_{HP} = 32Ω (P_{OUT} = 10mW, f = 1kHz)			0.016		%
		R_{HP} = 16Ω (P_{OUT} = 10mW, f = 1kHz), T_A = +25°C			0.03		
Signal-to-Noise Ratio	SNR	A-weighted, OUTMODE = 2, 3, 5, 6; R_{HP} = 16Ω	ΔIN_ = 0 (single-ended)		98		dB
			ΔIN_ = 1 (differential)		98		
		A-weighted, R_{HP} = 16Ω, OUTMODE = 8, 9	ΔIN_ = 0 (single-ended)		96		
			ΔIN_ = 1 (differential)		96		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 3.3V. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	SR				0.35		V/µs
Capacitive Drive	C_L				100		pF
Crosstalk		HPL to HPR, HPR to HPL, f = 20Hz to 20kHz			65		dB
Charge-Pump Frequency		Spread-spectrum modulation mode, OSC = 00			588 ±30		kHz
		Fixed-frequency mode, OSC = 01		430	550	670	
		Fixed-frequency mode, OSC = 10		220	350	500	
VOLUME CONTROL							
Minimum Setting		_VOL = 1			-75		dB
Maximum Setting		_VOL = 31			0		dB
Preamp Gain		Input A or B	PGAIN_ = 00		0		dB
			PGAIN_ = 01		9		
			PGAIN_ = 10		20		
Mute Attenuation		f = 1kHz, _VOL = 0	Speaker		100		dB
			Headphone		110		
Zero-Crossing Detection Timeout		ZCD = 1			60		ms
ANALOG SWITCH							
On-Resistance	R_{ON}	$I_{RXIN_}$ = 20mA, RXIN_ = 0V and V_{DD}, BYPASS = 1	T_A = +25°C		1.6	4.5	Ω
			T_A = T_{MIN} to T_{MAX}			5.2	
Total Harmonic Distortion		V_{DIF} = $2V_{P-P}$, V_{CM} = $V_{DD}/2$, f = 1kHz, BYPASS = 1, T_A = +25°C	Series resistance is 9.1Ω per switch		0.05	0.25	%
			No series resistors		0.3		
Off-Isolation		BYPASS = 0, RXIN+ and RXIN- to GND = 50Ω, Z_{SPK} = 8Ω + 68µH, f = 10kHz, referred to speaker output signal			88		dB
DIGITAL INPUTS							
Input-Voltage High (SDA, SCL)	V_H			1.4			V
Input-Voltage Low (SDA, SCL)	V_L					0.4	V
Input-Voltage Low (BIAS)	V_{BL}					0.15	V
Input Hysteresis (SDA, SCL)	V_{HYS}				80		mV
SDA, SCL Input Capacitance	C_{IN}				4		pF
Input Leakage Current	I_{IN}	SDA, SCL; T_A = +25°C				±1.0	µA
BIAS Pullup Current	I_{BIAS}				94		µA
DIGITAL OUTPUTS (SDA Open Drain)							
Output Low Voltage SDA	V_{OL}	I_{SINK} = 3mA				0.4	V
Output Fall Time SDA	t_{OF}	$V_{H(MIN)}$ to $V_{L(MAX)}$ bus capacitance = 10pF to 400pF, I_{SINK} = 3mA				250	ns

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE INTERFACE TIMING						
External Pullup Voltage Range: SDA and SCL			1.7		3.6	V
Serial Clock Frequency	f_{SCL}		DC		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold	$t_{HD:STA}$		0.6			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0		900	ns
Maximum Receive SCL/SDA Rise Time	t_R				300	ns
Maximum Receive SCL/SDA Fall Time	t_F				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF

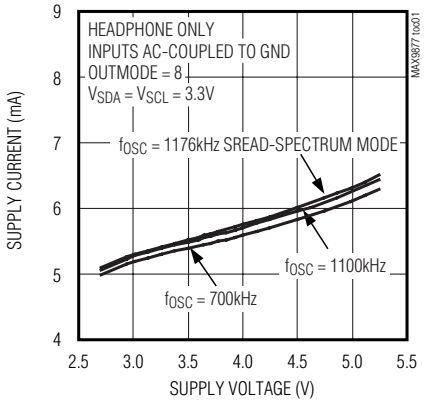
Note 3: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.
Note 4: Amplifier inputs are AC-coupled to GND.
Note 5: Output levels higher than 825mW are not recommended for extended durations. Production tested with Z_{SPK} = 8Ω + 68µH only.

Typical Operating Characteristics

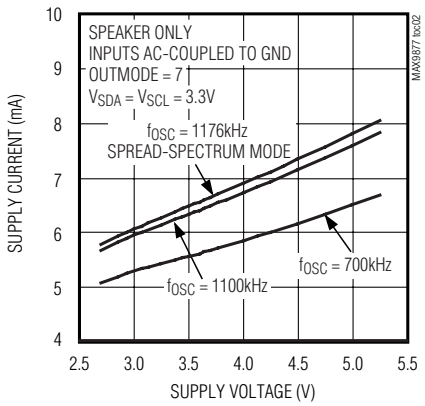
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GENERAL

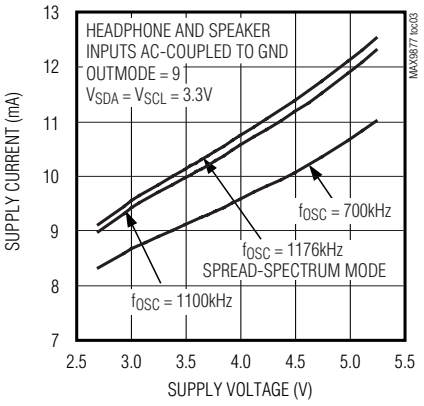
SUPPLY CURRENT vs. SUPPLY VOLTAGE



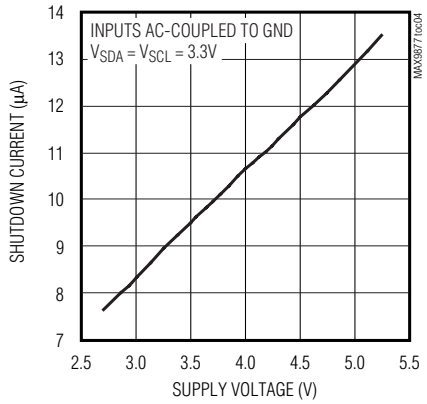
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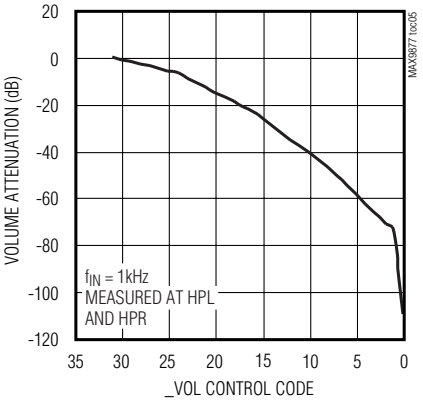
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



VOLUME ATTENUATION vs. _VOL CONTROL CODE



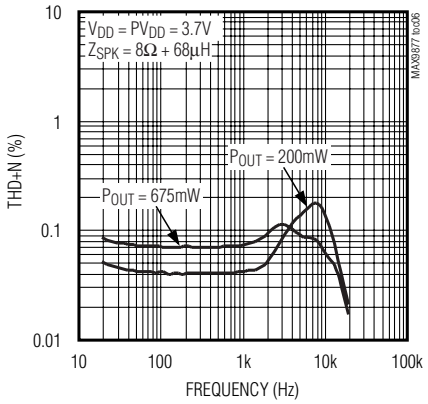
Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

Typical Operating Characteristics (continued)

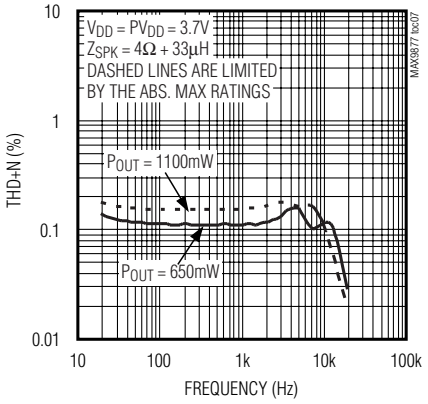
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SPEAKER AMPLIFIER

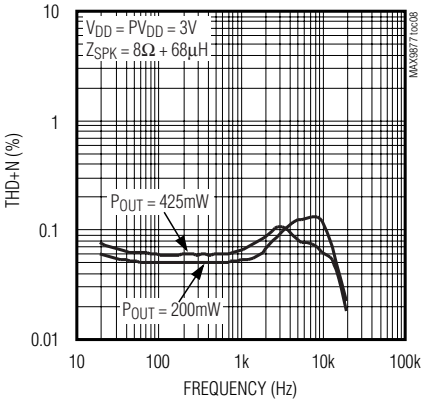
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



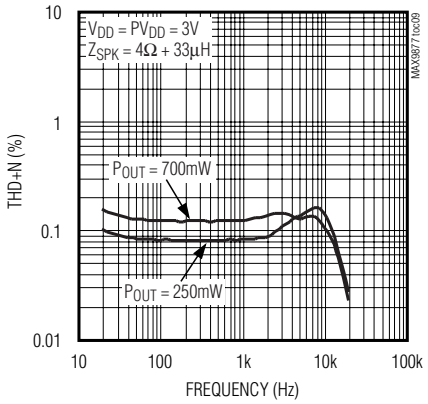
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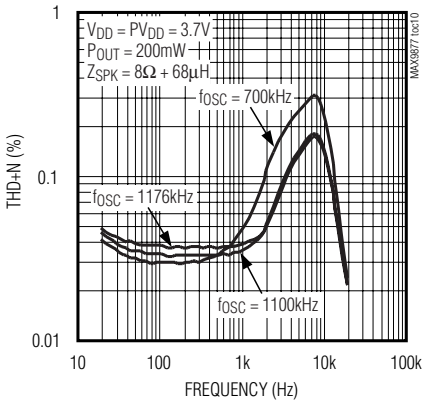
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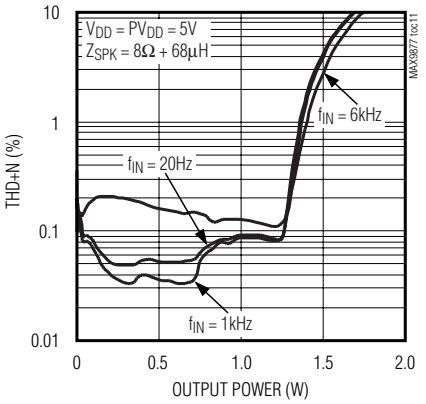
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



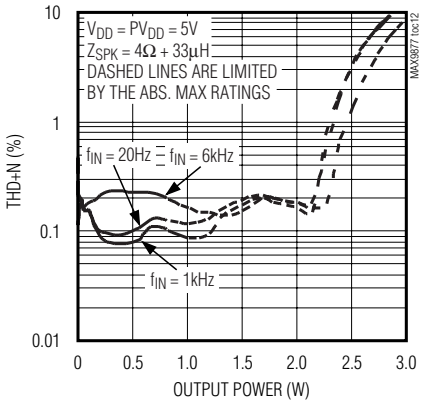
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



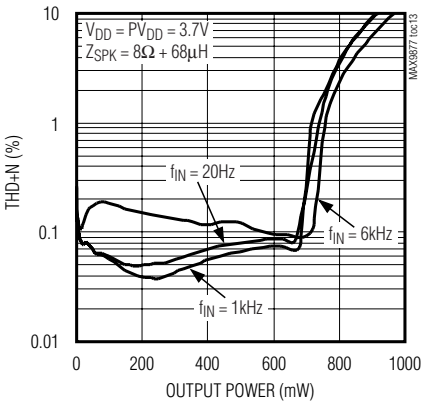
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



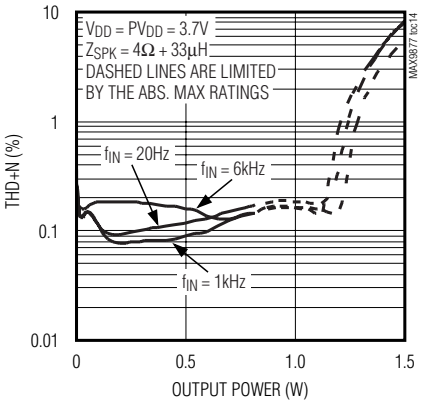
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



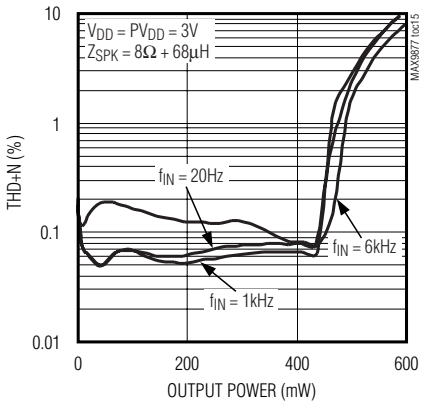
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

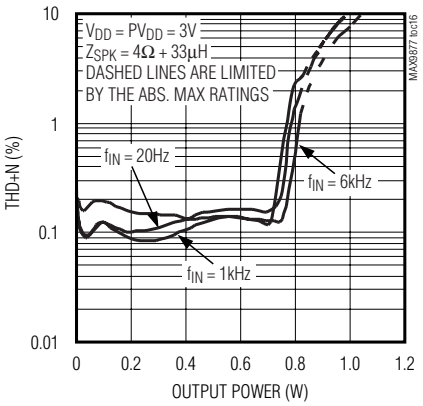
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



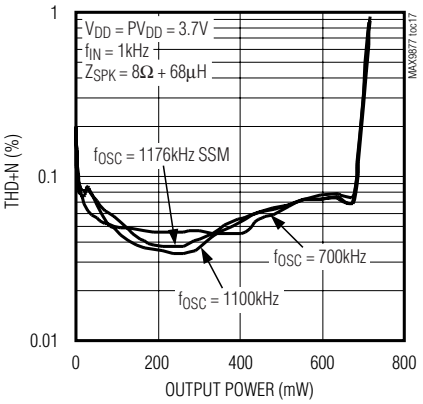
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



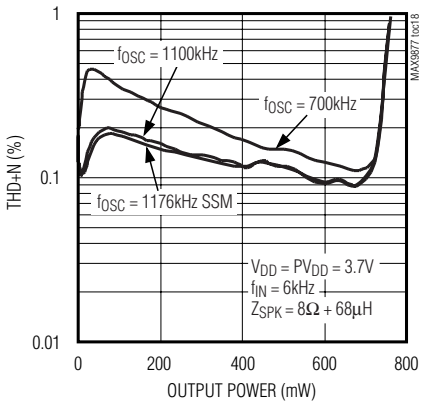
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



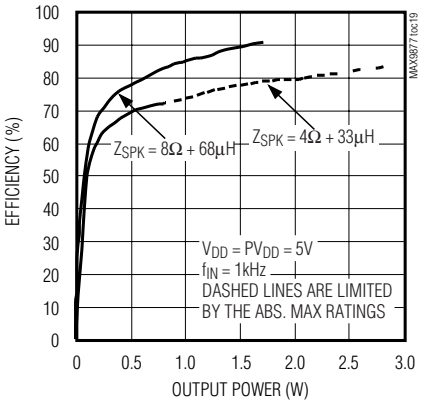
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



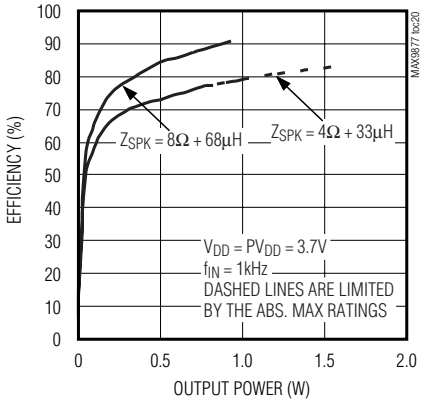
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



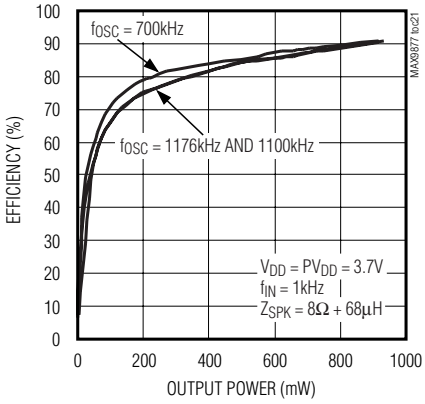
EFFICIENCY vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER

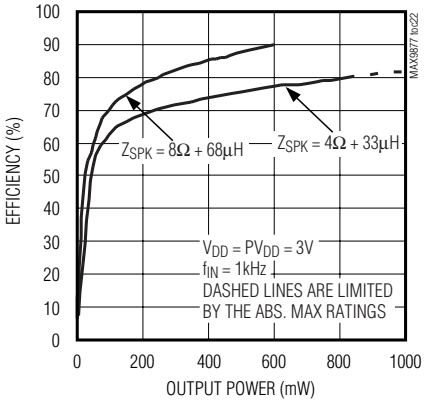


Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

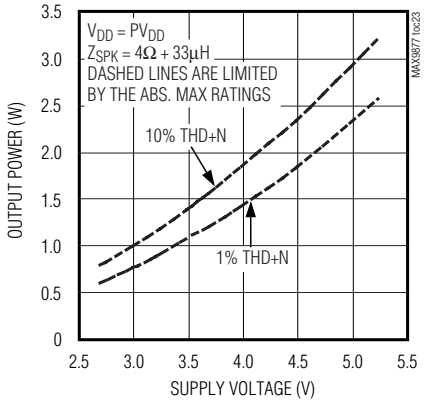
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

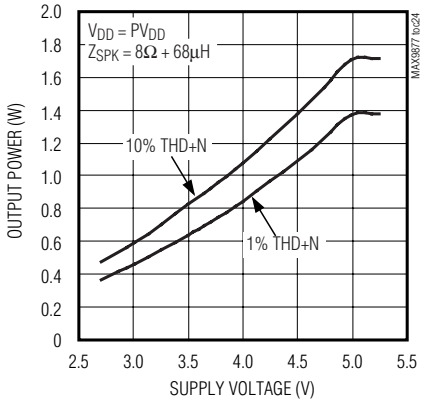
EFFICIENCY vs. OUTPUT POWER



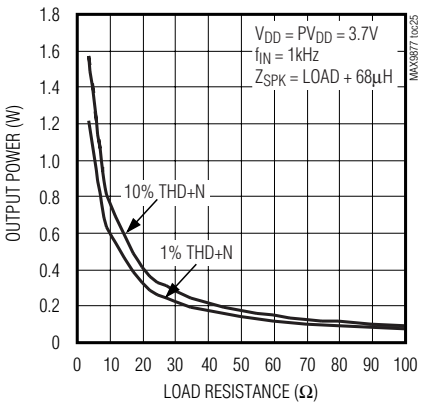
OUTPUT POWER vs. SUPPLY VOLTAGE



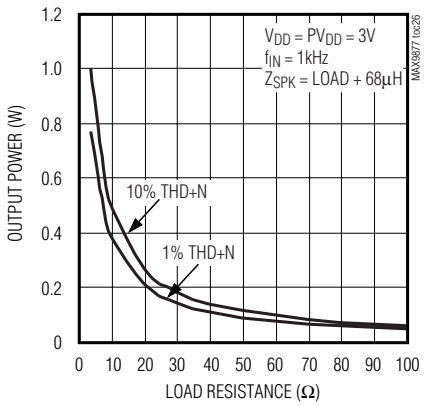
OUTPUT POWER vs. SUPPLY VOLTAGE



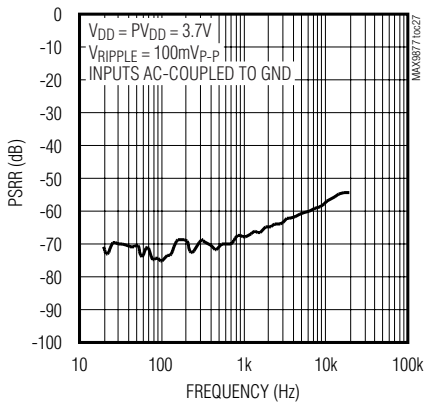
OUTPUT POWER vs. LOAD RESISTANCE



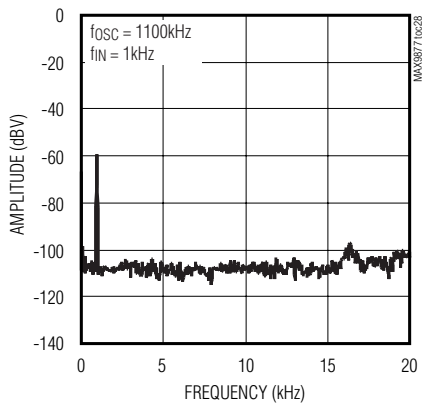
OUTPUT POWER vs. LOAD RESISTANCE



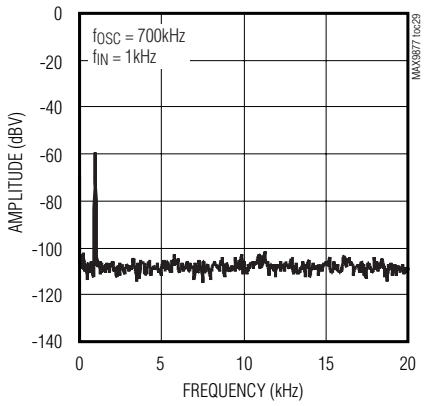
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



IN-BAND OUTPUT SPECTRUM



IN-BAND OUTPUT SPECTRUM

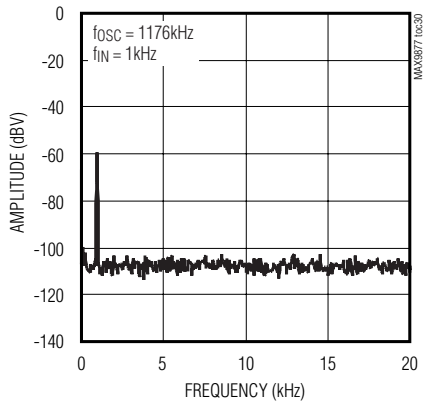


Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

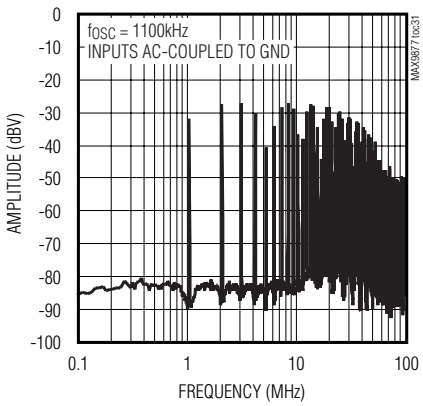
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

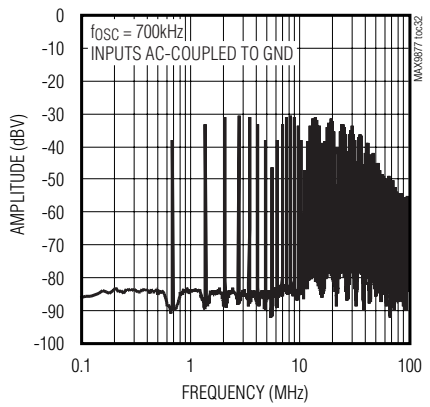
IN-BAND OUTPUT SPECTRUM



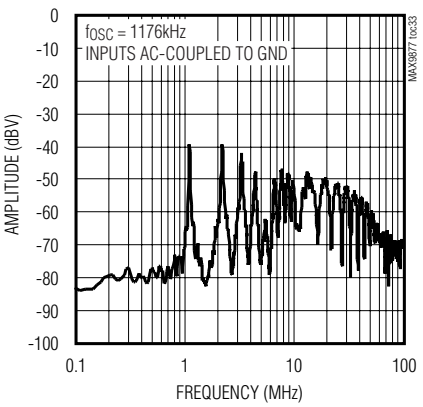
WIDEBAND OUTPUT SPECTRUM



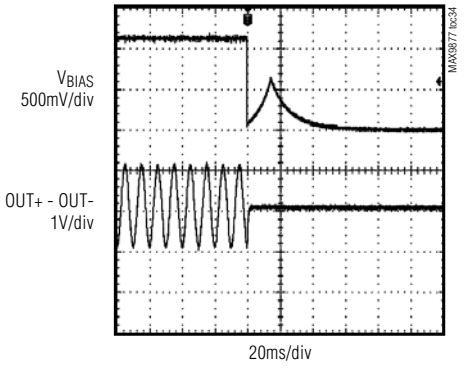
WIDEBAND OUTPUT SPECTRUM



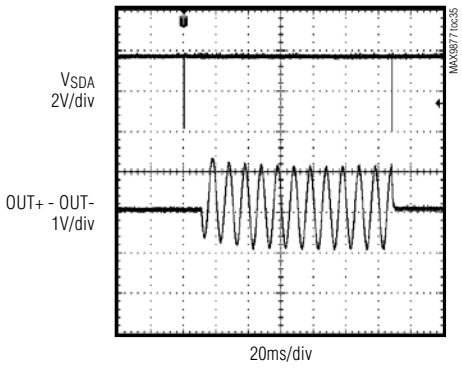
WIDEBAND OUTPUT SPECTRUM



HARDWARE SHUTDOWN RESPONSE



SOFTWARE SHUTDOWN ON- AND OFF-RESPONSE



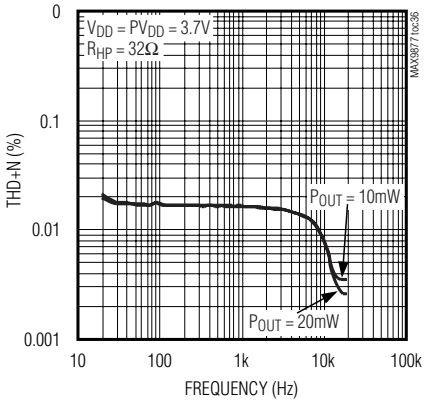
Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

Typical Operating Characteristics (continued)

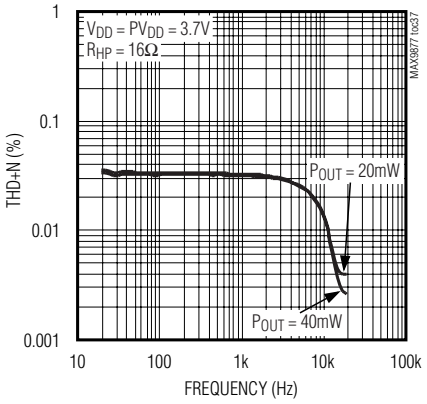
(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

HEADPHONE AMPLIFIER

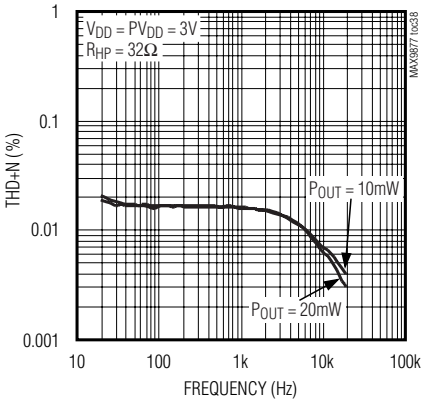
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



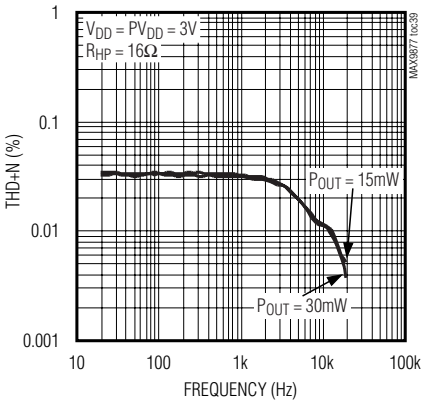
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



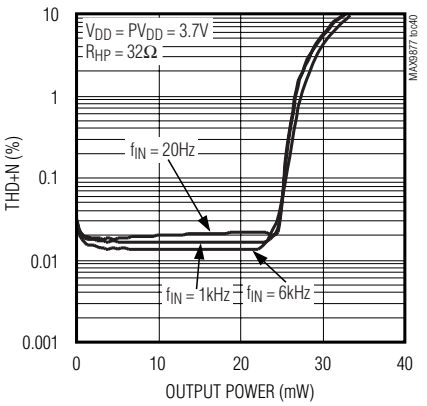
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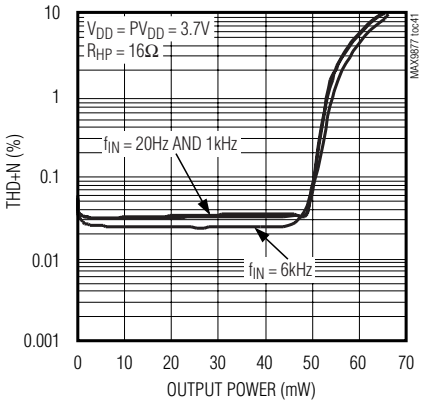
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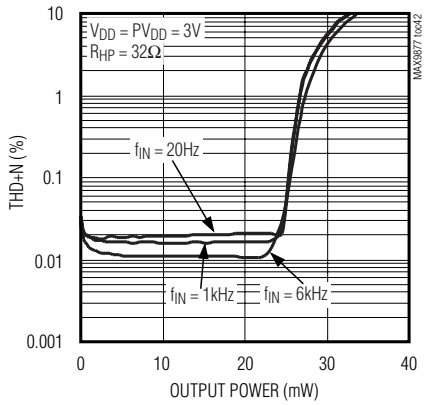
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



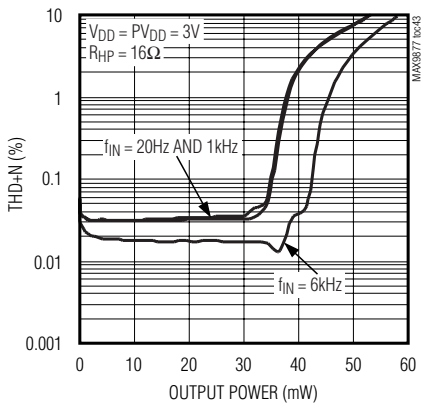
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



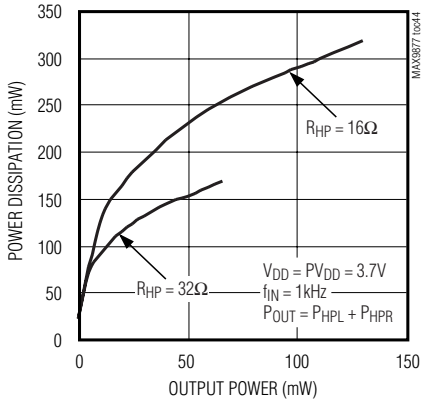
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



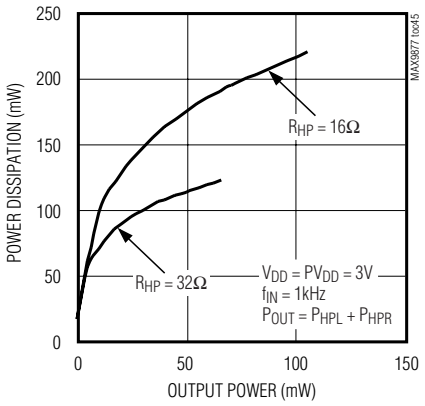
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

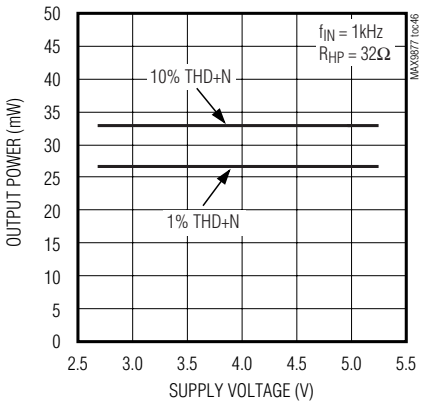
POWER DISSIPATION vs. OUTPUT POWER



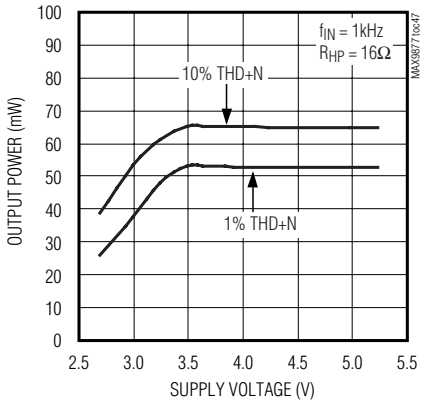
POWER DISSIPATION vs. OUTPUT POWER



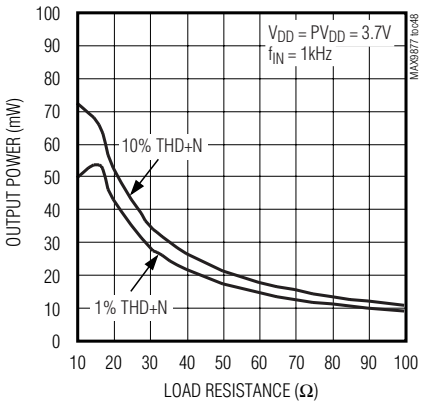
OUTPUT POWER vs. SUPPLY VOLTAGE



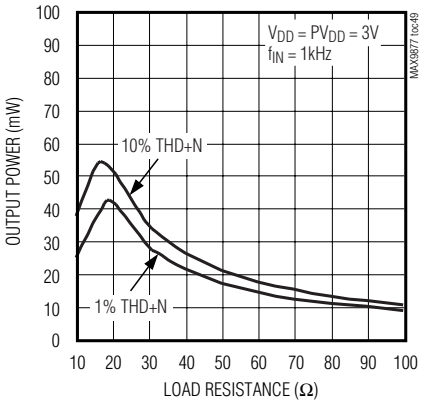
OUTPUT POWER vs. SUPPLY VOLTAGE



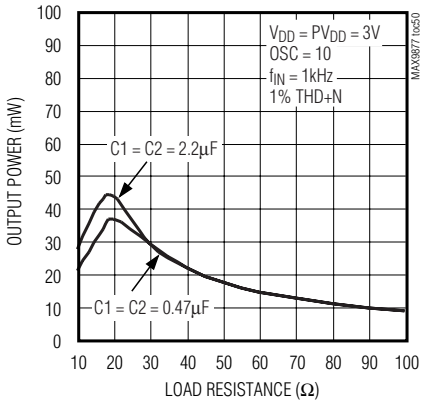
OUTPUT POWER vs. LOAD RESISTANCE



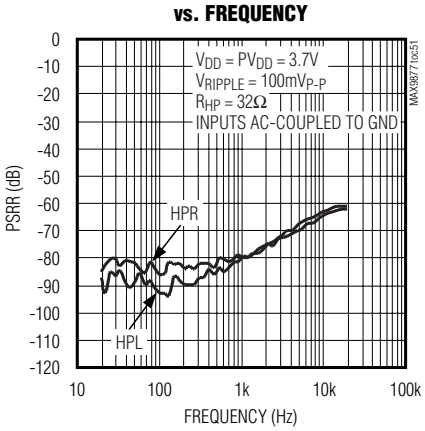
OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. LOAD RESISTANCE



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY

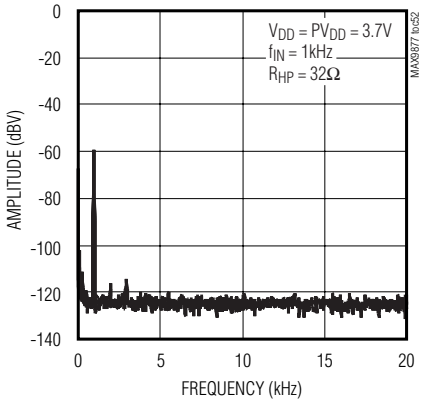


Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

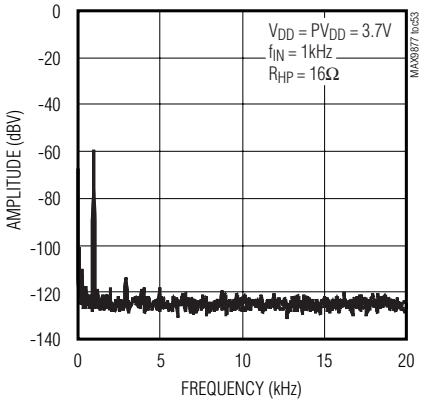
Typical Operating Characteristics (continued)

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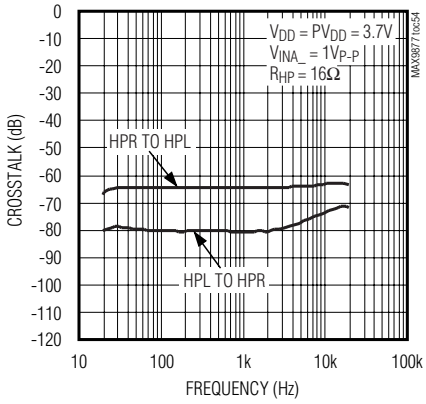
OUTPUT SPECTRUM



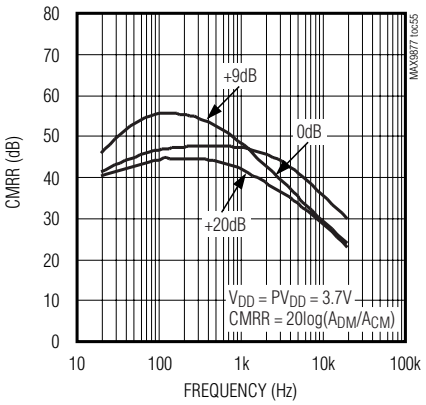
OUTPUT SPECTRUM



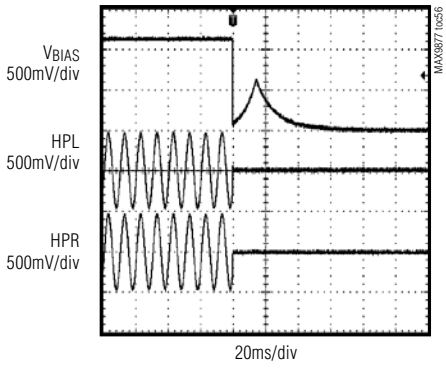
CROSSTALK vs. FREQUENCY



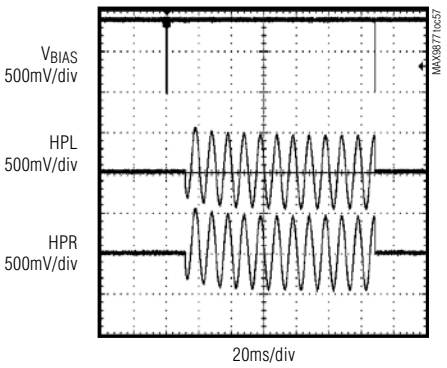
COMMON-MODE REJECTION RATIO vs. FREQUENCY



HARDWARE SHUTDOWN RESPONSE



SOFTWARE SHUTDOWN ON- AND OFF-REPSONSE

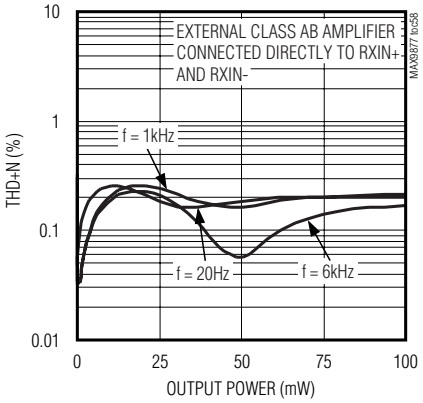


Typical Operating Characteristics (continued)

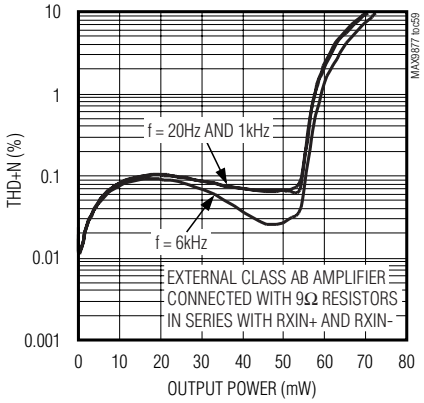
(V_{DD} = PV_{DD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, volume controls = 0dB, OSC = 00, BYPASS = 0, $\overline{SHDN}$ = 1. Speaker loads (Z_{SPK}) connected between OUT+ and OUT-. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. C1 = C2 = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

ANALOG SWITCH

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

Pin Description

PIN	NAME	FUNCTION
A1	HPR	Right Headphone Output
A2	HPL	Left Headphone Output
A3	V_{SS}	Headphone Amplifier Negative Power Supply. Bypass with a 1µF capacitor to PGND.
A4	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF capacitor between C1P and C1N.
A5	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF capacitor between C1P and C1N.
B1	V_{DD}	Analog Supply. Connect to PV_{DD}. Bypass with a 1µF capacitor to GND.
B2	BIAS	Common-Mode Bias. Bypass to GND with a 1µF capacitor. Pulse low to reset the part and place in shutdown (see the *Typical Application Circuit*).
B3	SDA	Serial-Data Input. Connect a pullup resistor from SDA to a 1.7V to 3.6V supply.
B4	RXIN+	Receiver Bypass Positive Input
B5	OUT+	Positive Speaker Output
C1	INB2	Input B2. Right input or positive input (see the *Differential Input Configuration (ΔIN_)* section).
C2	INB1	Input B1. Left input or negative input (see the *Differential Input Configuration (ΔIN_)* section).
C3	SCL	Serial-Clock Input. Connect a pullup resistor from SCL to a 1.7V to 3.6V supply.
C4	PGND	Power Ground
C5	PV_{DD}	Class D and Charge-Pump Power Supply. Bypass with a 1µF capacitor to PGND.
D1	INA2	Input A2. Right input or positive input (see the *Differential Input Configuration (ΔIN_)* section).
D2	INA1	Input A1. Left input or negative input (see the *Differential Input Configuration (ΔIN_)* section).
D3	GND	Analog Ground
D4	RXIN-	Receiver Bypass Negative Input
D5	OUT-	Negative Speaker Output

Detailed Description

Signal Path

The MAX9877 signal path consists of flexible inputs, signal mixing, volume control, and output amplifiers (Figure 1).

The inputs can be configured for single-ended or differential signals (Figure 2). The internal preamplifiers feature three programmable gain settings of 0dB, +9dB, and +20dB. Following preamplification, the input signals are mixed, volume adjusted, and routed to the headphone and speaker amplifiers based on the output mode configuration (see Table 7). The volume control stages provide up to 75dB attenuation. The headphone amplifier is configured as a unity-gain buffer while the speaker amplifier provides +12dB of additional gain.

When an input is configured as mono differential it can be routed to the speaker or to both headphones. When an input is stereo, it is mixed to mono without attenuation for the speaker and kept stereo for the headphones.

When the application does not require the use of both INA_ and INB_, the SNR of the MAX9877 is improved by deselecting the unused input through the I^2C output mode register and AC-coupling the unused inputs to ground with a 330pF capacitor. The 330pF capacitor and the input resistance to the MAX9877 form a high-pass filter preventing audible noise from coupling into the outputs.

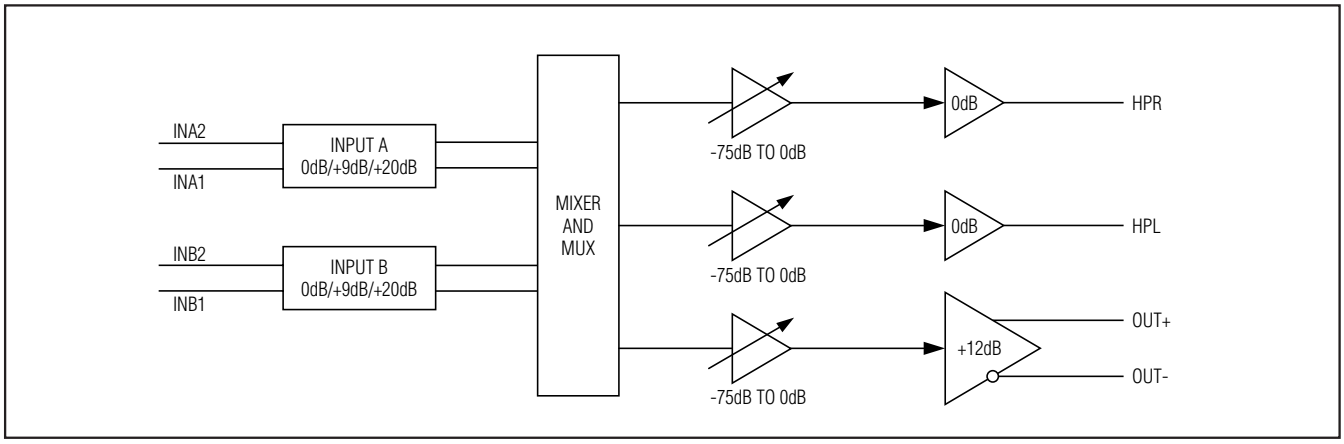


Figure 1. Signal Path

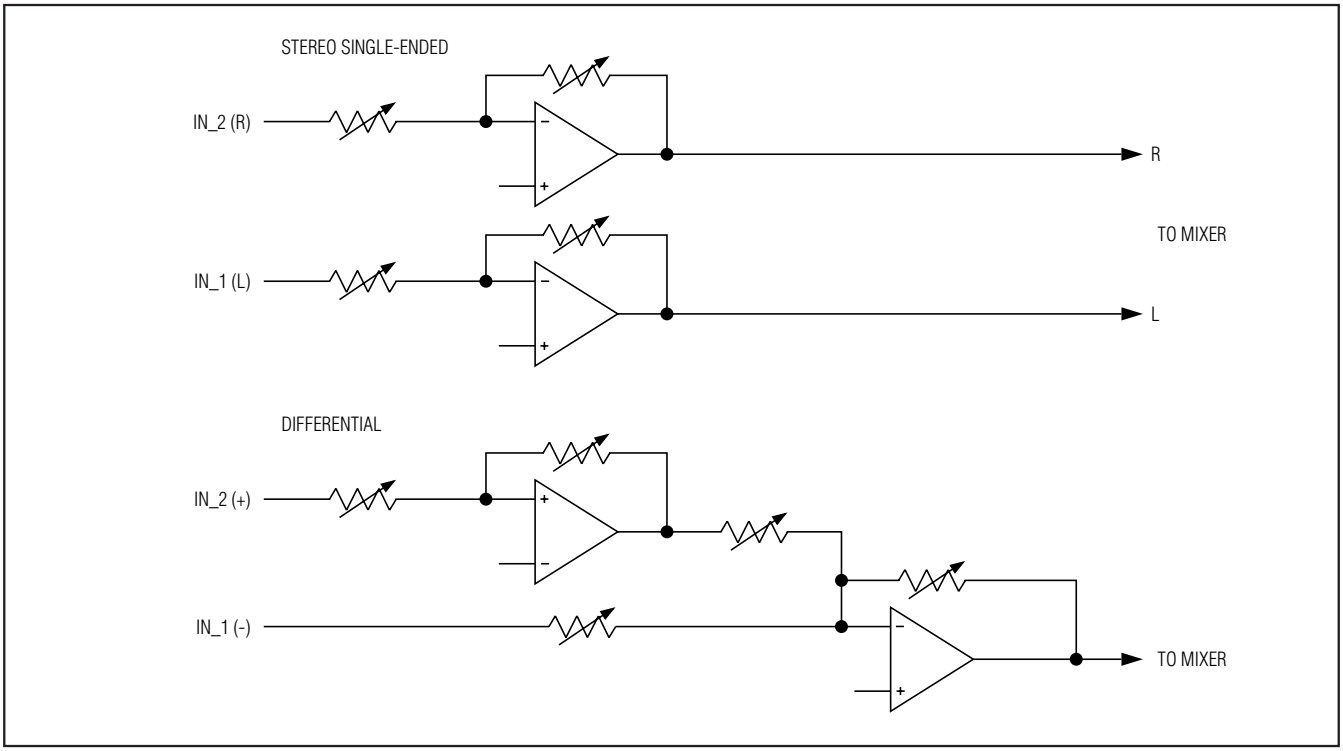


Figure 2. Differential and Stereo Single-Ended Input Configurations

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Volume Control and Mute

The MAX9877 features three volume control registers (see Table 4) allowing independent volume control of mono speaker and stereo headphone amplifier outputs. Each volume control register has 31 steps providing 0 to 75dB (typ) of attenuation and a mute function.

Class D Speaker Amplifier

The MAX9877 integrates a filterless Class D amplifier that offers much higher efficiency than Class AB without the typical disadvantages.

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%, however, that efficiency is only exhibited at peak output power. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9877 still exhibits 70% efficiency under the same conditions (Figure 3).

Ultra-Low EMI Filterless Output Stage

In traditional Class D amplifiers, the high dV/dt of the rising and falling edge transitions results in increased EMI emissions, which requires the use of external LC filters or shielding to meet EN55022 electromagnetic-interference (EMI) regulation standards. Limiting the dV/dt normally results in decreased efficiency. Maxim's active emissions limiting circuitry actively limits the dV/dt of the rising and falling edge transitions, providing reduced EMI emissions, while maintaining up to 87% efficiency.

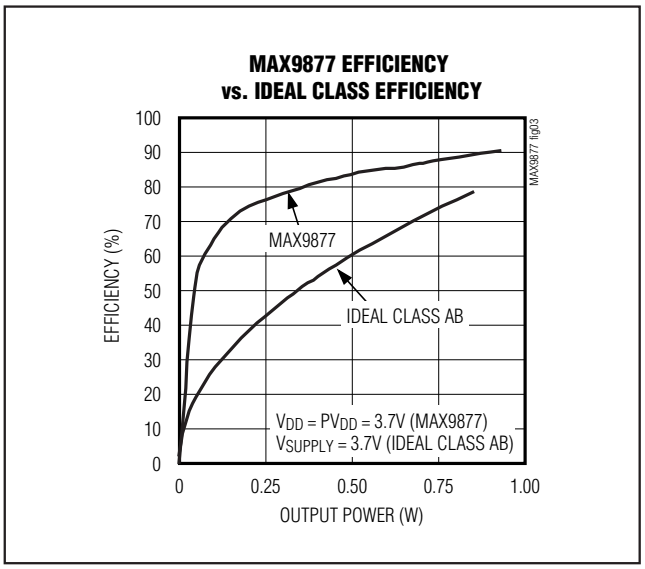


Figure 3. MAX9877 Efficiency vs. Class AB Efficiency

In addition to active emission limiting, the MAX9877 features a spread-spectrum modulation mode that flattens the wideband spectral components. Proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency (see the *Typical Operating Characteristics*). Select spread-spectrum modulation mode through the I^2C interface (Table 6). In spread-spectrum modulation mode, the switching frequency varies randomly by ±60kHz around the center frequency (1.176MHz). The effect is to reduce the peak energy at harmonics of the switching frequency. Above 10MHz, the wideband spectrum looks like white noise for EMI purposes (see Figure 4).

Speaker Current Limit

Most applications will not enter current limit unless the output is short circuited or connected incorrectly.

When the output current of the speaker amplifier exceeds the current limit (1.5A, typ) the MAX9877 disables the outputs for approximately 250µs. At the end of 250µs, the outputs are re-enabled, if the fault condition still exists, the MAX9877 will continue to disable and re-enable the outputs until the fault condition is removed.

Bypass Mode

The integrated DPST analog audio switch allows the MAX9877's Class D amplifier to be bypassed. In bypass mode, the Class D amplifier is automatically disabled allowing an external amplifier to drive the speaker connected between OUT+ and OUT- through RXIN+ and RXIN- (see the *Typical Application Circuit*).

The bypass switch is enabled at startup. The switch can be opened or closed even when the MAX9877 is in software shutdown (see the *I^2C Register Description* section).

Unlike discrete solutions, the switch design reduces coupling of Class D switching noise to the RXIN_ inputs. This eliminates the need for a costly T-switch.

The bypass switch is typically used with two 9.1Ω resistors connected to each input. These resistors, in combination with the switch on-resistance and an 8Ω load, approximate the 32Ω load expected by the external amplifier. Although not required, using the resistors optimizes THD+N.

Drive RXIN+ and RXIN- with a low-impedance source to minimize noise on the pins. In applications that do not require the bypass mode, leave RXIN+ and RXIN- unconnected.

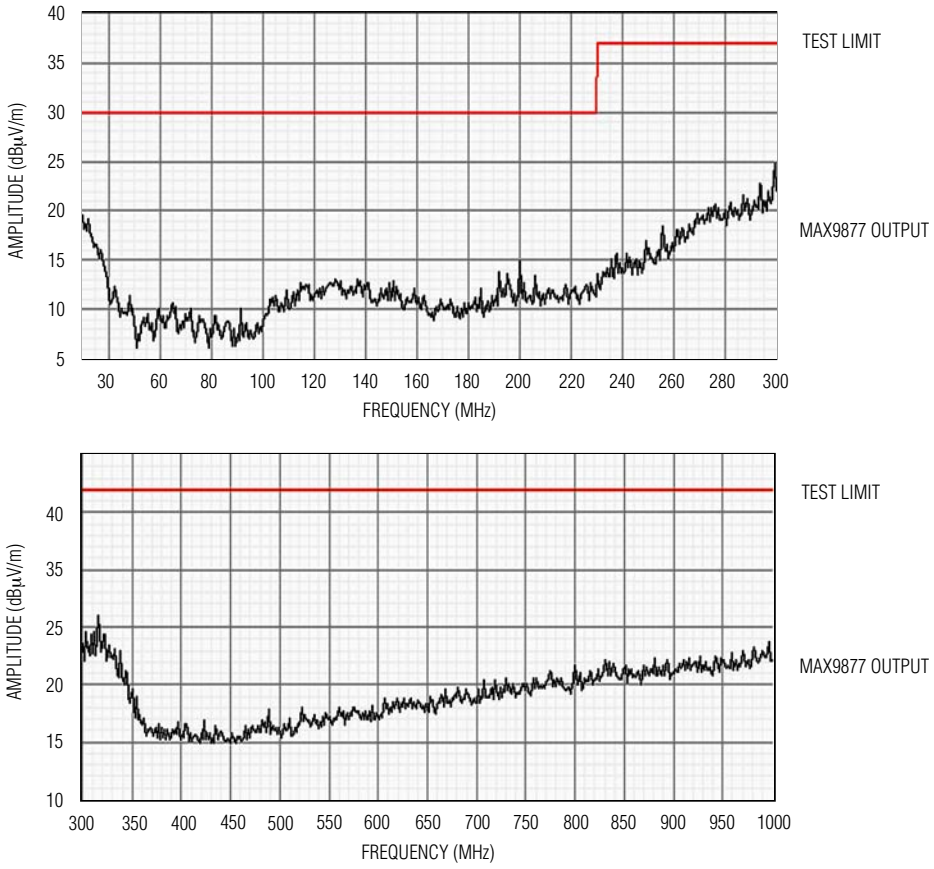


Figure 4. EMI with 152mm of Speaker Cable

DirectDrive Headphone Amplifier

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the MAX9877 to be biased at GND while operating from a single supply (Figure 5). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) capacitors, the MAX9877 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the offset of the MAX9877 is typically ±0.15mV, which, when combined with a 32Ω load, results in less than 10µA of DC current flow to the headphones.

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises some issues:

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1) The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
2) During an ESD strike, the amplifier's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full energy from an ESD strike.
3) When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

The MAX9877 features a low-noise charge pump. The switching frequency of the charge pump is $^1/_2$ of the Class D switching frequency, regardless of the operating mode. When the Class D amplifiers are operated in spread-spectrum mode, the charge pump also switches with a spread-spectrum pattern. The nominal switching frequency is well beyond the audio range, and thus does not interfere with audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic trace inductance is minimized. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C2 (see the *Typical Application Circuit*). The charge pump is active only in headphone modes.

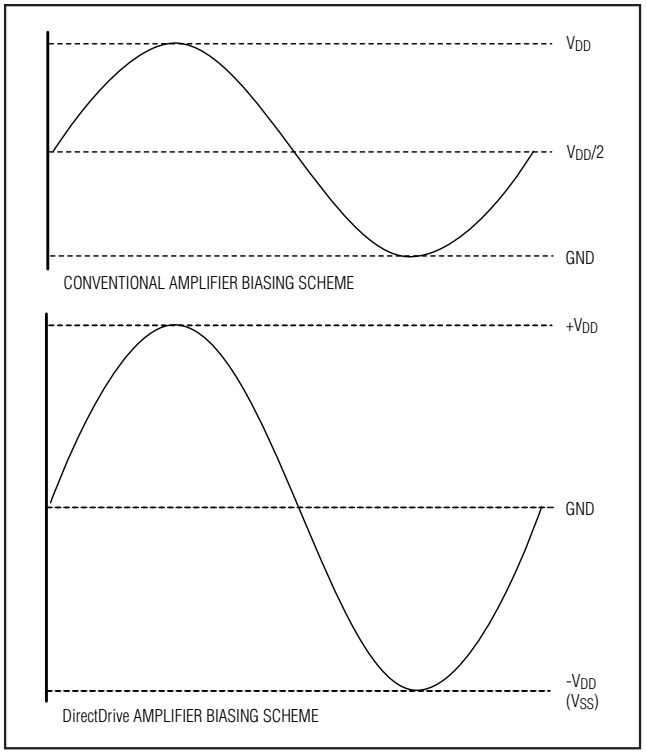


Figure 5. Traditional Amplifier Output vs. MAX9877 DirectDrive Output

Headphone Current Limit

The headphone amplifier current is limited to 140mA (typ). The current limit clamps the output current, which appears as clipping when the maximum current is exceeded.

Shutdown Mode

The MAX9877 features two ways of entering low-power shutdown. The hardware shutdown function is controlled by pulsing BIAS low for 1ms. While BIAS is low the amplifiers are shut down. Following an 80ms reset period, the MAX9877 reverts to its power-on-reset condition. Pull BIAS low using an open-drain output that is not pulled up with a resistor (see the *Typical Application Circuit*). The open-drain output leakage must not exceed 100nA and must be able to sink at least 1mA.

The device can also be placed in shutdown mode by writing to the $\overline{SHDN}$ bit in the Output Control Register.

Click-and-Pop Suppression

The MAX9877 features click-and-pop suppression that eliminates audible transients from occurring at startup and shutdown.

Use the following procedure to start up the MAX9877:

1) Configure the desired output mode and preamplifier gain.
2) Set the $\overline{SHDN}$ bit to 1 to start up the amplifier.
3) Wait 10ms for the startup time to pass.
4) Increase the output volume to the desired level.

To disable the device simply set $\overline{SHDN}$ to 0.

During the startup period, the MAX9877 precharges the input capacitors to prevent clicks and pops. If the output amplifiers have been programmed to be active they are held in shutdown until the precharge period is complete.

When power is initially applied to the MAX9877, the power-on-reset state of all three volume control registers is mute. For most applications, the volume can be set to the desired level once the device is active. If the click-and-pop is too high, step through intermediate volume settings with zero-crossing detection disabled. Stepping through higher volume settings has a greater impact on click-and-pop than lower volume settings.

For the lowest possible click-and-pop, start up the device at minimum volume and then step through each volume setting until the desired setting is reached. Disable zero-crossing detection if no input signal is expected.

I²C Interface

The MAX9877 is controlled through five I²C programmable registers. Table 1 shows the MAX9877's complete register map. Tables 2, 3, and 5 show the individual registers.

I²C Address

The slave address of the MAX9877 is 1001101R/($\overline{W}$).

Table 1. Register Map

REGISTER	REGISTER ADDRESS	POR STATE	B7	B6	B5	B4	B3	B2	B1	B0
Input Mode Control	0x00	0x40	0	ZCD	ΔINA	ΔINB	PGAINA		PGAINB	
Speaker Volume Control	0x01	0x00	0	0	0	SVOL (Table 4)				
Left Headphone Volume Control	0x02	0x00	0	0	0	HPLVOL (Table 4)				
Right Headphone Volume Control	0x03	0x00	0	0	0	HPRVOL (Table 4)				
Output Mode Control	0x04	0x49	$\overline{SHDN}$	BYPASS	OSC (Table 6)		OUTMODE (Table 7)			

Table 2. Input Mode Control

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x00	0	ZCD	ΔINA	ΔINB	PGAINA		PGAINB	

I²C Register Description

Zero-Crossing Detection (ZCD)

Zero-crossing detection limits distortion in the output signal during volume transitions by delaying the transition until the mixer output crosses the internal bias voltage. A timeout period (typically 60ms) forces the volume transition if the mixer output signal does not cross the bias voltage.

1 = Zero-crossing detection is enabled.

0 = Zero-crossing detection is disabled.

Differential Input Configuration (ΔIN_)

The inputs INA_ and INB_ can be configured for mono differential or stereo single-ended operation.

1 = IN_ is configured as a mono differential input with IN_2 as the positive and IN_1 as the negative input.

0 = IN_ is configured as a stereo single-ended input with IN_2 as the right and IN_1 as the left input.

Preamplifier Gain (PGAIN_)

The preamplifier gain of INA_ and INB_ can be programmed by writing to PGAIN_.

00 = 0dB

01 = +9dB

10 = +20dB

11 = Reserved

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Table 3. Speaker/Left Headphone/Right Headphone Volume Control

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x01	0	0	0	SVOL (Table 4)				
0x02	0	0	0	HPLVOL (Table 4)				
0x03	0	0	0	HPRVOL (Table 4)				

Volume Control

The device has a separate volume control for left headphone, right headphone, and speaker amplifiers. The total system gain is a combination of the input gain, the volume control, and the output amplifier gain. Table 4 shows the volume settings for each volume control.

Table 4. Volume Control Settings

CODE	_VOL					GAIN (dB)
	B4	B3	B2	B1	B0	
0	0	0	0	0	0	MUTE
1	0	0	0	0	1	-75
2	0	0	0	1	0	-71
3	0	0	0	1	1	-67
4	0	0	1	0	0	-63
5	0	0	1	0	1	-59
6	0	0	1	1	0	-55
7	0	0	1	1	1	-51
8	0	1	0	0	0	-47
9	0	1	0	0	1	-44
10	0	1	0	1	0	-41
11	0	1	0	1	1	-38
12	0	1	1	0	0	-35
13	0	1	1	0	1	-32
14	0	1	1	1	0	-29
15	0	1	1	1	1	-26

CODE	_VOL					GAIN (dB)
	B4	B3	B2	B1	B0	
16	1	0	0	0	0	-23
17	1	0	0	0	1	-21
18	1	0	0	1	0	-19
19	1	0	0	1	1	-17
20	1	0	1	0	0	-15
21	1	0	1	0	1	-13
22	1	0	1	1	0	-11
23	1	0	1	1	1	-9
24	1	1	0	0	0	-7
25	1	1	0	0	1	-6
26	1	1	0	1	0	-5
27	1	1	0	1	1	-4
28	1	1	1	0	0	-3
29	1	1	1	0	1	-2
30	1	1	1	1	0	-1
31	1	1	1	1	1	0

Table 5. Output Mode Control

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x04	$\overline{SHDN}$	BYPASS	OSC (Table 6)		OUTMODE (Table 7)			

Shutdown ($\overline{SHDN}$)

1 = MAX9877 operational.

0 = MAX9877 in low-power shutdown mode.

$\overline{SHDN}$ is an active-low shutdown bit that overrides all settings and places the entire device in low-power shutdown mode. The I^2C interface is fully active in this shutdown mode and bypass mode remains operational. All register settings are preserved while in shutdown.

Bypass Mode (BYPASS)

1 = MAX9877 bypass switches are closed and the Class D amplifier is disabled.

0 = Bypass mode disabled.

This mode does not control headphone operation.

Output Configuration (OUTMODE)

The MAX9877 has a stereo DirectDrive headphone amplifier and a mono Class D amplifier. Table 7 shows how each of the output amplifiers can be configured and connected to the input signals. For simplicity, not all possible combinations of ΔINA and ΔINB are shown.

Table 6. Oscillator Modes

OSC		CLASS D OSCILLATOR MODE (kHz)	CHARGE-PUMP OSCILLATOR MODE (kHz)
B1	B0		
0	0	1176, spread spectrum	588, spread spectrum
0	1	1100, fixed frequency	550, fixed frequency
1	0	700, fixed frequency	350, fixed frequency
1	1	Reserved	

Table 7. Output Modes

MODE	OUTMODE				ΔIN_ = 0 (THE SINGLE-ENDED INPUT SIGNALS ARE DEFINED AS IN_1 = LEFT AND IN_2 = RIGHT)			ΔIN_ = 1 (THE DIFFERENTIAL INPUT SIGNAL IS DEFINED AS IN_Δ = IN_2 - IN_1)		
	B3	B2	B1	B0	SPK	LEFT HP	RIGHT HP	SPK	LEFT HP	RIGHT HP
0	0	0	0	0	Reserved			Reserved		
1	0	0	0	1	INA1+INA2	—	—	INAΔ	—	—
2	0	0	1	0	—	INA1	INA2	—	INAΔ	INAΔ
3	0	0	1	1	INA1+INA2	INA1	INA2	INAΔ	INAΔ	INAΔ
4	0	1	0	0	INB1+INB2	—	—	INBΔ	—	—
5	0	1	0	1	—	INB1	INB2	—	INBΔ	INBΔ
6	0	1	1	0	INB1+INB2	INB1	INB2	INBΔ	INBΔ	INBΔ
7	0	1	1	1	INA1+INA2 +INB1+INB2	—	—	INAΔ+INBΔ	—	—
8	1	0	0	0	—	INA1+INB1	INA2+INB2	—	INAΔ +INBΔ	INAΔ +INBΔ
9	1	0	0	1	INA1+INA2 +INB1+INB2	INA1+INB1	INA2+INB2	INAΔ+INBΔ	INAΔ +INB_	INAΔ +INBΔ
10–15					Reserved			Reserved		

— = Amplifier Off

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I²C Interface Specification

The MAX9877 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9877 and the master at clock rates up to 400kHz. Figure 6 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX9877 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9877 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9877 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9877 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9877 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 7). A START condition from the master signals the beginning of a transmission to the MAX9877. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

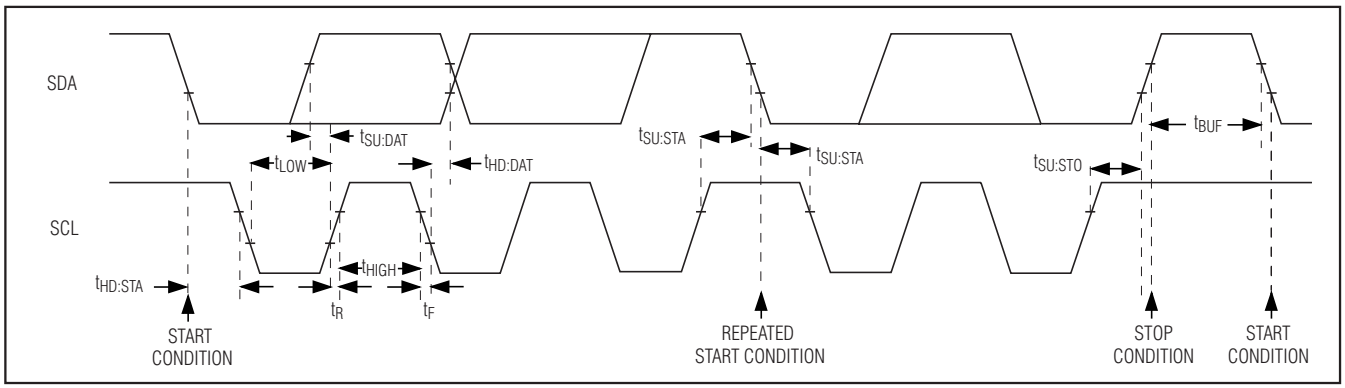


Figure 6. 2-Wire Interface Timing Diagram

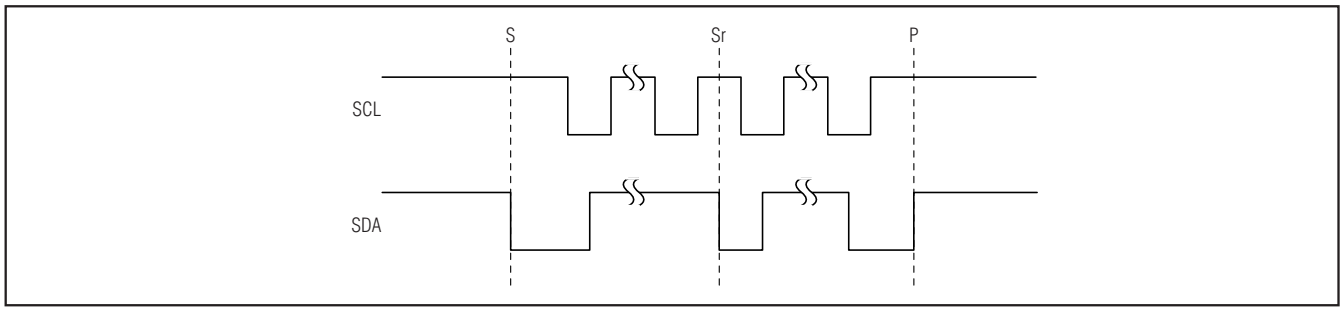


Figure 7. START, STOP, and REPEATED START Conditions

SMBus is a trademark of Intel Corp.

Early STOP Conditions

The MAX9877 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The MAX9877 is preprogrammed with a slave address of 1001101R/($\overline{W}$). The address is defined as the seven most significant bits (MSBs) followed by the Read/Write bit. Setting the Read/Write bit to 1 configures the MAX9877 for read mode. Setting the Read/Write bit to 0 configures the MAX9877 for write mode. The address is the first byte of information sent to the MAX9877 after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9877 uses to handshake receipt each byte of data when in write mode (see Figure 8). The MAX9877 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication.

The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9877 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9877, followed by a STOP condition.

Write Data Format

A write to the MAX9877 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 9 illustrates the proper frame format for writing one byte of data to the MAX9877. Figure 10 illustrates the frame format for writing n-bytes of data to the MAX9877.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9877. The MAX9877 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

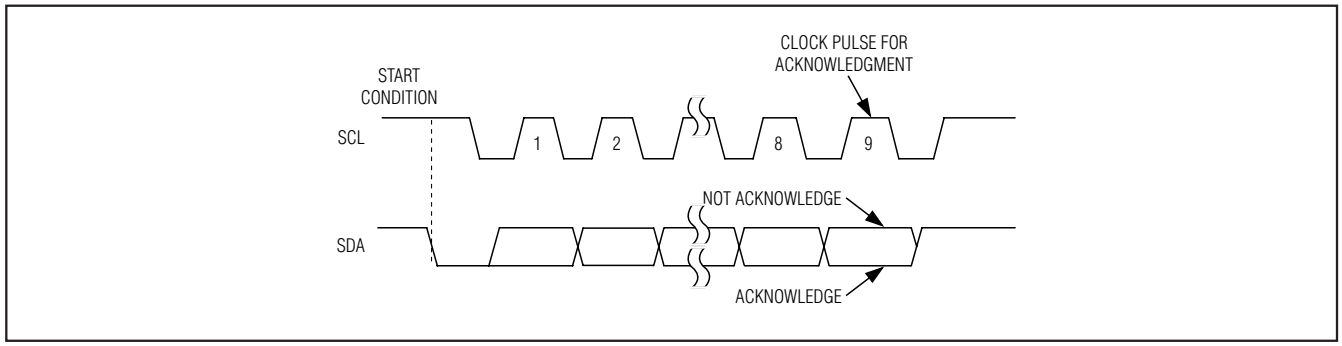


Figure 8. Acknowledge

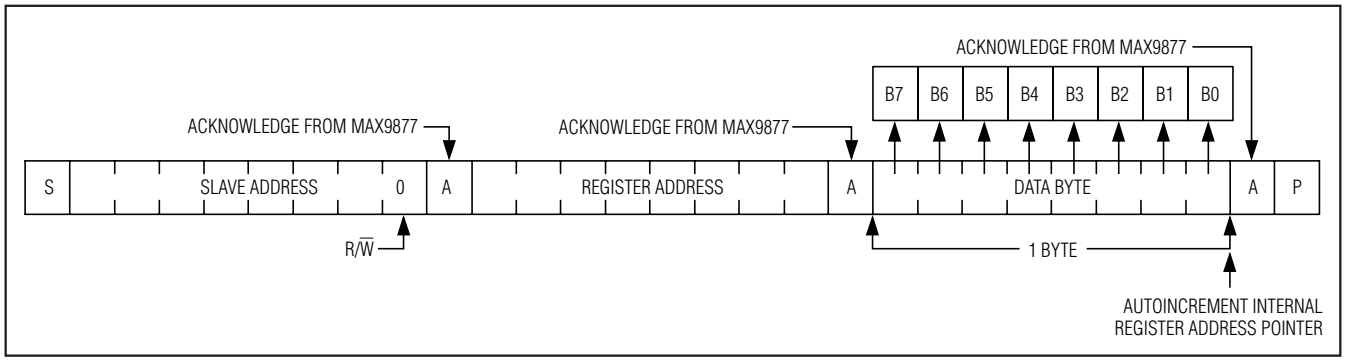


Figure 9. Writing One Byte of Data to the MAX9877

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The second byte transmitted from the master configures the MAX9877's internal register address pointer. The pointer tells the MAX9877 where to write the next byte of data. An acknowledge pulse is sent by the MAX9877 upon receipt of the address pointer data.

The third byte sent to the MAX9877 contains the data that will be written to the chosen register. An acknowledge pulse from the MAX9877 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 10 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

Register addresses greater than 0x04 are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX9877 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00. The first byte transmitted from the MAX9877 will be the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9877's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9877 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 11 illustrates the frame format for reading one byte from the MAX9877. Figure 12 illustrates the frame format for reading multiple bytes from the MAX9877.

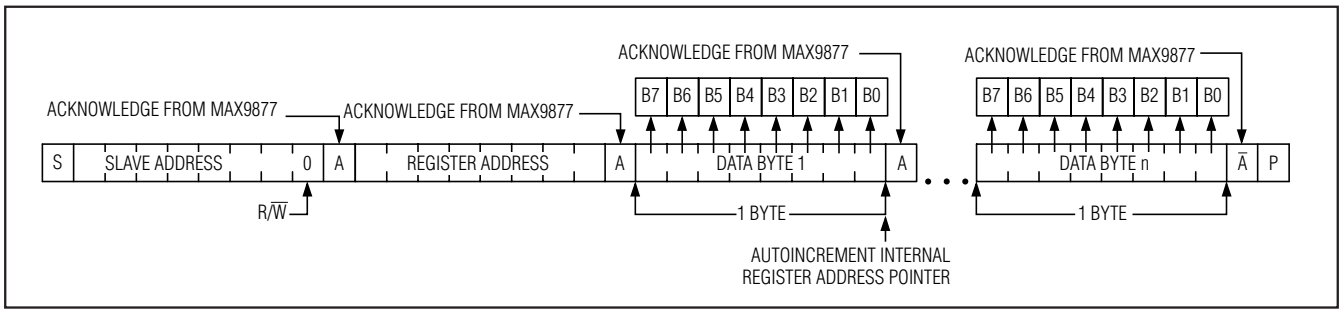


Figure 10. Writing n-Bytes of Data to the MAX9877

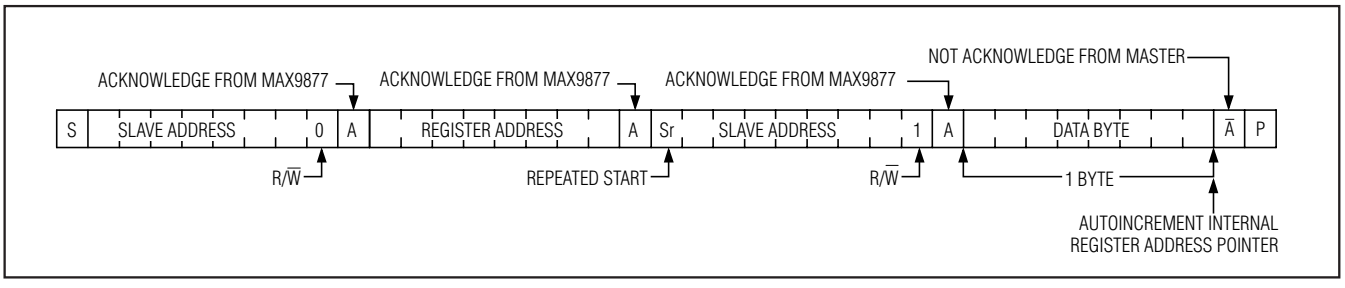


Figure 11. Reading One Indexed Byte of Data from the MAX9877

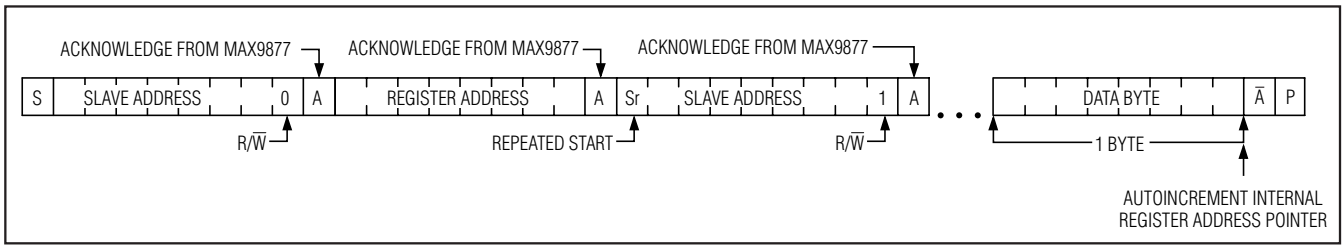


Figure 12. Reading n-Bytes of Indexed Data from the MAX9877

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (2 x $V_{DD(P-P)}$) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The MAX9877 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Because the frequency of the MAX9877 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Component Selection

Optional Ferrite Bead Filter

In applications where speaker leads exceed 20mm, additional EMI suppression can be achieved by using a filter constructed from a ferrite bead and a capacitor to ground. A ferrite bead with low DC resistance, high-frequency (> 1.176MHz) impedance of 100Ω to 600Ω, and rated for at least 1A should be used. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF based on EMI performance.

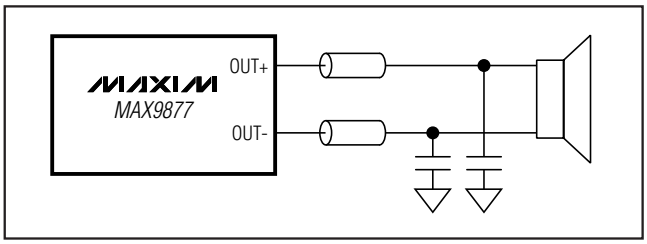


Figure 13. Optional Ferrite Bead Filter

Input Capacitor

An input capacitor, C_{IN}, in conjunction with the input impedance of the MAX9877 forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

BIAS Capacitor

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor, C_{BIAS}, reduces power supply and other noise sources at the common-mode bias node. Bypass BIAS with a 1µF capacitor to GND.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface-mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the output resistance of the charge pump. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage.

Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

Increasing the value of C1 reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Output Holding Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at V_{SS}. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics*.

PV_{DD} Bulk Capacitor (C3)

In addition to the recommended PV_{DD} bypass capacitance, bulk capacitance equal to C3 should be used. Place the bulk capacitor as close to the device as possible.

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use wide traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Wide traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PCB. Route all traces that carry switching transients away from GND and the traces/components in the audio signal path.

Connect PV_{DD} to a 2.7V to 5.25V source. Bypass PV_{DD} to the PGND pin with a 1µF ceramic capacitor. Additional bulk capacitance should be used to prevent power-supply pumping. Place the bypass capacitors as close to the MAX9877 as possible.

Connect V_{DD} to PV_{DD}. Bypass V_{DD} to GND with a 1µF capacitor. Place the bypass capacitors as close to the MAX9877 as possible.

RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz that is easily demodulated by audio amplifiers. Figure 14 shows the susceptibility of the MAX9877 to a transmitting GSM radio placed in close proximity. Although there is measurable noise at 217Hz and its harmonics, the noise is well below the threshold of hearing using typical headphones.

In RF applications, improvements to both layout and component selection decreases the MAX9877's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Trace lengths should be kept below $^1/_4$ the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the MAX9877. The wavelength λ in meters is given by:

$$\lambda = c/f$$

where $c = 3 \times 10^8$ m/s, and f = the RF frequency of interest.

Route audio signals on middle layers of the PCB to allow ground planes above and below shield them from RF interference. Ideally the top and bottom layers of the PCB should primarily be ground planes to create effective shielding.

Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the MAX9877. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Do not use microvias to connect to the ground plane as these vias do not conduct well at RF frequencies.

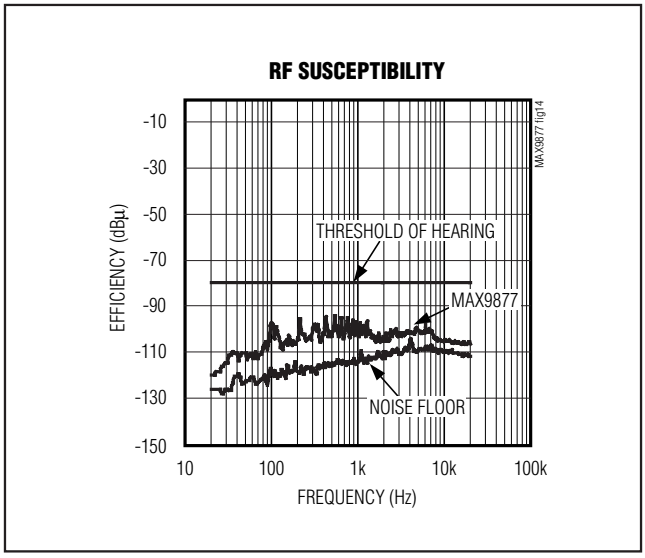


Figure 14. MAX9877 Susceptibility to a GSM Cell Phone Radio

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the *Application Note: UCSP—A Wafer-Level Chip-Scale Package* on Maxim's website at www.maxim-ic.com/ucsp. See Figure 15 for the recommended PCB footprint for the MAX9877.

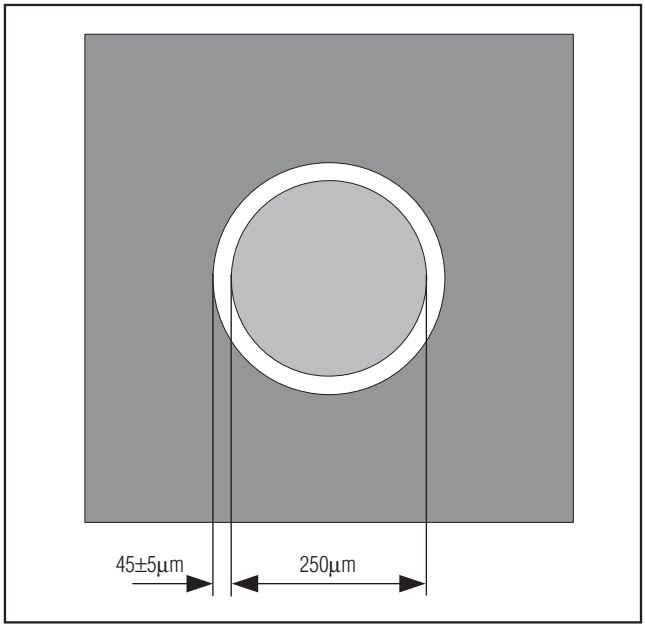
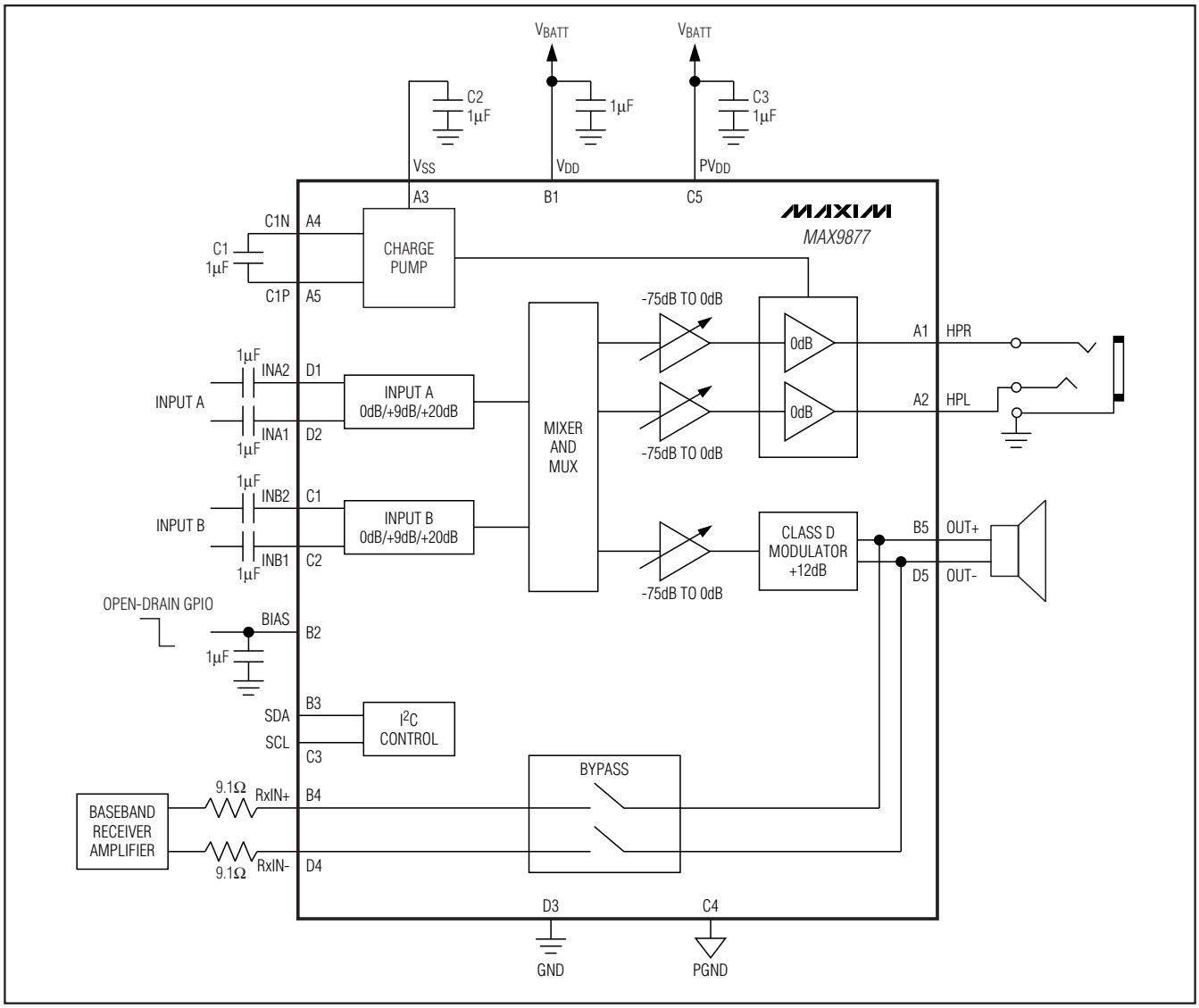


Figure 15. PCB Footprint Recommendation Diagram

Low RF Susceptibility, Mono Audio Subsystem with DirectDrive Headphone Amplifier

Typical Application Circuit



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 WLP	W202A2+2	**21-0059**

Chip Information

PROCESS: BiCMOS

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