19-0866; Rev 1; 1/08

EVALUATION KIT AVAILABLE

2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

General Description

The MAX9796 combines a high-efficiency Class D, mono audio power amplifier with a mono DirectDrive™ receiver amplifier and a stereo DirectDrive headphone amplifier.

Maxim's 3rd-generation, ultra-low EMI, Class D audio power amplifiers provide Class AB performance with Class D efficiency. The MAX9796 delivers 2.3W into a 4Ω load from a 5V supply and offers efficiencies up to 80%. Active emissions limiting circuitry and spread-spectrum modulation greatly reduce EMI, eliminating the need for output filtering found in traditional Class D devices.

The MAX9796 features a fully differential architecture, a full-bridged output, and comprehensive click-and-pop suppression. The device utilizes a flexible, user-defined mixer architecture that includes an input mixer, volume control, and output mixer. All controls are done through an I²C interface.

The mono receiver amplifier and stereo headphone amplifier use Maxim's DirectDrive architecture, that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, space, and component height.

The MAX9796 is available in a 36-bump UCSP™ (3mm x 3mm) package and is specified over the extended -40°C to +85°C temperature range.

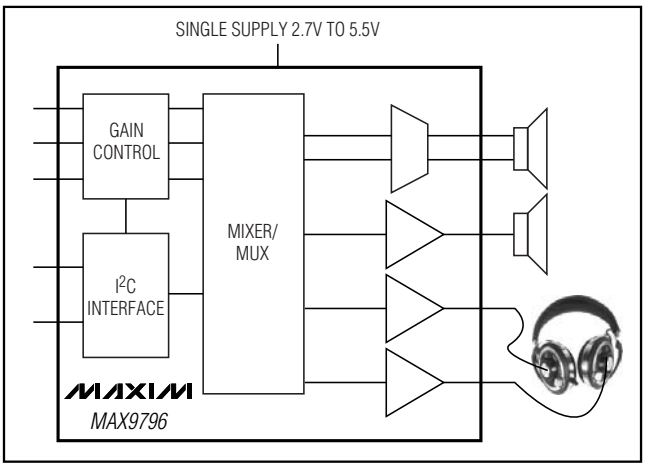
Applications

Cell Phones

Portable Multimedia Players

Handheld Gaming Consoles

Simplified Block Diagram



UCSP is a trademark of Maxim Integrated Products, Inc.

Features

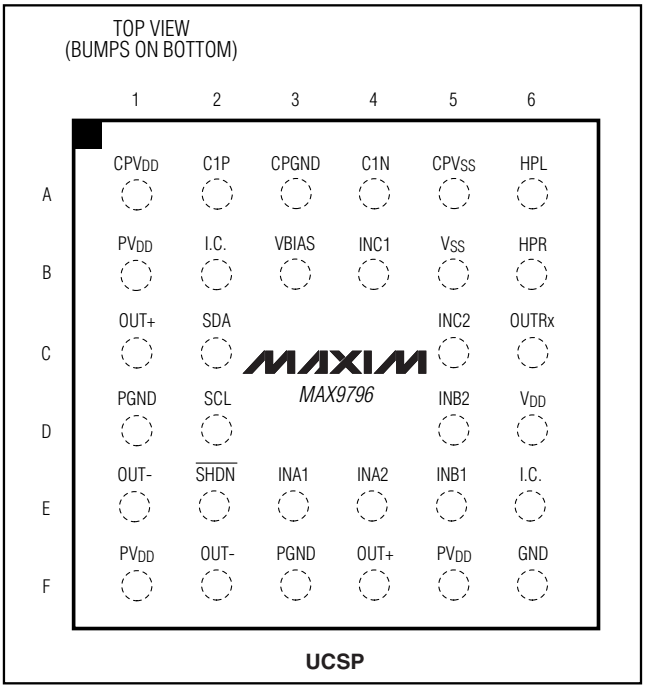
- **Unique Spread-Spectrum Modulation and Active Emissions Limiting Significantly Reduces EMI**
- **Up to 3 Stereo Inputs**
- **2.3W Mono Speaker Output (4Ω, V_{DD} = 5V)**
- **50mW Mono Receiver/Stereo Headphone Outputs (32Ω, V_{DD} = 3.3V)**
- **High PSRR (68dB at 217Hz)**
- **80% Efficiency (V_{DD} = 3.3V, R_L = 8Ω, P_{OUT} = 600mW)**
- **I²C Control—Input Configuration, Volume Control, Output Mode**
- **Click-and-Pop Suppression**
- **Low Total Harmonic Distortion (0.03% at 1kHz)**
- **Current-Limit and Thermal Protection**
- **Available in Space-Saving, 36-Bump UCSP (3mm x 3mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9796EBX+T	-40°C to +85°C	36 UCSP-36*	B36-4

+Denotes a lead-free package.
**Four center bumps depopulated.*

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....+6V
PV_{DD} to PGND .....+6V
CPV_{DD} to CPGND .....+6V
CPV_{SS} to CPGND .....-6V to +0.3V
V_{SS} to CPGND .....-6V to +0.3V
C1N .....(CPV_{SS} - 0.3V) to (CPGND + 0.3V)
C1P .....(CPGND - 0.3V) to (CPV_{DD} + 0.3V)
HPL, HPR to GND .....(CPV_{SS} - 0.3V) to (CPV_{DD} + 0.3V)
GND to PGND and CPGND .....±0.3V
V_{DD} to PV_{DD} and CPV_{DD} .....±0.3V
SDA, SCL to GND .....-0.3V to +6V
All other pins to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current In/Out of PV_{DD}, PGND, CPV_{DD}, CPGND, OUT_ _, HPR, and HPL .....±800mA
Continuous Input Current CPV_{SS} .....+260mA
Continuous Input Current (all other pins) .....±20mA
Duration of Short Circuit Between OUT+ and OUT- .....Continuous
Duration of HP_ OUT_ Short Circuit to GND or PV_{DD} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
36-Bump (3mm x 3mm) UCSP Multilayer Board (derate 17.0mW/°C above +70°C) 1360.5mW
Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	V_{DD}, PV_{DD}, CPV_{DD}	Inferred from PSRR test		2.7		5.5	V
Quiescent Current	I_{DD}	Output mode 1, 6, 11 (Rx mode)			6.3	10	mA
		Output mode 4, 9, 14 (HP mode)			8	12.6	
		Output mode 2, 7, 12 (SP mode)			11.8	17.5	
		Output mode 3, 8, 13 (SP and HP modes)			15.1	21	
Mute Current	I_{MUTE}	Current in mute			4.7	10	mA
Shutdown Current	I_{SHDN}	Hard shutdown	$\overline{SHDN}$ = GND		0.1	10	µA
		Soft shutdown	See the *I^2C Interface* section		8.5	15	
Turn-On Time	t_{ON}	Time from shutdown or power-on to full operation			30		ms
Input Resistance	R_{IN}	B and C pair inputs, T_A = +25°C, VOL = max		17.5	28	41.0	kΩ
		A pair inputs, T_A = +25°C, +20dB		3.5	5.5	8.0	kΩ
Common-Mode Rejection Ratio	CMRR	T_A = +25°C, V_{IN} = ±500mV		45	50		dB
Input DC Bias Voltage	V_{BIAS}	IN_ inputs		1.12	1.25	1.38	V

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SPEAKER AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C			±5.5	±23.5	mV
		$T_{MIN} \le T_A \le T_{MAX}$				±40	
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Notes 3, 4)	Into shutdown		-62		dB
			Out of shutdown		-60		
			Into mute		-63		
			Out of mute		-62		
Power-Supply Rejection Ratio (Note 3)	PSRR	T_A = +25°C	V_{DD} = 2.7V to 5.5V	48	70		dB
			f = 217Hz, 100mV_{P-P} ripple		68		
			f = 1kHz, 100mV_{P-P} ripple		60		
			f = 20kHz, 100mV_{P-P} ripple		50		
Output Power (Note 4)	P_{OUT}	THD+N = 1%, T_A = +25°C	R_L = 4Ω, V_{DD} = 5V, f = 1kHz		2300		mW
			R_L = 8Ω, V_{DD} = 3.3V, f = 1kHz		600		
			R_L = 8Ω, V_{DD} = 5V, f = 1kHz		1300		
Current Limit					1.6		A
Total Harmonic Distortion Plus Noise (Note 4)	THD+N	f = 1kHz	R_L = 8Ω, P_{OUT} = 800mW		0.03		%
			R_L = 4Ω, P_{OUT} = 830mW		0.04		
Signal-to-Noise Ratio	SNR	V_{OUT} = 1.8V_{RMS}, R_L = 8Ω (Note 3)	BW = 20Hz to 20kHz		81		dB
			A-weighted		84		
Output Frequency	f_{OSC}	Fixed-frequency modulation (SSM = 0)			1100		kHz
		Spread-spectrum modulation (SSM = 1)			1100 ±30		
Efficiency	η	P_{OUT} = 470mW, f = 1kHz both channel driven, L = 68µH in series with 8Ω load			80		%
Gain	A_V				12		dB

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C			±1.8		mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Notes 3, 5)	Into shutdown		-62		dB
			Into mute		-67		
			Out of shutdown		-63		
			Out of mute		-66		
Power-Supply Rejection Ratio (Note 3)	PSRR	T_A = +25°C	V_{DD} = 2.7V to 5.5V	58	80		dB
			f = 217Hz, 100mV_{P-P} ripple		80		
			f = 1kHz, 100mV_{P-P} ripple		70		
			f = 20kHz, 100mV_{P-P} ripple		62		
Output Power	P_{OUT}	T_A = +25°C, THD+N = 1%	R_L = 16Ω		60		mW
			R_L = 32Ω		50		
Gain	A_V				3		dB
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω (V_{OUT} = 800mV_{RMS}, f = 1kHz)			0.03		%
		R_L = 32Ω (V_{OUT} = 800mV_{RMS}, f = 1kHz)			0.024		
Signal-to-Noise Ratio	SNR	R_L = 16Ω, V_{OUT} = 800mV_{RMS} (Note 3)	BW = 20Hz to 20kHz		87		dB
			A-weighted		89		
Slew Rate	SR				0.3		V/µs
Capacitive Drive	C_L				300		pF
HEADPHONE AMPLIFIERS							
Output Offset Voltage	V_{OS}	T_A = +25°C			±1.8		mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Notes 2, 5)	Into shutdown		-61		dB
			Into mute		-65		
			Out of shutdown		-60		
			Out of mute		-64		
ESD Protection		HP_	Contact		±4		kV
			Air		±8		
Power-Supply Rejection Ratio (Note 3)	PSRR	T_A = +25°C	V_{DD} = 2.7V to 5.5V	58	80		dB
			f = 217Hz, 100mV_{P-P} ripple		80		
			f = 1kHz, 100mV_{P-P} ripple		70		
			f = 20kHz, 100mV_{P-P} ripple		62		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power	P_{OUT}	T_A = +25°C, THD+N = 1%	R_L = 16Ω		60		mW
			R_L = 32Ω		50		
Current Limit					170		mA
Gain	A_V				+3		dB
Channel-to-Channel Gain Tracking		T_A = +25°C			±1		%
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω (V_{OUT} = 800mV_{RMS}, f = 1kHz)			0.03		%
		R_L = 32Ω (V_{OUT} = 800mV_{RMS}, f = 1kHz)			0.024		
Signal-to-Noise Ratio	SNR	R_L = 16Ω, V_{OUT} = 800mV_{RMS}	BW = 20Hz to 20kHz		92		dB
			A-weighted		93		
Slew Rate	SR				0.3		V/µs
Capacitive Drive	C_L				300		pF
Crosstalk		L to R, R to L, f = 10kHz, R_L = 16Ω, V_{OUT} = 160mV_{RMS}			75		dB
VOLUME CONTROL							
Volume Control		IN+6dB = 0 (minimum gain setting)	HP gain (max)		3		dB
			SP gain (max)		12		
			HP gain (min)		-72		
			SP gain (min)		-63		
		IN+6dB = 1 (maximum gain setting)	HP gain (max)		9		
			SP gain (max)		18		
			HP gain (min)		-61		
			SP gain (min)		-57		
Mono Gain		All outputs	Mono + 6dB = 0		0		dB
			Mono + 6dB = 1		6		
Input Pair A Control		INA+20dB = 0 (minimum gain setting)			Set by IN+6dB		dB
		INA+20dB = 1 (maximum gain setting)			20		
Mute Attenuation (Minimum Volume)		V_{IN} = 1V_{RMS}			80		dB
DIGITAL INPUTS ($\overline{SHDN}$, SDA, SCL)							
Input-Voltage High	V_{IH}			1.4			V
Input-Voltage Low	V_{IL}					0.4	V
Input Hysteresis (SDA, SCL)	V_{HYS}				200		mV
SDA, SCL Input Capacitance	C_{IN}				10		pF
Input Leakage Current	I_{IN}					1.0	µA
Pulse Width of Spike Suppressed	t_{SP}				50		ns

2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (SDA Open Drain)						
Output Low Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V
Output Fall Time SDA	t_{OF}	$V_{H(MIN)}$ to $V_{L(MAX)}$ bus capacitance = 10pF to 400pF, I_{SINK} = 3mA		250		ns
I^2C INTERFACE TIMING						
Serial-Clock Frequency	f_{SCL}		DC		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STA}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0		900	ns
Maximum Receive SCL/SDA Rise Time	t_R				300	ns
Maximum Receive SCL/SDA Fall Time	t_F				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF

Note 1: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.

Note 2: Measured at headphone outputs.

Note 3: Amplifier inputs AC-coupled to GND.

Note 4: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 8Ω L = 68µH, R_L = 4Ω L = 47µH.

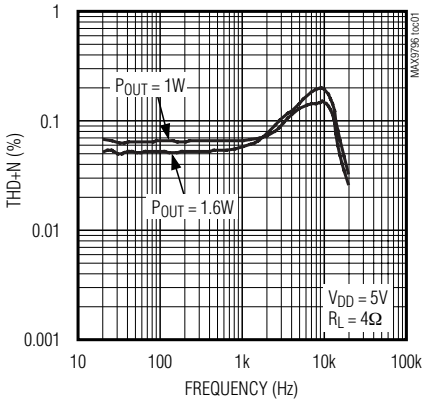
Note 5: Testing performed at room temperature with an 8Ω resistive load in series with 68µH inductive load connected across BTL outputs for speaker amplifier. Testing performed with 32Ω resistive load connected between OUT_ and GND for headphone amplifier. Testing performed with a 32Ω resistive load connected between OUTRx and GND for mono receiver amplifier. Mode transitions are controlled by $\overline{SHDN}$ pin.

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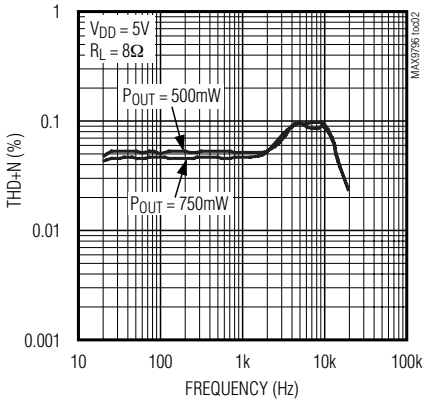
Typical Operating Characteristics

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). C1 = C2 = C3 = 1µF. Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted.)

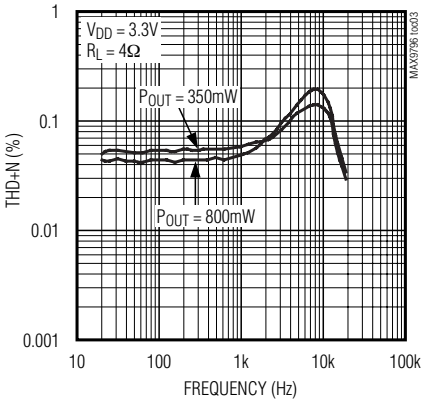
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



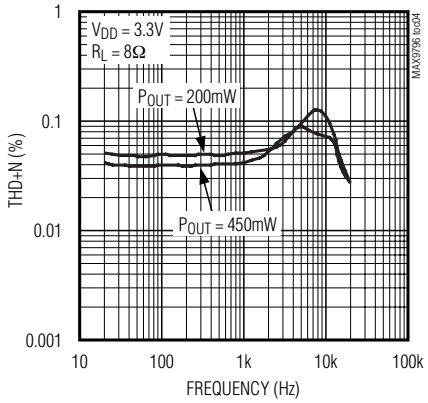
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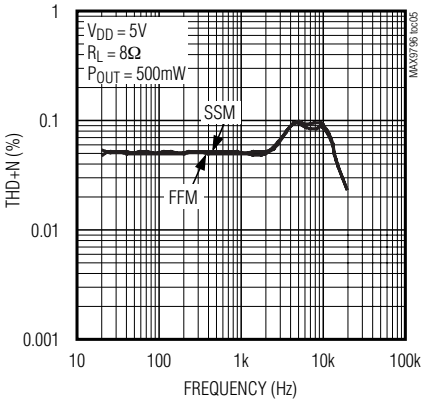
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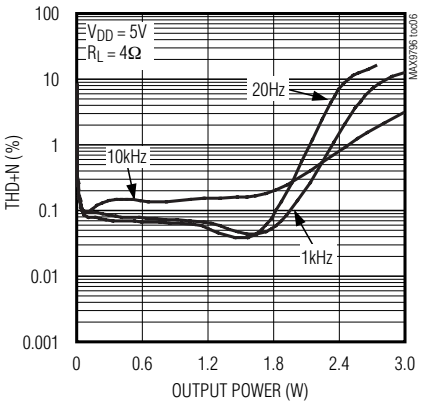
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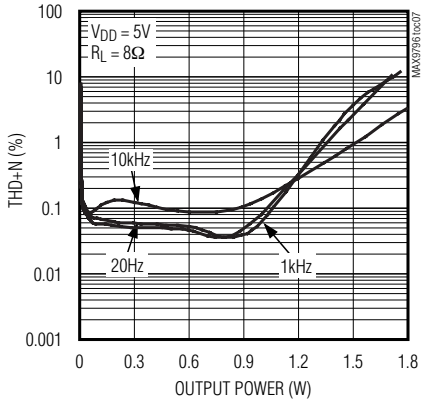
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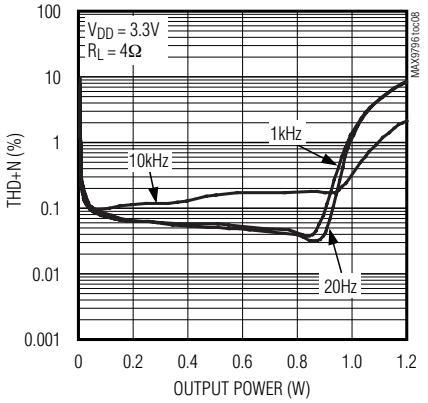
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



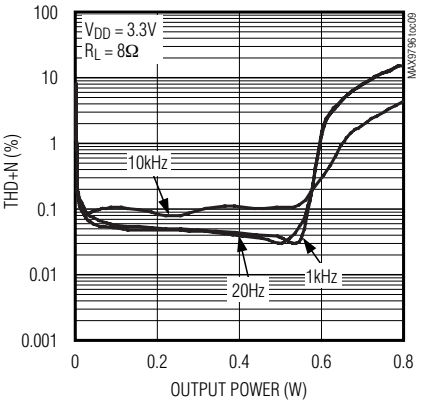
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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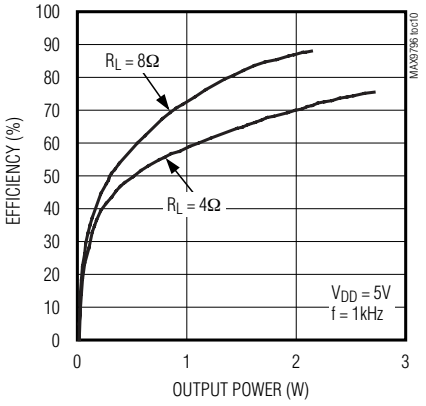


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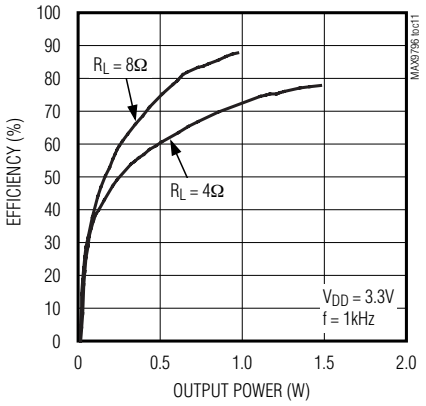
Typical Operating Characteristics (continued)

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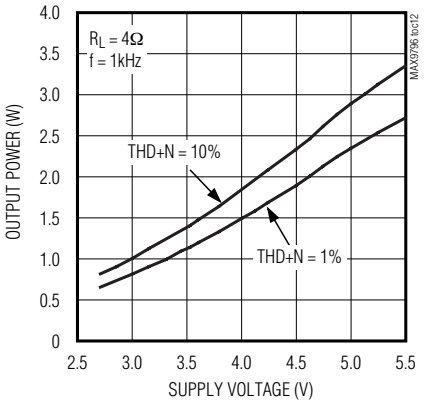
EFFICIENCY vs. OUTPUT POWER



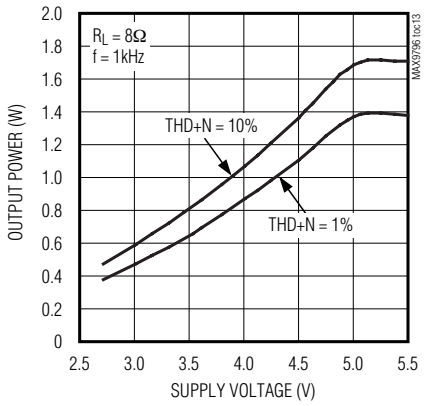
EFFICIENCY vs. OUTPUT POWER



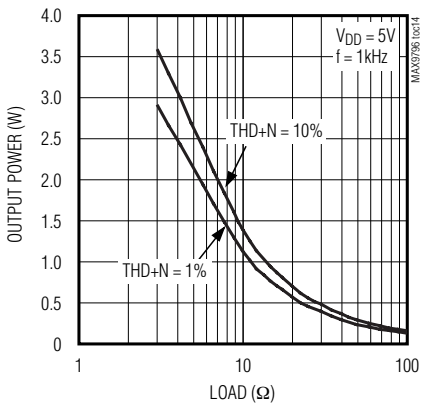
OUTPUT POWER vs. SUPPLY VOLTAGE



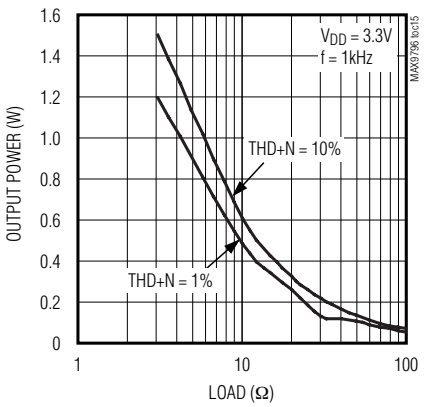
OUTPUT POWER vs. SUPPLY VOLTAGE



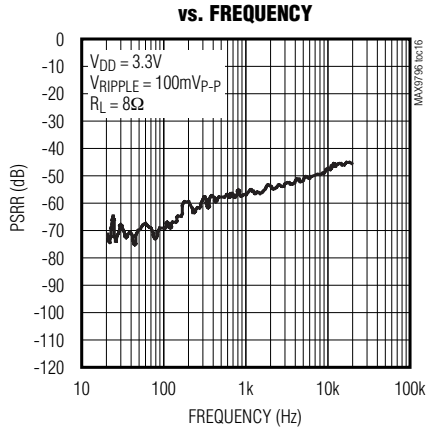
OUTPUT POWER vs. LOAD



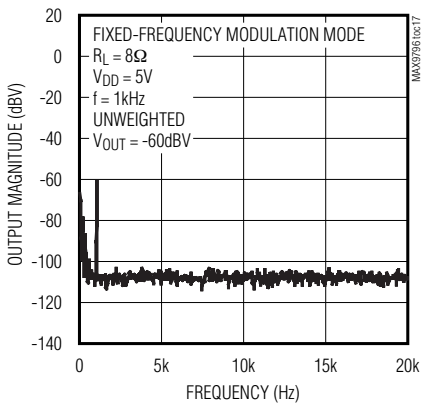
OUTPUT POWER vs. LOAD



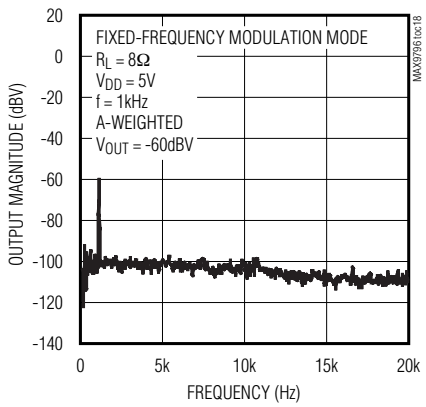
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



INBAND OUTPUT SPECTRUM



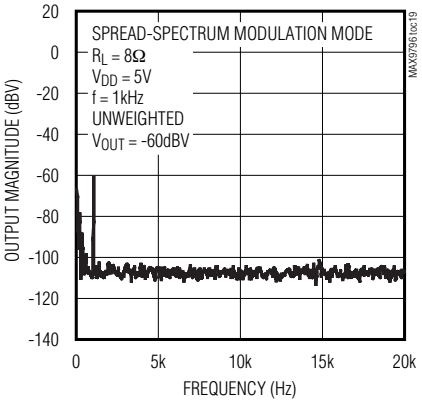
INBAND OUTPUT SPECTRUM



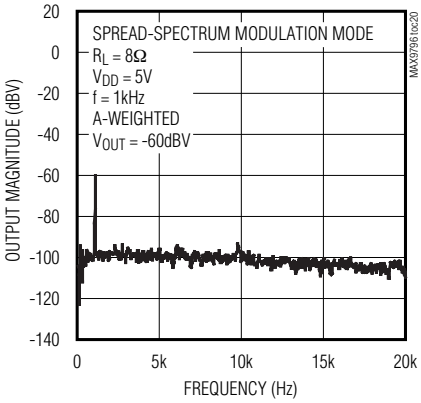
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). C1 = C2 = C3 = 1µF. Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted.)

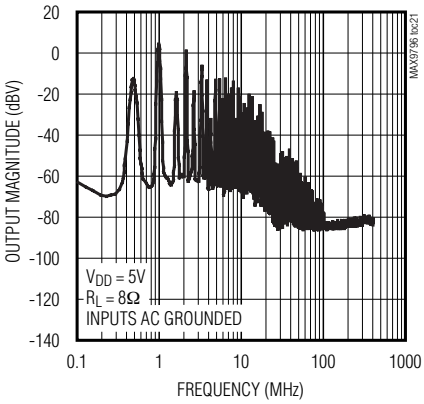
INBAND OUTPUT SPECTRUM



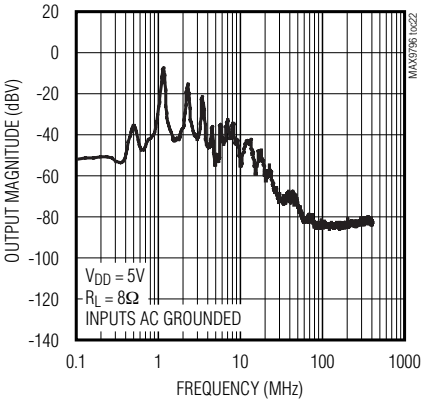
INBAND OUTPUT SPECTRUM



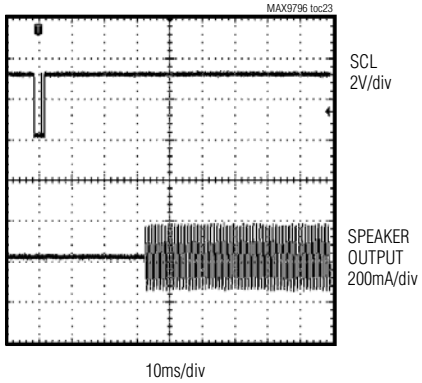
WIDEBAND OUTPUT SPECTRUM FIXED-FREQUENCY MODE



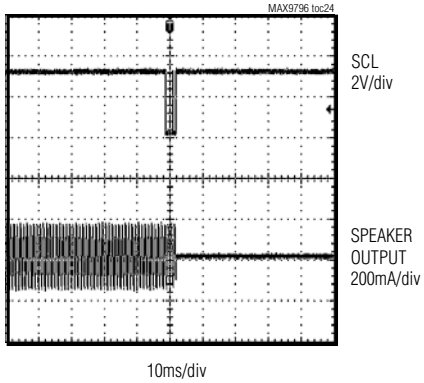
WIDEBAND OUTPUT SPECTRUM SPREAD-SPECTRUM MODE



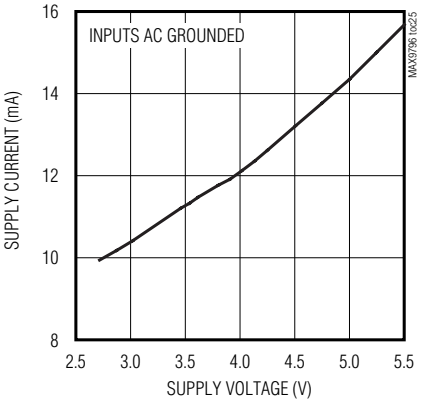
TURN-ON RESPONSE



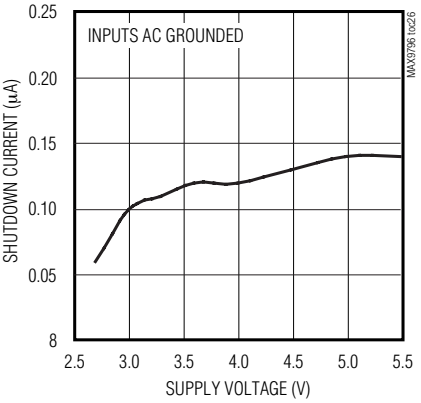
TURN-OFF RESPONSE



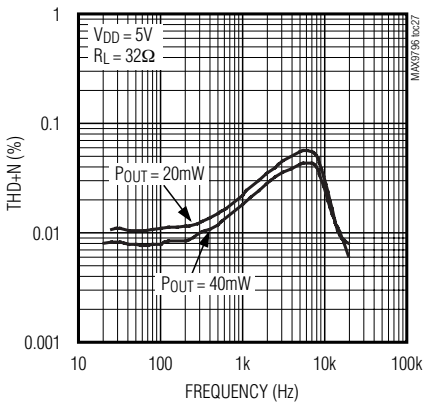
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

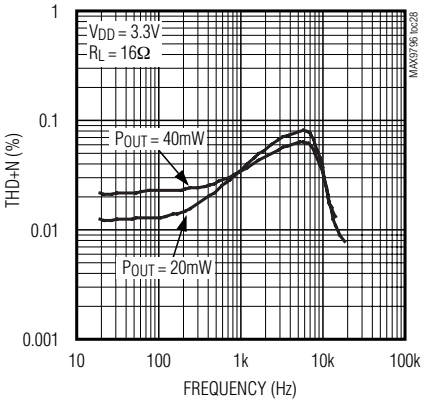


2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

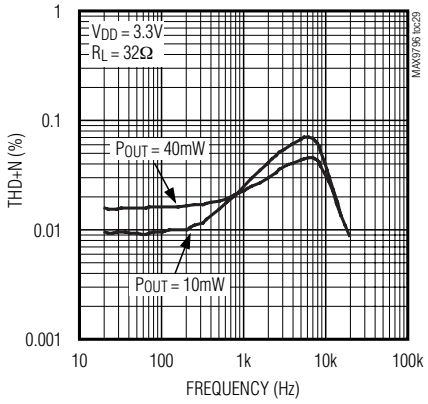
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). C1 = C2 = C3 = 1µF. Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted.)

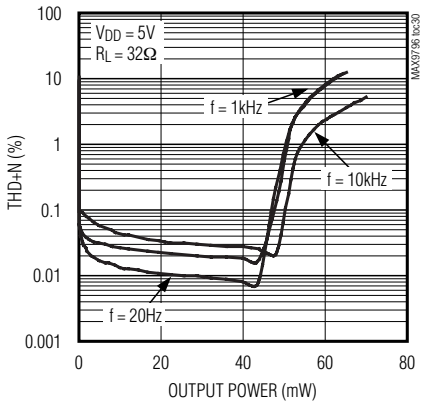
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



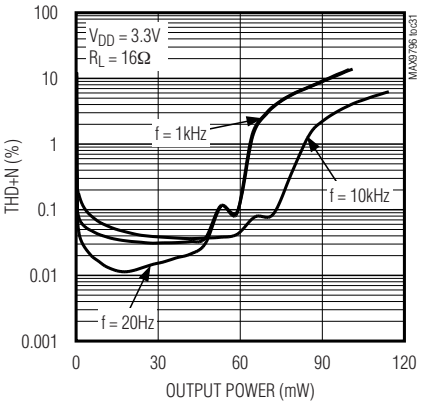
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



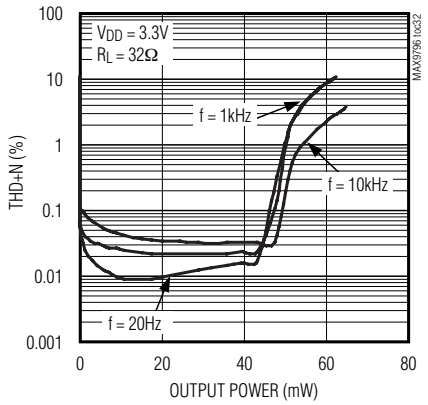
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



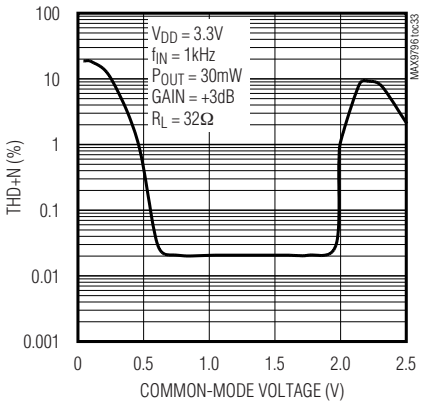
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



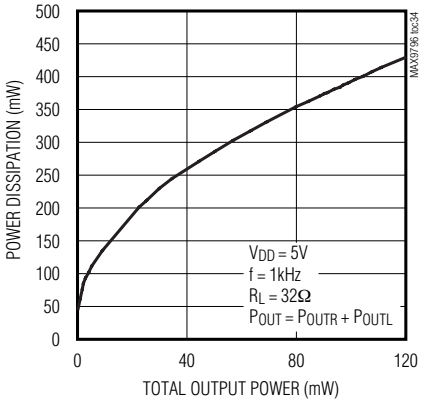
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



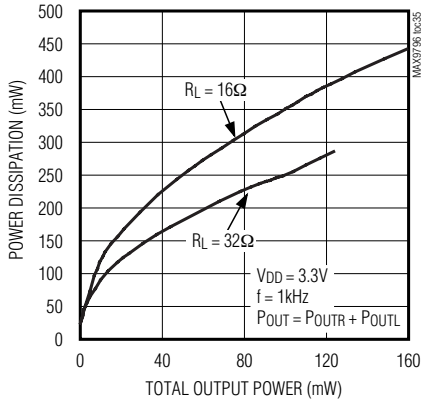
TOTAL HARMONIC DISTORTION PLUS NOISE vs. COMMON-MODE VOLTAGE



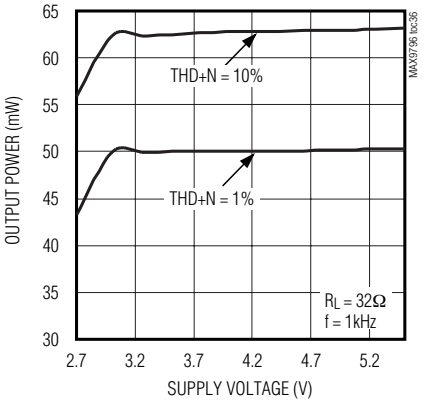
POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



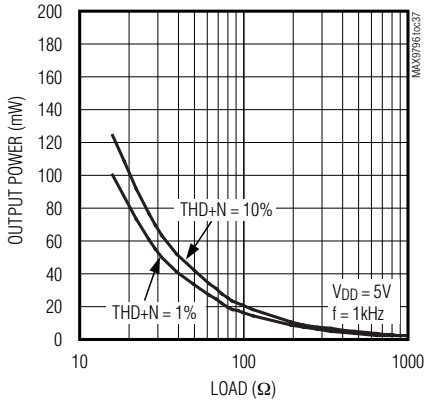
OUTPUT POWER vs. SUPPLY VOLTAGE



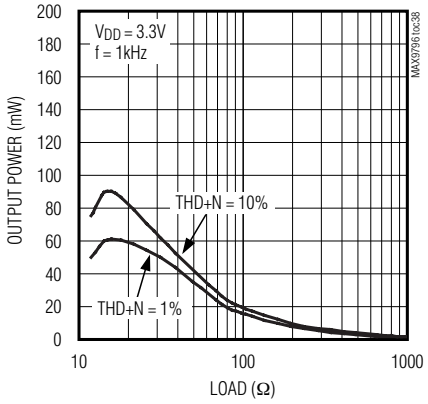
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). C1 = C2 = C3 = 1µF. Speaker load resistors (R_{LSP}) are terminated between OUT+ and OUT-, headphone load resistors are terminated to GND, unless otherwise noted.)

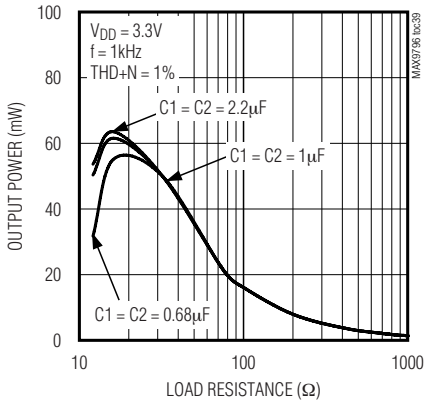
OUTPUT POWER vs. LOAD



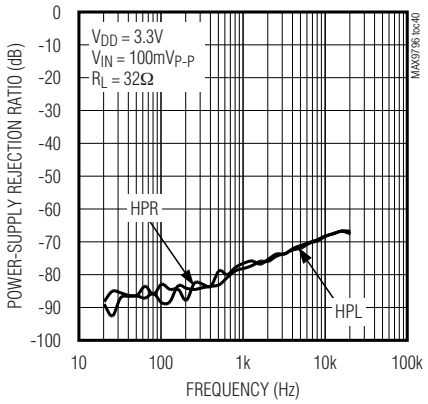
OUTPUT POWER vs. LOAD



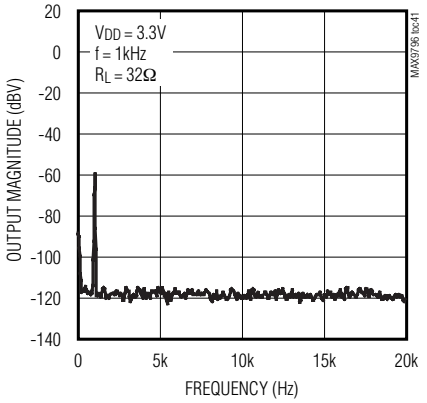
OUTPUT POWER vs. LOAD RESISTANCE AND CHARGE-PUMP CAPACITOR SIZE



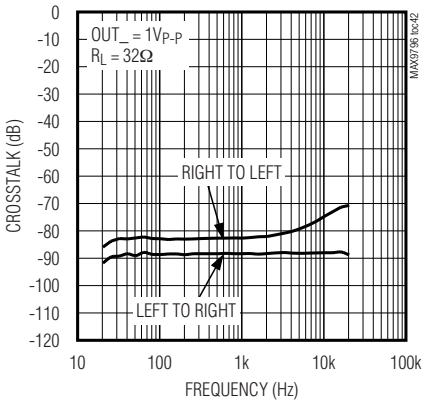
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



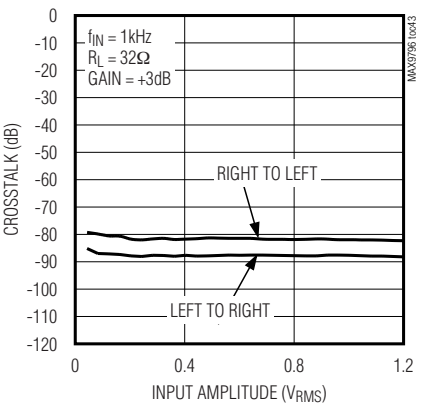
OUTPUT FREQUENCY SPECTRUM



CROSSTALK vs. FREQUENCY



CROSSTALK vs. INPUT AMPLITUDE

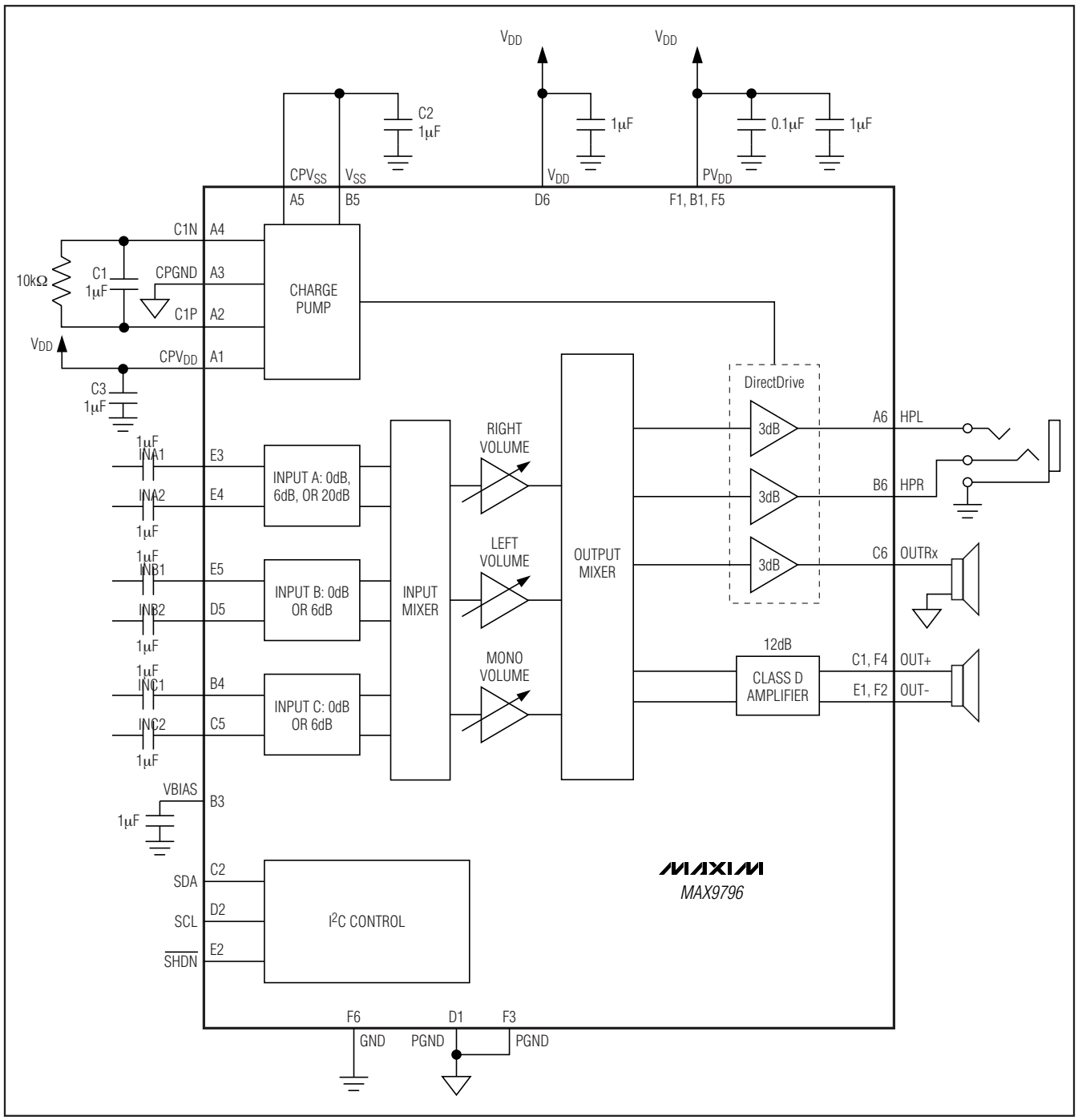


2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

Pin Description

BUMP	NAME	FUNCTION
A1	CPV_{DD}	Charge-Pump Power Supply
A2	C1P	Charge-Pump Flying Capacitor Positive Terminal
A3	CPGND	Charge-Pump GND
A4	C1N	Charge-Pump Flying Capacitor Negative Terminal
A5	CPV_{SS}	Charge-Pump Output. Connect to V_{SS}.
A6	HPL	Left Headphone Output
B1, F1, F5	PV_{DD}	Class D Power Supply
B2, E6	I.C.	Internal Connection. Leave unconnected. This pin is internally connected to the signal path. Do not connect together or to any other pin.
B3	VBIAS	Common-Mode Bias
B4	INC1	Input C1. Left input or positive input (see Table 5a).
B5	V_{SS}	Headphone Amplifier Negative Power Supply. Connect to CPV_{SS}.
B6	HPR	Right Headphone Output
C1, F4	OUT+	Positive Speaker Output
C2	SDA	Serial Data Input. Connect a 1kΩ pullup resistor from SDA to V_{DD}.
C5	INC2	Input C2. Right input or negative input (see Table 5a).
C6	OUTRx	Mono Receiver Output
D1, F3	PGND	Power Ground
D2	SCL	Serial Clock Input. Connect a 1kΩ pullup resistor from SCL to V_{DD}.
D5	INB2	Input B2. Right input or negative input (see Table 5a).
D6	V_{DD}	Analog Power Supply
E1, F2	OUT-	Negative Speaker Output
E2	$\overline{SHDN}$	Active-Low Hardware Shutdown
E3	INA1	Input A1. Left input or positive input (see Table 5a).
E4	INA2	Input A2. Right input or negative input (see Table 5a).
E5	INB1	Input B1. Left input or positive input (see Table 5a).
F6	GND	Analog Ground

Typical Application Circuit



2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

Detailed Description

The MAX9796 ultra-low-EMI, filterless, Class D audio power amplifier features several improvements to switch-mode amplifier technology. The MAX9796 features active emissions limiting circuitry to reduce EMI. Zero dead-time technology maintains state-of-the-art efficiency and THD+N performance by allowing the output FETs to switch simultaneously without cross-conduction. A unique filterless modulation scheme and a spread-spectrum modulation create a compact, flexible, low-noise, efficient audio power amplifier while occupying minimal board space. The differential input architecture reduces common-mode noise pickup with or without the use of input-coupling capacitors. The MAX9796 can also be configured as a single-ended input amplifier without performance degradation.

The MAX9796 features three fully differential input pairs (INA_, INB_, INC_) that can be configured as stereo single-ended or mono differential inputs. I^2C provides control for input configuration, volume level, and mixer configuration. DirectDrive allows the headphone and mono receiver amplifiers to output ground-referenced signals from a single supply, eliminating the need for large DC-blocking capacitors. Comprehensive click-and-pop suppression minimizes audible transients during the turn-on and turn-off of amplifiers.

Class D Speaker Amplifier

Comparators monitor the audio inputs and compare the complementary input voltages to a sawtooth waveform. The comparators trip when the input magnitude of the sawtooth exceeds their corresponding input voltage. The active emissions limiting circuitry slightly reduces the turn-on rate of the output H-bridge by slew-rate limiting the comparator output pulse. Both comparators reset at a fixed time after the rising edge of the second comparator trip point, generating a minimum-width pulse ($t_{ON(MIN)}$, 100ns typ) at the output of the second comparator (Figure 1). As the input voltage increases or decreases, the duration of the pulse at one output increases while the other output pulse duration remains the same. This causes the net voltage across the speaker (V_{OUT+} - V_{OUT-}) to change. The minimum-width pulse helps the device to achieve high levels of linearity.

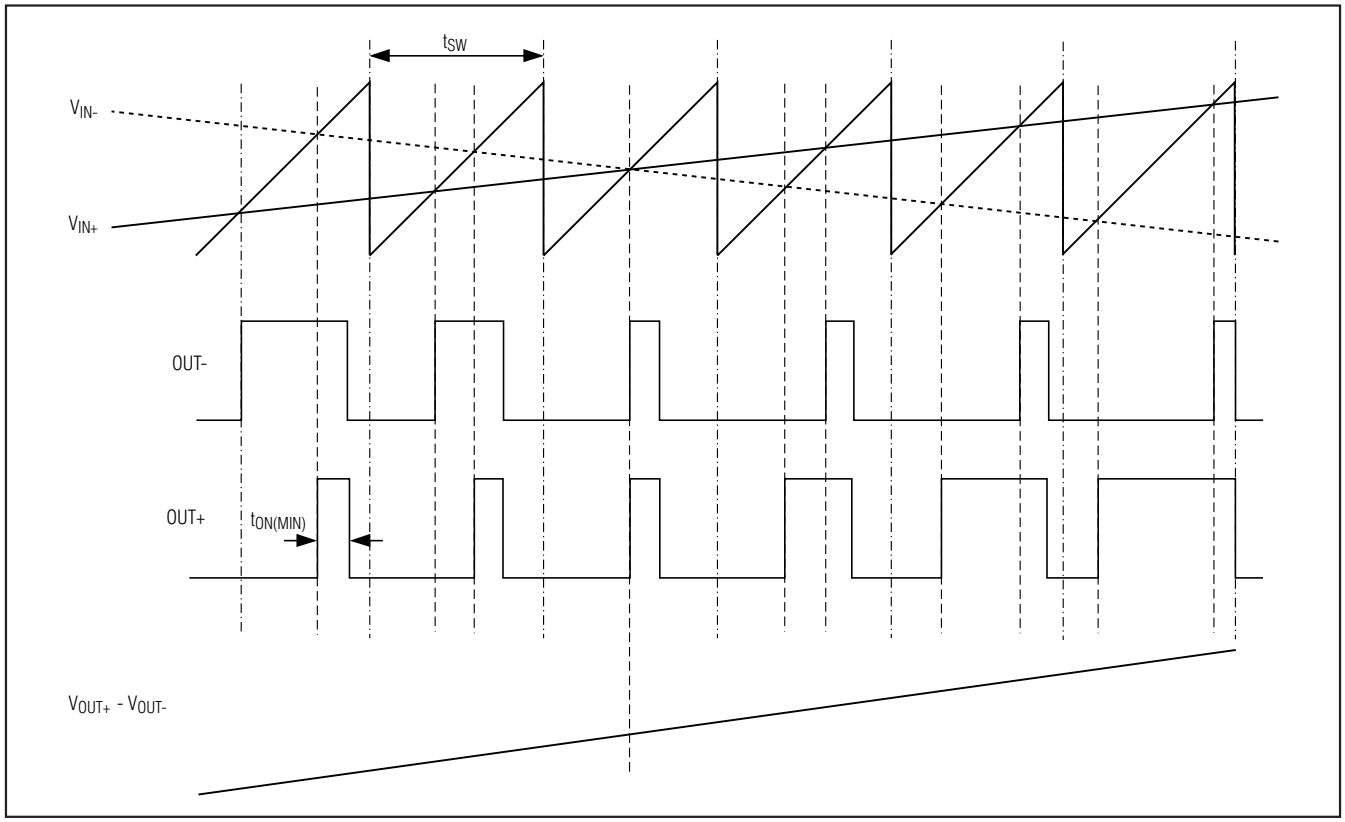


Figure 1. Outputs with an Input Signal Applied

Operating Modes

Fixed-Frequency Modulation

The MAX9796 features a fixed-frequency modulation mode with a 1.1MHz switching frequency, set through the I²C interface (Table 2). In fixed-frequency modulation mode, the frequency spectrum of the Class D output consists of the fundamental switching frequency and its associated harmonics (see the Wideband Output Spectrum Fixed-Frequency Mode graph in the *Typical Operating Characteristics*).

Spread-Spectrum Modulation

The MAX9796 features a unique spread-spectrum modulation that flattens the wideband spectral components. Proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency (see the *Typical Operating Characteristics*). Select the spread-spectrum modulation mode through the I²C interface (Table 2). In spread-spectrum modulation mode, the switching frequency varies randomly by ±30kHz around the center frequency (1.16MHz). The modulation scheme remains the same, but the period of the sawtooth waveform changes from cycle to cycle (Figure 2). Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes (see Figure 3).

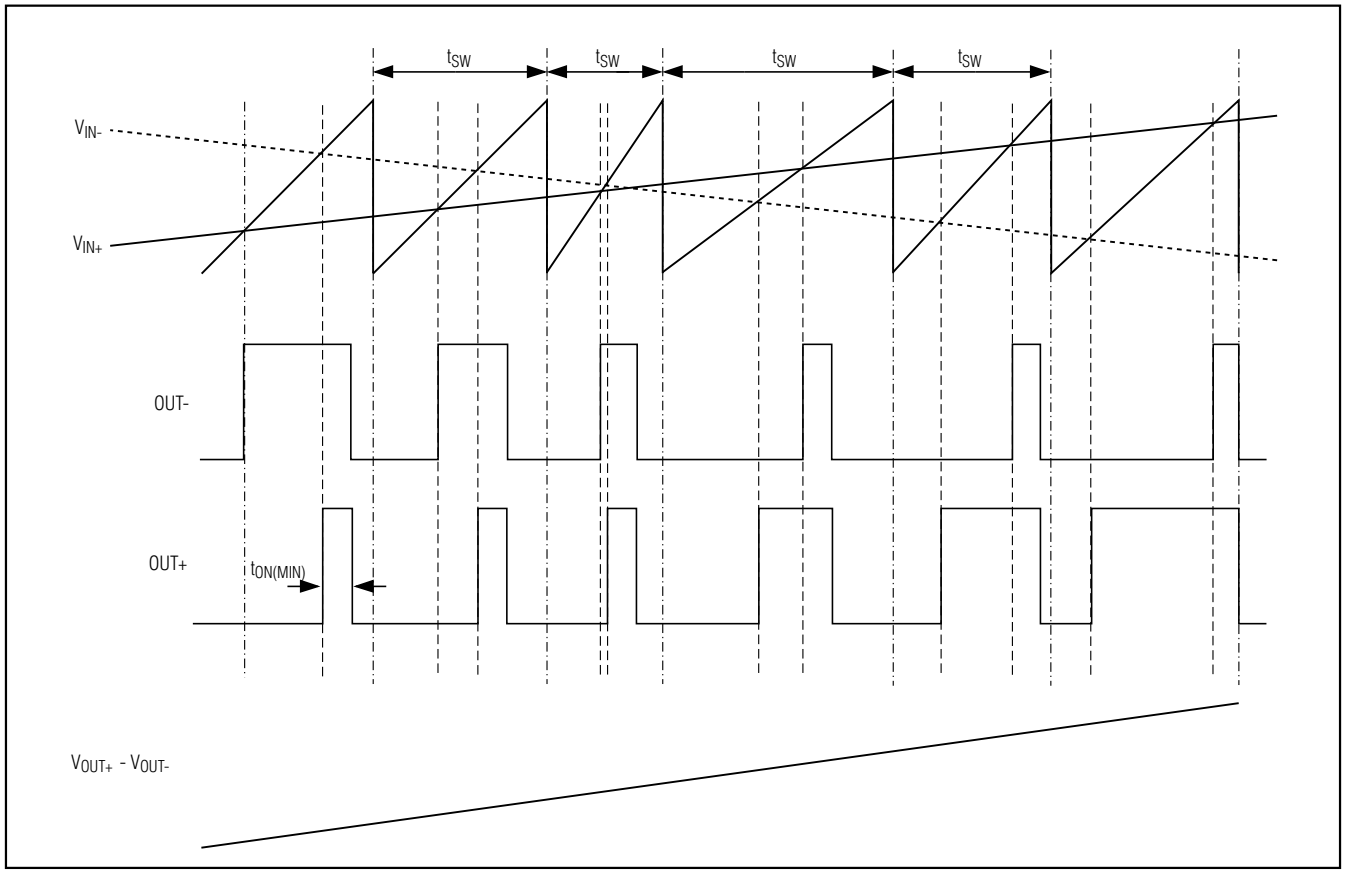


Figure 2. Output with an Input Signal Applied (Spread-Spectrum Modulation Mode)

2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

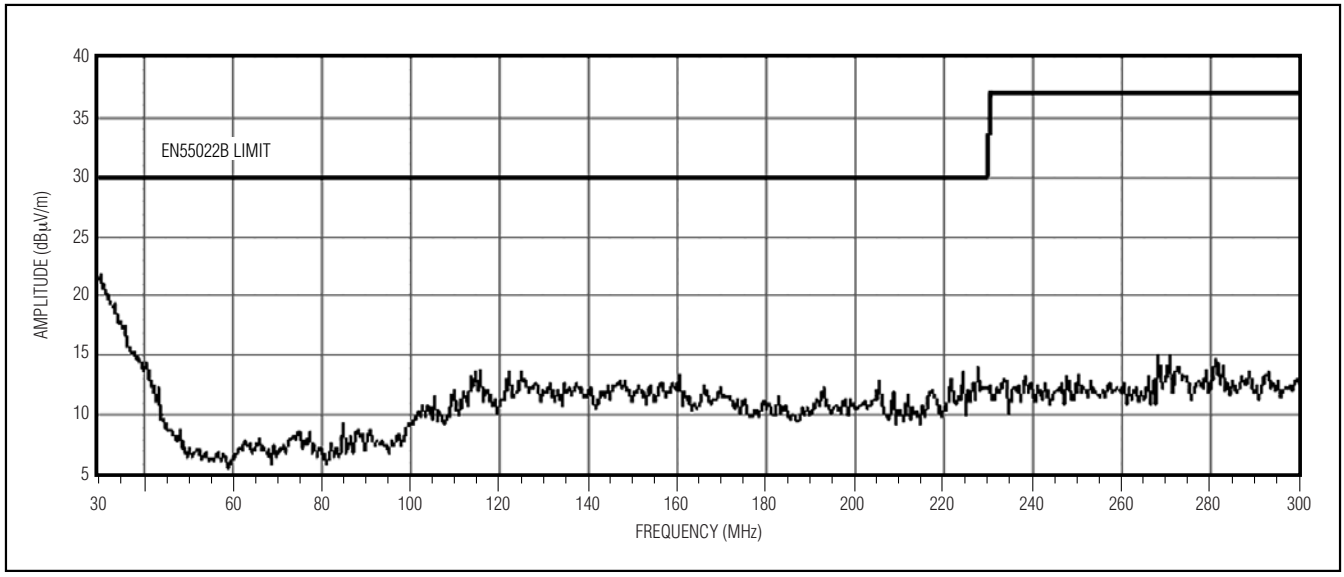


Figure 3. EMI with 76mm of Speaker Cable

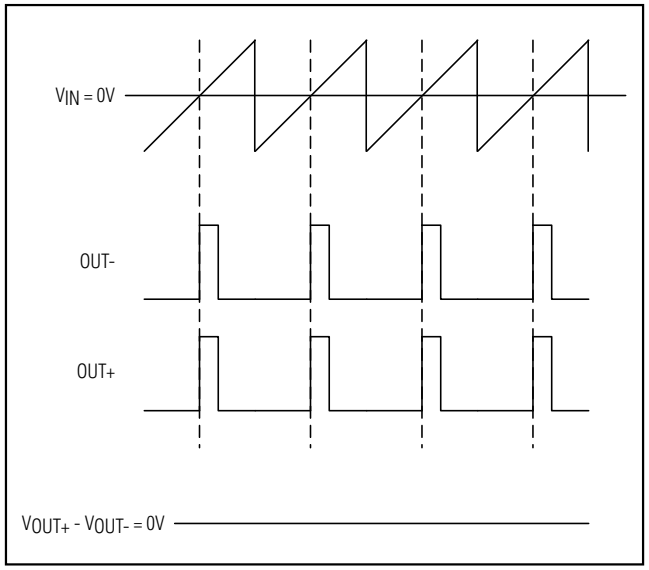


Figure 4. Outputs with No Input Signal

Filterless Modulation/Common-Mode Idle

The MAX9796 uses Maxim's unique modulation scheme that eliminates the LC filter required by traditional Class D amplifiers, improving efficiency, reducing component count, conserving board space and system cost. Conventional Class D amplifiers output a 50% duty-cycle square wave when no signal is present. With no filter, the square wave appears across the load as a DC voltage, resulting in finite load current, increasing power consumption, especially when idling. When no signal is present at the input of the MAX9796, the outputs switch as shown in Figure 4. Because the MAX9796 drives the speaker differentially, the two outputs cancel each other, resulting in no net idle mode voltage across the speaker, minimizing power consumption.

DirectDrive

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the MAX9796 to be biased at GND, almost doubling dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) tantalum capacitors, the MAX9796 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Load Resistance and Charge-Pump Capacitor Size graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes. There is a low DC voltage on the driver outputs

due to amplifier offset. However, the offset of the MAX9796 is typically 1.4mV, which, when combined with a 32Ω load, results in less than 44nA of DC current flow to the headphones.

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises some issues:

1) The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
2) During an ESD strike, the driver's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full ESD strike.
3) When using the headphone jack as a lineout to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

Charge Pump

The MAX9796 features a low-noise charge pump. The switching frequency of the charge pump is half the switching frequency of the Class D amplifier, regardless of the operating mode. The nominal switching frequency is well beyond the audio range, and thus does not interfere with the audio signals, resulting in an SNR of 93dB. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C2 (see the *Typical Application Circuit*). The charge pump is active in both speaker and headphone modes.

Signal Path

The audio inputs of the MAX9796 (INA, INB, and INC) are preamplified and then mixed by the input mixer to create three internal signals: left (L), right (R), and mono (M). Tables 5a and 5b show how the inputs are mixed to create L, R, and M. These signals are then independently volume adjusted by the L, R, and M volume control and routed to the output mixer. The output mixer mixes the internal L, R, and M signals to create a variety of audio mixes that are output to the headphone, speaker, and the mono receiver amplifiers. Figure 6 shows the signal path that the audio signals take.

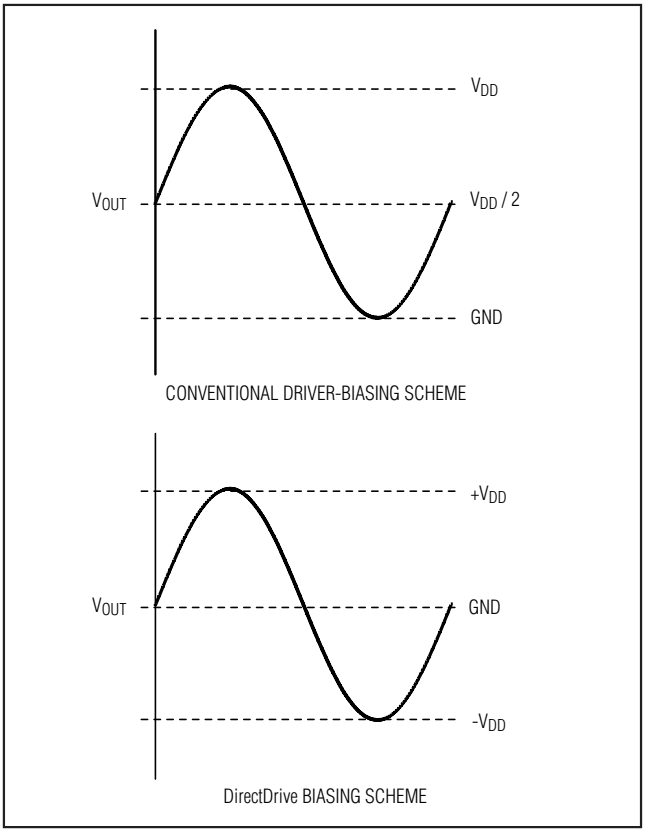


Figure 5. Traditional Amplifier Output vs. MAX9796 DirectDrive Output

Signal amplification takes place in three stages. In the first stage, the inputs (INA, INB, and INC) are preamplified. The amount by which each input is amplified is determined by the bits INA+20dB (B4 in the Input Mode Control Register) and IN+6dB (B3 in the Global Control Register). After preamplification, they are mixed in the input mixer to create the internal signals L, R and M.

In the second stage of amplification, the internal L, R, and M signals are independently volume adjusted.

Finally, each output amplifier has its own internal gain. The speaker, headphone, and mono receiver amplifiers have fixed gains of 12dB, 3dB and 3dB, respectively.

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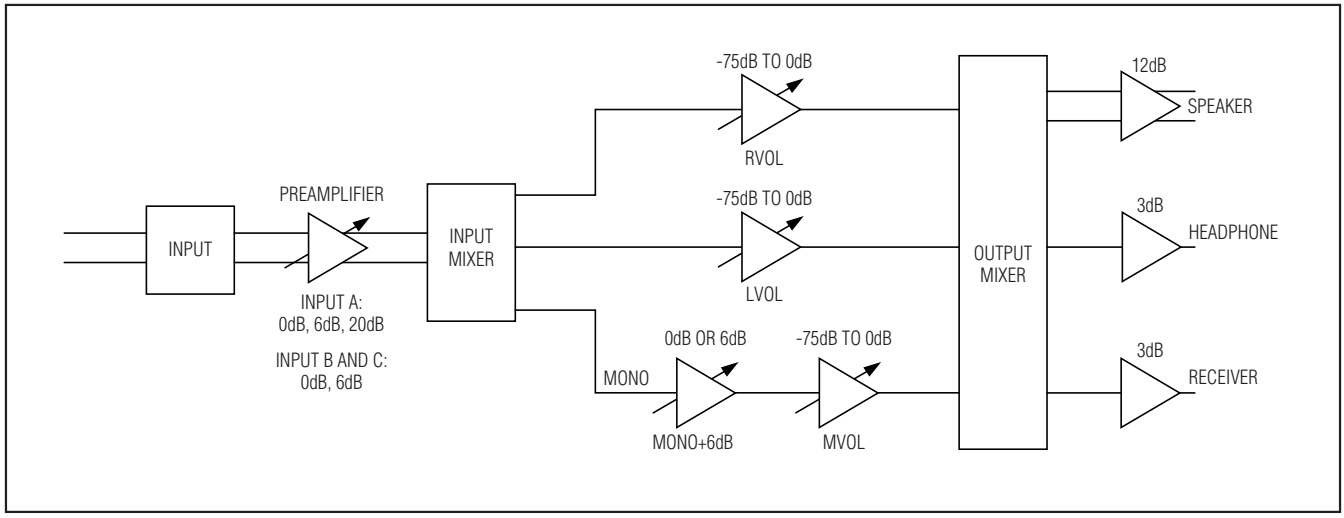


Figure 6. Signal Path

Current-Limit and Thermal Protection

The MAX9796 features current limiting and thermal protection to protect the device from short circuits and overcurrent conditions. The headphone amplifier pulses in the event of an overcurrent condition with a pulse every 100µs as long as the condition is present. Should the current still be high, the above cycle is repeated. The speaker amplifier current-limit protection clamps the output current without shutting down the output. This can result in a distorted output. Current is limited to 1.6A in the speaker amplifiers and 170mA in the headphone and mono receiver amplifiers.

The MAX9796 has thermal protection that disables the device at +150°C until the temperate decreases to +120°C.

Click-and-Pop Suppression

In conventional single-supply headphone amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, during shutdown, the capacitor is discharged to GND. This results in a DC shift across the capacitor, which in turn, appears as an audible transient at the speaker. Since the MAX9796 headphone amplifier does not require output-coupling capacitors, this problem does not arise.

In most applications, the output of the preamplifier driving the MAX9796 has a DC bias of typically half the supply. During startup, the input-coupling capacitor is charged to the preamplifier's DC bias voltage, resulting in a DC shift across the capacitor and an audible click-and-pop. An internal delay of 30ms eliminates the click-and-pop caused by the input filter.

Shutdown

The MAX9796 features a 0.1µA hard shutdown mode that reduces power consumption to extend battery life and a soft shutdown where current consumption is typically 8.5µA. Hard shutdown is controlled by connecting $\overline{SHDN}$ to GND, disabling the amplifiers, bias circuitry, charge pump, and I^2C. In shutdown, the headphone amplifier output impedance is 1.4kΩ and the speaker output impedance is 300kΩ. Similarly, the MAX9796 enters soft shutdown when the $\overline{SHDN}$ bit = 0 (see Table 2). The I^2C interface is active and the contents of the command register are not affected when in soft shutdown. This allows the master to write to the MAX9796 while in shutdown. The I^2C interface is completely disabled in hardware shutdown. When the MAX9796 is reenabled the default settings are applied (see Table 3).

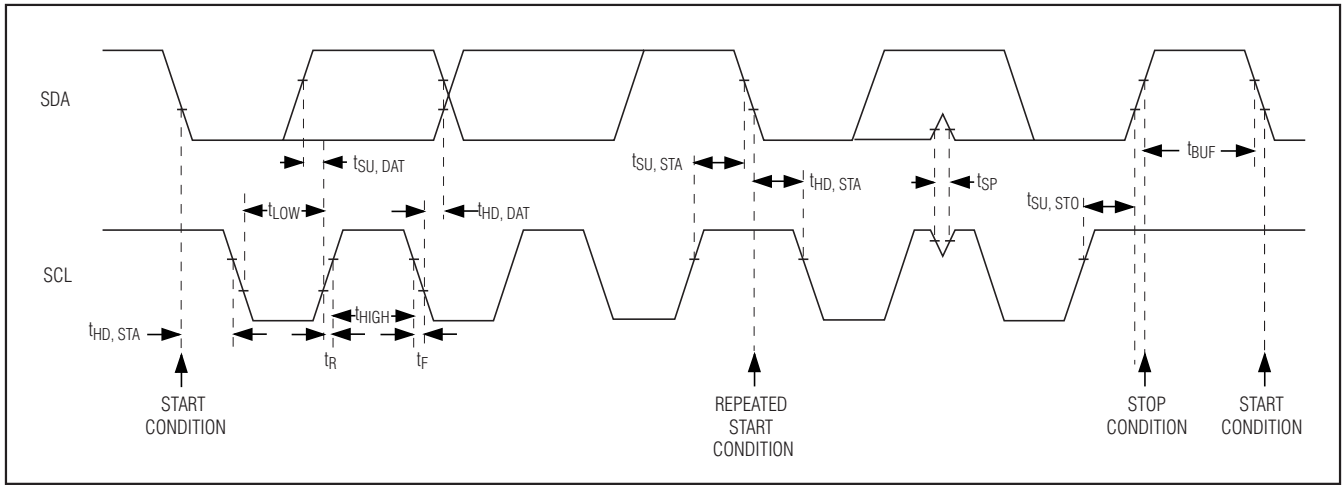


Figure 7. 2-Wire Serial-Interface Timing Diagram

I²C Interface

The MAX9796 features an I²C 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9796 and the master at clock rates up to 400kHz. Figure 7 shows the 2-wire interface timing diagram. The MAX9796 is a receive-only slave device relying on the master to generate the SCL signal. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. The MAX9796 cannot write to the SDA bus except to acknowledge the receipt of data from the master. The MAX9796 does not acknowledge a read command from the master.

A master device communicates to the MAX9796 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9796 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9796 SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9796 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

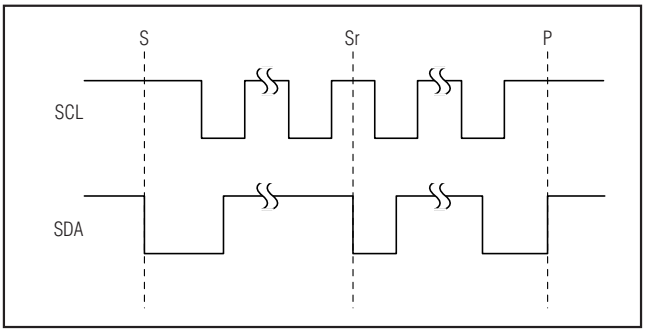


Figure 8. START, STOP, and REPEATED START Conditions

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 8). A START condition from the master signals the beginning of a transmission to the MAX9796. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

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Early STOP Conditions

The MAX9796 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Slave Address

The MAX9796 is available with one preset slave address (see Table 1). The address is defined as the seven most significant bits (MSBs) followed by the read/write (R/$\overline{W}$) bit. The address is the first byte of information sent to the MAX9796 after the START condition. The MAX9796 is a slave device only capable of being written to. The R/$\overline{W}$ bit should be a zero when configuring the MAX9796.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9796 uses to handshake receipt of each byte of data (see Figure 9). The MAX9796 pulls down SDA during the master-generated 9th clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may reattempt communications.

Write Data Format

A write to the MAX9796 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0 (Table 1), one byte of data to configure the Command Register, and a STOP condition. Figure 10 illustrates the proper format for one frame.

The MAX9796 only accepts write data, but it acknowledges the receipt of the address byte with the R/$\overline{W}$ bit set high. The MAX9796 does not write to the SDA bus in the event that the R/$\overline{W}$ bit is set high. Subsequently, the master reads all 1's from the MAX9796. Always set the R/$\overline{W}$ bit to zero to avoid this situation.

Programming the MAX9796

The MAX9796 is programmed through six control registers. Each register is addressed by the three MSBs (B5–B7) followed by five configure bits (B0–B4) as shown in Table 2. Correct programming of the MAX9796 requires writing to all six control registers. Upon power-on, their default settings are as listed in Table 3.

Table 1. MAX9796 Address Map

SLAVE ADDRESS							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/$\overline{W}$**
1	0	0	1	1	0	1	0

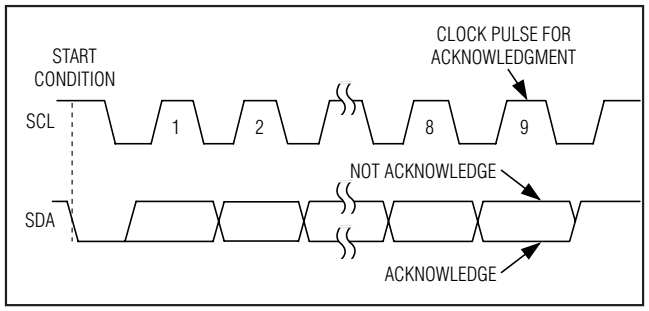


Figure 9. Acknowledge

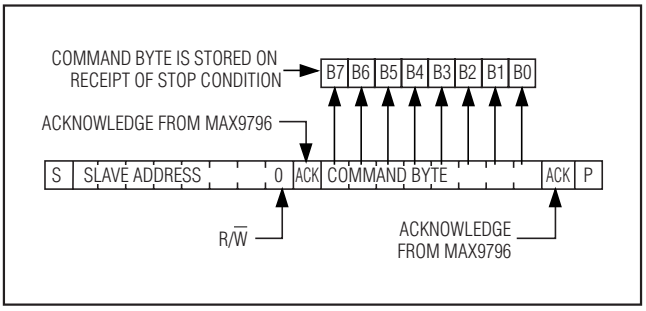


Figure 10. Write Data Format Example

Table 2. Control Registers

FUNCTION	B7	B6	B5	B4	B3	B2	B1	B0
	COMMAND			DATA				
Input Mode Control	0	0	0	INA+20dB	INMODE (Tables 5a and 5b)			
Mono Volume Control	0	0	1	MVOL (Table 7)				
Left Volume Control	0	1	0	LVOL (Table 7)				
Right Volume Control	0	1	1	RVOL (Table 7)				
Output Mode Control	1	0	0	MONO+6dB	OUTMODE (Table 9)			
Global Control Register	1	0	1	$\overline{SHDN}$	IN+6dB	MUTE	SSM	MONO

Table 3. Power-On Reset Conditions

COMMAND	DATA	DESCRIPTION
Input Mode (000)	10000	Input A gain = +20dB; input A, B, and C singled-ended stereo inputs
Mono Volume (001)	11111	Maximum volume
Left Volume (010)	11111	Maximum volume
Right Volume (011)	11111	Maximum volume
Output Mode (100)	01000	Mode 8: stereo headphone, mono speaker
Global Control Register (101)	00011	Powered-off, input B/C gain = 0dB, MUTE off, SSM on, MONO on

Input Mode Control

The MAX9796 has three flexible inputs that can be configured as single-ended stereo inputs or differential mono inputs. All input signals are summed into three unique signals, Left (L), Right (R), and Mono (M), which are routed to the output amplifiers. The bit B4 allows the option of boosting low-level signals on INA. B4 can be set as follows:

1 = Input A's gain +20dB for low-level signals such as FM receivers.

0 = Input A's gain is either 0dB or +6dB as set by IN+6dB (bit B3 of the Control Register).

Tables 5a and 5b show how the inputs–INA, INB, and INC–are mixed to create the internal signals left (L), right (R), and mono (M).

Table 4. Input Mode Control Register

	B7	B6	B5	B4	B3	B2	B1	B0
Input Mode Control	0	0	0	INA+20dB	INMODE (Tables 5a and 5b)			

Table 5a. Input Mode

PROGRAMMING MODE				INPUT CONFIGURATION					
INMODE				INA1	INA2	INB1	INB2	INC1	INC2
B3	B2	B1	B0						
0	0	0	0	L	R	L	R	L	R
0	0	0	1	L	R	L	R	M+	M-
0	0	1	0	L	R	M+	M-	L	R
0	0	1	1	L	R	M+	M-	M+	M-
0	1	0	0	L	R	R+	R-	L+	L-
0	1	0	1	L	R	L+	L-	R+	R-
0	1	1	0	M+	M-	L	R	L	R
0	1	1	1	M+	M-	L	R	M+	M-
1	0	0	0	M+	M-	M+	M-	L	R
1	0	0	1	M+	M-	M+	M-	M+	M-
1	0	1	0	M+	M-	R+	R-	L+	L-
1	0	1	1	M+	M-	L+	L-	R+	R-

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Table 5b. Internal Signals L, R, and M

PROGRAMMING MODE				INTERNAL SIGNALS LEFT (L), RIGHT (R), AND MONO (M)		
INMODE				L	R	M
B3	B2	B1	B0			
0	0	0	0	INA1 + INB1 + INC1	INA2 + INB2 + INC2	—
0	0	0	1	INA1 + INB1	INA2 + INB2	INC1 - INC2
0	0	1	0	INA1 + INC1	INA2 + INC2	INB1 - INB2
0	0	1	1	INA1	INA2	(INB1 - INB2) + (INC1 - INC2)
0	1	0	0	INA1 + (INC1 - INC2)	INA2 + (INB1 - INB2)	—
0	1	0	1	INA1 + (INB1 - INB2)	INA2 + (INC1 - INC2)	—
0	1	1	0	INB1 + INC2	INB2 + INC2	INA1 - INA2
0	1	1	1	INB1	INB2	(INA1 - INA2) + (INC1 - INC2)
1	0	0	0	INC1	INC2	(INA1 - INA2) + (INB1 - INB2)
1	0	0	1	—	—	(INA1 - INA2) + (INB1 - INB2)
1	0	1	0	INC1 - INC2	INB1 - INB2	INA1 - INA2
1	0	1	1	INB1 - INB2	INC1 - INC2	INA1 - INA2

Mono/Left/Right Volume Control

The MAX9796 has separate volume control for each of the internal signals: left (L), right (R), and mono (M). The final gain of each signal is determined by the way the following bits are set: MVOL, LVOL, RVOL, INA+20dB, IN+6dB, and MONO+6dB. Table 7 shows how to configure the L, R, and M amplifiers for specific gains.

Table 6. Mono/Left/Right Volume Control Registers

	B7	B6	B5	B4	B3	B2	B1	B0
Mono Volume Control	0	0	1	MVOL				
Left Volume Control	0	1	0	LVOL				
Right Volume Control	0	1	1	RVOL				

Table 7. Volume Control Settings

MVOL/LVOL/RVOL					GAIN (dB)
B4	B3	B2	B1	B0	
0	0	0	0	0	Mute
0	0	0	0	1	-75
0	0	0	1	0	-71
0	0	0	1	1	-67
0	0	1	0	0	-63
0	0	1	0	1	-59
0	0	1	1	0	-55
0	0	1	1	1	-51

MVOL/LVOL/RVOL					GAIN (dB)
B4	B3	B2	B1	B0	
0	1	0	0	0	-47
0	1	0	0	1	-44
0	1	0	1	0	-41
0	1	0	1	1	-38
0	1	1	0	0	-35
0	1	1	0	1	-32
0	1	1	1	0	-29
0	1	1	1	1	-26

Table 7. Volume Control Settings (continued)

MVOL/LVOL/RVOL					GAIN (dB)
B4	B3	B2	B1	B0	
1	0	0	0	0	-23
1	0	0	0	1	-21
1	0	0	1	0	-19
1	0	0	1	1	-17
1	0	1	0	0	-15
1	0	1	0	1	-13
1	0	1	1	0	-11
1	0	1	1	1	-9
1	1	0	0	0	-7
1	1	0	0	1	-6
1	1	0	1	0	-5
1	1	0	1	1	-4
1	1	1	0	0	-3
1	1	1	0	1	-2
1	1	1	1	0	-1
1	1	1	1	1	0

Output Mode Control

MONO+6dB in the Output Mode Control register allows an extra 6dB of gain on the internal mono signal:

1 = Additional 6dB of gain is applied to the internal Mono (M) signal path.

0 = No additional gain is applied to the Internal Mono (M) signal path.

The MAX9796 has four output amplifiers: a mono receiver amplifier, a stereo DirectDrive headphone amplifier, and one mono Class D amplifier.

Table 8. Output Mode Control Register

	B7	B6	B5	B4	B3	B2	B1	B0
Output Mode Control	1	0	0	Mono+6dB	OUTMODE (Table 9)			

Table 9 shows how each of the three internal signals, left (L), right (R), and mono (M), are mixed and routed to the various outputs.

Table 9. Output Modes

MODE	OUTMODE				RECEIVER	LEFT HP	RIGHT HP	SPK
	B3	B2	B1	B0				
0	0	0	0	0	—	—	—	—
1	0	0	0	1	M	—	—	—
2	0	0	1	0	—	—	—	M
3	0	0	1	1	—	M	M	M
4	0	1	0	0	—	M	M	—
5	0	1	0	1	—	—	—	—
6	0	1	1	0	L + R	—	—	—
7	0	1	1	1	—	—	—	L + R
8	1	0	0	0	—	L	R	L + R
9	1	0	0	1	—	L	R	—
10	1	0	1	0	—	—	—	—
11	1	0	1	1	M + L + R	—	—	—
12	1	1	0	0	—	—	—	L+R+M
13	1	1	0	1	—	L + M	R + M	L+R+M
14	1	1	1	0	—	L + M	R + M	—
15	1	1	1	1	MUTE	MUTE	MUTE	MUTE

— = Amplifier off, R = Right signal
L = Left signal, M = Mono signal

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Global Control Register

The Global Control Register is used for global configurations, those affecting all inputs and outputs. The bits in the Control Register affect the inputs and outputs as shown in Table 11.

Table 10. Global Control Register

	B7	B6	B5	B4	B3	B2	B1	B0
Global Control Register	1	0	1	$\overline{SHDN}$	IN+6dB	MUTE	SSM	MONO

Table 11. Global Control Register Configurations

BIT	NAME	FUNCTION
B4	$\overline{SHDN}$	1 = Normal operation. 0 = Low-power shutdown mode. I^2C settings are saved.
B3	IN+6dB	1 = All input signals are boosted by 6dB. 0 = All input signals are passed unamplified. This bit does not affect INA if the INA+20dB bit (B4 of the Input Mode Control Register) is set to 1, in which case INA is boosted by 20dB.
B2	MUTE	1 = Mute all outputs. 0 = All outputs are active.
B1	SSM	1 = Spread-spectrum Class D modulation. 0 = Fixed-frequency Class D modulation.
B0	MONO	1 = Speaker outputs L+R in modes 7, 8, 12, and 13 (see Table 9). 0 = Speaker outputs L in modes 7, 8, 12, and 13 (see Table 9).

Applications Information

Class D Filterless Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's PWM output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency. The traditional PWM scheme uses large differential output swings (2 x $V_{DD(P-P)}$) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The MAX9796 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Because the switching frequency of the MAX9796 speaker output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power may be damaged. For optimum results, use a speaker with a series inductance >10µH. Typical 8Ω speakers, for portable audio applications, exhibit series inductances in the range of 20µH to 100µH.

Input Amplifier

Differential Input

The MAX9796 features a programmable differential input structure, making it compatible with many CODECs, and offering improved noise immunity over a single-ended input amplifier. In devices such as cellular phones, high-frequency signals from the RF transmitter can be picked up by the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs and any signal common to both is cancelled.

Single-Ended Input

The MAX9796 can be configured as a single-ended input amplifier by appropriately configuring the Input Control Register (see Tables 5a and 5b).

DC-Coupled Input

The input amplifier can accept DC-coupled inputs that are biased to the amplifier's bias voltage. DC-coupling eliminates the input-coupling capacitors; reducing component count to potentially six external components (see the *Typical Application Circuit*). However, the highpass filtering effect of the capacitors is lost, allowing low-frequency signals to feed through to the load.

Unused Inputs

Connect any unused input directly to V_{BIAS}. This saves input capacitors on unused inputs and provides the highest noise immunity on the input.

Component Selection

Input Filter

An input capacitor (C_{IN}) in conjunction with the input impedance of the MAX9796 forms a highpass filter that removes the DC bias from the incoming signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system and the actual frequency band of interest. Although high-fidelity audio calls for a flat-gain response between 20Hz and 20kHz, portable voice-reproduction devices, such as cell phones and two-way radios, need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 300Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

Class D Output Filter

The MAX9796 does not require a Class D output filter. The device passes EN55022B emissions standards with 152mm of unshielded speaker cables. However, output filtering can be used if a design is failing radiated emissions due to board layout or cable length, or the circuit is near EMI-sensitive devices. Use a ferrite bead filter when radiated frequencies above 10MHz are of concern. Use an LC filter when radiated frequencies below 10MHz are of concern, or when long leads (>152mm) connect the amplifier to the speaker. Figure 11 shows optional speaker amplifier output filters.

External Component Selection

BIAS Capacitor

V_{BIAS} is the output of the internally generated DC bias voltage. The V_{BIAS} bypass capacitor, C_{VBIAS} improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, startup/shutdown DC bias waveforms for the speaker amplifiers. Bypass V_{BIAS} with a 1µF capacitor to GND.

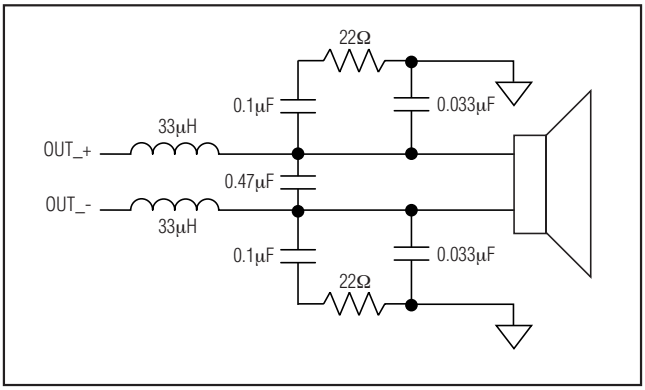


Figure 11. Speaker Amplifier Output Filter

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Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface-mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric or better. Table 12 lists suggested manufacturers.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the output resistance of the charge pump. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Output Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at CPV_{SS}. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance and Charge-Pump Capacitor Size graph in the *Typical Operating Characteristics*.

CPV_{DD} Bypass Capacitor (C3)

The CPV_{DD} bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the MAX9796's charge-pump switching transients. Bypass CPV_{DD} with C3 to PGND and place it physically close to the CPV_{DD} and PGND. Use a value for C3 that is equal to C1.

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PCB. Route all traces that carry switching transients away from GND and the traces/components in the audio signal path.

Connect all of the power-supply inputs (CPV_{DD}, V_{DD}, and PV_{DD}) together. Bypass CPV_{DD} with a 1µF capacitor to CPGND. Bypass V_{DD} with a 1µF capacitor to GND. Bypass PV_{DD} with a 1µF capacitor in parallel with a 0.1µF capacitor to PGND. Place the bypass capacitors as close as possible to the MAX9796. Place a bulk capacitor between PV_{DD} and PGND, if needed.

Use large, low-resistance output traces. Current drawn from the outputs increase as load impedance decreases. High output trace resistance decreases the power delivered to the load. Large output, supply, and GND traces allow more heat to move from the MAX9796 to the PCB, decreasing the thermal impedance of the circuit.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information of reliability testing results, refer to Application Note: UCSP—A Wafer-Level Chip-Scale Package available on Maxim's website at www.maxim-ic.com/ucsp.

UCSP Thermal Consideration

When operating at maximum output power, the UCSP thermal dissipation can become a limiting factor. The UCSP package does not dissipate heat as efficiently as packages with a thermal pad. As a result, in some applications, the thermal performance of the package may limit performance.

Table 12. Suggested Capacitor Manufacturers

SUPPLIER	PHONE	FAX	WEBSITE
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com

Chip Information

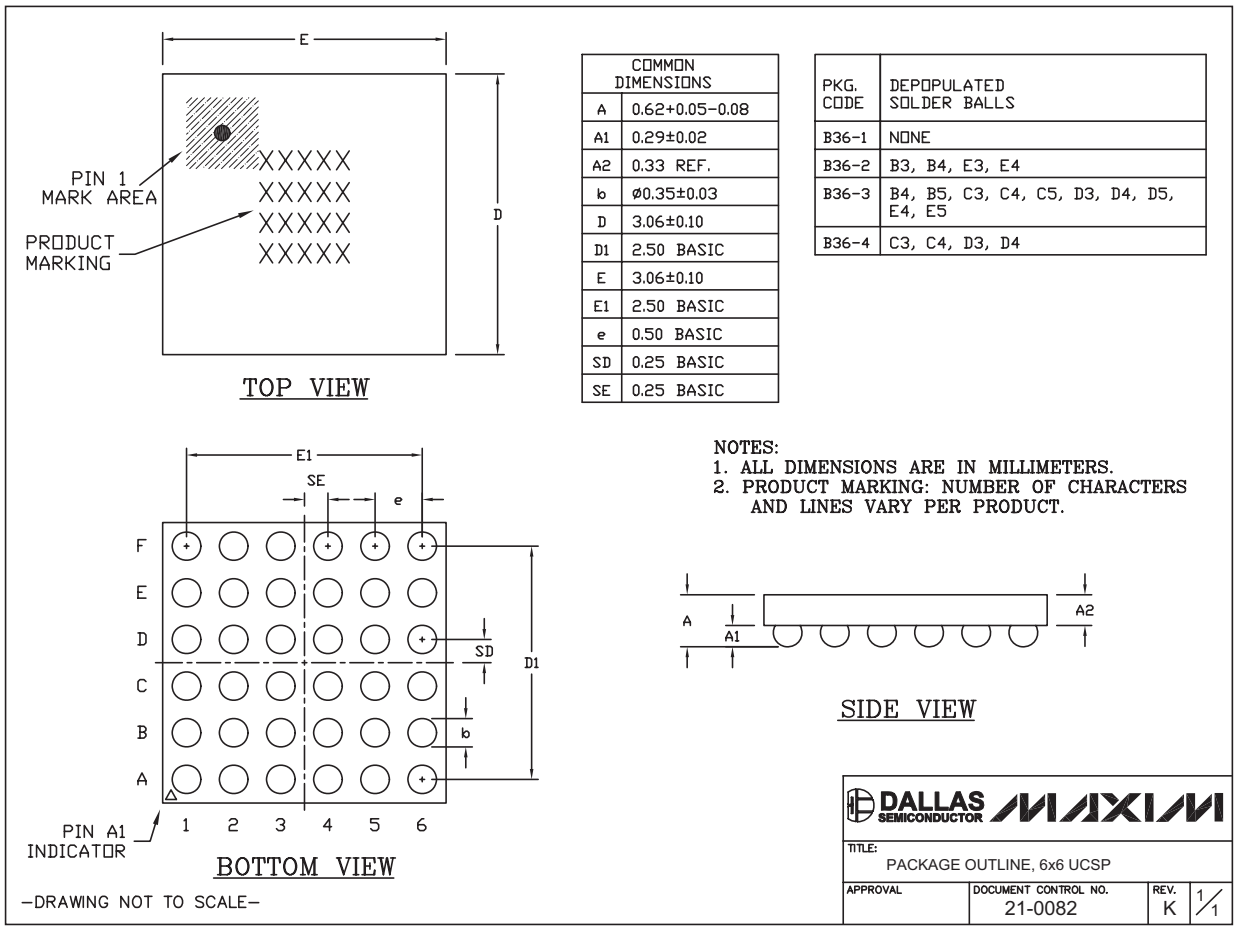
PROCESS: BiCMOS

2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

36L,UCSP.EPS



COMMON DIMENSIONS	
A	0.62+0.05–0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D	3.06±0.10
D1	2.50 BASIC
E	3.06±0.10
E1	2.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	DEPOPULATED SOLDER BALLS
B36-1	NONE
B36-2	B3, B4, E3, E4
B36-3	B4, B5, C3, C4, C5, D3, D4, D5, E4, E5
B36-4	C3, C4, D3, D4

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6x6 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0082	K	1/1

2.3W, High-Power Class D Audio Subsystem with DirectDrive Headphone Amplifiers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/07	Initial release	—
1	1/08	Updated Typical Application Circuit	13

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