MAX7326

I²C Port Expander with 12 Push-Pull Outputs and 4 Inputs

General Description

The MAX7326 2-wire serial-interfaced peripheral features 16 I/O ports. The ports are divided into 12 push-pull outputs and four input ports with selectable internal pullups. Input ports are overvoltage protected to +6V and feature transition detection with interrupt output.

The four input ports are continuously monitored for state changes (transition detection). The interrupt is latched, allowing detection of transient changes. Any combination of inputs can be selected using the interrupt mask to assert the open-drain, +6V-tolerant $\overline{INT}$ output. When the MAX7326 is subsequently accessed through the serial interface, any pending interrupt is cleared. The 12 push-pull outputs are rated to sink 20mA and are capable of driving LEDs. The $\overline{RST}$ input clears the serial interface, terminating any I²C communication to or from the MAX7326.

The MAX7326 uses two address inputs with four-level logic to allow 16 I²C slave addresses. The slave address also sets the power-up default state for the 12 output ports and enables or disables internal 40kΩ pullups in groups of two input ports.

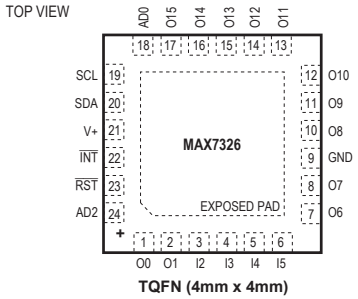
The MAX7326 is one device in a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see Table 1).

The MAX7326 is available in 24-pin QSOP and TQFN packages and is specified over the -40°C to +125°C automotive temperature range.

Applications

- Cell Phones
- SAN/NAS
- Servers
- Notebooks
- Satellite Radio

Pin Configurations



TQFN (4mm x 4mm)

Pin Configurations continued at end of data sheet.

Features

- 400kHz I²C Serial Interface
- +1.71V to +5.5V Operating Voltage
- 12 Push-Pull Outputs Rated at 20mA Sink Current
- 4 Input Ports with Matchable Latching Transition Detection
- Input Ports are Overvoltage Protected to +6V
- Transient Changes are Latched, Allowing Detection Between Read Operations
- $\overline{INT}$ Output Alerts Change on Any Selection of Inputs
- AD0 and AD2 Inputs Select from 16 Slave Addresses
- Low 0.6µA Standby Current
- -40°C to +125°C Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7326AEG+	-40°C to +125°C	24 QSOP
MAX7326ATG+	-40°C to +125°C	24 TQFN-EP* (4mm x 4mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Selector Guide

PART	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS
MAX7324	8	Yes	—	8
MAX7325	Up to 8	—	Up to 8	8
MAX7326	4	Yes	—	12
MAX7327	Up to 4	—	Up to 4	12

Typical Application Circuit and Functional Diagram appear at end of data sheet.

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Absolute Maximum Ratings

(All voltages referenced to GND.)

Supply Voltage V+ ..... -0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{RST}$, $\overline{INT}$, I2–I5 ..... -0.3V to +6V
O0, O1, O6–O15 ..... -0.3V to V+ + 0.3V
O0, O1, O6–O15 Output Current ..... ?25mA
SDA Sink Current 10mA
$\overline{INT}$ Sink Current 10mA
Total V+ Current 50mA
Total GND Current 100mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.5mW/°C over +70°C) 761.9mW
24-Pin TQFN (derate 20.8mW/°C over +70°C) 1666.7mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+	T_A = -40°C to +125°C		1.71		5.50	V
Power-On-Reset Voltage	V_{POR}	V+ falling				1.6	V
Standby Current (Interface Idle)	I_{STB}	SCL and SDA and other digital inputs at V+			0.6	1.9	µA
Supply Current (Interface Running)	I+	f_{SCL} = 400kHz, other digital inputs at V+			23	55	µA
Input High-Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5	V_{IH}	V+ < 1.8V		0.8 x V+			V
		V+ ≥ 1.8V		0.7 x V+			
Input Low-Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5	V_{IL}	V+ < 1.8V				0.2 x V+	V
		V+ ≥ 1.8V				0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5	I_{IH}, I_{IL}	SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5 at V+ or GND		-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5					10		pF
Output Low-Voltage O0, O1, O6–O15	V_{OL}	V+ = +1.71V, I_{SINK} = 5mA	QSOP		90	180	mV
			TQFN		90	230	
		V+ = +2.5V, I_{SINK} = 10mA	QSOP		110	210	
			TQFN		110	260	
		V+ = +3.3V, I_{SINK} = 15mA	QSOP		130	230	
			TQFN		130	280	
		V+ = +5V, I_{SINK} = 20mA	QSOP		140	250	
			TQFN		140	300	
Output High-Voltage O0, O1, O6–O15	V_{OH}	V+ = +1.71V, I_{SOURCE} = 2mA		V+ - 250	V+ - 30		mV
		V+ = +2.5V, I_{SOURCE} = 5mA		V+ - 360	V+ - 30		
		V+ = +3.3V, I_{SOURCE} = 5mA		V+ - 260	V+ - 30		
		V+ = +5V, I_{SOURCE} = 10mA		V+ - 360	V+ - 30		
Output Low-Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA				250	mV
Output Low-Voltage $\overline{INT}$	V_{OLINT}	I_{SINK} = 5mA			130	250	mV
Port Input Pullup Resistor	R_{PU}			25	40	55	kΩ

Port and Interrupt $\overline{INT}$ Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t_{PPV}	C_L ≤ 100pF			4	µs
Port Input Setup Time	t_{PSU}	C_L ≤ 100pF	0			µs
Port Input Hold Time	t_{PH}	C_L ≤ 100pF	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	C_L ≤ 100pF			4	µs
$\overline{INT}$ Reset Delay Time from STOP	t_{IP}	C_L ≤ 100pF			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	C_L ≤ 100pF			4	µs

Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

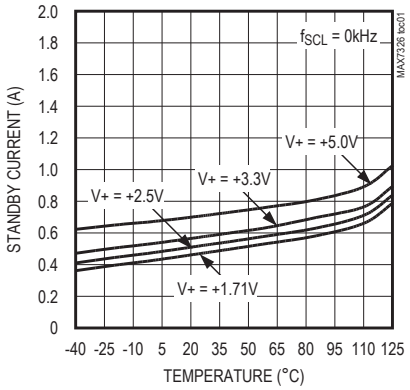
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU,STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 2)			0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		20 + 0.1C_b	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		20 + 0.1C_b	300	ns
Fall Time of SDA Transmitting	$t_{F,TX}$	(Notes 3, 4)		20 + 0.1C_b	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF
$\overline{RST}$ Pulse Width	t_W		500			ns
$\overline{RST}$ Rising to START Condition Setup Time	$t_{\overline{RST}}$		1			µs

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 3: Guaranteed by design.
Note 4: Cb = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3 x V+ and 0.7 x V+.
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

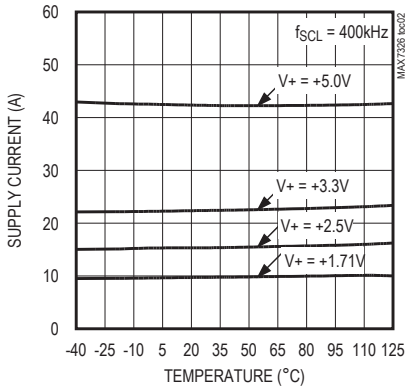
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

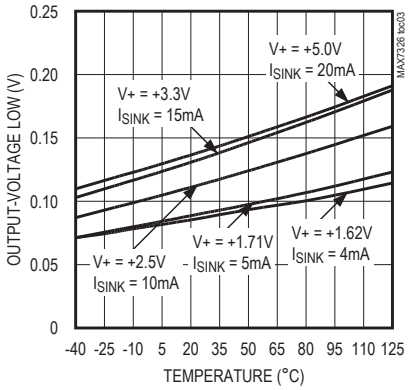
STANDBY CURRENT vs. TEMPERATURE



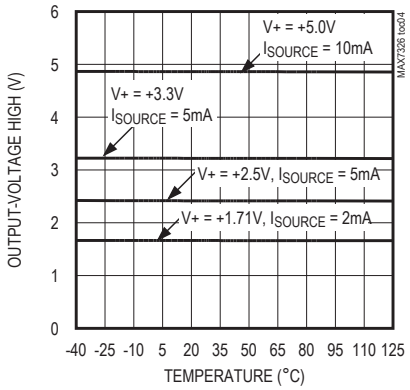
SUPPLY CURRENT vs. TEMPERATURE



OUTPUT-VOLTAGE LOW vs. TEMPERATURE



OUTPUT-VOLTAGE HIGH vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1	22	$\overline{INT}$	Interrupt Output, Active Low. $\overline{INT}$ is an open-drain output.
2	23	$\overline{RST}$	Reset Input, Active Low. Drive $\overline{RST}$ low to clear the 2-wire interface.
3, 21	24, 18	AD2, AD0	Address Inputs. Select device slave address with AD0 and AD2 To either GND, V+, SCL, or SDA to give four logic combinations (see Tables 2 and 3).
4, 5, 10, 11, 13–20	1, 2, 7, 8, 10–17	O0, O1, O6–O15	Output Ports. These push-pull outputs are rated at 20mA.
6–9	3–6	I2–I5	Input Ports. I2 and I5 are CMOS-logic inputs protected to +6V.
12	9	GND	Ground
22	19	SCL	I²C-Compatible Serial-Clock Input
23	20	SDA	I²C-Compatible Serial-Data I/O
24	21	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047µF ceramic capacitor.
—	EP	EP	Exposed Pad. Connect EP to GND.

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7326 is a general-purpose port expander operating from a +1.71V to +5.5V supply that provides 12 push-pull output ports with 20mA sink, 10mA source drive capability, and four CMOS input ports that are overvoltage protected to +6V. The MAX7326 is rated to sink a total of 100mA and source a total of 50mA from all 12 combined outputs.

The MAX7326 is set to two of 32 I²C slave addresses (see Tables 2 and 3) using address inputs AD0 and AD2, and is accessed over an I²C serial interface up to 400kHz. Eight outputs use a different slave address from the other four outputs and four inputs. Eight push-pull outputs (O8–O15) use the 101xxxx addresses while the four outputs (O0, O1, O6, and O7) and inputs (I2–I5) use addresses with 110xxxx. The $\overline{RST}$ input clears the serial interface in case of a bus lockup, terminating any serial transaction to or from the MAX7326.

Table 1. MAX7319–MAX7329 Family Comparison

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	CONFIGURATION
16-PORT EXPANDERS						
MAX7324	101xxxx And 110xxxx	8	Yes	—	8	8 inputs and 8 push-pull outputs version: 8 input ports with programmable latching transition detection interrupt and selectable pullups. 8 push-pull outputs with selectable default logic levels. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even if only for a transient) since the ports were last read.
MAX7325		Up to 8	—	Up to 8	8	8 I/O and 8 push-pull outputs version: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 8 push-pull outputs with selectable default logic levels. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors, but pullups draw current when output is low. Any open-drain port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which open-drain port inputs have changed (even if only for a transient) since the ports were last read.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	CONFIGURATION
MAX7326	101xxxx and 110xxxx	4	Yes	—	12	4 input-only, 12 push-pull output versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups. 12 push-pull outputs with selectable default logic levels. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even if only for a transient) since the ports were last read.
MAX7327		Up to 4	—	Up to 4	12	4 I/O, 12 push-pull output versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 12 push-pull outputs with selectable default logic levels. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors, but pullups draw current when output is low. Any open-drain port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which open-drain port inputs have changed (even if only for a transient) since the ports were last read.
8-PORT EXPANDERS						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: 8 input ports with programmable latching transition detection interrupt and selectable pullups.
MAX7320	101xxxx	—	—	—	8	Output-only versions: 8 push-pull outputs with selectable power-up default levels.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups.
MAX7322	110xxxx	4	Yes	—	4	4 input-only, 4 output-only versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	CONFIGURATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	4 I/O, 4 output-only versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	8 open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports.

When the MAX7326 is read through the serial interface, the actual logic levels at the ports are read back.

The four input ports offer latching transition detection functionality. All input ports are continuously monitored for changes. An input change sets 1 of 4 flag bits that identify the changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7326.

A latching interrupt output ($\overline{INT}$) is programmed to flag input data changes on the four input ports through an interrupt mask register. By default, data changes on any input port force $\overline{INT}$ to a logic-low. Interrupt output $\overline{INT}$ and all transition flags are deasserted when the MAX7326 is next accessed through the serial interface.

Internal pullup resistors to V+ are selected by the address select inputs (AD0 and AD2). Pullups are enabled on the input ports in groups of two (see Table 2).

Initial Power-Up

On power-up, the transition detection logic is reset, and $\overline{INT}$ is deasserted. The interrupt mask register is set to 0x3C, enabling the interrupt output for transitions on all four input ports. The transition flags are cleared to indicate no data changes. The power-up default states of the 12 push-pull outputs are set according to the I²C slave address selection inputs, AD0 and AD2 (see Tables 2 and 3). Pullups are enabled on the input port in groups of two (see Table 2).

Power-On Reset (POR)

The MAX7326 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. When V+ rises above V_{POR} (1.6V max), the POR circuit releases the registers and 2-wire interface for normal operation. When V+ drops below V_{POR}, the MAX7326 resets all output register contents to the POR defaults (Tables 2 and 3).

$\overline{RST}$ Input

The active-low $\overline{RST}$ input operates as a reset that voids any I²C transaction involving the MAX7326 and forcing the MAX7326 into the I²C STOP condition. The reset action does not clear the interrupt output ($\overline{INT}$).

Standby Mode

When the serial interface is idle, the MAX7326 automatically enters standby mode, drawing minimal supply current.

Slave Address, Power-Up Default Logic Levels, and Input Pullup Selection

Address inputs AD0 and AD2 determine the MAX7326 slave address and select which inputs have pullup resistors. Pullups are enabled on the input ports in groups of two (see Table 2).

The MAX7326 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7326. The MAX7326 distinguishes whether address inputs AD0 and AD2 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. This means that the MAX7326 slave address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7326 cannot decode address inputs AD0 and AD2 fully until the first I²C transmission. This is important because the address selection is used to determine the power-up logic state (output low or I/O high), and whether pullups are enabled. However, at power-up, the I²C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave) connected to the bus, including the MAX7326. This is guaranteed as part of the I²C specification. Therefore, when address inputs AD0 and AD2 are connected to SDA or SCL during power-up, they appear to be connected to V+. The port

Table 2. MAX7326 Address Map for Ports O0, O1, I2–I5, O6, and O7

PIN CONNECTION		DEVICE ADDRESS							PORT POWER-UP DEFAULT								40kΩ INPUT PULLUPS ENABLED							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**O7**	**O6**	**I5**	**I4**	**I3**	**I2**	**O1**	**O0**	**O7**	**O6**	**I5**	**I4**	**I3**	**I2**	**O1**	**O0**
SCL	GND	1	1	0	0	0	0	0	1	1	Inputs				0	0	Pullups are not enabled for push-pull outputs.		Y	Y	—	—	Pullups are not enabled for push-pull outputs.	
SCL	V+	1	1	0	0	0	0	1	1	1					1	1			Y	Y	Y	Y		
SCL	SCL	1	1	0	0	0	1	0	1	1					1	1			Y	Y	Y	Y		
SCL	SDA	1	1	0	0	0	1	1	1	1					1	1			Y	Y	Y	Y		
SDA	GND	1	1	0	0	1	0	0	1	1					0	0			Y	Y	—	—		
SDA	V+	1	1	0	0	1	0	1	1	1					1	1			Y	Y	Y	Y		
SDA	SCL	1	1	0	0	1	1	0	1	1					1	1			Y	Y	Y	Y		
SDA	SDA	1	1	0	0	1	1	1	1	1					1	1			Y	Y	Y	Y		
GND	**GND**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**					**0**	**0**			**—**	**—**	**—**	**—**		
GND	**V+**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**					**1**	**1**			**—**	**—**	**Y**	**Y**		
GND	SCL	1	1	0	1	0	1	0	0	0					1	1			—	—	Y	Y		
GND	SDA	1	1	0	1	0	1	1	0	0					1	1			—	—	Y	Y		
V+	**GND**	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**					**0**	**0**			**Y**	**Y**	**—**	**—**		
V+	**V+**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**					**1**	**1**			**Y**	**Y**	**Y**	**Y**		
V+	SCL	1	1	0	1	1	1	0	1	1					1	1			Y	Y	Y	Y		
V+	SDA	1	1	0	1	1	1	1	1	1					1	1			Y	Y	Y	Y		

selection logic uses AD0 to select whether pullups are enabled for ports I2 and I3, and to set the initial logic level for those ports, and AD2 for ports I4 and I5. The rule is that a logic-high, SDA, or SCL connection selects the pullups and sets the default logic state to high. A logic-low sets the default to low (Tables 2 and 3). This means that the port configuration is correct on power-up for a standard I²C configuration, where SDA or SCL are pulled up to V+ by the external I²C pullup resistors.

The power-up default states of the 12 push-pull outputs are set according to the I²C slave address selection inputs, AD0 and AD2 (Tables 2 and 3).

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true—for example, in applications in which there is legitimate bus activity during power-up. Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7326's supply voltage, and if that pullup supply rises later than the MAX7326's supply, then SDA or SCL may appear at power-up to be connected to GND. In applications like this, use the four address combinations that are selected by strapping address inputs AD0 and AD2 to V+ or ground (shown in **bold** in Tables 2 and 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, an unexpected combination of pullups might be asserted until the first I²C transmission (to any device, not necessarily the MAX7326) is put on the bus, and an unexpected combination of ports may initialize as logic-low outputs instead of inputs or logic-high outputs.

Port Inputs

Port inputs switch at CMOS-logic levels as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

Port-Input Transition Detection

All four input ports are monitored for changes since the expander was last accessed through the serial interface. The state of the input ports is stored in an internal "snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port input, then an internal transition flag is set for that port. The four port inputs are sampled (internally latched into the snapshot register) and the old transition flags are cleared during the I²C acknowledge of every MAX7326 read and write access. The previous port transition flags are read through the serial interface as the second byte of a 2-byte read sequence.

Table 3. MAX7326 Address Map for Outputs O8–O15

PIN CONNECTION		DEVICE ADDRESS							OUTPUTS POWER-UP DEFAULT							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**O15**	**O14**	**O13**	**O12**	**O11**	**O10**	**O9**	**O8**
SCL	GND	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0
SCL	V+	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1
SCL	SCL	1	0	1	0	0	1	0	1	1	1	1	1	1	1	1
SCL	SDA	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
SDA	GND	1	0	1	0	1	0	0	1	1	1	1	0	0	0	0
SDA	V+	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1
SDA	SCL	1	0	1	0	1	1	0	1	1	1	1	1	1	1	1
SDA	SDA	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1
GND	**GND**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
GND	**V+**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
GND	SCL	1	0	1	1	0	1	0	0	0	0	0	1	1	1	1
GND	SDA	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1
V+	GND	1	0	1	1	1	0	0	1	1	1	1	0	0	0	0
V+	**V+**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
V+	**SCL**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
V+	SDA	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

A long read sequence (more than 2 bytes) can be used to poll the expander continuously without the overhead of resending the slave address. If more than 2 bytes are read from the expander, the expander repeatedly returns the 2 bytes of input port data followed by the transition flags. The inputs are repeatedly resampled and the transition flags repeatedly reset for each pair of bytes read. All changes that occur during a long read sequence are detected and reported.

The MAX7326 includes a 4-bit interrupt mask register that selects which inputs generate an interrupt upon change. Each input's transition flag is set when its input changes, independent of the interrupt mask register settings. The interrupt mask register allows the processor to be interrupted for critical events, while the inputs and the transition flags can be polled periodically to detect less-critical events.

The $\overline{INT}$ output is not reasserted during a read sequence to avoid recursive reentry into an interrupt service routine. Instead, if a data change occurs that would normally cause the $\overline{INT}$ output to be set, the $\overline{INT}$ assertion is delayed until the STOP condition. $\overline{INT}$ is not reasserted upon a STOP condition if the changed input data is read before the STOP occurs. The $\overline{INT}$ logic ensures that unnecessary interrupts are not asserted, yet data changes are detected and reported no matter when the change occurs.

Transition-Detection Masks

The transition-detection logic incorporates a change flag and an interrupt mask bit for each of the four input ports. The four change flags can be read through the serial interface, and the 4-bit interrupt mask is set through the serial interface.

Each port's change flag is set when that port's input changes, and the change flag remains set even if the input returns to its original state. The port's interrupt mask determines whether a change on that input port generates an interrupt. Enable interrupts for high-priority inputs using the interrupt mask. The interrupt allows the system to respond quickly to changes on these inputs. Poll the MAX7326 periodically to monitor less-important inputs. The change flags indicate whether a permanent or transient change has occurred on any input since the MAX7326 was last accessed.

Serial Interface

Serial Addressing

The MAX7326 operates as a slave that sends and receives data through an I²C interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7326 and generates the SCL clock that synchronizes the data transfer (Figure 1).

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7326's 7-bit slave addresses plus R/$\overline{W}$ bits, 1 or more data bytes, and finally a STOP condition (Figure 2).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

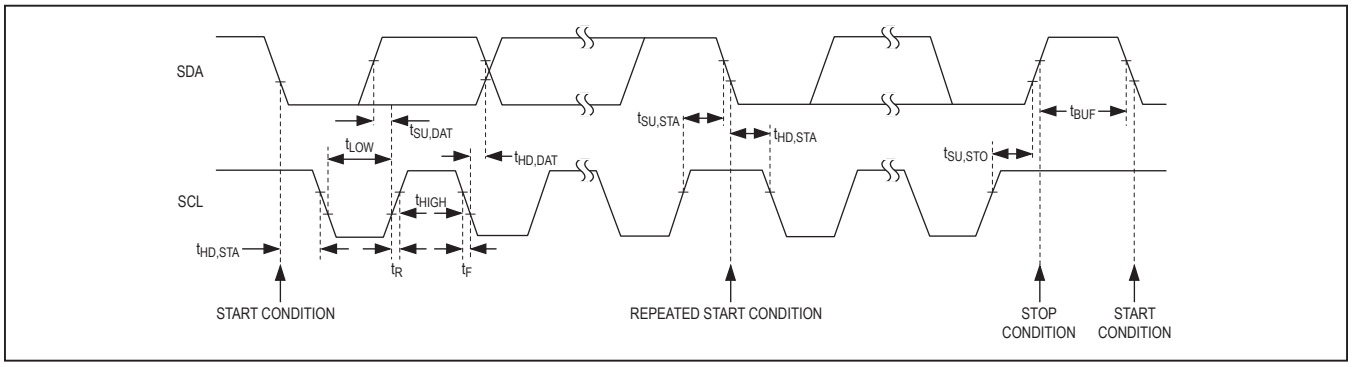


Figure 1. 2-Wire Serial-Interface Timing Details

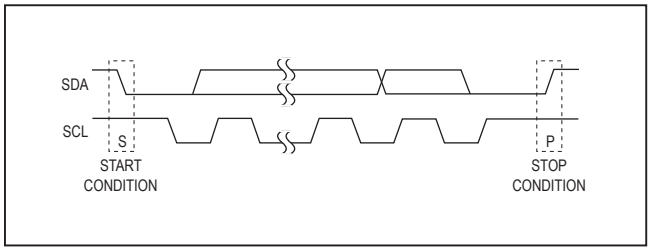


Figure 2. Start and Stop Conditions

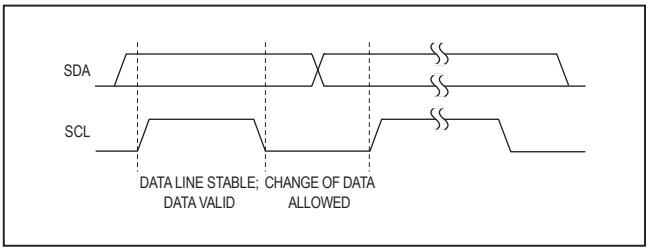


Figure 3. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7326, the MAX7326 generates the acknowledge bit because the device is the recipient. When the MAX7326 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7326 has two different 7-bit slave addresses (Figure 5). The addresses are different to communicate to the eight push-pull outputs (O8–O15) or the other eight I/Os. The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command and high for a read command.

The first (A6), second (A5), and third (A4) bits of the MAX7326 slave address are always 1, 1, and 0 (O0, O1, I2–I5, O6, and O7) or 1, 0, and 1 (O8–O15). Connect AD0 and AD2 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7326 has 16 possible slave addresses (Tables 2 and 3), allowing up to 16 MAX7326 devices on an I²C bus.

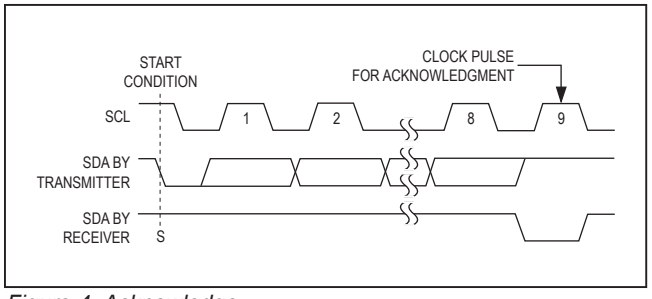


Figure 4. Acknowledge

Accessing the MAX7326

The MAX7326 is accessed though an I²C interface. The MAX7326 provides two different 7-bit slave addresses for either the group A of eight ports (O0, O1, I2–I5, O6, O7) or the group B of eight ports (O8–O15). See Tables 2 and 3.

A **single-byte read** from the group A ports of the MAX7326 returns the status of the four input ports and four output ports (read back as inputs), and clears both the internal transition flags and the $\overline{INT}$ output when the master acknowledges the salve address byte. A single-byte read from the group B ports of the MAX7326 returns the status of the eight output ports, read back as inputs.

A **2-byte read** from the group A ports of the MAX7326 returns the status of the four input ports (as for a single-byte read), followed by the four transition flags for the four input ports and four output ports. The internal transition flags and the $\overline{INT}$ output are cleared when the master acknowledges the slave address byte, but the previous transition flag data is sent as the second byte. A 2-byte read from the group B ports of the MAX7326 repeatedly returns the status of the eight output ports, read back as inputs.

A **multibyte read** (more than 2 bytes before the I²C STOP bit) from the group A ports of the MAX7326 repeatedly returns the port data, followed by the transition flags. As the data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing input ports.

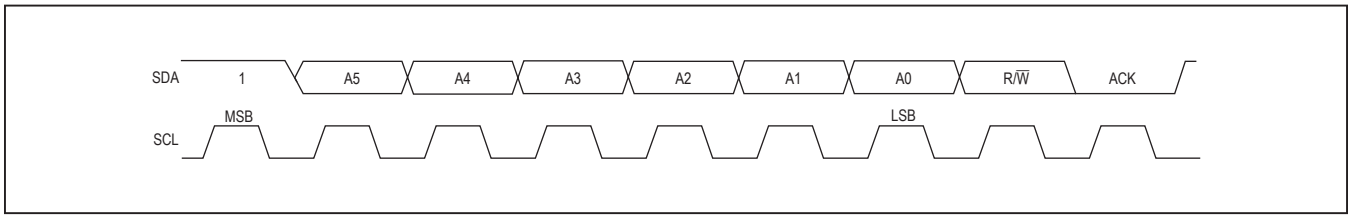


Figure 5. Slave Address

If a port input data change occurs during the read sequence, then $\overline{INT}$ is reasserted during the I²C STOP bit. The MAX7326 does not generate another interrupt during a single-byte or multibyte read.

Input port data is sampled during the preceding I²C acknowledge bit (the acknowledge bit for the I²C slave address in the case of a single-byte or 2-byte read).

A multibyte read (more than 2 bytes before the I²C STOP bit) from the group B ports of the MAX7326 repeatedly returns the status of the eight output ports, read back as inputs.

A **single-byte write** to the group A ports of the MAX7326 sets the logic state of the four I/O ports and the 4-bit interrupt mask register and clears both the internal transition flags and $\overline{INT}$ output when the master acknowledges the slave address byte.

A single-byte write to the output ports of the MAX7326 sets the logic state of all eight ports.

A **multibyte write** to the group A ports of the MAX7326 repeatedly sets the logic state of the four I/O ports and interrupt mask register.

A multibyte write to the group B ports of the MAX7326 repeatedly sets the logic state of all eight ports.

Reading from the MAX7326

A read from the group A ports of the MAX7326 starts with the master transmitting the port group's slave address with the R/$\overline{W}$ bit set to high. The MAX7326 acknowledges the slave address and samples the ports (takes a snapshot) during the acknowledge bit. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The master can then issue a STOP condition after the acknowledge (Figure 6). The snapshot is not taken, and the $\overline{INT}$ status remains unchanged if the master terminates the serial transaction with no acknowledge.

Typically, the master reads 1 or 2 bytes from the MAX7326 with each byte being acknowledged by the master upon reception.

The master can read one byte from the group A ports of the MAX7326 and issue a STOP condition (Figure 6). In this case, the MAX7326 transmits the current port data, clears the transition flags, and resets the transition detection. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The new snapshot data is the current port data transmitted to the master, and therefore, port changes occuring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

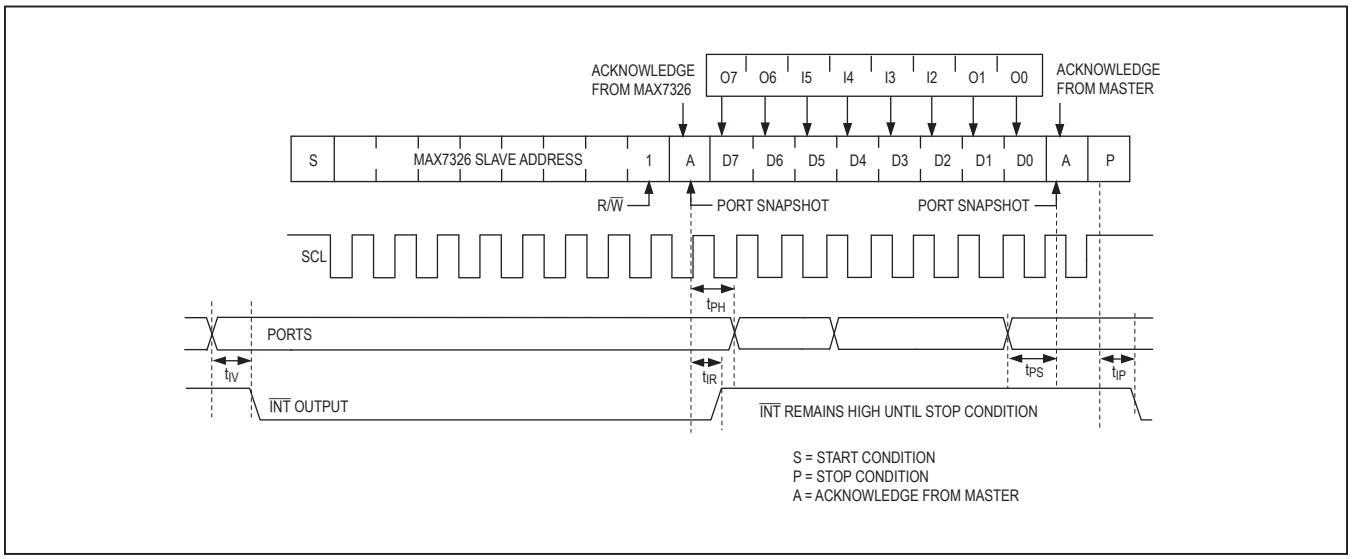


Figure 6. Reading Group A Ports of the MAX7326 (1 Data Byte)

The master can read 2 bytes from the group A ports of the MAX7326 and then issue a STOP condition (Figure 7). In this case, the MAX7326 transmits the current port data, followed by the transition flags. The transition flags are then cleared, and transition detection restarts. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge. The new snapshot data is the current port data transmitted to the master, and therefore, port transitions occuring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

A read from the group B ports of the MAX7326 starts with the master transmitting the group's slave address with the R/$\overline{W}$ bit set high. The MAX7326 acknowledges the slave address and samples the logic state of the output ports during the acknowledge bit. The master can read one or more bytes from the output ports of the MAX7326, and then issue a STOP condition (Figure 8). The MAX7326 transmits the current port data, read back from the actual port outputs (not the port output latches) during the acknowledge bit. If a port is forced to a logic state other than its programmed state, the readback reflects this. If driving a capacitive load, the readback port level verification algorithms may need to take the RC rise/fall time into account.

Typically, the master reads one byte from the group B ports of the MAX7326, then issues a STOP condition (Figure 8). However, the master can read two or more bytes from the output ports of the MAX7326, and then issue a STOP condition. In this case, the MAX7326 resamples the port outputs during each acknowledge and transmits the new data each time.

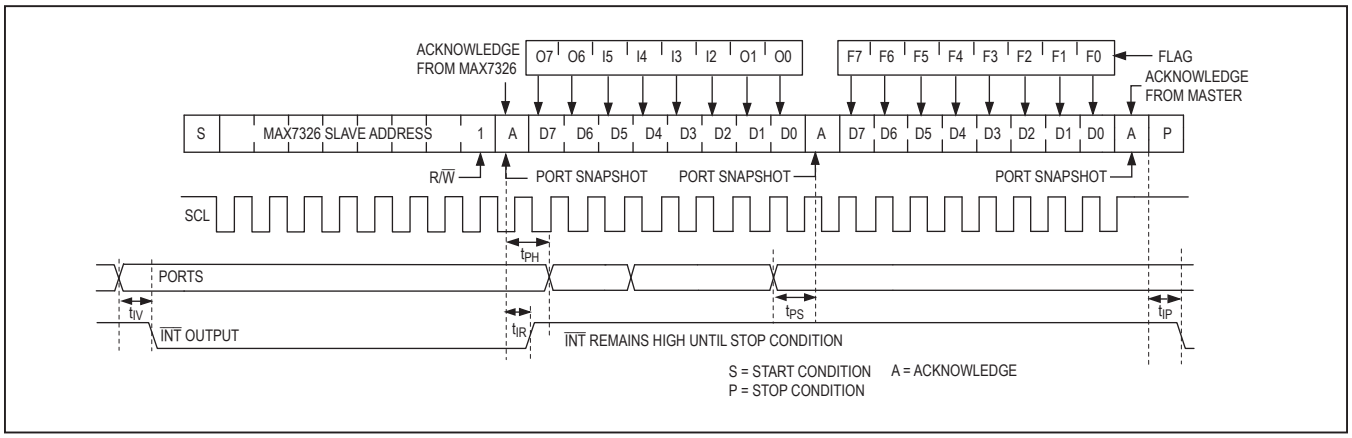


Figure 7. Reading Group A Ports of the MAX7326 (2 Data Bytes)

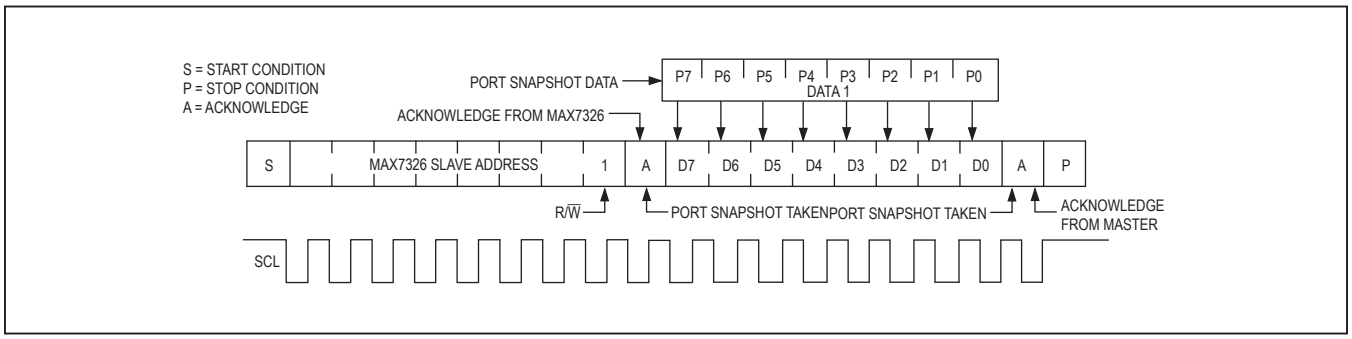


Figure 8. Reading Group B Ports of the MAX7326

Writing to the MAX7326

A write to the group A ports of the MAX7326 starts with the master transmitting the group's slave address with the R/$\overline{W}$ bit set low. The MAX7326 acknowledges the slave address and samples the ports during the acknowledge. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The master can then issue a STOP condition after the acknowledge (Figure 6), but typically the master proceeds to transmit one or more bytes of data. The MAX7326 acknowledges these subsequent bytes of data and updates the four output ports and the 4-bit interrupt mask register with each new byte until the master issues a STOP condition (Figure 9).

A write to the group B ports of the MAX7326 starts with the master transmitting the group's slave address with the R/$\overline{W}$ bit set low. The MAX7326 acknowledges the slave address and samples the ports during the acknowledge bit. The master can now transmit one or more bytes of data. The MAX7326 acknowledges these subsequent bytes of data and updates the corresponding group's ports with each new byte until the master issues a STOP condition (Figure 10).

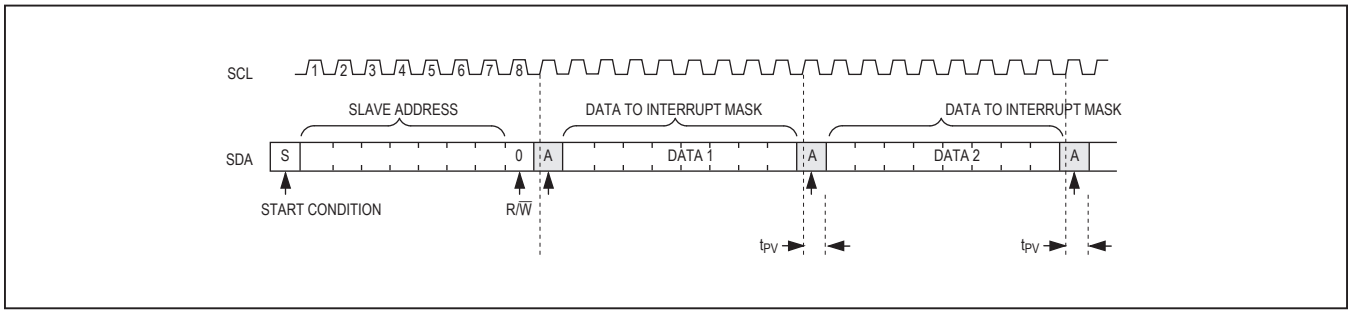


Figure 9. Writing to the Group A Ports of the MAX7326

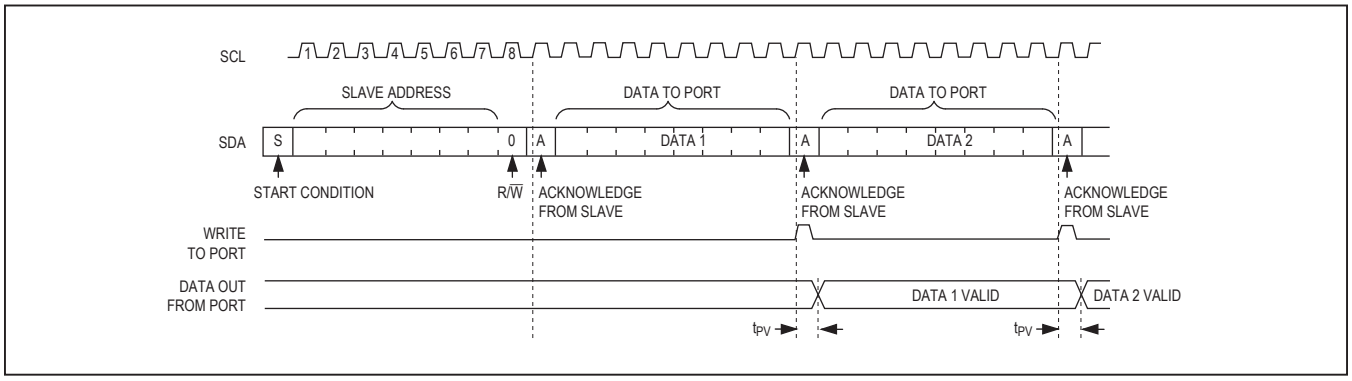


Figure 10. Writing to the Group B Ports of the MAX7326

Applications Information

Port Input and I²C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7326's SDA, SCL, AD0, AD2, $\overline{RST}$, $\overline{INT}$, and I2–I5 are overvoltage protected to +6V, independent of V+. This allows the MAX7326 to operate from a lower supply voltage, such as +3.3V, while the I²C interface and/or any of the four input ports are driven from a higher logic level, such as +5V.

The MAX7326 can operate from a higher supply voltage, such as +3V, while the I²C interface and/or some of the four input ports (I2–I5) are driven from a lower logic level, such as +2.5V. For V+ < 1.8V, apply a minimum voltage of 0.8 x V+ to assert a logic-high on any input. For V+ ≥ 1.8V, apply a voltage of 0.7 x V+ to assert a logic-high. For example, a MAX7326 operating from a +5V supply may not recognize a +3.3V nominal logic-high. One solution for input-level translation is to drive the MAX7326 inputs from open-drain outputs. Use a pullup resistor to V+ or a higher supply to ensure a high logic voltage of greater than 0.7 x V+.

Port Output Signal-Level Translation

Each of the push-pull output ports (O0, O1, and O6–O15) has protection diodes to V+ and GND (Figure 11). When a port output is driven to a voltage higher than V+ or below GND, the appropriate protection diode clamps the output to a diode drop above V+ or below GND. Do not overvolt output ports O0, O1, and O6–O15. When the MAX7326 is powered down (V+ = 0), each output port appears as a diode clamp to GND (Figure 11).

Each of the four input ports ((I2–I5) has a protection diode to GND (Figure 12). When a port input is driven to a voltage lower than GND, the protection diode clamps the output to a diode drop below GND.

Each of the four input ports (I2–I5) also has a 40kΩ (typ) pullup resistor that can be enabled or disabled. When a port input is driven to a voltage higher than V+, the body diode of the pullup enable switch conducts and the 40kΩ pullup resistor is enabled. When the MAX7326 is powered down (V+ = 0), each input port appears as a 40kΩ resistor in series with a diode connected to zero. Input ports are protected to +6V under any of these circumstances (Figure 12).

Driving LED Loads

When driving LEDs from one of the 12 output ports (O0, O1, or O6–O15), a resistor must be fitted in series with the LED to limit the LED current to no more than 20mA. Connect the LED cathode to the MAX7326 port, and the LED anode to V+ through the series current-limiting resistor (R_{LED}). Set the port output low to light the LED.

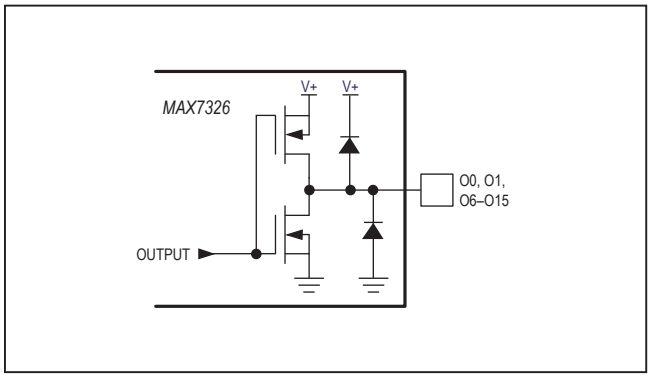


Figure 11. MAX7326 Push-Pull Output Port Structure

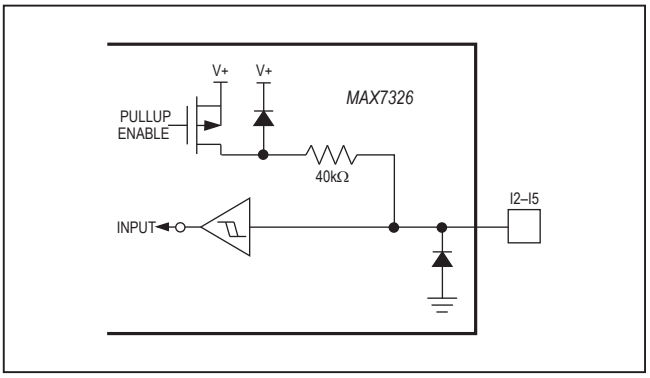


Figure 12. MAX7326 Input Port Structure

Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL})/I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).

V_{SUPPLY} is the supply voltage used to drive the LED (V).

V_{LED} is the forward voltage of the LED (V).

V_{OL} is the output low voltage of the MAX7326 when sinking I_{LED} (V).

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 10mA from a +5V supply:

$$R_{LED} = (5 - 2.2 - 0.1)/0.01 = 270\Omega$$

Driving Load Currents Higher than 20mA

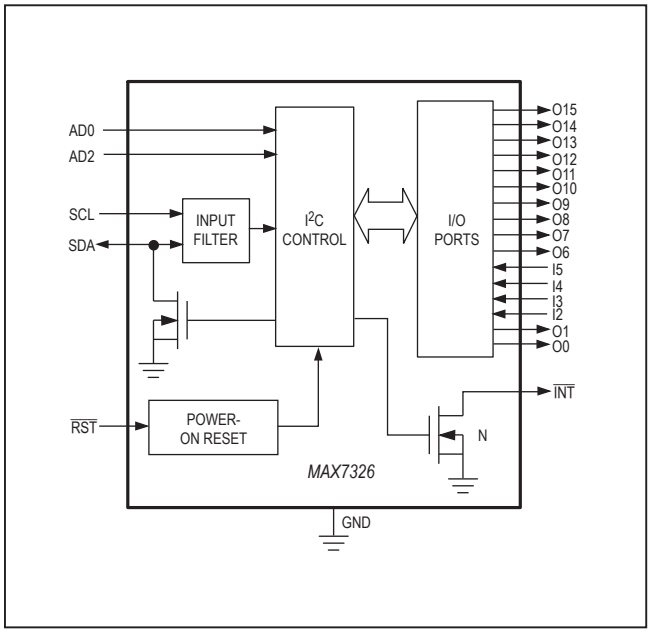
The MAX7326 can be used to drive loads such as relays that draw more than 20mA by paralleling outputs. Use at least one output per 20mA of load current (for example, a 5V, 330mW relay draws 66mA and therefore requires four paralleled outputs). Any combination of outputs can be used as part of a load-sharing design, because any combination of ports can be set or cleared at the same time by writing to the MAX7326. Do not exceed a total sink current of 100mA for the device.

The MAX7326 must be protected from the negative-voltage transient generated when switching off inductive loads (such as relays) by connecting a reverse-biased diode across the inductive load. Choose the peak current for the diode to be greater than the inductive load's operating current.

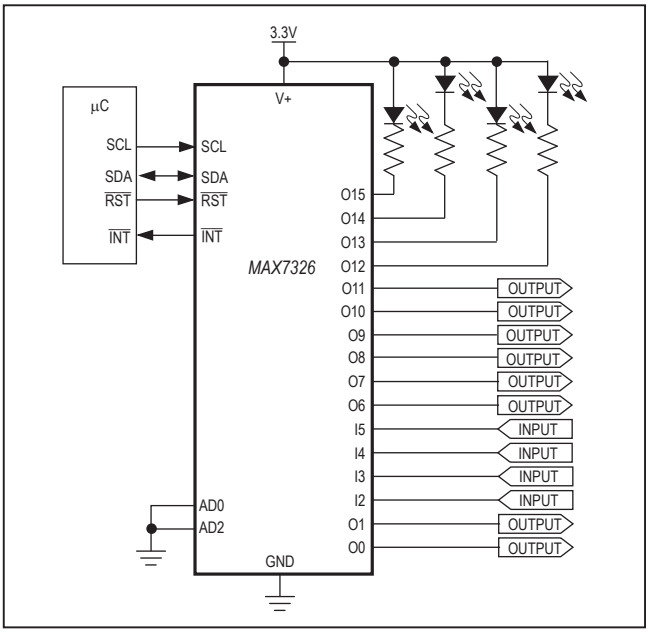
Power-Supply Considerations

The MAX7326 operates with a supply voltage of +1.71V to +5.5V over the -40°C to +125°C temperature range. Bypass the supply to GND with a ceramic capacitor of at least 0.047µF as close as possible to the device. For the TQFN version, additionally connect the exposed pad to GND.

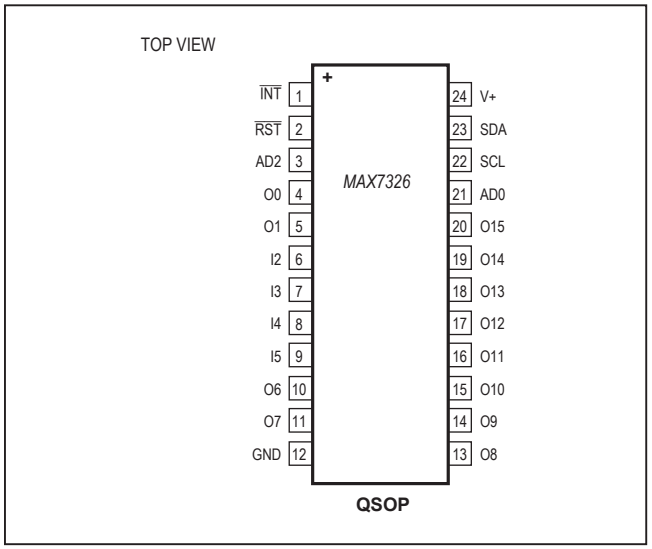
Functional Diagram



Typical Application Circuit



Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 QSOP	E24+1	21-0055	90-0172
24 TQFN	T2444+3	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/06	Initial release	—
1	7/14	No /V OPNs; removed automotive reference from *Applications* section; updated *Package Information*	1, 18–20

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