MAX703/MAX704

Low-Cost Microprocessor Supervisory Circuits with Battery Backup

General Description

The MAX703/MAX704 microprocessor (µP) supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery control functions in µP systems. These devices significantly improve system reliability and accuracy compared to that obtained with separate ICs or discrete components.

The MAX703/MAX704 are available in 8-pin DIP and SO packages and provide four functions:

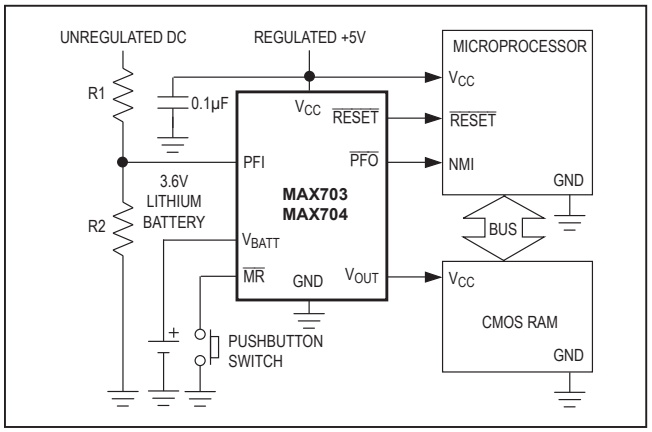
1) An active-low reset during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µPs, or other low-power logic circuitry.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual reset input.

The MAX703 and MAX704 differ only in their supplyvoltage monitor levels. The MAX703 generates a reset when the supply drops below 4.65V, while the MAX704 generates a reset below 4.40V.

Applications

- Computers
- Controllers
- Intelligent Instruments
- Critical µP Power Monitoring

Typical Operating Circuit



Features

- Battery-Backup Power Switching
- Precision Supply-Voltage Monitor
  - 4.65V (MAX703)
  - 4.40V (MAX704)
- 200ms Reset Pulse Width
- Debounced TTL/CMOS-Compatible Manual Reset Input
- 200µA Quiescent Current
- 50nA Quiescent Current in Battery-Backup Mode
- Voltage Monitor for Power-Fail or Low-Battery Warning
- 8-Pin DIP and SO Packages
- Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V

Ordering Information

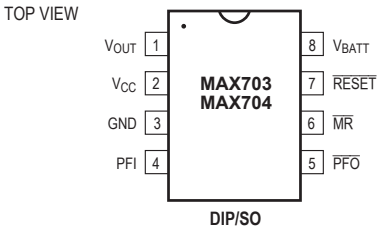
PART	TEMP RANGE	PIN-PACKAGE
MAX703C/D	0°C to +70°C	Dice*
MAX703CPA	0°C to +70°C	8 PDIP
MAX703CSA	0°C to +70°C	8 SO
MAX703EPA	-40°C to +85°C	8 PDIP
MAX703ESA	-40°C to +85°C	8 SO
MAX703MJA	-55°C to +125°C	8 CERDIP**
MAX704C/D	0°C to +70°C	Dice*
MAX704CPA	0°C to +70°C	8 PDIP
MAX704CSA	0°C to +70°C	8 SO
MAX704EPA	-40°C to +85°C	8 PDIP
MAX704ESA	-40°C to +85°C	8 SO
MAX704MJA	-55°C to +125°C	8 CERDIP**

**Dice are tested at T_A = +25°C only.*

***Contact factory for availability and processing to MIL-STD-883.*

Devices in PDIP and SO packages are available in both leaded and lead(Pb)-free packaging. Specify lead(Pb)-free by adding the "+" symbol at the end of the part number when ordering. Lead(Pb)-free not available for CERDIP package.

Pin Configuration



maxim integrated™

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6.0V
- V_{BATT} ..... -0.3V to +6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CB} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for Up to 10s
- All Other Outputs 20mA

Rate-of-Rise V_{BATT}, V_{CC} 100V/µs

Operating Temperature Range
- C Suffix ..... 0°C to +70°C
- E Suffix ..... -40°C to +85°C
- M Suffix ..... -55°C to +125°C

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin PDIP (derated 9.09mW/°C above +70°C) 727mW
- 8-Pin SO (derated 5.88mW/°C above +70°C) 471mW
- 8-Pin CERDIP (derated 8.00mW/°C above +85°C) 640mW

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1: V_{CB} is the greater of V_{CC} and V_{BATT}. The input voltage limits on PFI and $\overline{MR}$ may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +4.75V to +5.5V for MAX703, V_{CC} = +4.5V to +5.5V for MAX704, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, V_{BATT}		(Note 2)		0		5.5	V
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX70_C			200	350	µA
		MAX70_E/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
VBATT Standby Current (Note 3)		5.5V > V_{CC} > V_{BATT} + 0.2V	T_A = +25°C	-0.10		+0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.00		+0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05	V_{CC} - 0.025		V
		I_{OUT} = 50mA		V_{CC} - 0.5	V_{CC} - 0.25		
VOUT in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Battery Switch Threshold (V_{CC} - V_{BATT})		V_{CC} < V_{RST}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV
$\overline{RESET}$ Threshold	V_{RST}	MAX703		4.50	4.65	4.75	V
		MAX704		4.25	4.40	4.50	
$\overline{RESET}$ Threshold Hysteresis					40		mV
$\overline{RESET}$ Pulse Width	t_{RST}			140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA		V_{CC} - 1.5			V
	V_{OL}	I_{SINK} = 3.2mA				0.4	
		MAX70_C, V_{CC} = 1V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 50µA				0.3	
		MAX70_E/M, V_{CC} = 1.2V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 100µA				0.3	

Electrical Characteristics (continued)

(V_{CC} = +4.75V to +5.5V for MAX703, V_{CC} = +4.5V to +5.5V for MAX704, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

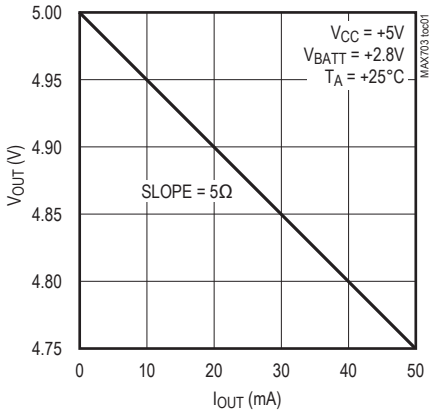
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Input Threshold	V_{IL}	Low			0.8	V
	V_{IH}	High	2.0			
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ to $\overline{RESET}$ Delay	t_{MD}				250	ns
$\overline{MR}$ Pullup Current		$\overline{MR}$ = 0V	100	250	600	µA
PFI Input Threshold		V_{CC} = 5V	1.20	1.25	1.30	V
PFI Input Current			-25	+0.01	+25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA	V_{CC} - 1.5			V
	V_{OL}	I_{SINK} = 3.2mA			0.4	

Note 2: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.
Note 3: "-" = battery-charging current, "+" = battery-discharging current.

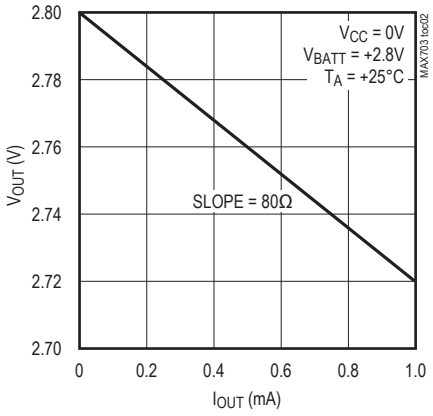
Typical Operating Characteristics

(V_{CC} = +5V, V_{BATT} = 2.8V, T_A = +25°C, unless otherwise noted.)

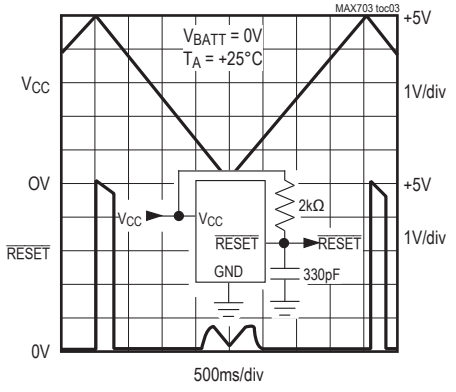
OUTPUT VOLTAGE vs. LOAD CURRENT



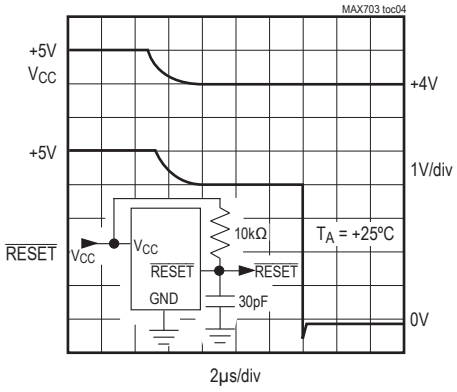
OUTPUT VOLTAGE vs. LOAD CURRENT



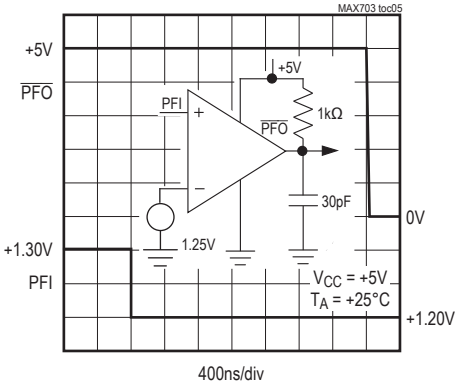
MAX703 $\overline{RESET}$ OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



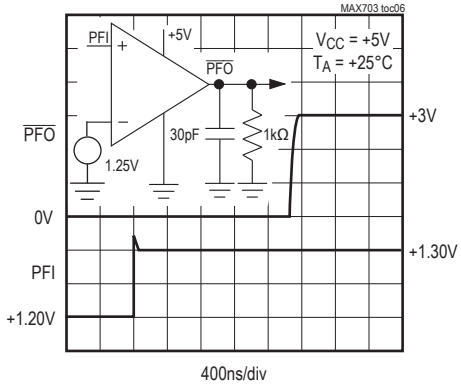
MAX703 $\overline{RESET}$ RESPONSE TIME



POWER-FAIL COMPARATOR RESPONSE TIME



POWER-FAIL COMPARATOR RESPONSE TIME



Pin Description

PIN	NAME	FUNCTION
1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a p-channel MOSFET switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or V_{BATT} is connected to V_{OUT}.
2	V_{CC}	+5V Supply Input
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Comparator Output. It goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ remains high.
6	$\overline{MR}$	Manual Reset Input. Generates a reset pulse when pulled below 0.8V. This active-low input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250µA pullup current. Leave floating when not used.
7	$\overline{RESET}$	Reset Output. Remains low while V_{CC} is below the reset threshold (4.65V for the MAX703, 4.40V for the MAX704). It remains low for 200ms after V_{CC} rises above the reset threshold (Figure 2) or $\overline{MR}$ goes from low to high.
8	V_{BATT}	Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} is switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises 20mV above V_{BATT}, V_{CC} is switched to V_{OUT}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

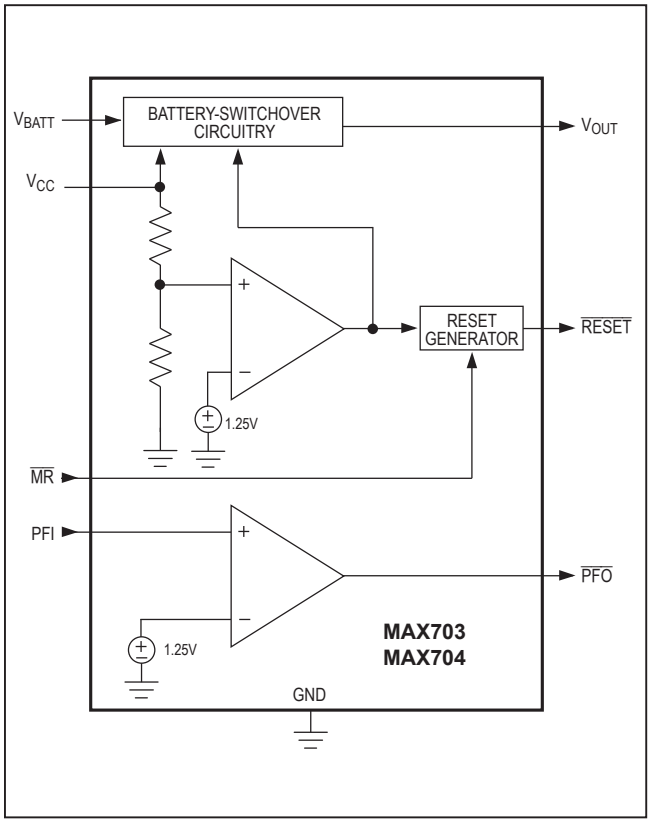


Figure 1. Block Diagram

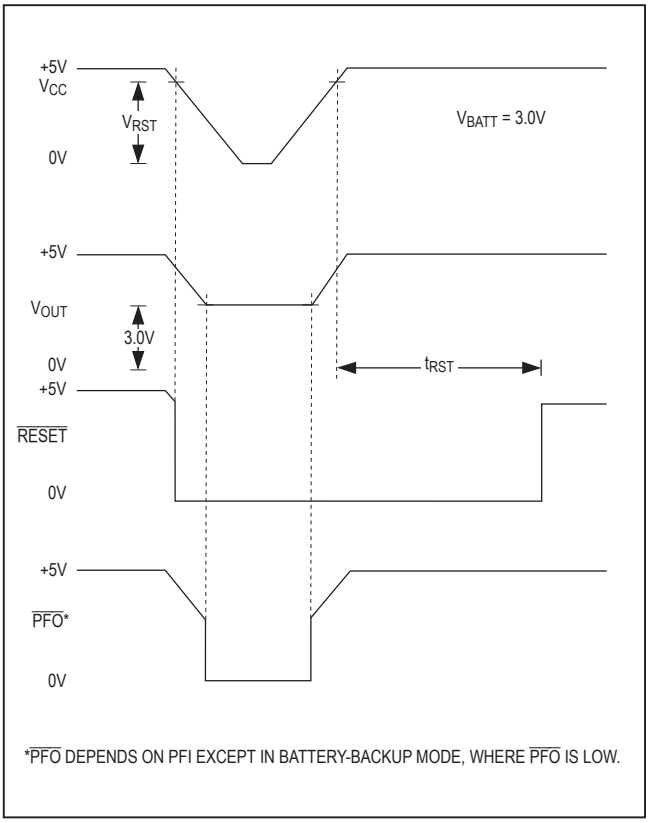


Figure 2. Timing Diagram

Detailed Description

$\overline{\text{RESET}}$ Output

A µP's reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX703/MAX704 assert reset when V_{CC} is low, preventing code-execution errors during power-up, power-down, or brownout conditions.

When V_{BATT} is 2V or more, $\overline{\text{RESET}}$ is always valid, irrespective of V_{CC}. On power-up, as V_{CC} rises, $\overline{\text{RESET}}$ remains low. When V_{CC} exceeds the reset threshold, an internal timer holds $\overline{\text{RESET}}$ low for a time equal to the reset pulse width (typically 200ms); after this interval, $\overline{\text{RESET}}$ goes high (Figure 2). If a power-fail or brownout condition occurs (i.e., V_{CC} drops below the reset threshold), $\overline{\text{RESET}}$ is asserted. As long as V_{CC} remains below the reset threshold, the internal timer is continually restarted, causing the $\overline{\text{RESET}}$ output to remain low. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the end of the last interruption.

Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. The power-fail comparator can be used as an undervoltage detector to signal a failing power supply. In the *Typical Operating Circuit*, an external voltage-divider at PFI is used to monitor the unregulated DC voltage from which the regulated +5V supply is derived.

The voltage-divider can be chosen so the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{\text{PFO}}$ is then used as an interrupt to prepare the µP for power-down.

To conserve power, the power-fail comparator is turned off and $\overline{\text{PFO}}$ is forced low when the MAX703/MAX704 enter battery-backup mode.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the MAX703/MAX704 automatically switch RAM to backup power when V_{CC} fails.

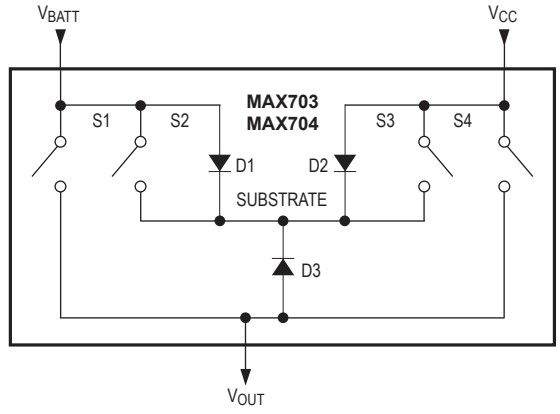
As long as V_{CC} exceeds the reset threshold, V_{CC} connects to V_{OUT} through a 5Ω p-channel MOSFET power switch. Once V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ goes low and V_{CC} or V_{BATT} (whichever is higher) switches to V_{OUT}. Note that V_{BATT} switches to V_{OUT} through an 80Ω switch only if V_{CC} is below the resetthreshold voltage **and** V_{BATT} is greater than V_{CC}. When V_{CC} exceeds the reset threshold, it is connected to the MAX703/MAX704 substrate, regardless of the voltage applied to V_{BATT} (Figure 3). During this time, diode D1 (between V_{BATT} and the substrate) conducts current from V_{BATT} to V_{CC} if $V_{BATT} \geq (V_{CC} + 0.6V)$.

When the battery-backup mode is activated, V_{BATT} connects to V_{OUT}. In this mode, the substrate connects to V_{BATT} and internal circuitry is powered from the battery (Figure 3). Table 1 shows the status of the MAX703/MAX704 inputs and outputs in battery-backup mode.

When V_{CC} is below, but within, 1V of V_{BATT}, the internal switchover comparator draws about 30µA. Once V_{CC}

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}.
V_{OUT}	Connected to V_{BATT} through an internal 80Ω p-channel MOSFET switch.
V_{BATT}	Connected to V_{OUT}. Supply current is < 1µA when V_{CC} < (V_{BATT} - 1V).
$\overline{\text{RESET}}$	Logic-low.
PFI	Power-fail comparator is disabled.
$\overline{\text{PFO}}$	Logic-low.
$\overline{\text{MR}}$	Disabled.



CONDITION	S1/S2	S1/S2
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

Figure 3. Battery-Switchover Block Diagram

drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Manual Reset

The manual reset input ($\overline{MR}$) allows $\overline{RESET}$ to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. Because it is TTL/CMOS compatible, $\overline{MR}$ can be driven by an external logic line.

Applications Information

Using a Supercap as a Backup Power Source

Supercaps are capacitors with extremely high capacitance values (on the order of 0.1 Farad). When using supercaps, if V_{CC} exceeds the MAX703/MAX704 reset thresholds (4.65V and 4.40V, respectively), V_{BATT} may not exceed V_{CC} by more than 0.6V. Thus, with a 5% tolerance on V_{CC}, V_{BATT} should not exceed V_{CC} (min) + 0.6V = 5.35V. Similarly, with a 10% tolerance on V_{CC}, V_{BATT} should not exceed 5.1V.

Figure 4's supercap circuit uses the MAX703 with a ±5% tolerance voltage supply. In this circuit, the supercap rapidly charges to within a diode drop of V_{CC}. However, the diode leakage current with trickle charge the supercap voltage to V_{CC}. If V_{BATT} = 5.25V and the power is suddenly removed and then reapplied with V_{CC} = 4.75V, V_{BATT} - V_{CC} does not exceed the allowable 0.6V difference voltage.

Figure 5's circuit uses the MAX704 with a ±10% tolerance voltage supply. Note that if V_{CC} = 5.5V and V_{BATT} ≤ 5.1V, the power can be suddenly removed and reapplied with V_{CC} = 4.5V, and V_{BATT} - V_{CC} will not exceed the allowable 0.6V voltage difference.

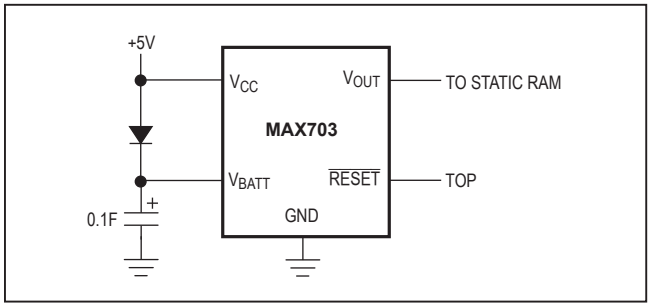


Figure 4. Using a Supercap as a Backup Power Source with a MAX703 and a +5V ±5% Supply

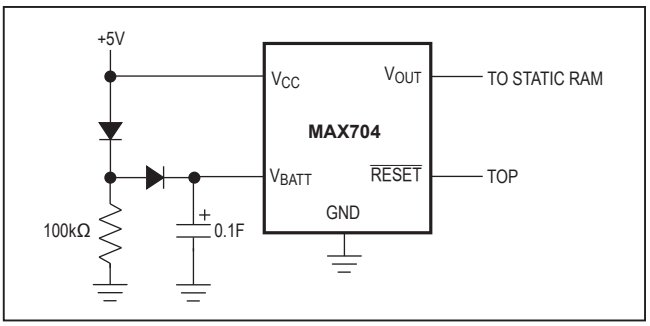


Figure 5. Using a Supercap as a Backup Power Source with the MAX704 and a +5V ±10% Supply

Batteries and Power Supplies as Backup Power Sources

Lithium batteries work well as backup batteries because they have very low self-discharge rates and high-energy density. Single lithium batteries with opencircuit voltages of 3.0V to 3.6V are ideal for use with the MAX703/MAX704. Batteries with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be directly connected to the MAX703/MAX704 V_{BATT} input with no additional circuitry (see the *Typical Operating Circuit*).

However, batteries with open-circuit voltages greater than the reset threshold plus 0.3V **cannot** be used as backup batteries, since they source current into the substrate through diode D1 (Figure 3) when V_{CC} is close to the reset threshold.

Table 2. Allowable Backup-Battery Voltages

PART	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX703	4.80
MAX704	4.55

Using the MAX703/MAX704 without a Backup Power Source

If a backup power source is not used, ground V_{BATT} and connect V_{CC} to V_{OUT}. A direct connection to V_{CC} eliminates any voltage drop across the internal switch, which would otherwise appear at V_{OUT}. Alternatively, use the MAX705–MAX708, which do not have batterybackup capabilities.

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX703/MAX704 $\overline{\text{RESET}}$ output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pulldown resistor is added to the $\overline{\text{RESET}}$ pin as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding $\overline{\text{RESET}}$ low. Resistor value R1 is not critical. It should be about 100kΩ, which is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

Replacing the Backup Battery

The backup battery can be removed while V_{CC} remains valid without triggering a reset. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered. This is an improvement on switchover ICs that initiate a reset when V_{CC} and V_{BATT} are at or near the same voltage level (regardless of the reset threshold voltage). If the voltage on the unconnected V_{BATT} pin floats up toward V_{CC}, this condition alone cannot initiate a reset when using the MAX703/MAX704.

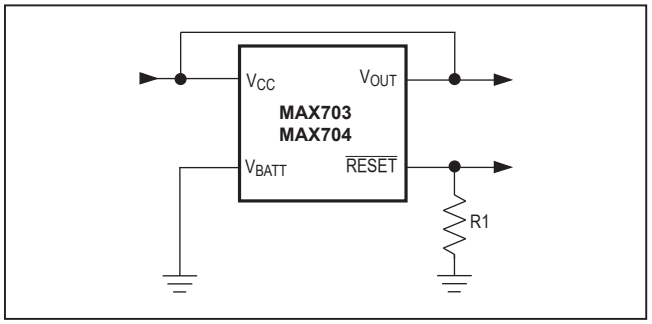


Figure 6. $\overline{\text{RESET}}$ Valid to Ground Circuit

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{\text{PFO}}$ when V_{IN} is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 so that PFI sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{\text{PFO}}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 8's circuit. When the negative supply is valid, $\overline{\text{PFO}}$ is low. When the negative supply voltage droops, $\overline{\text{PFO}}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

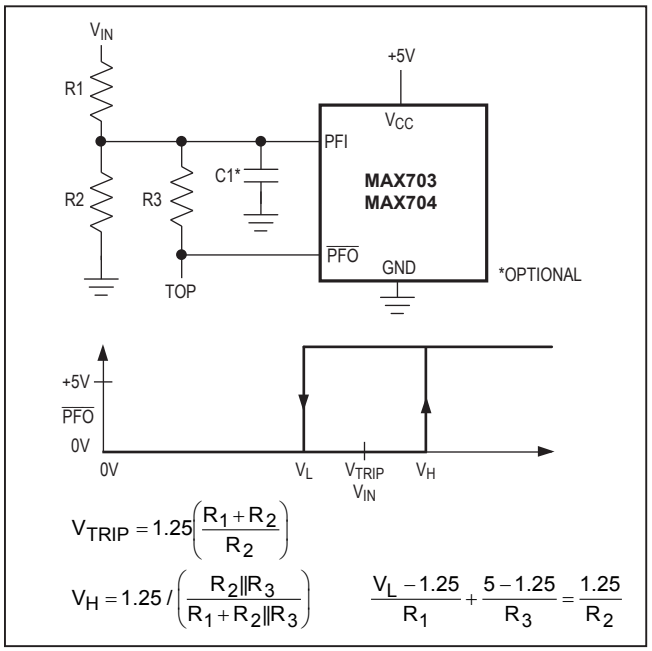


Figure 7. Adding Hysteresis to the Power-Fail Comparator

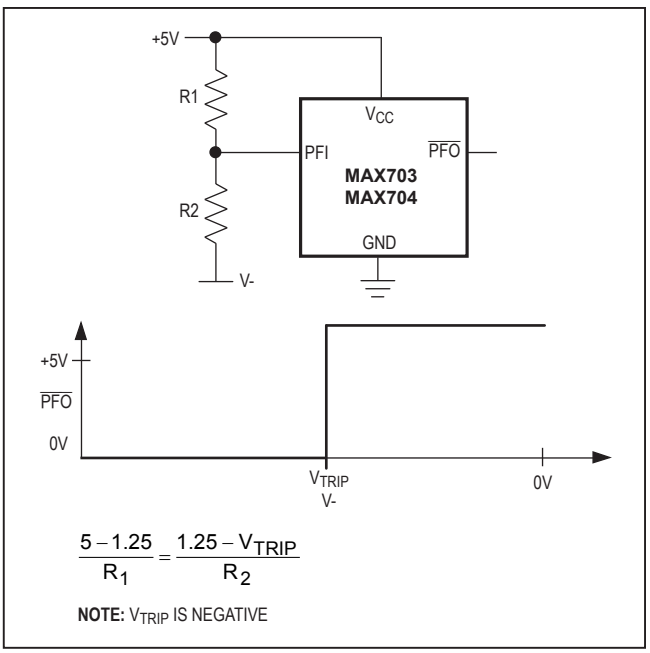


Figure 8. Monitoring a Negative Voltage

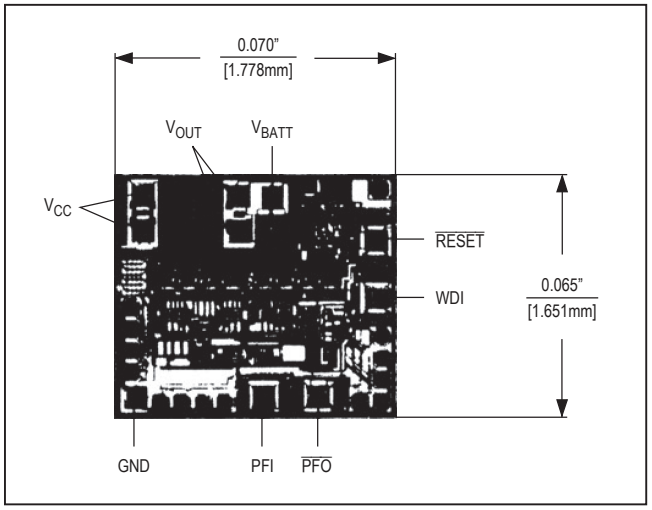
Using the Power-Fail Comparator to Assert Reset

In addition to asserting reset at the V_{CC} reset threshold voltage, reset can also be asserted at the PFI input threshold voltage. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a reset pulse when the monitored supply drops below a user-specified threshold or when V_{CC} falls below the reset threshold. For additional noise rejection, place a capacitor between PFI and GND.

Table 3. Maxim Microprocessor Supervisory Products

PART	NOMINAL RESET THRESHOLD (V)	MINIMUM RESET PULSE WIDTH (ms)	NOMINAL WATCH-DOG TIMEOUT PERIOD (s)	BACKUP-BATTERY SWITCH	$\overline{CE}$ WRITE PROTECT	POWER-FAIL COMPARATOR	MANUAL RESET INPUT	WATCH-DOG INPUT	LOW-LINE OUTPUT	ACTIVE-HIGH RESET	BATT ON OUTPUT
MAX690A	4.65	140	1.6	Yes	No	Yes	No	No	No	No	No
MAX691A	4.65	140/Adj.	1.6/Adj.	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
MAX692A	4.40	140	1.6	Yes	No	Yes	No	No	No	No	No
MAX693A	4.40	140/Adj.	1.6/Adj.	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
MAX696	Adj.	35/Adj.	1.6/Adj.	Yes	No	Yes	No	Yes	Yes	Yes	Yes
MAX697	Adj.	35/Adj.	1.6/Adj.	No	Yes	Yes	No	Yes	Yes	Yes	No
MAX700	4.65/Adj.	200	—	No	No	No	Yes	No	No	Yes	No
MAX703	4.65	140	—	Yes	No	Yes	Yes	No	No	No	No
MAX704	4.40	140	—	Yes	No	Yes	Yes	No	No	No	No
MAX705	4.65	140	1.6	No	No	Yes	Yes	Yes	No	No	No
MAX706	4.40	140	1.6	No	No	Yes	Yes	Yes	No	No	No
MAX707	4.65	140	—	No	No	Yes	Yes	No	No	Yes	No
MAX708	4.40	140	—	No	No	Yes	Yes	No	No	Yes	No
MAX791	4.65	140	1.0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MAX1232	4.50/4.75	250	0.15/ 0.60/1.2	No	No	No	Yes	No	No	Yes	No
MAX1259	—	—	—	Yes	No	Yes	No	No	No	No	No

Chip Topography



SUBSTRATE MUST BE LEFT UNCONNECTED

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP	P8+1	21-0043	—
8 SO	S8+2	21-0041	90-0096
8 CERDIP	J8+2	21-0045	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	5/14	Removed “Automotive Systems” from the *Applications* section	1

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