MAX5112

9-Channel, 14-Bit, Current DAC with I²C Interface

General Description

The MAX5112 is a 14-bit, 9-channel, current-output digital-to-analog converter (DAC). The device operates from a low +3.0V power supply and provides 14-bit performance without any adjustment.

The device's output ranges are optimized to bias a high-power tunable laser source. Each of the 9 channels provides a current source. Channels 1 and 2 provide 10mA current. An internal multiplexer switches the outputs of each channel to one of four external nodes. Channel 3 provides a selectable current of 2mA or 20mA. Channel 4 provides 90mA. Channel 5 provides 180mA. Channel 6 provides a selectable current of -60mA or +300mA. Channel 7 provides 90mA. Channels 8 and 9 provide a selectable current of 15mA or 35mA. Connect DAC outputs in parallel to obtain additional current or to achieve higher resolution. The device contains an internal reference.

An I²C-compatible interface drives the device with clock rates of up to 400kHz. An active-high asynchronous CLR input resets DAC codes to zero independent of the serial interface. The device provides a separate power-supply input for driving the interface logic.

The MAX5112 is specified over the -40°C to +105°C temperature range, and is available in 3mm x 3mm, 36-bump WLP and 5mm x 5mm, 32-pin TQFN packages.

Features

- **Low 3.0V Supply**
- **Integrated Multiplexers for Outputs 1 and 2**
- **Increased Current or Resolution with Outputs Connected in Parallel**
- **I²C-Compatible Serial Interface**
- **Internal Reference**
- **Overtemperature Protection**
- **-40°C to +105°C Temperature Range**
- **Available in 36-Bump WLP or 32-Pin TQFN Packages**

Applications

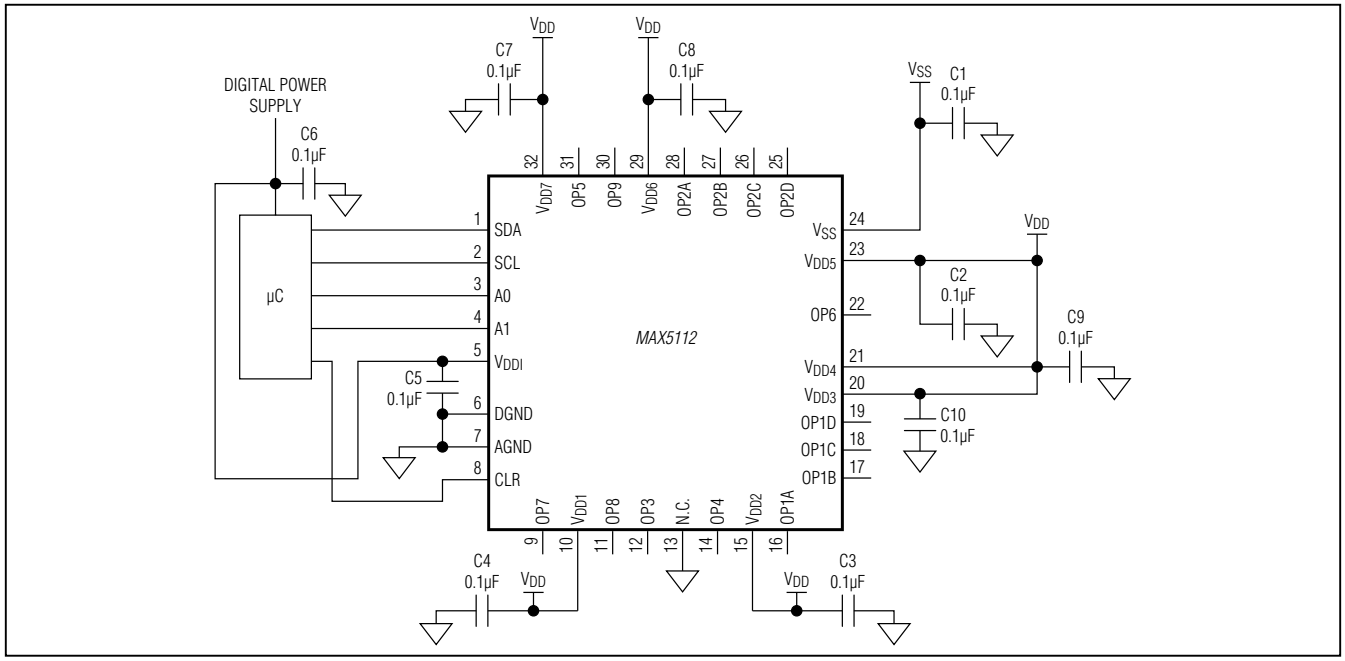
Tunable Laser Diode Biasing

Ordering Information

PART	INTERFACE	PIN-PACKAGE
MAX5112GWX+T	I²C	36 WLP
MAX5112GTJ+	I²C	32 TQFN-EP*

Note: *All devices are specified over the -40°C to +105°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6060; Rev 2; 5/13

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +4.0V
V_{SS} to AGND .....-6.0V to +0.3V
V_{DDI} to AGND .....-0.3V to +6.0V
OP6 to AGND.....the higher of (V_{DD} - 9V), (V_{SS} - 0.3V) and -6.0V to the lower of (V_{DD} + 0.3V) and +4.0V
OP1 to OP5 and OP7, OP8, OP9 to AGND...-0.3V to the lower of (V_{DD} + 0.3V) and +4.0V
A1 to DGND .... -0.3V to the lower of (V_{DDIO} + 0.3V) and +6.0V
N.C. to AGND.....-0.3V to the lower of (V_{DD} + 0.3V) and +4.0V
Digital I/Os to DGND.....-0.3V to +6.0V
AGND to DGND .....-0.3V to +0.3V
All Other Pins to AGND.....-0.3V to +4.0V
Continuous Power Dissipation (T_A = +70°C)
WLP (derate at 26.3mW/°C above +70°C)..... 2104mW
TQFN (derate at 34.5mW/°C above +70°C).....2758mW
Maximum Current Into Any Pin 380mA
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (TQFN only, soldering 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....1.7°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....38°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.6V to +3.3V, V_{SS} = -4.75V to -5.46V, V_{DDI} = +1.8V to +5.25V, AGND = DGND, T_A = -40°C to +105°C, V_{OP1}–V_{OP5} = V_{OP6} sourcing = V_{OP7}, V_{OP8}, and V_{OP9} = V_{DD} - 1V, V_{OP6} sinking = V_{SS} + 1V. Typical specifications at V_{DD} = 3.0V, V_{SS} = -5.2V, T_A = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			14			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic			±0.5	±1.0	LSB
Integral Nonlinearity	INL	OP1 to OP6 source, OP7, OP8, OP9			±2	±8	LSB
		OP6 sink			±8		
Full-Scale Output	I_{MAX}	OP1 and OP2			10		mA
		OP3	2mA FS range		2		
			20mA FS range		20		
		OP4			90		
		OP5			180		
		OP6 current source			300		
		OP6 current sink			-60		
		OP7			90		
		OP8 and OP9	15mA FS range		15		
			35mA FS range		35		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.6V to +3.3V, V_{SS} = -4.75V to -5.46V, V_{DDI} = +1.8V to +5.25V, AGND = DGND, T_A = -40°C to +105°C, V_{OP1}–V_{OP5} = V_{OP6} sourcing = V_{OP7}, V_{OP8}, and V_{OP9} = V_{DD} - 1V, V_{OP6} sinking = V_{SS} + 1V. Typical specifications at V_{DD} = 3.0V, V_{SS} = -5.2V, T_A = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Offset Error (Note 3)	OE	OP1 and OP2		-120	-60	0	µA
		OP3	2mA FS range	-24	-12	0	
			20mA FS range	-240	-120	0	
		OP4		-1080	-540	0	
		OP5		-2160	-1080	0	
		OP6 current source		-3600	-1800	0	
		OP6 current sink		0	360	720	
		OP7		-1080	-540	0	
		OP8 and OP9	15mA FS range	-180	-90	0	
			35mA FS range	-420	-210	0	
Offset Error Tempco (Note 4)	OETC	OP1 and OP2				±250	nA/°C
		OP3	2mA FS range			±50	
			20mA FS range			±500	
		OP4				±2250	
		OP5				±4500	
		OP6 current source				±7500	
		OP6 current sink				±1500	
		OP7				±2250	
		OP8 and OP9	15mA FS range			±375	
			35mA FS range			±875	
Ideal Gain	I_{GAIN}				$I_{MAX}/2^{14}$		mA/LSB
Gain Error (Note 3)	GE	All but OP3, 2mA and OP6 sink				±1.3	%FS
		OP3, 2mA				±1.5	
		OP6 sink				±5	
Gain Error Tempco (Note 4)	GETC	All but OP6 sink				±50	ppm/°C
		OP6 sink			±15		
Output Compliance Range	V_{OR}	All but OP6 sink		V_{GND}		V_{DD} - 1	V
		OP6 sink		V_{SS} + 1		V_{DD}	
DYNAMIC PERFORMANCE							
Output Resistance	R_{OUT}	OP1 and OP2			2		MΩ
		OP3	2mA FS range		10		
			20mA FS range		1		
		OP4			0.2		
		OP5			0.1		
		OP6 current source			0.06		
		OP6 current sink			0.04		
		OP7			0.2		
		OP8 and OP9	15mA FS range		1.3		
			35mA FS range		0.56		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.6V to +3.3V, V_{SS} = -4.75V to -5.46V, V_{DDI} = +1.8V to +5.25V, AGND = DGND, T_A = -40°C to +105°C, V_{OP1}–V_{OP5} = V_{OP6} sourcing = V_{OP7}, V_{OP8}, and V_{OP9} = V_{DD} - 1V, V_{OP6} sinking = V_{SS} + 1V. Typical specifications at V_{DD} = 3.0V, V_{SS} = -5.2V, T_A = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Output Slew Rate	SR	OP1 and OP2			5		mA/µs
		OP3	2mA FS range		1		
			20mA FS range		10		
		OP4			45		
		OP5			90		
		OP6 current source			150		
		OP6 current sink			30		
		OP7			45		
		OP8 and OP9	15mA FS range		7.5		
			35mA FS range		17.5		
Output Settling Time	t_{OS}	t_O ±0.1%			15		µs
Noise at Full Scale (10kHz)	INO	OP1 and OP2			1.6		nA/√Hz
		OP3	2mA FS range		0.4		
			20mA FS range		3.4		
		OP4			16		
		OP5			31		
		OP6 current source			56		
		OP6 current sink			11		
		OP7			16		
		OP8 and OP9	15mA FS range		2.8		
			35mA FS range		6.5		
DAC Glitch Impulse Major-Carry Transition	IOGE	OP1 and OP2			60		pC
		OP3, 20mA			120		
		OP4			540		
		OP5			1080		
		OP6 current source			1800		
		OP6 current sink			360		
		OP7			540		
		OP8 and OP9	15mA FS range		90		
			35mA FS range		210		
DAC Output GND Switch Resistance	R_{GSW}	At 0.7V				50	Ω
DAC Output GND Switch Current	I_{GSW}	At 0.7V		14			mA
OVERTEMPERATURE DETECTORS							
Overtemperature Disable Threshold	T_{OVTD}				+160		°C
Overtemperature Warning Threshold	T_{OVTW}				+150		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.6V to +3.3V, V_{SS} = -4.75V to -5.46V, V_{DDI} = +1.8V to +5.25V, AGND = DGND, T_A = -40°C to +105°C, V_{OP1}–V_{OP5} = V_{OP6} sourcing = V_{OP7}, V_{OP8}, and V_{OP9} = V_{DD} - 1V, V_{OP6} sinking = V_{SS} + 1V. Typical specifications at V_{DD} = 3.0V, V_{SS} = -5.2V, T_A = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Power-Supply Range	V_{DD}		2.6		3.3	V
Interface Power-Supply Range	V_{DDI}		1.8		5.25	V
Negative Supply Range	V_{SS}		-5.46	-5.2	-4.75	V
Supply Current	I_{DD}	No load, no input/output		500	600	µA
Negative Supply Current	I_{SS}		-20	-11		µA
POWER-ON RESET (POR)						
POR Threshold	V_{POR}			1.6		V
POR Threshold Hysteresis	V_{PORH}			0.025		V
DIGITAL INPUT CHARACTERISTICS (SDA, SCL, A1, A0)						
Input Low Voltage	V_{IL}	V_{DDI} = 2.2V to 5.25V			0.3 x V_{DDI}	V
		V_{DDI} = 1.8V to 2.2V			0.2 x V_{DDI}	
Input High Voltage	V_{IH}	V_{DDI} = 2.2V to 5.25V	0.7 x V_{DDI}			V
		V_{DDI} = 1.8V to 2.2V	0.8 x V_{DDI}			
Input Hysteresis	V_{HYS}			250		mV
Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}	Input = 0V or V_{DDI}			±10	µA
DIGITAL OUTPUT CHARACTERISTICS (SDA)						
SDA Output Low Voltage	V_{OL}	V_{DDI} = 2.2V to 5.5V, I_{SINK} = 3mA			0.4	V
		V_{DDI} = 1.8V to 2.2V, I_{SINK} = 3mA			0.2 x V_{DDI}	
TIMING CHARACTERISTICS (Note 5)						
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time for a Repeated START Condition	$t_{HD:STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}	V_{DDI} = 2.2V to 5.25V	1.3			µs
		V_{DDI} = 1.8V to 2.2V	1.9			
SCL Pulse Width High	t_{HIGH}	V_{DDI} = 2.2V to 5.25V	0.6			µs
		V_{DDI} = 1.8V to 2.2V	0.8			
Setup Time for Repeated Start Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	V_{DDI} = 2.2V to 5.25V	0		900	ns
		V_{DDI} = 1.8V to 2.2V	0		1100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.6V to +3.3V, V_{SS} = -4.75V to -5.46V, V_{DDI} = +1.8V to +5.25V, AGND = DGND, T_A = -40°C to +105°C, V_{OP1}–V_{OP5} = V_{OP6} sourcing = V_{OP7}, V_{OP8}, and V_{OP9} = V_{DD} - 1V, V_{OP6} sinking = V_{SS} + 1V. Typical specifications at V_{DD} = 3.0V, V_{SS} = -5.2V, T_A = +25°C. Specifications apply to all DACs and outputs, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU:DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R		20 + (C_B/10)		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + (C_B/10)		300	ns
SDA Transmitting Fall Time	t_F		20 + (C_B/10)		250	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Bus Capacitance Allowed	C_b		10		400	pF
Pulse Width of Suppressed Spike	t_{SP}			50		ns
CLR Removal Time Prior to a Recognized START	t_{CLRSTA}	Applies to DACs in reset mode only	100			ns
CLR Pulse-Width High	t_{CLRPW}	No DAC is in shutter or gate mode	40			ns
		Any DAC is in shutter or gate mode (Note 6)	4			µs

Note 2: Specifications are 100% production tested at $T_A \geq$ +25°C. Specifications for $T_A <$ +25°C are guaranteed by design.

Note 3: Configuration register write operation required following power-up for output offset adjustment. See the *DAC Outputs* section in the *Detailed Description*. All gain and offset errors include the effect of the internal reference and are guaranteed over temperature. Gain error = (measured gain - I_{GAIN})/I_{GAIN}. Measured gain = (code 16383 DAC output - code 500 DAC output)/15883. Offset error = code 500 DAC output - (500 x measured gain).

Note 4: Guaranteed by design and characterization. Not production tested. All gain and offset temperature coefficients include the effect of the internal reference. Temperature coefficients are calculated by the "box" method. Refer to Application Note 4300: *Calculating the Error Budget in Precision Digital-to-Analog Converter (DAC) Applications* for additional information.

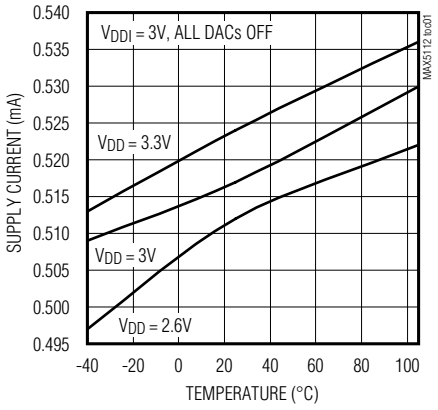
Note 5: Timing characteristics are tested and guaranteed with digital input conditions at V_{IH} = V_{DDI} and V_{IL} = 0V. For V_{DDI} > 2.2V, I²C fast-mode specifications are met. Reduced SCL clock rate for V_{DDI} < 2.2V.

Note 6: Minimum pulse width required to realize functionally useful DAC transitions. Not production tested. See the Shutter Mode Settling Time Down and Shutter Mode Settling Time Up graphs in the *Typical Operating Characteristics* section.

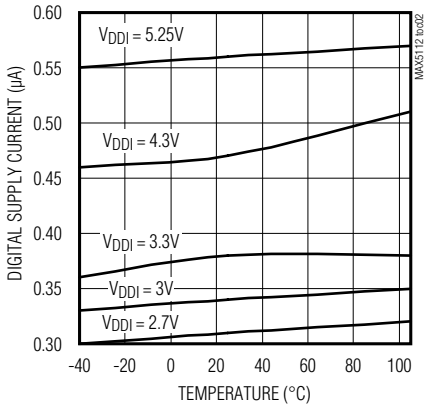
Typical Operating Characteristics

(V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

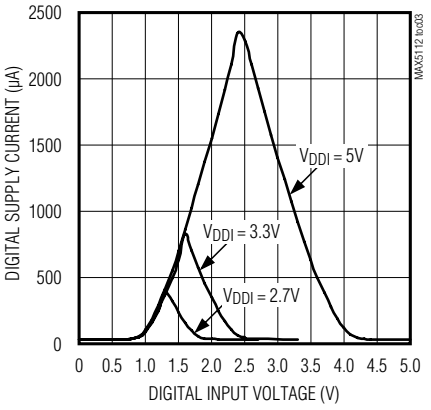
ANALOG SUPPLY CURRENT vs. TEMPERATURE



DIGITAL SUPPLY CURRENT vs. TEMPERATURE



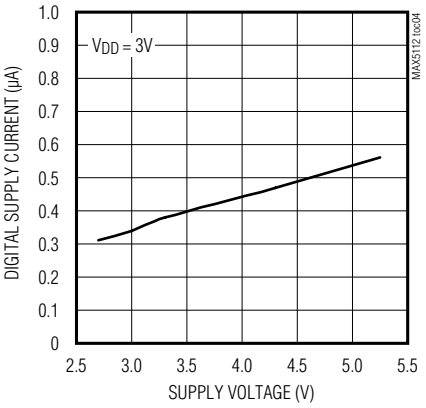
DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



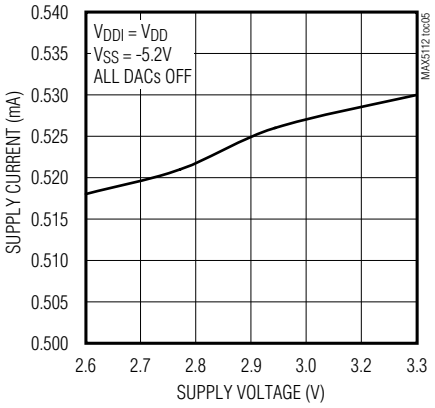
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

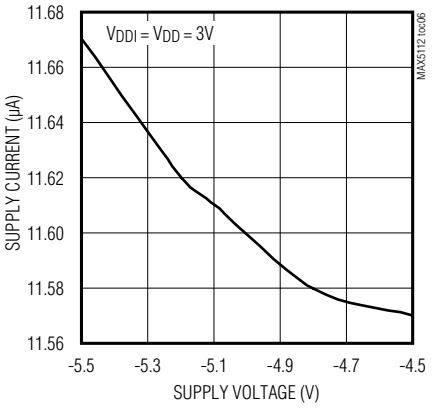
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



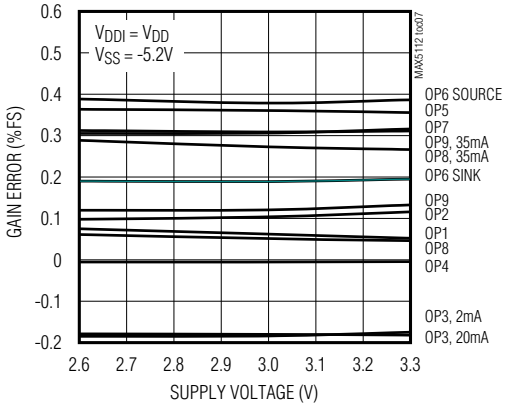
POSITIVE ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



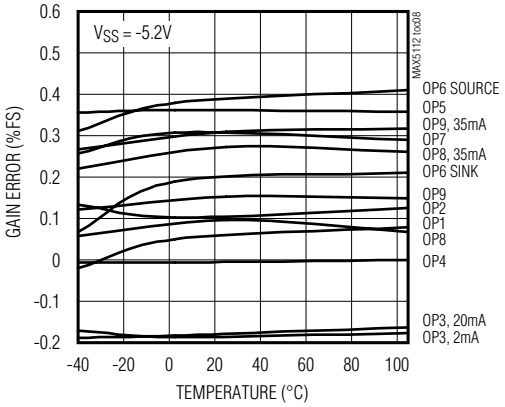
NEGATIVE ANALOG SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE



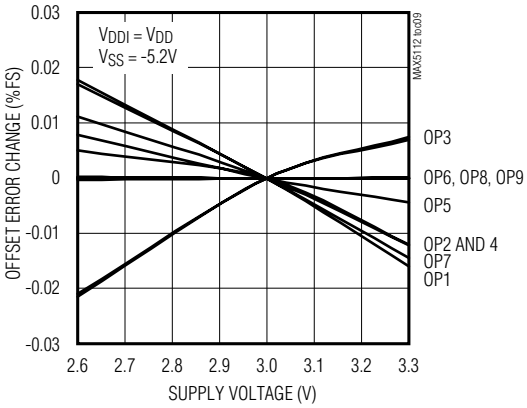
GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



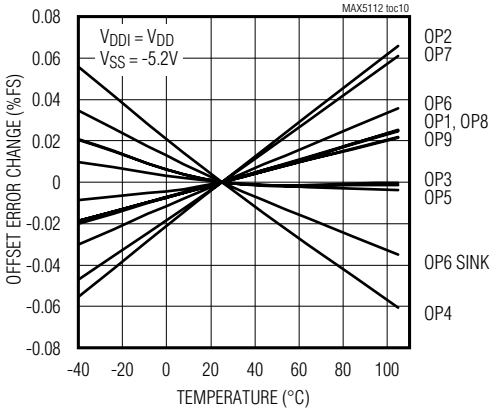
GAIN ERROR vs. TEMPERATURE



OFFSET ERROR CHANGE vs. ANALOG SUPPLY VOLTAGE



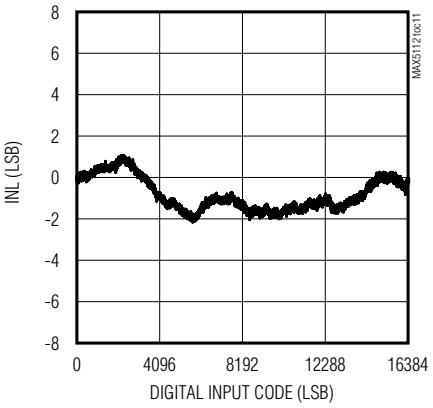
OFFSET ERROR CHANGE vs. TEMPERATURE



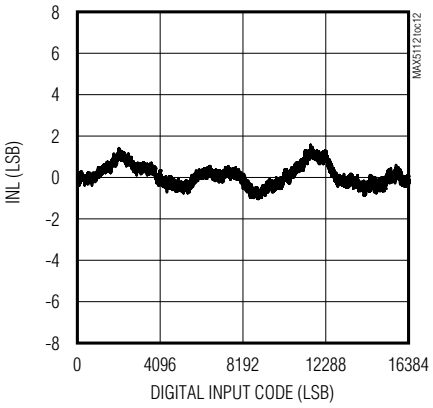
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

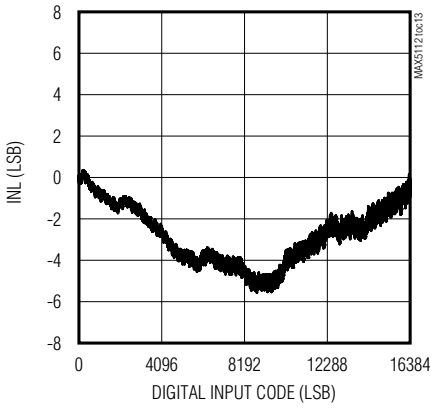
OP4 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



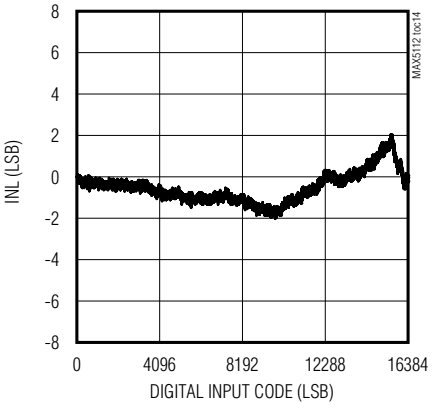
OP3, 2mA INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



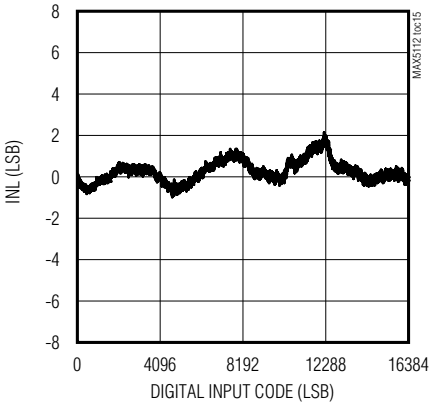
OP6 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



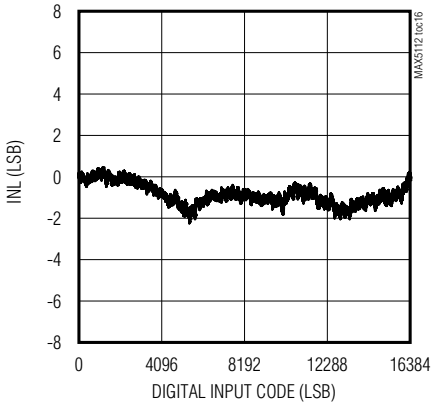
OP5 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



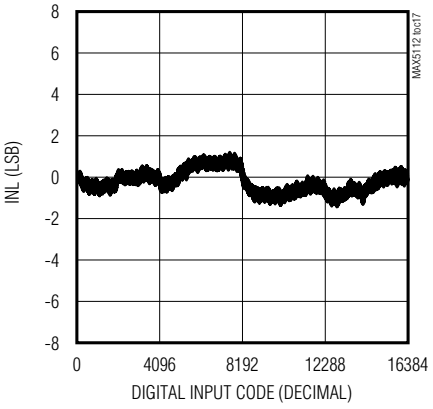
OP1 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



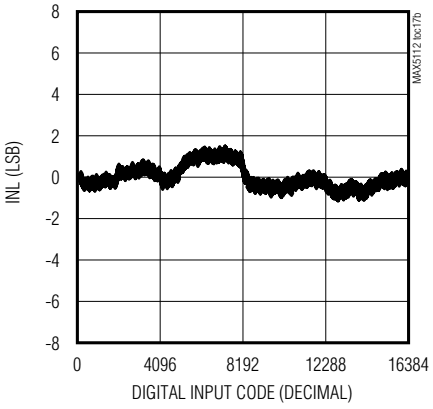
OP2 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



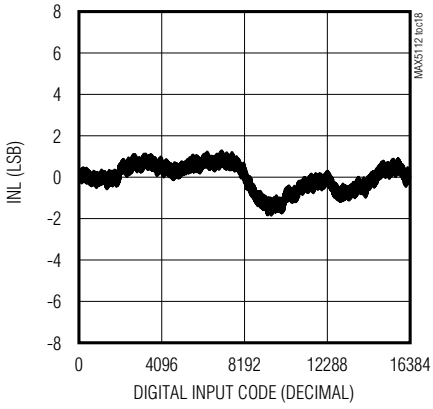
OP9, 15mA INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



OP9, 35mA INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



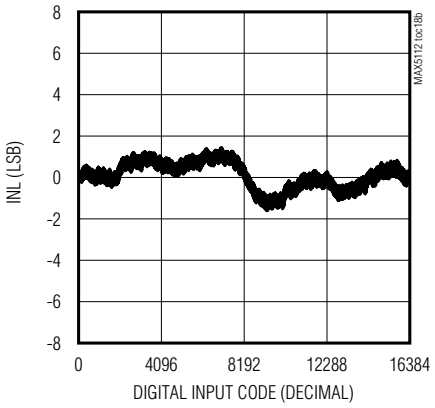
OP8, 15mA INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



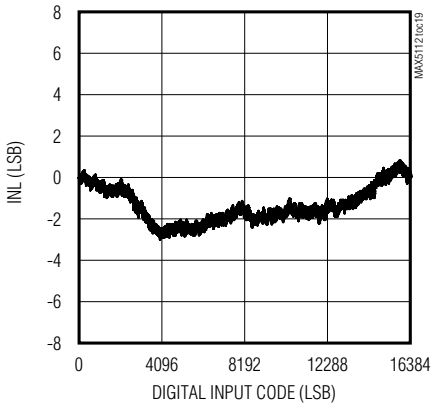
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

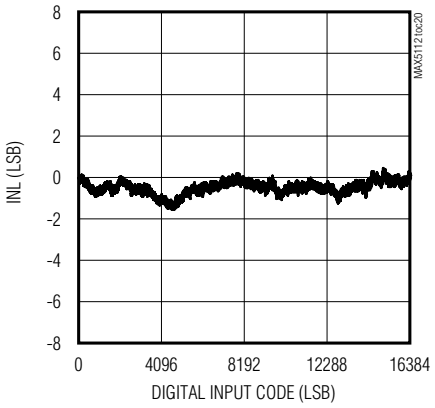
OP8, 35mA INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



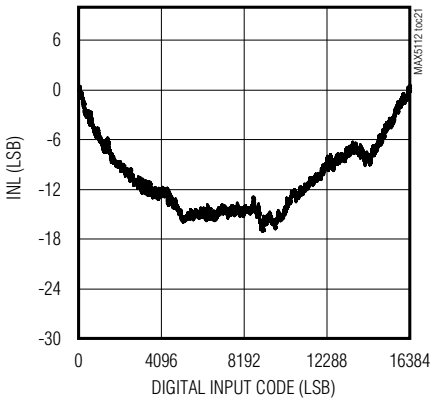
OP7 INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



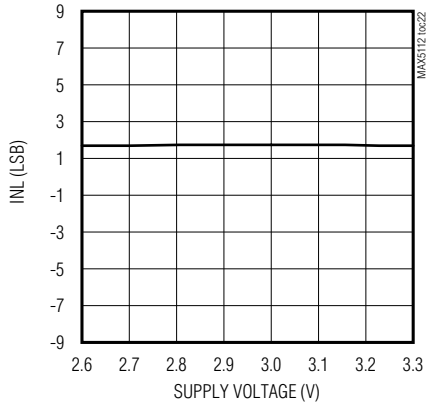
OP3, 20mA INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



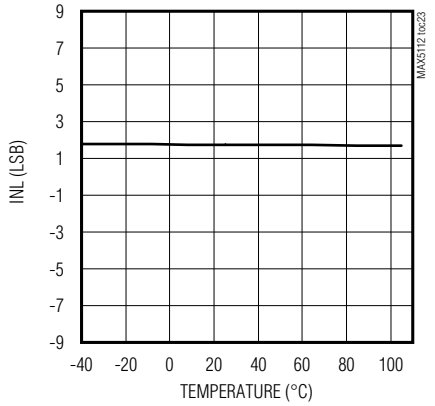
OP6 SINK INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



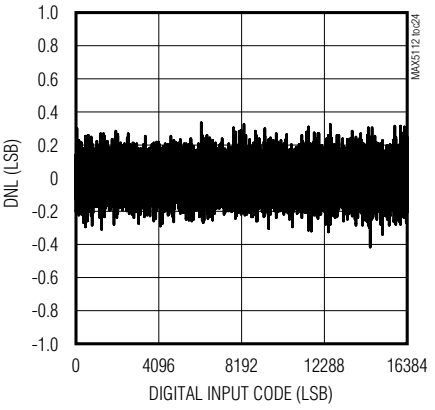
INTEGRAL NONLINEARITY vs. ANALOG SUPPLY VOLTAGE



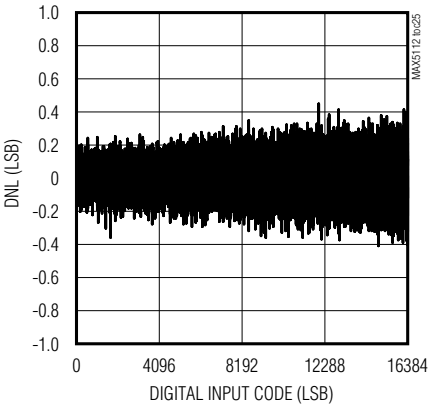
INTEGRAL NONLINEARITY vs. TEMPERATURE



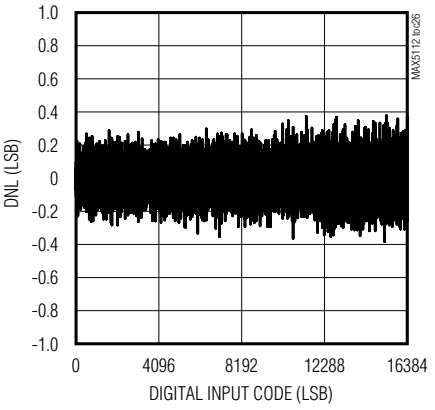
OP4 DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



OP6 DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



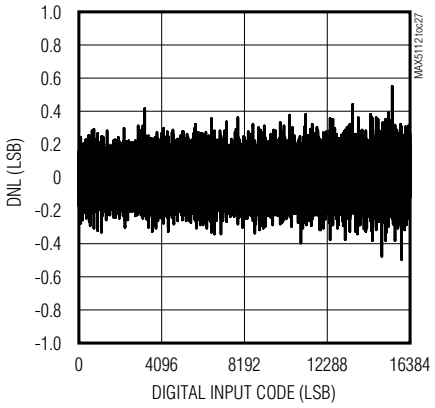
OP1 DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



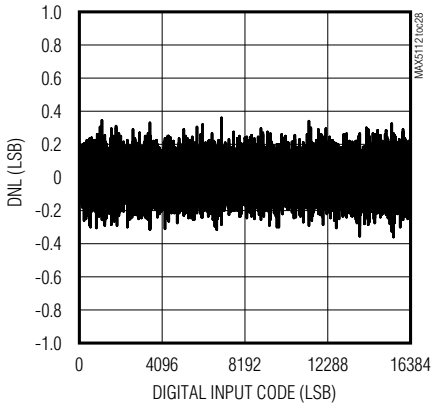
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

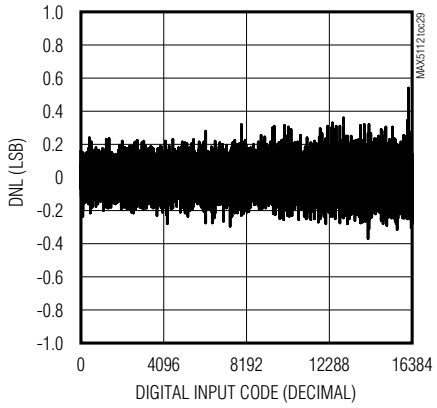
OP3, 2mA DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



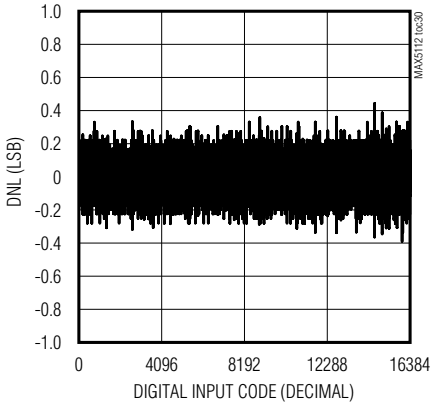
OP5 DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



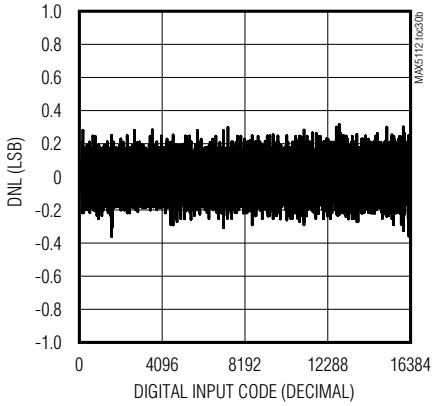
OP2 DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



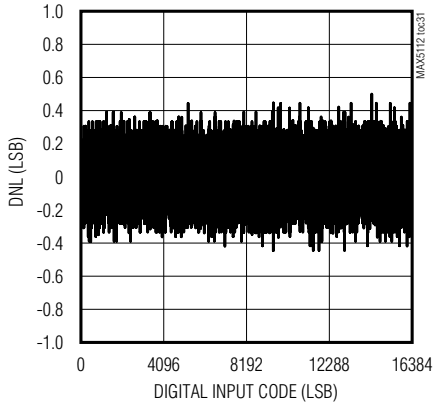
OP9, 15mA DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



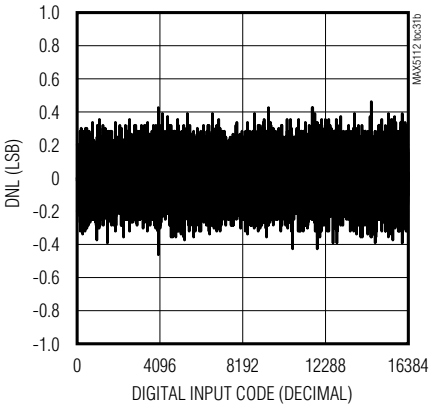
OP9, 35mA DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



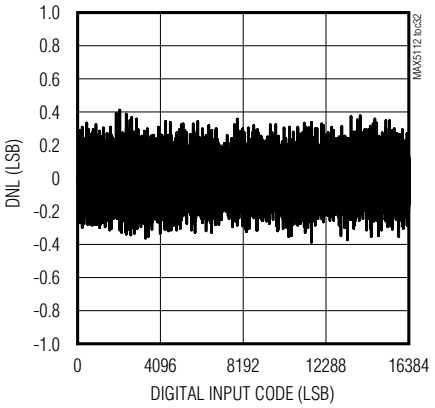
OP8, 15mA DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



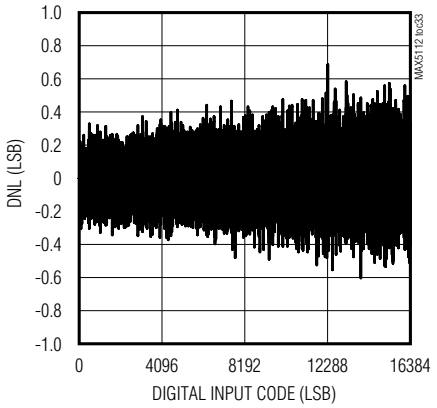
OP8, 35mA DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



OP7 DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



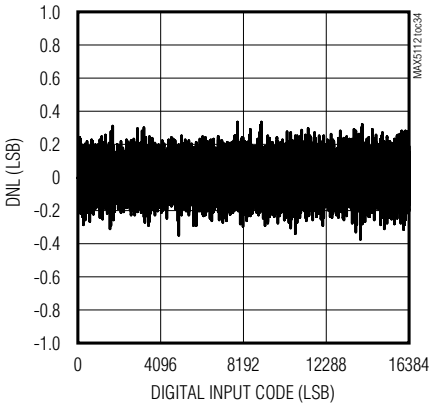
OP6 SINK DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



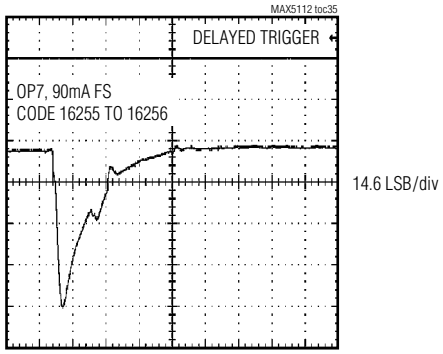
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

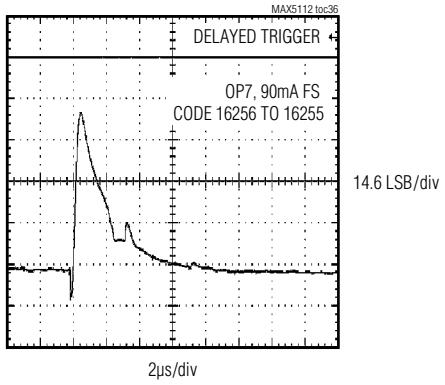
OP3, 20mA DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



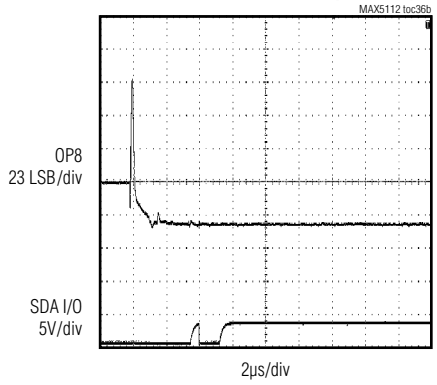
LOW-TO-HIGH MAJOR CODE TRANSITION OUTPUT TRANSIENT



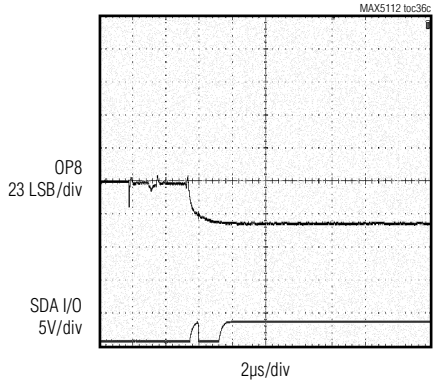
HIGH-TO-LOW MAJOR CODE TRANSITION OUTPUT TRANSIENT



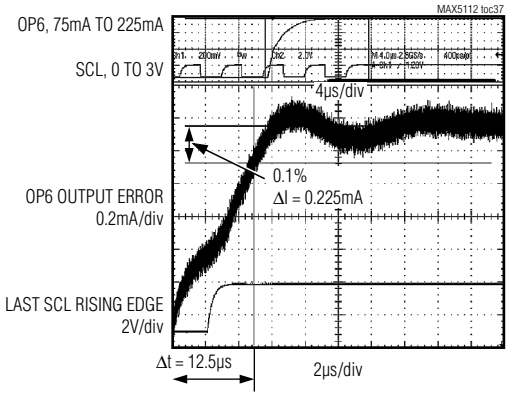
MULTICODE TRANSITION TRANSIENT OP8 CODE 9690 TO 9630 (T/H OFF)



MULTICODE TRANSITION TRANSIENT OP8 CODE 9690 TO 9630 (T/H ON)



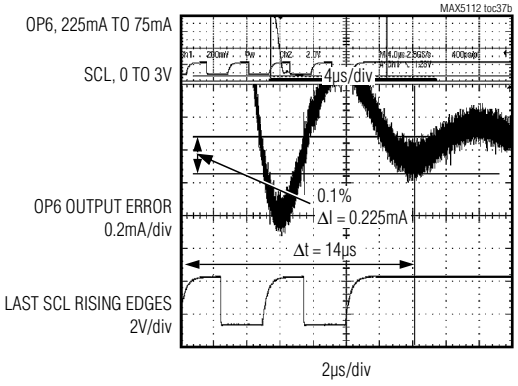
OUTPUT 6 LOW TO HIGH CODE 0.1% SETTLING TIME



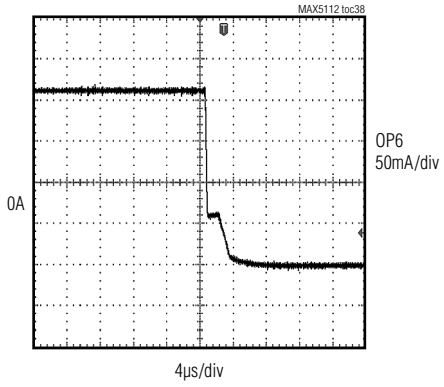
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

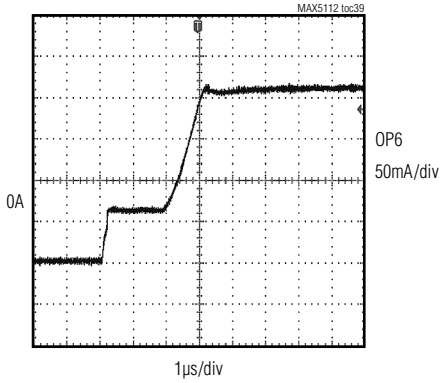
OUTPUT6 HIGH TO LOW CODE 0.1% SETTLING TIME



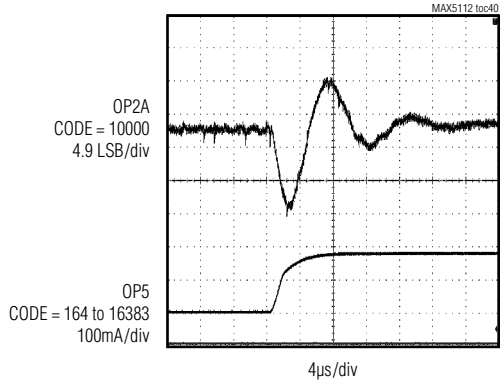
SHUTTER MODE SETTLING TIME DOWN



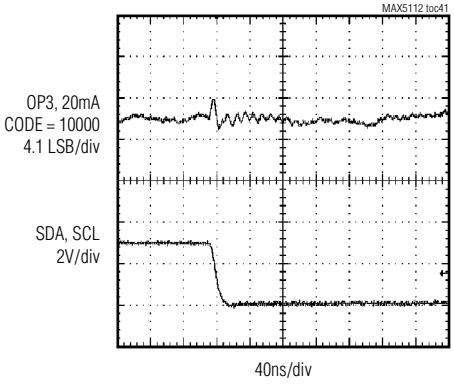
SHUTTER MODE SETTLING TIME UP



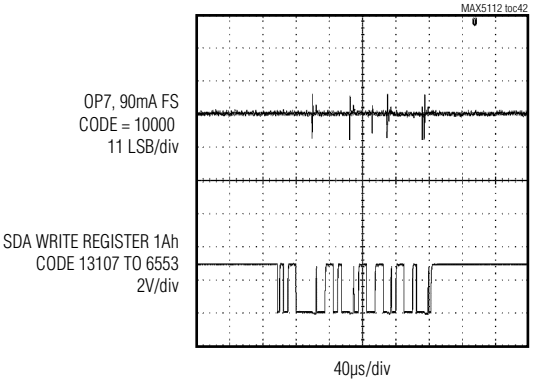
CHANNEL-TO-CHANNEL ANALOG CROSSTALK



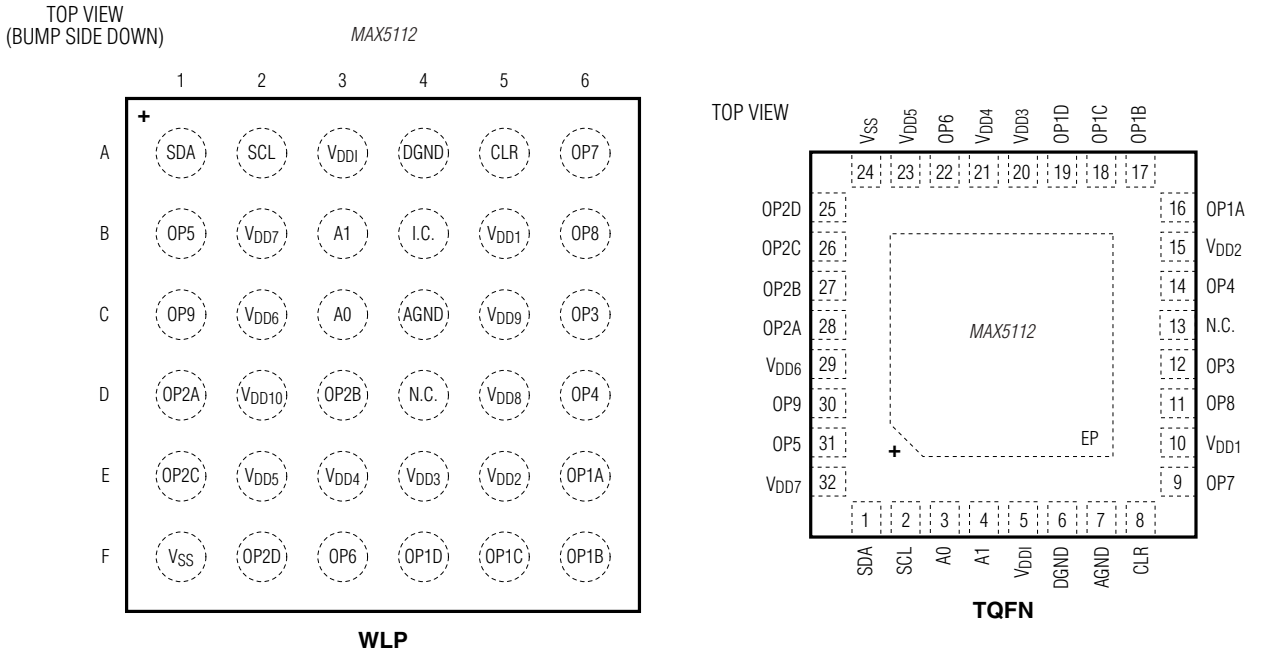
INTERFACE FEEDTHROUGH



COMMAND SEQUENCE FEEDTHROUGH



Pin Configurations



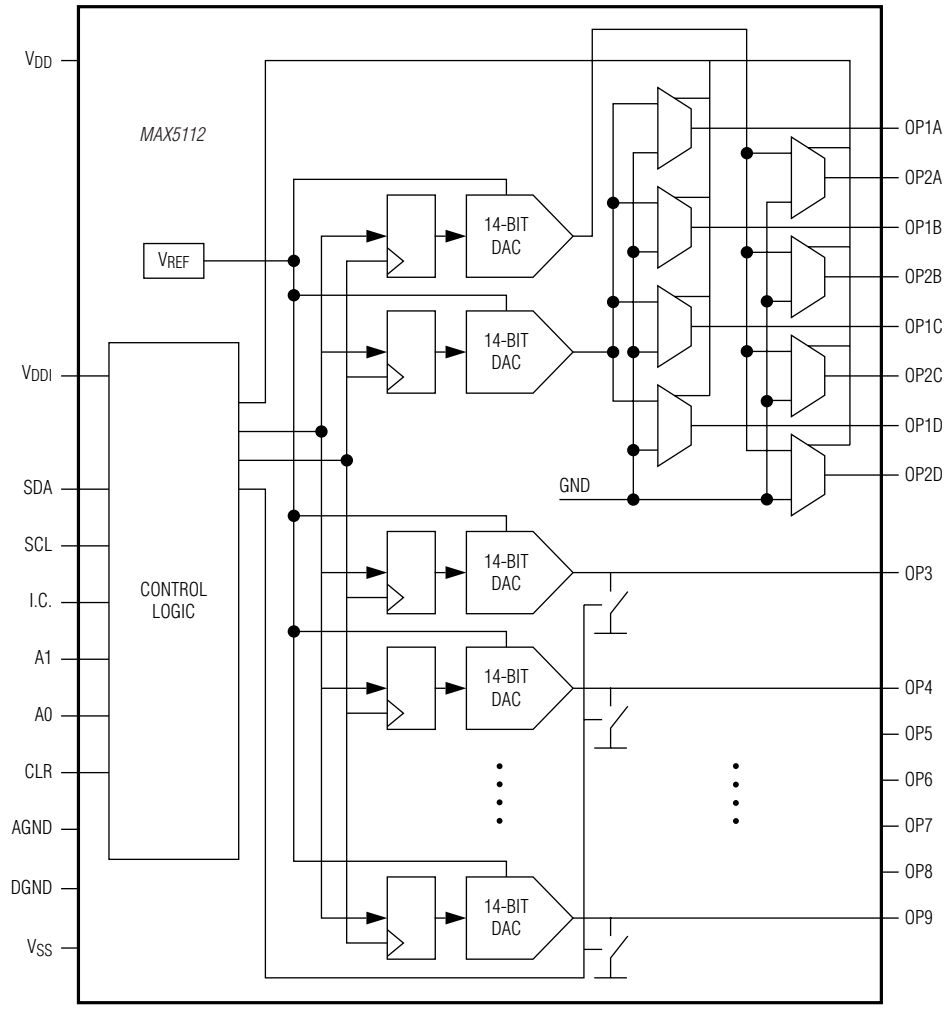
Pin Description

PIN		NAME	FUNCTION
WLP	TQFN-EP		
A1	1	SDA	I²C Bidirectional Serial Data
B1	31	OP5	DAC 5 Output, 180mA Full Scale
C1	30	OP9	DAC 9 Output, 15mA or 35mA Full Scale
D1	28	OP2A	DAC 2 Multiplexer Output A, 10mA Full Scale
E1	26	OP2C	DAC 2 Multiplexer Output C, 10mA Full Scale
F1	24	V_{SS}	Negative Power Supply
A2	2	SCL	I²C Clock Input
B2	32	V_{DD7}	DAC 5 Output Positive Power Supply. Internally connected to V_{DD6} and V_{DD10}.
C2	29	V_{DD6}	DAC 5 Output Positive Power Supply (WLP). Internally connected to V_{DD7} and V_{DD10}.
			DAC 5 Output and DAC 2 Output Positive Power Supply (TQFN). Internally connected to V_{DD7} and V_{DD10}.
D2	—	V_{DD10}	DAC 2 Output and DAC 9 Output Positive Power Supply. Internally connected to V_{DD6} and V_{DD7}.
E2	23	V_{DD5}	DAC 6 Output Positive Power Supply. Internally connected to V_{DD3} and V_{DD4}.
F2	25	OP2D	DAC 2 Multiplexer Output D, 10mA Full Scale

Pin Description (continued)

PIN		NAME	FUNCTION
WLP	TQFN-EP		
A3	5	V_{DDI}	Interface Power Supply. Connect to V_{DD} or to a separate supply to allow for a different interface voltage.
B3	4	A1	I²C Address Bit 1
C3	3	A0	I²C Address Bit 0
D3	27	OP2B	DAC 2 Multiplexer Output B, 10mA Full Scale
E3	21	V_{DD4}	DAC 6 Output Positive Power Supply. Internally connected to V_{DD5} and V_{DD3}.
F3	22	OP6	DAC 6 Output, -60mA or 300mA Full Scale
A4	6	DGND	Digital Ground
B4	—	I.C.	Internally Connected. Connect to V_{DDI}.
C4	7	AGND	Analog Ground
D4	13	N.C.	No Internal Connection. Must obey *Absolute Maximum Ratings* limits.
E4	20	V_{DD3}	DAC 6 Output Positive Power Supply. Internally connected to V_{DD5} and V_{DD4}.
F4	19	OP1D	DAC 1 Multiplexer Output D, 10mA Full Scale
A5	8	CLR	Active High Clear
B5	10	V_{DD1}	DAC 7 Output Positive Power Supply (WLP) DAC 3 Output and DAC 7 Output and DAC 8 Output Positive Power Supply (TQFN)
C5	—	V_{DD9}	DAC 3 Output and DAC 8 Output Positive Power Supply
D5	—	V_{DD8}	DAC 4 Output Positive Power Supply
E5	15	V_{DD2}	DAC 1 Output Positive Power Supply (WLP) DAC 1 Output and DAC 4 Output Positive Power Supply (TQFN)
F5	18	OP1C	DAC 1 Multiplexer Output C, 10mA Full Scale
A6	9	OP7	DAC 7 Output, 90mA Full Scale
B6	11	OP8	DAC 8 Output, 15mA or 35mA Full Scale
C6	12	OP3	DAC 3 Output, 2mA or 20mA Full Scale
D6	14	OP4	DAC 4 Output, 90mA Full Scale
E6	16	OP1A	DAC 1 Multiplexer Output A, 10mA Full Scale
F6	17	OP1B	DAC 1 Multiplexer Output B, 10mA Full Scale
—	—	EP	Exposed Pad (TQFN only). Internally connected to AGND. Connect to a ground plane to enhance thermal dissipation.

Functional Diagram



Detailed Description

The MAX5112 output ranges are optimized to bias a high-power tunable laser source. See Table 1 for the output current range available on each DAC output.

The DACs and highly stable internal reference are factory trimmed to ensure the outputs are within the specifications. Connect DACs in parallel to increase current drive or resolution.

DAC Outputs

The DAC configuration registers (01h–09h) control the configuration of each DAC individually. The Individual Configuration Register for each channel must be written to after a power-up event, even if the default values are written. This ensures the device will meet guaranteed offset performance specifications. DACs 1 and 2 drive four 2:1 multiplexers. The multiplexers route each DAC output to one of four outputs. Configure unused outputs as high impedance or connect to AGND. DAC 3 full-scale output is selectable between 2mA and 20mA.

DAC 6 provides 300mA full-scale output when selected as a current source. When selected as a current sink the full 14 bits are available between 0 and -60mA. A typical application for DAC 6 is to drive an optical amplifier where a current source is varied to set the gain or where a current sink is varied to set the attenuation.

All other DACs are positive current source DACs. DAC 8 and 9 full-scale outputs are selectable between 15mA and 35mA.

Table 1. Typical Full-Scale Output Currents

OUTPUT	OUTPUT-CURRENT RANGE CAPABILITY (mA)	
	LOW RANGE (DEFAULT)	HIGH RANGE
OP1	0 to 10	Reserved
OP2	0 to 10	Reserved
OP3	0 to 2	0 to 20
OP4	0 to 90	Reserved
OP5	0 to 180	Reserved
OP6	-60 to 0 or 0 to 300	Reserved
OP7	0 to 90	Reserved
OP8	0 to 15	0 to 35
OP9	0 to 15	0 to 35

The output range of DACs 3, 8, and 9 is selectable using the RNG bit in the Indiviual Configuration registers. The DAC 6 polarity and full-scale output is set by the SW_POL bit in the DAC 6 register.

Output Track and Hold

All channels feature a track-and-hold circuit to improve glitch performance. In common with all DACs of this type, the MAX5112 DACs will glitch when in transition from one code to another. The size of the glitch is defined by the size of the transition and where in the overall range the transition occurs. In general, a small transition results in a small glitch. However, this is not absolute. The track-and-hold circuit may be enabled to reduce the glitch size to close to zero. The track and hold can be enabled independently for each channel by setting bit-12 in the Individual DAC Configuration registers (01h–09h).

When enabled, the track and hold will engage after the 35th SCL transition in the I²C frame, setting a new DAC code in a single register write sequence as shown in Figure 2. See Figure 3 for details on a multiple register write sequence. This will hold the output level until the DAC section has settled. There is a small offset present in the output level while the track and hold is engaged approximately 10 LSB. The track and hold is engaged for 6µs (typical). It then disengages and the channel will transition to its new level with no glitch.

DAC Ground Switch

All DACs include a programmable switch to connect the output to ground when the DAC code is set to zero. The switch is open when the configuration bit is set to 0 and code zero is programmed. In this case, the output drivers are disabled, and the outputs set to high impedance. The DAC switch configuration is set for each individual DAC, see the *01h–09h: Individual DAC (1 to 9) Configuration Registers* section. The global DAC switch-override bits (GSWG[1:0]) in the General Configuration register (00h) override all switch selections when applied.

Clear Function (CLR)

The clear function allows the access of modes of operation through a single active-high input, CLR. The behavior of each DAC with CLR asserted is independently configurable. See the *CLR Interaction* section.

The clear function can also be asserted in software by setting the SW_CLR bit in the Software Reset Command register; see the *0Fh: Software Reset Command Register* section.

The clear function for each DAC is programmed through the CLR_CFG[1:0] bits in the Individual DAC Configuration registers (01h–09h) as shown in the following examples:

- **00 (Ignore):** The assertion of CLR does not affect the DAC.
- **01 (Shutter):** Shutter mode applies to OP6 only. For all other DACs, shutter mode produces the same effect as ignore. For OP6, the output polarity stays negative for as long as CLR is asserted (level sensitive). The current-sink level is defined by the DAC 6 Shutter Mode Code register (1Bh). Once CLR releases, the DAC output returns to the previously programmed value as set in the DAC 6 Source Mode Code register (16h).
- **10 (Gate):** The DAC is held at code zero (with ground switches engaged if enabled) as long as CLR is asserted (level sensitive). Once CLR releases, the DAC output returns to the previously programmed value as set in the DAC 1–9 Code register (10h–1Ah).
- **11 (Reset):** The DAC is set to code zero (with ground switches engaged if enabled) when CLR is asserted and remains at code zero after CLR is released (edge sensitive).

While the clear operation is in effect, DAC channels configured in ignore, shutter, or gate mode continue to accept new code settings. DAC channels configured in reset mode do not accept code changes until the clear operation is terminated.

Software Clear Interactions

The device provides a software-accessible version of the clear function (SW_CLR), which allows access to the clear functionality directly through the I²C interface (see the *0Fh: Software Reset Command Register* section). When the command 0Fh is used to launch a clear operation, the affected DAC outputs are held in the clear position, determined by the clear configuration settings. This happens from the time when the 0Fh command requesting a clear operation is completed until a second 0Fh command requesting removal of the clear operation is completed. The software- and pin-based clear operations are independently controlled and can be used individually or together without conflict. The devices provide an internal logic-OR circuitry.

Power-On Reset (POR), Power Brownout

The device contains a POR circuit with a threshold of 1.6V (typ) and a hysteresis of 0.025V (typ). POR ensures that the device resets all registers to default conditions as V_{DD} rises through the upper POR threshold. The default condition of all DAC registers is code zero, with ground switches engaged, ensuring that no large output current transients damage the load during initial power-up.

In a V_{DD} brownout situation, V_{DD} must fall below the lower POR threshold before a POR is issued when V_{DD} rises again. As V_{DD} falls, the device eventually loses regulation. However, the device is designed to avoid any large output current transients that could damage the load.

Software Reset and Standby Functions

The device contains a software reset function. The software reset function resets all code and configuration registers to default conditions. Write a 1 to the RST bit in the Software Reset Command register (0Fh) to initiate reset. The RST bit is not persistent, so writing a 0 to reset the bit is not required.

The device includes a software standby function that causes all DAC code registers (10h–1Bh) to be set to code zero. Write a 1 to the STDBY bit in the Software Reset Command register (0Fh) to initiate the standby function. The STDBY bit is not persistent, so writing a 0 to reset the bit is not required.

The software standby function is a subset of the software reset function. The software reset function takes effect when both functions are issued.

Overtemperature Error Handling

The device features an on-chip temperature protection circuit to prevent the device from overheating when all DACs output the maximum programmed current. When the die temperature rises above the threshold temperature, +160°C, the PRO_TEMP bit in the Status/Revision Readback Command register (0Eh) is set and the device enters an overtemperature shutdown mode. All DACs are set to code zero, but the control interface remains active, thereby allowing the host processor to read back the device status. The PRO_TEMP bit is latched and, therefore, the device can only be reset by a software reset command, a software standby command, or by cycling the power.

The device features an overtemperature status bit, OVR_TEMP. The OVR_TEMP bit is not latched, and is set if the device temperature is above the protection threshold. The OVR_TEMP bit allows the host processor to determine if the device is too hot to reset. If a software reset is attempted while the device is above the protection threshold, the command is ignored. Similarly, above the threshold die temperature, the device immediately enters shutdown mode when power is cycled.

The device features a warning bit, HI_TEMP. The warning bit is not latched and serves as a high-temperature status indicator bit. The HI_TEMP bit is set when the die temperature is typically 10°C below the overtemperature protection threshold.

See the *Applications Information* section for more detail on calculating die temperature and heat-sinking requirements.

User Configuration Registers

Table 2 shows a summary of the register map.

Table 2. User Register/Command Summary

REGISTER ADDRESS (hex)	ACCESS	PAIRABLE	REGISTER NAME
00h	W	Y	General Configuration
01h	W	Y	DAC 1 Configuration
02h	W	Y	DAC 2 Configuration
03h	W	Y	DAC 3 Configuration
04h	W	Y	DAC 4 Configuration
05h	W	Y	DAC 5 Configuration
06h	W	Y	DAC 6 Configuration
07h	W	Y	DAC 7 Configuration
08h	W	Y	DAC 8 Configuration
09h	W	Y	DAC 9 Configuration
0Ah	—	—	Reserved
0Bh	—	—	Reserved
0Ch	—	—	Reserved
0Dh	—	—	Reserved
0Eh	R	N	Status Feedback and Part ID
0Fh	W	Y	Software Reset/Standby/Clear
10h	W	Y	DAC 1–9 Code
11h	W	Y	DAC 1 Code
12h	W	Y	DAC 2 Code
13h	W	Y	DAC 3 Code
14h	W	Y	DAC 4 Code
15h	W	Y	DAC 5 Code
16h	W	Y	DAC 6 Source Mode Code
17h	W	Y	DAC 7 Code
18h	W	Y	DAC 8 Code
19h	W	Y	DAC 9 Code
1Ah	W	Y	DAC 6 Sink Mode Code
1Bh	W	Y	DAC 6 Shutter Mode Code
1Ch	—	—	Reserved
1Dh	—	—	Reserved
1Eh	—	—	Reserved
1Fh	W	Y	DAC 6 Polarity Control

Note: *The MAX5112 supports 7-bit command (register) addresses. The 7-bit register address listed above should be left-justified within the I²C command byte. The LSB of the command byte is a don't-care bit. See Figures 2, 3, and 4 for examples.*

Register Details

00h: General Configuration Register

BIT	15	14	13	12	11	10	9	8
NAME	GSWG[1:0]		X	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
NAME	X	X	X	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15:14	GSWG[1:0]	Global GSW Configuration Override 00: Individual DAC GSW settings are unaltered 01: Individual DAC GSW settings are set to 0 (ground switches disabled) 10: Individual DAC GSW settings are set to 1 (ground switches enabled) 11: Individual DAC GSW settings are unaltered
13:0	X	Reserved

01h–09h: Individual DAC (1 to 9) Configuration Registers

BIT	15	14	13	12	11	10	9	8
NAME	GSW	CLR_CFG[1:0]		T/H_EN	RNG	MUX[3:1]		
DEFAULT	1	0	0	0	1	1	1	0

BIT	7	6	5	4	3	2	1	0
NAME	MUX0	X	X	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15	GSW	Ground Switch Control 0: Output is left open when DAC code = 0000h 1: Output is connected to ground when DAC code = 0000h For DACs 1 and 2, this setting applies to the active mux output.
14:13	CLR_CFG[1:0]	Clear Configuration Settings (determine how CLR pin affects each DAC) 00 (Ignore): The DAC is not affected by the CLR pin (default) 01 (Shutter): DAC output polarity is held negative (current level determined by 1Bh) as long as the CLR pin is asserted (level sensitive, applies to DAC 6 only; otherwise, implements the ignore function) 10 (Gate): DAC output is held at zero scale (with ground switches engaged if enabled) as long as the CLR pin is asserted (level sensitive) 11 (Reset): DAC output is set to zero scale (with ground switches engaged if enabled) when CLR is asserted and remains valid after CLR is removed (edge sensitive)
12	T/H_EN	Track and Hold Enable 0: Track and Hold disabled 1: Track and Hold enabled
11	RNG	Range (DAC 3, 8, and 9) 0: DAC full-scale output level is set to high range. 1: DAC full-scale output level is set to low range. **Note:** For all DACs not suppporting RNG settings, this bit is reserved and should be set to 1 (default).
10:7	MUX[3:0]	Output Mux Settings for DAC (mux settings are only supported for DAC 1 and DAC 2) 0000: Output A active, all others high impedance 0001: Output B active, all others high impedance 0010: Output C active, all others high impedance 0011: Output D active, all others high impedance 01xx: All outputs high impedance (open) 1000: Output A active, all others shunted to GND 1001: Output B active, all others shunted to GND 1010: Output C active, all others shunted to GND 1011: Output D active, all others shunted to GND 11xx: All outputs shunted to GND (default)
6:0	X	Reserved

Note: *Any change to individual DAC configuration settings resets the affected DAC code to 0000h.*

0Eh: Status/Revision Readback Command Register

BIT	15	14	13	12	11	10	9	8
NAME	PRO_TEMP	OVR_TEMP	HI_TEMP	X	PART_ID[3:0]			
DEFAULT	0	0	0	0	0	0	0	1

BIT	7	6	5	4	3	2	1	0
NAME	REV_ID[3:0]				X	X	X	X
DEFAULT	0	1	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15	PRO_TEMP	Overtemperature Protection Indicator 0: Normal operation 1: Device overtemperature protection engaged
14	OVR_TEMP	Overtemperature Warning Indicator 0: Normal operation 1: Device temperature is too high (exceeding protection limit)
13	HI_TEMP	High-Temperature Warning Indicator 0: Normal operation 1: Device temperature is high (nearing protection limit)
12	X	Reserved
11:8	PART_ID[3:0]	Part ID Code (0001)
7:4	REV_ID[3:0]	Revision Code (0100)
3:0	X	Reserved

0Fh: Software Reset Command Register

BIT	15	14	13	12	11	10	9	8
NAME	RST	STDBY	SW_CLR	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
NAME	X	X	X	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15	RST	Global Reset (identical to a POR) 0: No operation 1: Reset: All DAC modes, configurations, and codes are returned to their default settings *Not Persistent: The reset operation is contained within the command. It is not necessary to issue a second 0Fh command to remove the reset condition.*
14	STDBY	Global Standby (identical to a global power-down) 0: No operation 1: Standby: All DAC codes are set to zero, but retain all configuration information *Not Persistent: The standby operation is contained within the command. It is not necessary to issue a second 0Fh command to remove the standby condition.* *Exclusive: If RST and STDBY are requested, STDBY is not issued.*
13	SW_CLR	Software Clear 0: No operation/remove SW_CLR 1: Assert SW_CLR *Persistent: The status of SW_CLR remains in effect until changed by a later 0Fh command.* *Exclusive: If SW_CLR and RST and/or STDBY are requested, SW_CLR is not issued.*
12:0	X	Reserved

Note: *A software reset or standby command is required to exit overtemperature-protection mode once engaged (software clear does not qualify for an exit).*

10h: Group DAC (1 to 9) Code Command Registers

BIT	15	14	13	12	11	10	9	8
NAME	B13	B12	B11	B10	B9	B8	B7	B6
DEFAULT	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
NAME	B5	B4	B3	B2	B1	B0	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15:2	B[13:0]	Group DAC Code Setting in Straight Binary Format. All DACs outputs update to code B[13:0] upon command completion. *This command is primarily useful for speeding up testing and qualification.*
1:0	X	Reserved

11h–1Bh: Individual DAC (1 to 9) Code Setting Registers

BIT	15	14	13	12	11	10	9	8
NAME	B13	B12	B11	B10	B9	B8	B7	B6
DEFAULT	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
NAME	B5	B4	B3	B2	B1	B0	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15:2	B[13:0]	DAC Code Settings in Straight Binary Format 3FFFh = Full-scale output 0000h = Zero-scale output (GSW configuration settings apply)
1:0	X	Reserved

Note: *11h–19h are DAC code settings for DACs 1–9, respectively. 1Ah is the sink mode code setting for DAC 6. 1Bh is the shutter mode setting for DAC6. See Table 2*

1Fh: DAC 6 Polarity Command Register

BIT	15	14	13	12	11	10	9	8
NAME	SW_POL	X	X	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
NAME	X	X	X	X	X	X	X	X
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	DESCRIPTION
15	SW_POL	Software Polarity Control (to DAC 6 only) 0: Source-mode operation (0 to 300mA determined by 16h code, with GSW operation) 1: Sink-mode operation (0 to -60mA determined by 1Ah code, GSW operation disabled)
14:0	X	Reserved

DAC 6 Polarity Operations

Software command 1Fh (SW_POL) or the CLR operation in shutter (01) mode controls the polarity of DAC 6. DAC 6 operates in a sink-current mode (0 to -60mA, determined by register 1Ah in sink mode) when SW_POL is set high. When the software command is used, the requested polarity is held in effect from the time when the 1Fh command requesting a polarity change is completed until a second 1Fh command requesting a polarity change operation is completed. When the shutter mode is used, DAC 6 remains in shutter mode as long as CLR is held high. The software- and CLR-driven polarity operations are independently controlled and can be used individually or together without conflict. The device provides an internal logic-OR operation. Shutter allows the fast access to a programmable negative code, based on register 1Bh, from either a source or sink mode with a controlled return to the original operating state upon release.

Gate mode is activated by asserting the CLR or through the SW_CLR bit. If gate mode is activated while the DAC is set to sink mode, the DAC remains in sink mode, but the current is reduced to 0mA for the duration of the gating event.

Similarly, when reset mode is set, the DAC remains in sink mode, but the current is reduced to 0mA and remains there during and after the reset event. All source-, sink-, and shutter-mode current settings are reset to zero by this operation. Shutter mode is inaccessible while DAC 6 is configured for reset.

Regardless of polarity/shutter setting, DAC 6 continues to accept updated code settings for either source (16h), sink (1Ah), or shutter mode code (1Bh) registers, provided the DAC is not being held in any reset mode (through CLR or SW_CLR).

I2C Interface

The device features an I2C-compatible, 2-wire interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). The SDA and SCL lines enable read and write communication between the IC and a master device at a rate of up to 400kHz. The IC is a slave device, relying on the master to generate the SCL signal. The master initiates data transfer on the bus and generates SCL to permit the transfer. Figure 1 shows the timing for the bus. The two bus lines (SDA and SCL) must be high when the bus is not in use. When in use, the port bits are toggled to generate the appropriate signals for SDA and SCL. The SDA state is allowed to change only while SCL is low. The state of SDA must remain stable while SCL is high, with the exception of START (S) and STOP (P) conditions. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer the data bits to the device, with the 9th clock cycle used for an acknowledge pulse. A separate V_{DDI} power-supply input and internal bidirectional level translators are provided to allow the device to interface to a microcontroller running on a voltage other than V_{DD}. The SDA driver is an open-drain output, requiring a pullup resistor to generate a logic-high voltage.

START and STOP Conditions

Both SCL and SDA must be high when the bus is not in use. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (see Figure 1). When the master has finished communicating with the slave, the master issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Slave Address

The device monitors the bus continuously, waiting for a START condition followed by a slave address. The 8th bit of the slave address byte is the R/$\overline{W}$ bit. R/$\overline{W}$ = 1 indicates a read operation and R/$\overline{W}$ = 0 indicates a write operation.

The device features a 7-bit-long slave address. The first 5 bits (MSBs) of the slave address are factory programmed to 10110. The logic states of the address inputs, A[1:0], determine the 2 least significant bits of the 7-bit slave address, as shown in Table 3. Connect address inputs to V_{DDI} or DGND and keep address inputs static during operation. There are a total of four possible slave addresses for the MAX5112, and, therefore, a maximum of four MAX5112 devices can be on the bus at one time.

Repeated START

Interrupting a transmission to the device with a repeated START (Sr) leaves the input latches with the data that has not been transferred to the output latches. The unused data are not stored. The aborted I2C sequence leaves all control registers unchanged.

Table 3. I2C Addresses

A1	A0	DEVICE ADDRESS
0	0	1011000
0	1	1011001
1	0	1011010
1	1	1011011

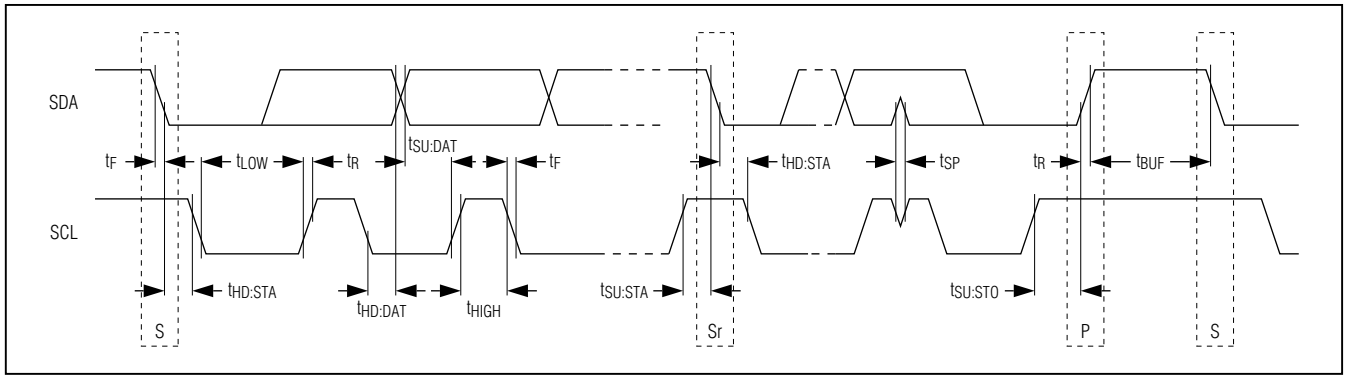


Figure 1. I2C Timing Diagram

Command Bytes and Data Bytes

A command byte follows the slave address. A command byte is followed by 2 data bytes unless the command byte is the last byte in the transmission, as in the case for read-back operations. When data bytes follow the command byte, the command byte indicates the address of the register that is to receive the following 2 data bytes. The data bytes are stored in a temporary register and then transferred to the appropriate register during the ACK periods between bytes, avoiding any glitching or digital feedthrough to the DACs while the interface is active, all while supporting multiple writes during a single I²C command.

The MAX5112 supports 7-bit command (register) addresses. The register address should be left-justified within the command byte. The LSB of the command byte is a don't-care bit and is shown as X in Figures 2, 3, and 4.

Early STOP Conditions

The device recognizes a STOP condition at any point in a transmission. When STOP occurs during a write-mode command byte or data-byte transmission, the interrupted command and output byte pairs are ignored and the transmission is terminated. When STOP occurs during a readback byte, the transmission is terminated and a later read-mode request begins transfer of the requested register data from the beginning.

I²C Write Operations

A master device communicates with the IC by transmitting the proper address followed by command and data words. Each transmit sequence is framed by a START or repeated START condition and a STOP condition. Each word is 8 bits long and is always followed by an acknowledge clock (ACK) pulse, as shown in Figure 2. The first byte contains the IC address with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the register (or command) to be written and the third and fourth bytes contain the data to be written. Repeat register address and data pairs (byte 2 to 4 in Figures 2 and 3) to perform multiple register writes using a single I²C command sequence. There is no limit to the number of registers written with a single command. The device supports this capability for all user-accessible write-mode commands.

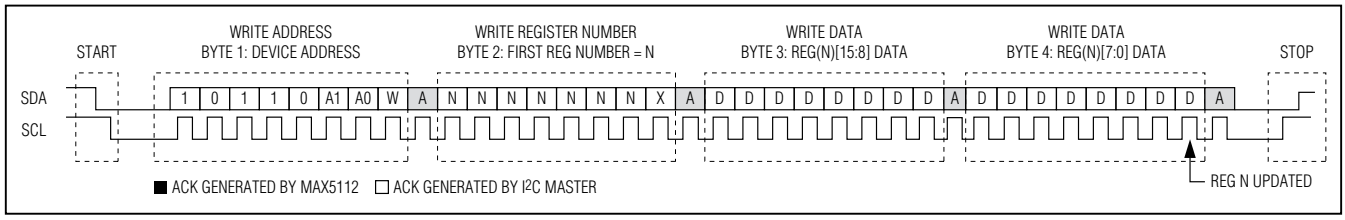


Figure 2. I²C Single Register Write Sequence

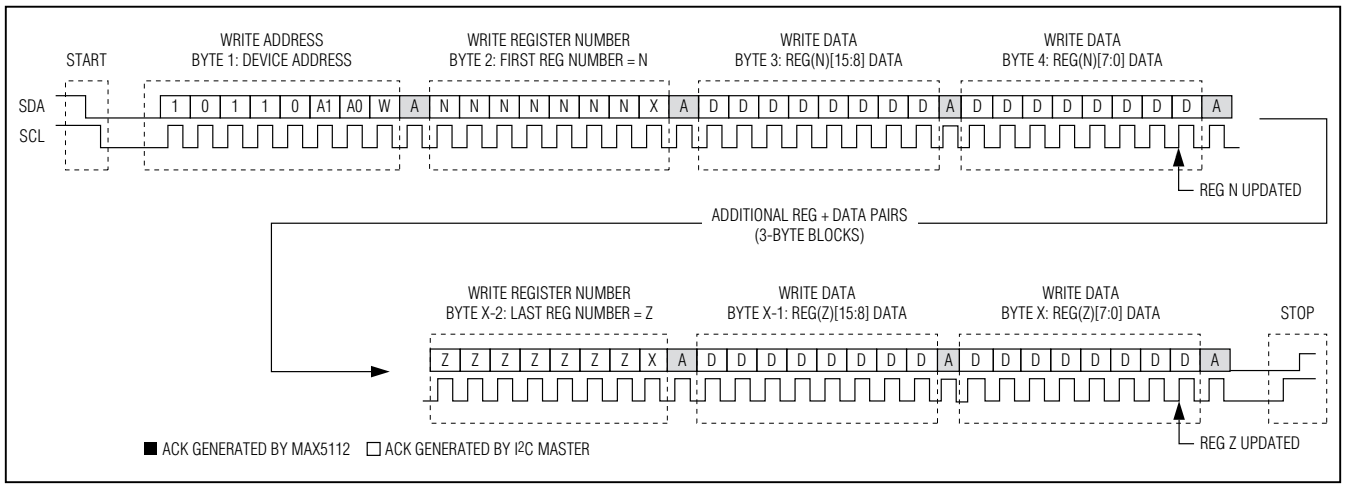


Figure 3. I²C Multiple Register Write Sequence

9-Channel, 14-Bit, Current DAC with I²C Interface

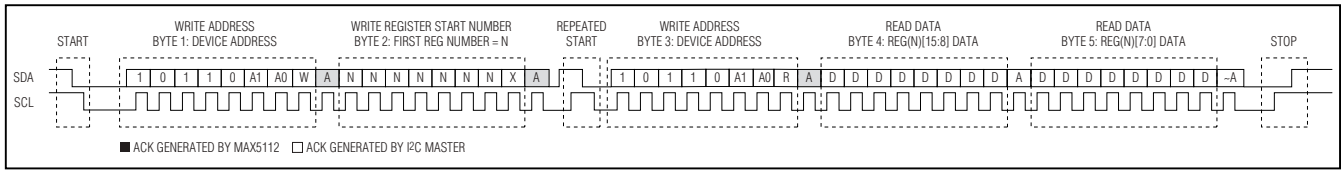


Figure 4. I²C Register Read Sequence

I²C Readback Operations

Each receive sequence is framed by a START or repeated START condition and a STOP condition, as shown in Figure 4. Each word is 8 bits long and is always followed by an acknowledge clock pulse. The first byte contains the device address with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the register that is to be read back. There is now a repeated START condition, followed by the device address with R/$\overline{W}$ = 1 to indicate a read and an acknowledge clock. The master still maintains control of the SCL line, but the device takes over the SDA line. The final 2 bytes in the frame contain the register data read back followed by a STOP condition. The device continues to read back zeros when additional bytes beyond those required to read back the requested data are provided.

I²C Compatibility

The device is fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs. SDA also features an open-drain output, which can pull the data line low as required for ACK pulses and readback operation. Figure 5 shows a typical I²C application.

CLR Interaction

The device's clear function allows the access of operation modes through a single input, CLR. Each DAC mode can be configured independently. The CLR input interacts with DAC code settings only. The CLR input does not interfere with configurations or readback operations. Ongoing I²C transfers continue uninterrupted when CLR is driven high. The effect of CLR being driven depends on the clear configurations of the individual DAC channel.

Code changes to any DAC channels configured in ignore (00), shutter (01), or gate (10) mode are recognized, regardless of the status of CLR. In shutter or gate mode, the DACs remain in the shutter or off positions for the duration of the CLR assertion. Once CLR is released, the DACs return to the most recently programmed output values.

Any DAC channels configured in reset (11) mode ignore code changes contained in the I²C commands, during which CLR is, or has been, asserted. In reset mode, the DAC code memories are reset to a zero code state and remain in that state until programmed by a subsequent command.

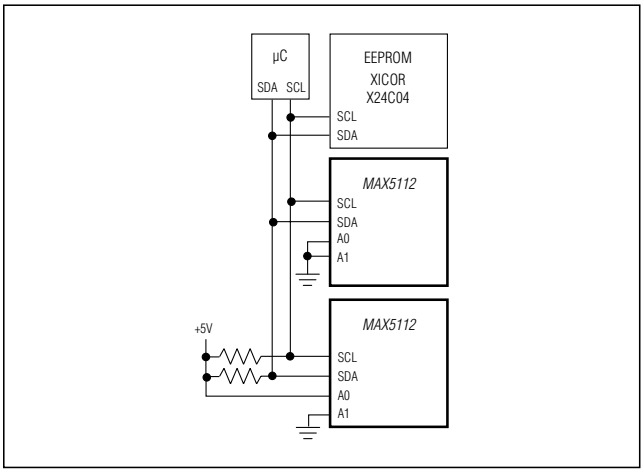


Figure 5. Typical I²C Application Circuit

Applications Information

Thermal Design

To reduce thermal resistance, include V_{DD} and ground planes in the application PCB. Connect the TQFN exposed pad to the ground plane through a large via. Connect the multiple V_{DD} inputs to the V_{DD} plane through multiple vias. Connect AGND and DGND to the ground plane via a star configuration. If possible, use a separate trace for V_{DDI} and connect this back to the supply in a star configuration.

Noise Immunity

Each V_{DD} pin should be bypassed with a separate 0.1uF capacitor as close as possible to the supply pin. Pay particular attention to the ESR value of the capacitors and add a 100pF capacitor in parallel to each 100nF capacitor. Noise is particularly important in fiber applications, thus it may be necessary to add 100pF capacitors to decouple the optical electrodes to ground. This ensures that any crosstalk between the interface and the DAC outputs caused by PCB parasitic is minimized.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
36 WLP	W363A3+1	21-0024	Refer to Application Note 1891
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	10/12	Released the TQFN package and revised the *Electrical Characteristics*, *Typical Operating Circuit*, *Absolute Maximum Ratings, 01h–09h: Individual DAC (1 to 9) Configuration Registers* sections, and Table 1.	1, 2, 4, 16, 20, 26
2	5/13	Updated Note 3 in the *Electrical Characteristics* and revised the *DAC Outputs* section.	6, 16

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