



## 4.5Ω Dual SPST Analog Switches in UCSP

### General Description

The MAX4721/MAX4722/MAX4723 low-voltage, low on-resistance ( $R_{ON}$ ), dual single-pole/single throw (SPST) analog switches operate from a single +1.8V to +5.5V supply. These devices are designed for USB 1.1 and audio switching applications.

The MAX4721/MAX4722/MAX4723 feature 4.5Ω  $R_{ON}$  (max) with 1.2Ω flatness and 0.3Ω matching between channels. These new switches feature guaranteed operation from +1.8V to +5.5V and are fully specified at 3V and 5V. These switches offer break-before-make switching (1ns) with  $t_{ON}$  <80ns and  $t_{OFF}$  <40ns at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply.

These switches are packaged in a chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 1.52mm × 1.52mm area and has a 3 × 3 bump array with a bump pitch of 0.5mm. These switches are also available in an 8-pin μMAX package.

### Applications

Battery-Operated Equipment  
Audio/Video-Signal Routing  
Low-Voltage Data-Acquisition Systems  
Sample-and-Hold Circuits  
Communications Circuits

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.  
UCSP is a trademark of Maxim Integrated Products, Inc.

### Features

- ◆ USB 1.1 Signal Switching
- ◆ <2ns Differential Skew
- ◆ -3dB Bandwidth: >300MHz
- ◆ Low 15pF On-Channel Capacitance
- ◆ Low  $R_{ON}$  (max) Switches  
4.5Ω (max) (+3V Supply)  
3Ω (max) (+5V Supply)
- ◆ 0.3Ω (max)  $R_{ON}$  Match (+3V Supply)
- ◆ 1.2Ω (max)  $R_{ON}$  Flatness (+3V Supply)
- ◆ <0.5nA Leakage Current at  $T_A = +25^\circ\text{C}$
- ◆ High Off-Isolation: -55dB (10MHz)
- ◆ Low Crosstalk: -80dB (10MHz)
- ◆ Low Distortion: 0.03%
- ◆ +1.8V CMOS-Logic Compatible
- ◆ Single-Supply Operation from +1.8V to +5.5V
- ◆ Rail-to-Rail® Signal Handling

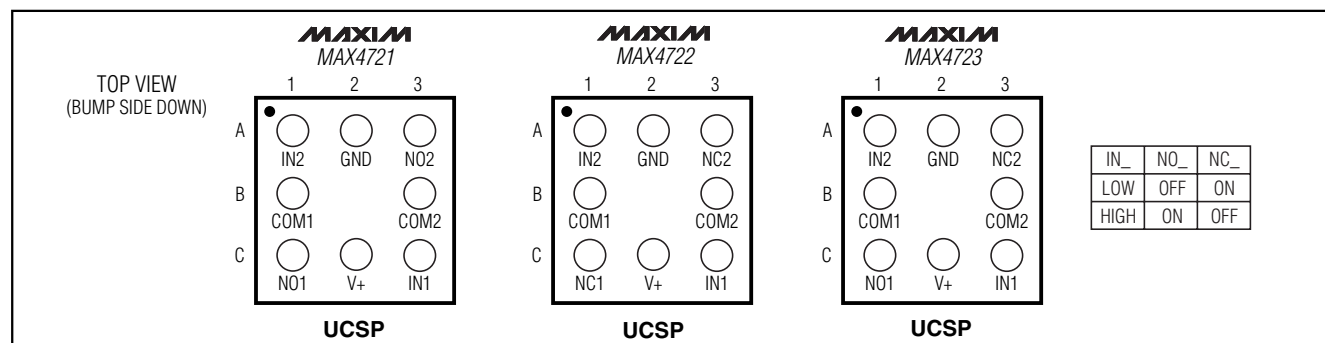
### Ordering Information

| PART          | TEMP RANGE     | PIN/BUMP-PACKAGE | TOP MARK |
|---------------|----------------|------------------|----------|
| MAX4721EUA    | -40°C to +85°C | 8 μMAX           | —        |
| MAX4721EBL-T* | -40°C to +85°C | 9 UCSP-9         | ABP      |
| MAX4722EUA    | -40°C to +85°C | 8 μMAX           | —        |
| MAX4722EBL-T* | -40°C to +85°C | 9 UCSP-9         | ABQ      |
| MAX4723EUA    | -40°C to +85°C | 8 μMAX           | —        |
| MAX4723EBL-T* | -40°C to +85°C | 9 UCSP-9         | ABR      |

**Note:** UCSP package requires special solder temperature profile described in the Absolute Maximum Ratings section.

\*UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. See the UCSP reliability notice in the UCSP Reliability section of this data sheet for more information.

### Pin Configurations/Functional Diagrams/Truth Tables



## 4.5Ω Dual SPST Analog Switches in UCSP

### ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

|                                                             |                      |
|-------------------------------------------------------------|----------------------|
| V+, IN_                                                     | -0.3V to +6.0V       |
| COM_, NO_, NC_ (Note 1)                                     | -0.3V to (V+ + 0.3V) |
| Continuous Current COM_, NO_, NC_                           | ±100mA               |
| Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle) | ±200mA               |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)       |                      |
| 8-Pin μMAX (derate 4.5mW/°C above +70°C)                    | 362mW                |
| 9-Bump UCSP (derate 4.7mW/°C above +70°C)                   | 379mW                |

|                                       |                 |
|---------------------------------------|-----------------|
| ESD Method 3015.7                     | >2kV            |
| Operating Temperature Range           | -40°C to +85°C  |
| Junction Temperature                  | +150°C          |
| Storage Temperature Range             | -65°C to +150°C |
| Lead Temperature (soldering, 10s)     | +300°C          |
| Bump Temperature (soldering) (Note 2) |                 |
| Infrared (15s)                        | +220°C          |
| Vapor Phase (60s)                     | +215°C          |

**Note 1:** Signals on COM\_, NO\_, or NC\_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

**Note 2:** This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry standard specification, JEDEC 020A, paragraph 7.6, table 3 for IR/VPF and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V<sub>IH</sub> = +1.4V, V<sub>IL</sub> = +0.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +3.0V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 3, 4)

| PARAMETER                                         | SYMBOL                                                  | CONDITIONS                                                                                                | T <sub>A</sub>                       | MIN  | TYP   | MAX  | UNITS |
|---------------------------------------------------|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|--------------------------------------|------|-------|------|-------|
| Analog Signal Range                               | V <sub>COM_</sub> , V <sub>NO_</sub> , V <sub>NC_</sub> |                                                                                                           |                                      | 0    |       | V+   | V     |
| <b>ANALOG SWITCH</b>                              |                                                         |                                                                                                           |                                      |      |       |      |       |
| On-Resistance (Note 5)                            | R <sub>ON</sub>                                         | V+ = 2.7V, I <sub>COM_</sub> = 10mA; V <sub>NO_</sub> or V <sub>NC_</sub> = 1.5V                          | +25°C                                |      | 3.0   | 4.5  | Ω     |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> |      |       | 5    |       |
| On-Resistance Match Between Channels (Notes 5, 6) | ΔR <sub>ON</sub>                                        | V+ = 2.7V, I <sub>COM_</sub> = 10mA; V <sub>NO_</sub> or V <sub>NC_</sub> = 1.5V                          | +25°C                                |      | 0.1   | 0.3  | Ω     |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> |      |       | 0.4  |       |
| On-Resistance Flatness (Note 7)                   | R <sub>FLAT(ON)</sub>                                   | V+ = 2.7V, I <sub>COM_</sub> = 10mA; V <sub>NO_</sub> or V <sub>NC_</sub> = 1.0V, 1.5V, 2.0V              | +25°C                                |      | 0.6   | 1.2  | Ω     |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> |      |       | 1.5  |       |
| NO_, NC_ Off-Leakage Current (Note 8)             | I <sub>NO_(OFF)</sub> , I <sub>NC_(OFF)</sub>           | V+ = 3.6V, V <sub>COM_</sub> = 0.3V, 3.3V; V <sub>NO_</sub> or V <sub>NC_</sub> = 3.3V, 0.3V              | +25°C                                | -0.5 | +0.01 | +0.5 | nA    |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> | -1.5 |       | +1.5 |       |
| COM_ Off-Leakage Current (Note 8)                 | I <sub>COM_(OFF)</sub> , I <sub>COM_(OFF)</sub>         | V+ = 3.6V, V <sub>COM_</sub> = 0.3V, 3.3V; V <sub>NO_</sub> or V <sub>NC_</sub> = 3.3V, 0.3V              | +25°C                                | -0.5 | +0.01 | +0.5 | nA    |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> | -1.5 |       | +1.5 |       |
| COM_ On-Leakage Current (Note 8)                  | I <sub>COM_(ON)</sub>                                   | V+ = 3.6V, V <sub>COM_</sub> = 0.3V, 3.3V; V <sub>NO_</sub> or V <sub>NC_</sub> = 0.3V, 3.3V, or floating | +25°C                                | -1   | +0.01 | +1   | nA    |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> | -2   |       | +2   |       |
| Turn-On Time                                      | t <sub>ON</sub>                                         | V <sub>NO_</sub> , V <sub>NC_</sub> = 1.5V; R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1        | +25°C                                |      | 40    | 80   | ns    |
|                                                   |                                                         |                                                                                                           | T <sub>MIN</sub> to T <sub>MAX</sub> |      |       | 100  |       |

## 4.5Ω Dual SPST Analog Switches in UCSP

### ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V<sub>+</sub> = +2.7V to +3.6V, V<sub>IH</sub> = +1.4V, V<sub>IL</sub> = +0.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>+</sub> = +3.0V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 3, 4)

| PARAMETER                                               | SYMBOL                                         | CONDITIONS                                                                                                                    | T <sub>A</sub>                          | MIN  | TYP  | MAX | UNITS |
|---------------------------------------------------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|------|------|-----|-------|
| DYNAMIC CHARACTERISTICS                                 |                                                |                                                                                                                               |                                         |      |      |     |       |
| Turn-Off Time                                           | t <sub>OFF</sub>                               | V <sub>NO_</sub> , V <sub>NC_</sub> = 1.5V;<br>R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1                         | +25°C                                   | 20   | 40   | ns  |       |
|                                                         |                                                |                                                                                                                               | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 50   |      |     |       |
| Break-Before-Make Time Delay<br>(MAX4723 Only) (Note 8) | t <sub>BBM</sub>                               | V <sub>NO_</sub> , V <sub>NC_</sub> = 1.5V;<br>R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2                         | +25°C                                   | 8    |      | ns  |       |
|                                                         |                                                |                                                                                                                               | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 1    |      |     |       |
| Skew (Note 8)                                           | t <sub>SKEW</sub>                              | R <sub>S</sub> = 39Ω, C <sub>L</sub> = 50pF, Figure 3                                                                         | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 0.15 | 0.2  | ns  |       |
| Charge Injection                                        | Q                                              | V <sub>GEN</sub> = 2V, R <sub>GEN</sub> = 0Ω,<br>C <sub>L</sub> = 1.0nF, Figure 4                                             | +25°C                                   | 5    |      | pC  |       |
| Off-Isolation (Note 9)                                  | V <sub>ISO</sub>                               | f = 10MHz; V <sub>NO_</sub> , V <sub>NC_</sub> = 1V <sub>P-P</sub> ;<br>R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 5a | +25°C                                   | -55  |      | dB  |       |
|                                                         |                                                | f = 1MHz; V <sub>NO_</sub> , V <sub>NC_</sub> = 1V <sub>P-P</sub> ;<br>R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 5a  |                                         | -80  |      |     |       |
| Crosstalk (Note 10)                                     | V <sub>CT</sub>                                | f = 10MHz; V <sub>NO_</sub> , V <sub>NC_</sub> = 1V <sub>P-P</sub> ;<br>R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 5b | +25°C                                   | -80  |      | dB  |       |
|                                                         |                                                | f = 1MHz; V <sub>NO_</sub> , V <sub>NC_</sub> = 1V <sub>P-P</sub> ;<br>R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, Figure 5b  |                                         | -110 |      |     |       |
| On-Channel -3dB Bandwidth                               | BW                                             | Signal = 0dBm, C <sub>L</sub> = 5pF,<br>R <sub>L</sub> = 50Ω, Figure 5a                                                       | +25°C                                   | >300 |      | MHz |       |
| Total Harmonic Distortion                               | THD                                            | R <sub>L</sub> = 600Ω                                                                                                         | +25°C                                   | 0.03 |      | %   |       |
| NO_, NC_ Off-Capacitance                                | C <sub>NO_(OFF)</sub><br>C <sub>NC_(OFF)</sub> | f = 1MHz, Figure 6                                                                                                            | +25°C                                   | 9    |      | pF  |       |
| Switch On-Capacitance                                   | C <sub>(ON)</sub>                              | f = 1MHz, Figure 6                                                                                                            | +25°C                                   | 15   |      | pF  |       |
| DIGITAL I/O                                             |                                                |                                                                                                                               |                                         |      |      |     |       |
| Input Logic High Voltage                                | V <sub>IH</sub>                                |                                                                                                                               | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 1.4  |      | V   |       |
| Input Logic Low Voltage                                 | V <sub>IL</sub>                                |                                                                                                                               | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      | 0.5  | V   |       |
| Input Leakage Current                                   | I <sub>IN</sub>                                | V <sub>+</sub> = +3.6V, V <sub>IN_</sub> = 0 or 5.5V                                                                          | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | -0.1 | +0.1 | μA  |       |
| SUPPLY                                                  |                                                |                                                                                                                               |                                         |      |      |     |       |
| Supply Voltage Range                                    | V <sub>+</sub>                                 |                                                                                                                               | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 1.8  | 5.5  | V   |       |
| Positive Supply Current                                 | I <sub>+</sub>                                 | V <sub>+</sub> = 5.5V, V <sub>IN_</sub> = 0V or V <sub>+</sub>                                                                | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      | 1    | μA  |       |

## 4.5Ω Dual SPST Analog Switches in UCSP

### ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.2V to +5.5V, V<sub>IH</sub> = +2.0V, V<sub>IL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V+ = +5.0V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 3, 4)

| PARAMETER                                               | SYMBOL                                                     | CONDITIONS                                                                                                      | T <sub>A</sub>                          | MIN  | TYP   | MAX  | UNITS |
|---------------------------------------------------------|------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------|------|-------|------|-------|
| Analog Signal Range                                     | V <sub>COM_</sub> ,<br>V <sub>NO_</sub> , V <sub>NC_</sub> |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 0    |       | V+   | V     |
| ANALOG SWITCH                                           |                                                            |                                                                                                                 |                                         |      |       |      |       |
| On-Resistance (Note 5)                                  | R <sub>ON</sub>                                            | V+ = 4.2V, I <sub>COM_</sub> = 10mA;<br>V <sub>NO_</sub> or V <sub>NC_</sub> = 3.5V                             | +25°C                                   |      | 1.7   | 3.0  | Ω     |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      |       | 3.5  |       |
| On-Resistance Match Between<br>Channels (Notes 5, 6)    | ΔR <sub>ON</sub>                                           | V+ = 4.2V, I <sub>COM_</sub> = 10mA;<br>V <sub>NO_</sub> or V <sub>NC_</sub> = 3.5V                             | +25°C                                   |      | 0.1   | 0.3  | Ω     |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      |       | 0.4  |       |
| On-Resistance Flatness (Note 7)                         | R <sub>FLAT(ON)</sub>                                      | V+ = 4.2V, I <sub>COM_</sub> = 10mA;<br>V <sub>NO_</sub> or V <sub>NC_</sub> = 1.0V, 2.0V, 3.5V                 | +25°C                                   |      | 0.4   | 1.2  | Ω     |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      |       | 1.5  |       |
| NO_ , NC_ Off-Leakage Current<br>(Note 8)               | I <sub>NO_(OFF)</sub> ,<br>I <sub>NC_(OFF)</sub>           | V+ = 5.5V, V <sub>COM_</sub> = 1.0V, 4.5V;<br>V <sub>NO_</sub> or V <sub>NC_</sub> = 4.5V, 1.0V                 | +25°C                                   | -0.5 | +0.01 | +0.5 | nA    |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | -1.5 |       | +1.5 |       |
| COM_ Off-Leakage Current<br>(Note 8)                    | I <sub>COM_(OFF)</sub>                                     | V+ = 5.5V, V <sub>COM_</sub> = 1V, 4.5V;<br>V <sub>NO_</sub> or V <sub>NC_</sub> = 4.5V, 1V                     | +25°C                                   | -0.5 | +0.01 | +0.5 | nA    |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | -1.5 |       | +1.5 |       |
| COM_ On-Leakage Current<br>(Note 8)                     | I <sub>COM_(ON)</sub>                                      | V+ = 5.5V, V <sub>COM_</sub> = 1.0V, 4.5V;<br>V <sub>NO_</sub> or V <sub>NC_</sub> = 1.0V, 4.5V, or<br>floating | +25°C                                   | -1   | +0.01 | +1   | nA    |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | -2   |       | +2   |       |
| DYNAMIC CHARACTERISTICS                                 |                                                            |                                                                                                                 |                                         |      |       |      |       |
| Turn-On Time                                            | t <sub>ON</sub>                                            | V <sub>NO_</sub> , V <sub>NC_</sub> = 3.0V;<br>R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1           | +25°C                                   |      | 30    | 80   | ns    |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      |       | 90   |       |
| Turn-Off Time                                           | t <sub>OFF</sub>                                           | V <sub>NO_</sub> , V <sub>NC_</sub> = 3.0V;<br>R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1           | +25°C                                   |      | 20    | 40   | ns    |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      |       | 50   |       |
| Break-Before-Make Time Delay<br>(MAX4723 Only) (Note 8) | t <sub>BBM</sub>                                           | V <sub>NO_</sub> , V <sub>NC_</sub> = 3.0V;<br>R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2           | +25°C                                   |      | 8     |      | ns    |
|                                                         |                                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 1    |       |      |       |
| Skew (Note 8)                                           | t <sub>SKEW</sub>                                          | R <sub>S</sub> = 39Ω, C <sub>L</sub> = 50pF, Figure 3                                                           | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      | 1.5   | 2    | ns    |
| DIGITAL I/O                                             |                                                            |                                                                                                                 |                                         |      |       |      |       |
| Input Logic High Voltage                                | V <sub>IH</sub>                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> | 2.0  |       |      | V     |
| Input Logic Low Voltage                                 | V <sub>IL</sub>                                            |                                                                                                                 | T <sub>MIN</sub> to<br>T <sub>MAX</sub> |      |       | 0.8  | V     |

## 4.5Ω Dual SPST Analog Switches in UCSP

### ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

( $V_+ = +4.2\text{V}$  to  $+5.5\text{V}$ ,  $V_{IH} = +2.0\text{V}$ ,  $V_{IL} = +0.8\text{V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_+ = +5.0\text{V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (Notes 3, 4)

| PARAMETER               | SYMBOL   | CONDITIONS                                            | $T_A$                  | MIN  | TYP | MAX  | UNITS         |
|-------------------------|----------|-------------------------------------------------------|------------------------|------|-----|------|---------------|
| Input Leakage Current   | $I_{IN}$ | $V_+ = 5.5\text{V}$ , $V_{IN\_} = 0\text{V}$ or $V_+$ | $T_{MIN}$ to $T_{MAX}$ | -0.1 |     | +0.1 | $\mu\text{A}$ |
| <b>POWER SUPPLY</b>     |          |                                                       |                        |      |     |      |               |
| Power-Supply Range      | $V_+$    |                                                       | $T_{MIN}$ to $T_{MAX}$ | 1.8  |     | 5.5  | V             |
| Positive Supply Current | $I_+$    | $V_+ = 5.5\text{V}$ , $V_{IN\_} = 0\text{V}$ or $V_+$ | $T_{MIN}$ to $T_{MAX}$ |      |     | 1    | $\mu\text{A}$ |

**Note 3:** UCSP parts are 100% tested at  $+25^\circ\text{C}$  only, and guaranteed by design over the specified temperature range.  $\mu\text{MAX}$  parts are 100% tested at  $T_{MAX}$  and guaranteed by design over the specified temperature range.

**Note 4:** The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

**Note 5:** Guaranteed by design for UCSP parts.

**Note 6:**  $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ .

**Note 7:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

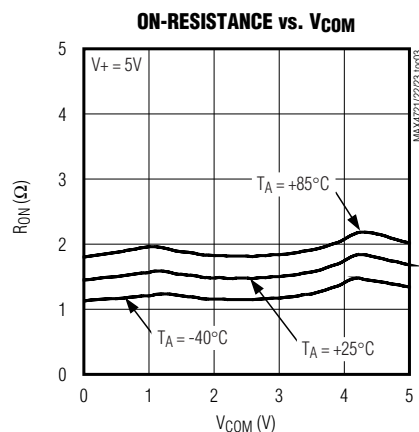
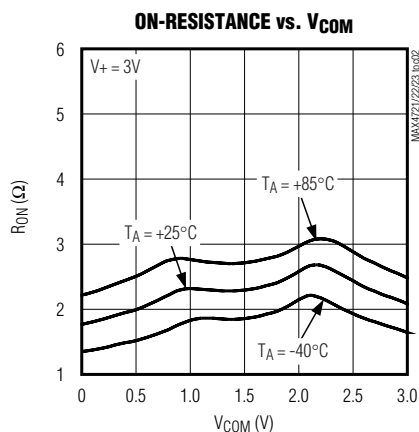
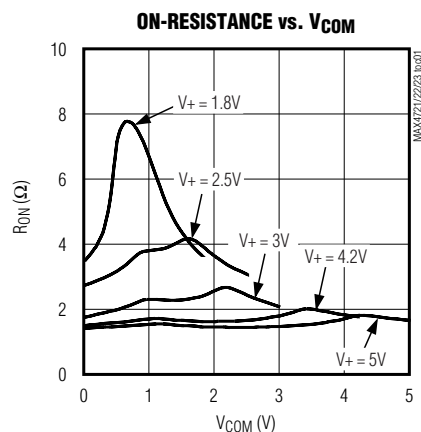
**Note 8:** Guaranteed by design.

**Note 9:** Off-Isolation =  $20\log_{10}(V_{COM} / V_{NO})$ ,  $V_{COM}$  = output,  $V_{NO}$  = input to off switch.

**Note 10:** Between any two switches.

### Typical Operating Characteristics

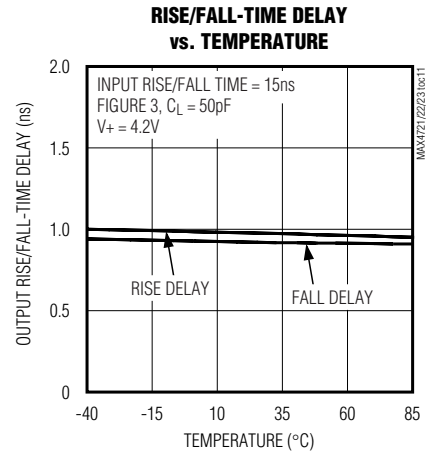
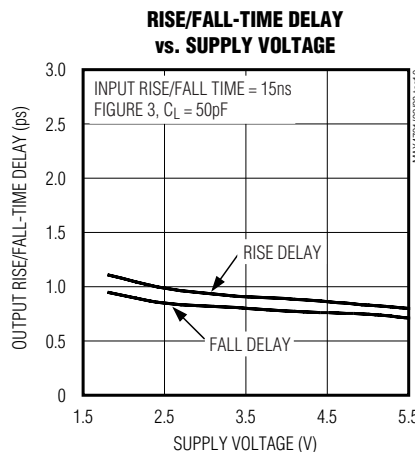
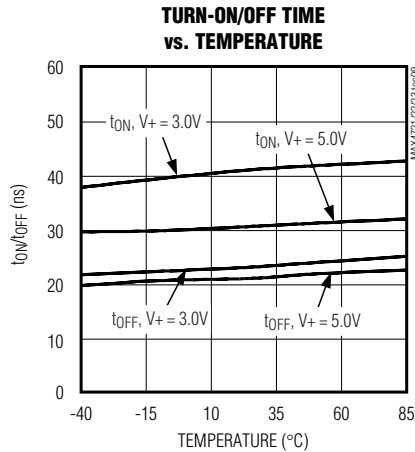
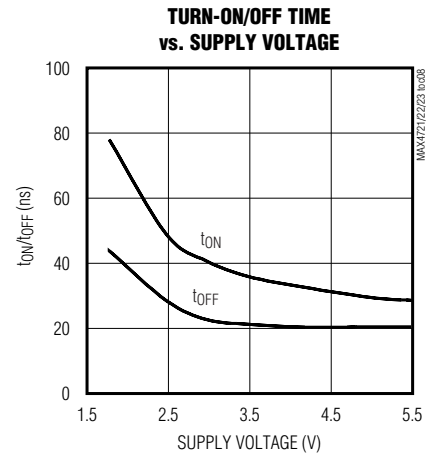
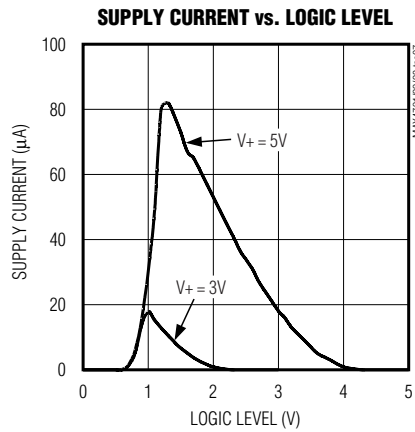
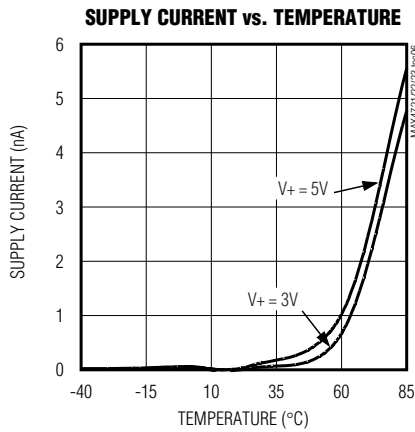
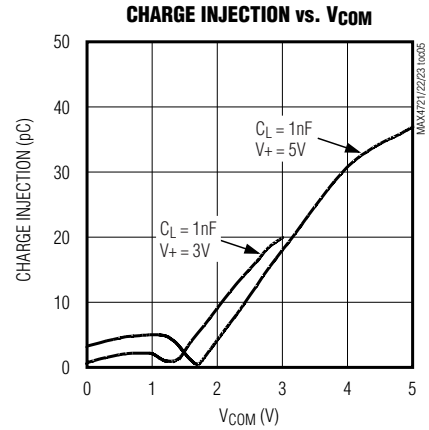
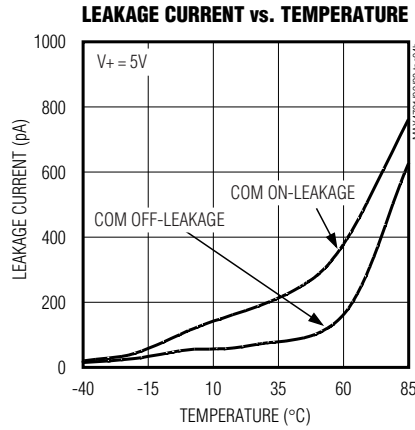
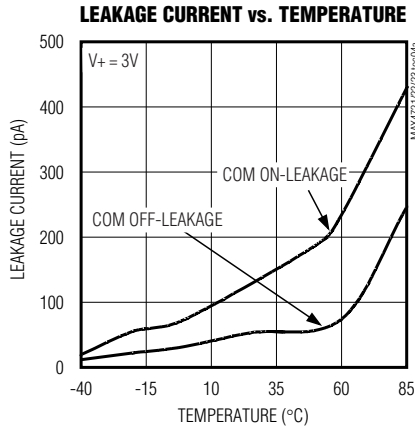
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# 4.5Ω Dual SPST Analog Switches in UCSP

## Typical Operating Characteristics (continued)

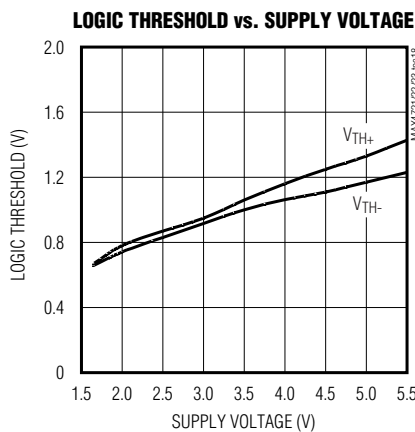
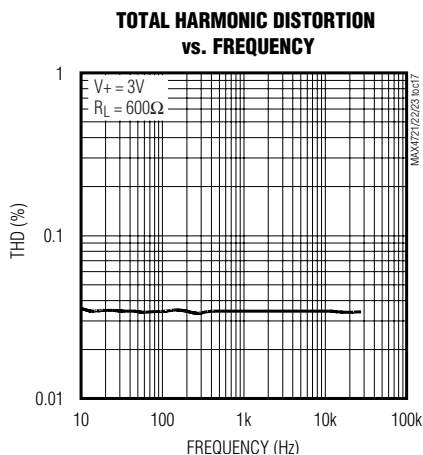
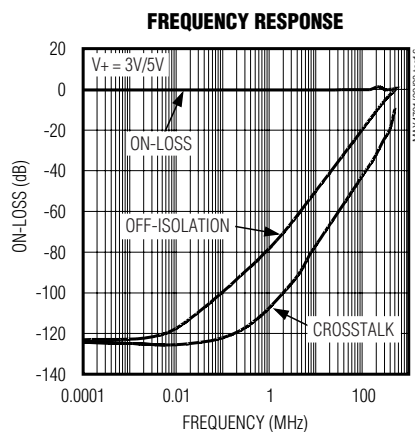
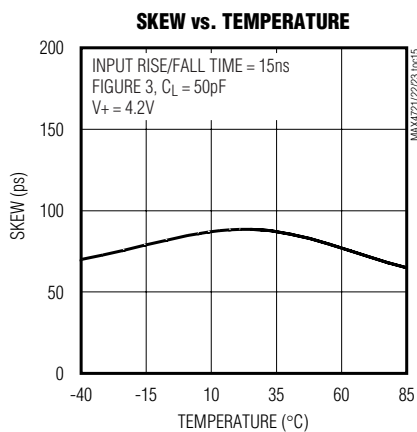
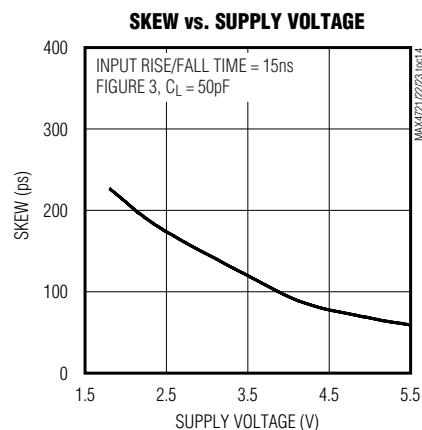
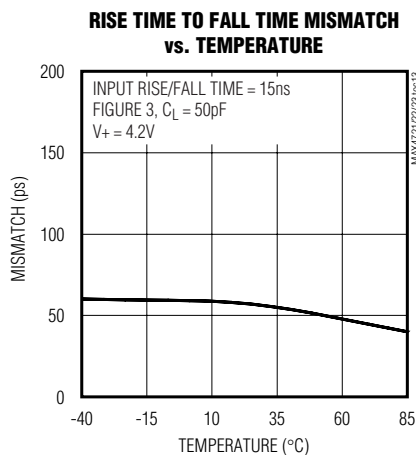
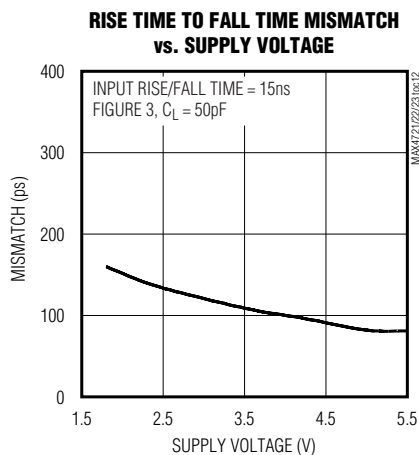
(T<sub>A</sub> = +25°C, unless otherwise noted.)



## 4.5Ω Dual SPST Analog Switches in UCSP

### Typical Operating Characteristics (continued)

(T<sub>A</sub> = +25°C, unless otherwise noted.)



MAX4721/MAX4722/MAX4723

## 4.5Ω Dual SPST Analog Switches in UCSP

### Pin Description

| PIN     |      |         |      |         |      | NAME | FUNCTION                               |
|---------|------|---------|------|---------|------|------|----------------------------------------|
| MAX4721 |      | MAX4722 |      | MAX4723 |      |      |                                        |
| UCSP    | μMAX | UCSP    | μMAX | UCSP    | μMAX |      |                                        |
| A1      | 3    | A1      | 3    | A1      | 3    | IN2  | Logic-Control Digital Input            |
| A2      | 4    | A2      | 4    | A2      | 4    | GND  | Ground. Connect to digital ground.     |
| A3      | 5    | —       | —    | —       | —    | NO2  | Analog-Switch Normally Open Terminal   |
| B1      | 2    | B1      | 2    | B1      | 2    | COM1 | Analog-Switch Common Terminal          |
| B3      | 6    | B3      | 6    | B3      | 6    | COM2 | Analog-Switch Common Terminal          |
| C1      | 1    | —       | —    | C1      | 1    | NO1  | Analog-Switch Normally Open Terminal   |
| C2      | 8    | C2      | 8    | C2      | 8    | V+   | Positive Analog Supply                 |
| C3      | 7    | C3      | 7    | C3      | 7    | IN1  | Logic-Control Digital Input            |
| —       | —    | C1      | 1    | —       | —    | NC1  | Analog-Switch Normally Closed Terminal |
| —       | —    | A3      | 5    | A3      | 5    | NC2  | Analog-Switch Normally Closed Terminal |

### Detailed Description

The MAX4721/MAX4722/MAX4723 dual SPST analog switches operate from a single +1.8V to +5.5V supply. The MAX4721/MAX4722/MAX4723 offer excellent AC characteristics, <0.5nA leakage current, less than 2ms differential skew, and 15pF on-channel capacitance. All of these devices are CMOS-logic compatible with rail-to-rail signal handling capability.

The MAX4721/MAX4722/MAX4723 are USB-compliant switches that provide 4.5Ω (max) on-resistance, and 15pF on-channel capacitance to maintain signal integrity. At 12Mbps (USB full-speed data rate specification) the MAX4721/MAX4722/MAX4723 introduce less than 2ns propagation delay between input and output signals and less than 0.5ns change in skew for the output signals (see Figure 3 for more details).

The MAX4721 has two normally open (NO) switches, the MAX4722 has two normally closed (NC) switches, and the MAX4723 has one NO switch and one NC switch.

### Applications Information

#### Digital Control Inputs

The MAX4721/MAX4722/MAX4723 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN<sub>+</sub> can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving the control logic inputs rail-to-rail minimizes power consumption. For a +3.0V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

#### Analog Signal Levels

Analog signals that range over the entire supply voltage (V<sub>+</sub> to GND) are passed with very little change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO<sub>+</sub>, NC<sub>+</sub>, and COM<sub>+</sub> pins can be either inputs or outputs.

## 4.5Ω Dual SPST Analog Switches in UCSP

### Test Circuits/Timing Diagrams

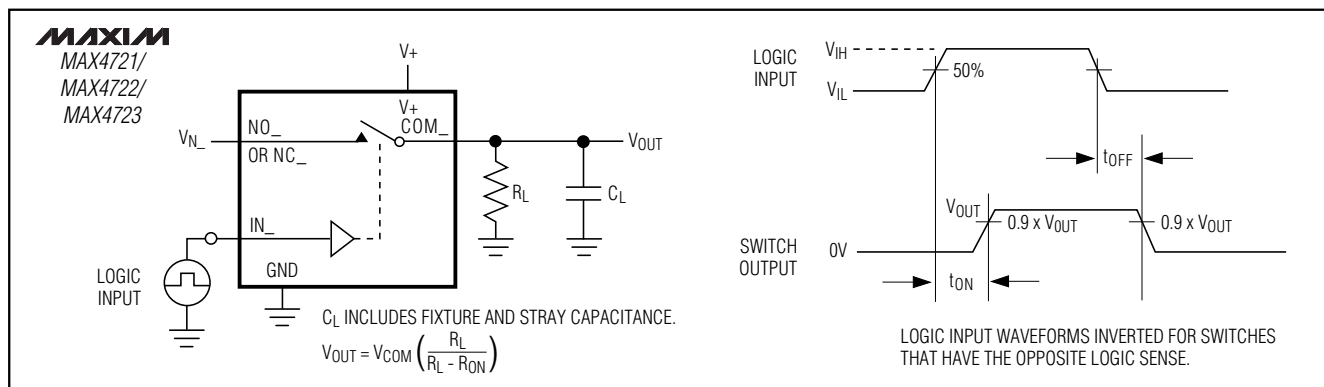


Figure 1. Switching Time

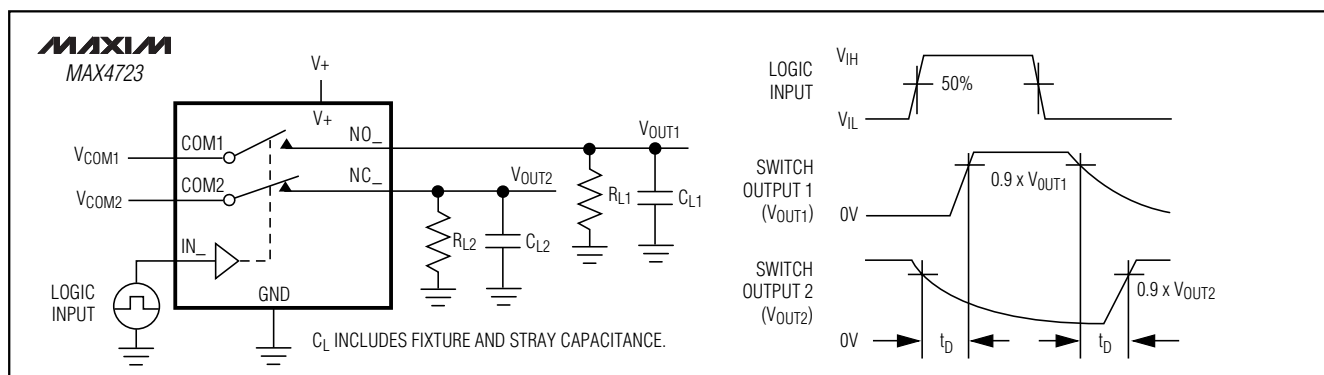


Figure 2. Break-Before-Make Interval

#### Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1μF capacitor connected from V+ to GND is adequate for most applications.

#### Power-Supply Sequencing and Overvoltage Protection

**Caution:** Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

#### UCSP Package Considerations

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Chip-Scale Package).

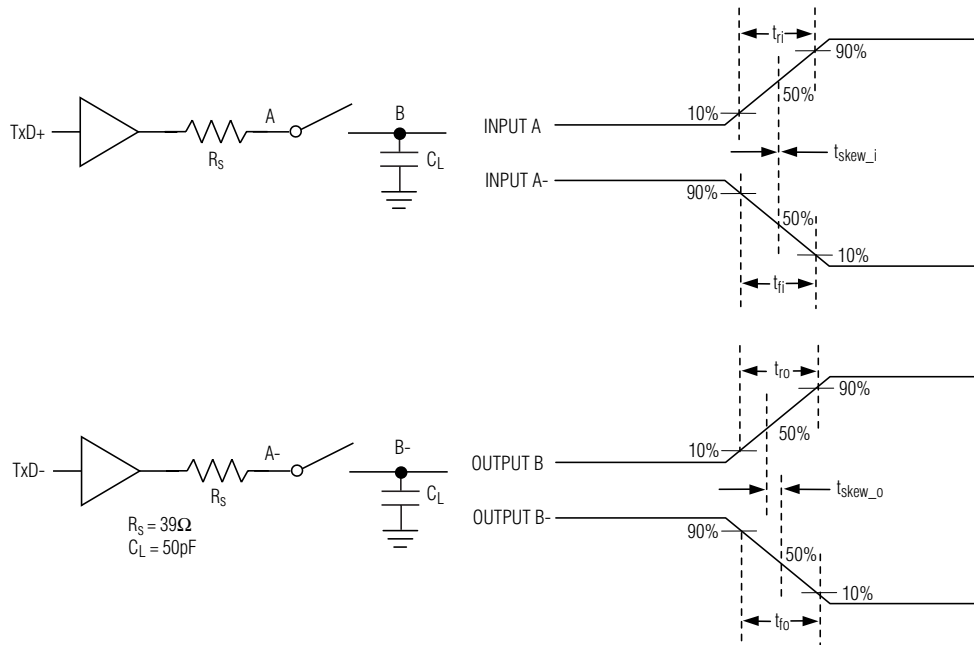
#### UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a UCSP package. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

## 4.5Ω Dual SPST Analog Switches in UCSP

### Test Circuits/Timing Diagrams (continued)



- $|t_{ro} - t_{ri}|$  DELAY DUE TO SWITCH FOR RISING INPUT AND RISING OUTPUT SIGNALS.
- $|t_{fo} - t_{fi}|$  DELAY DUE TO SWITCH FOR FALLING INPUT AND FALLING OUTPUT SIGNALS.
- $|t_{skew\_o}|$  CHANGE IN SKEW THROUGH THE SWITCH FOR OUTPUT SIGNALS.
- $|t_{skew\_i}|$  CHANGE IN SKEW THROUGH THE SWITCH FOR INPUT SIGNALS.

Figure 3. Input/Output Skew Timing Diagram

## 4.5Ω Dual SPST Analog Switches in UCSP

### Test Circuits/Timing Diagrams (continued)

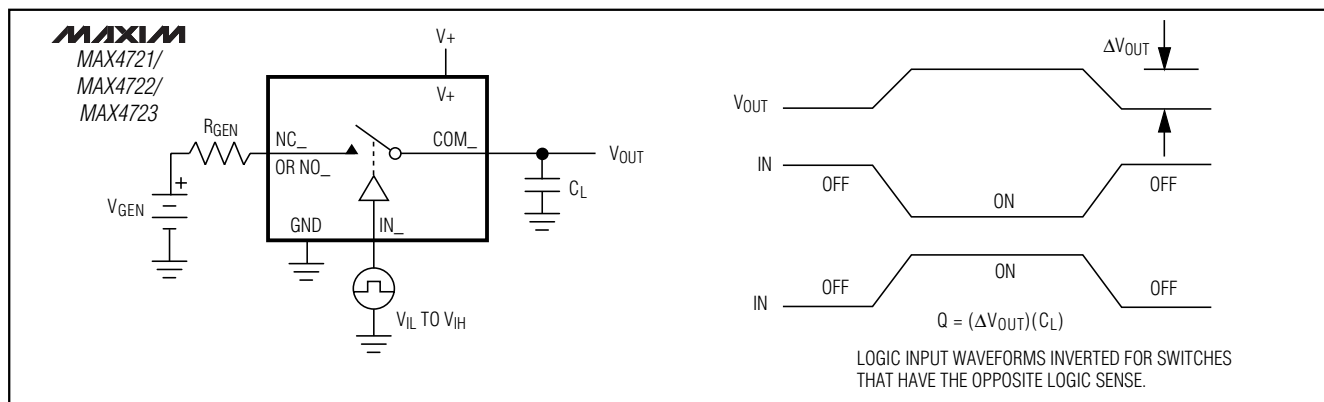


Figure 4. Charge Injection

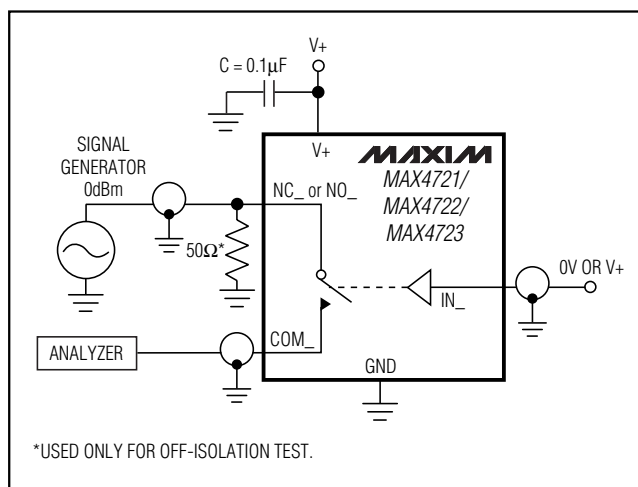


Figure 5a. On-Loss, Off-Isolation, and Crosstalk

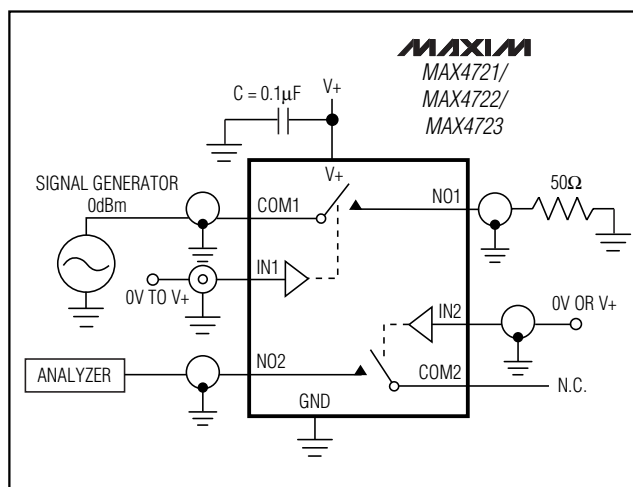


Figure 5b. Crosstalk Test Circuit

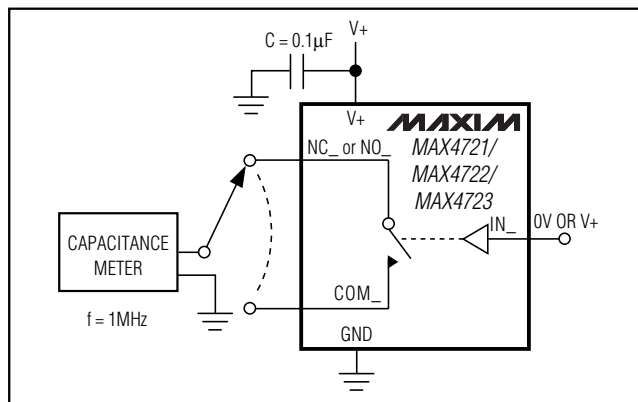


Figure 6. Channel Off/On-Capacitance

### Chip Information

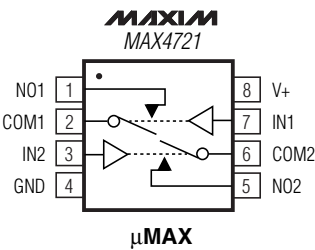
TRANSISTOR COUNT: 181

PROCESS: BiCMOS

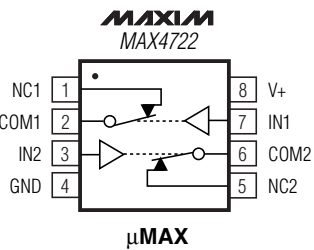
# 4.5Ω Dual SPST Analog Switches in UCSP

## Pin Configurations/Functional Diagrams/Truth Tables (continued)

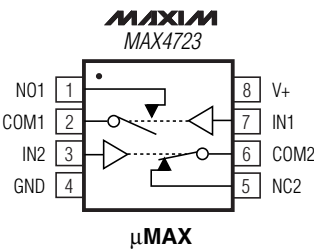
TOP VIEW



| LOGIC | SWITCH |
|-------|--------|
| 0     | OFF    |
| 1     | ON     |



| LOGIC | SWITCH |
|-------|--------|
| 0     | ON     |
| 1     | OFF    |



| LOGIC | SWITCH1 | SWITCH2 |
|-------|---------|---------|
| 0     | OFF     | ON      |
| 1     | ON      | OFF     |

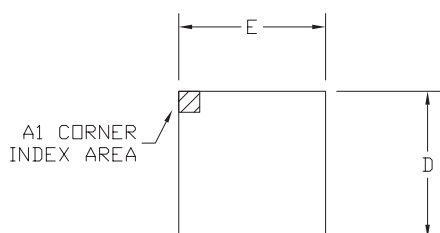
SWITCHES SHOWN FOR LOGIC "0" INPUT

## 4.5Ω Dual SPST Analog Switches in UCSP

### Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4721/MAX4722/MAX4723



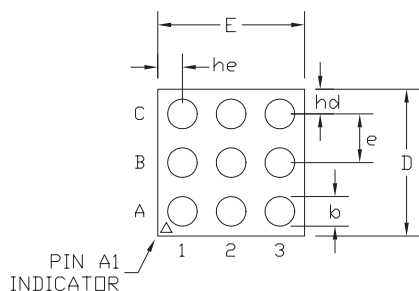
TOP VIEW

| SYMBOL | DIMENSIONS   |
|--------|--------------|
| A      | 0.60±0.05    |
| D      | 1.52±0.05    |
| E      | 1.52±0.05    |
| e      | 0.50 BASIC   |
| b      | ∅ 0.35 BASIC |
| A1     | 0.27±0.04    |
| A2     | 0.33 Ref.    |
| hd     | 0.26 Ref.    |
| he     | 0.26 Ref.    |

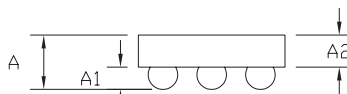
| SOLDER BALL DEPOPULATION |                  |
|--------------------------|------------------|
| PKG. CODE                | DEPOPULATED BALL |
| B9-1                     | NONE             |
| B9-2                     | B2               |
| B9-3                     | B1, B2, B3       |

#### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MEETS JEDEC M0195.



BOTTOM VIEW



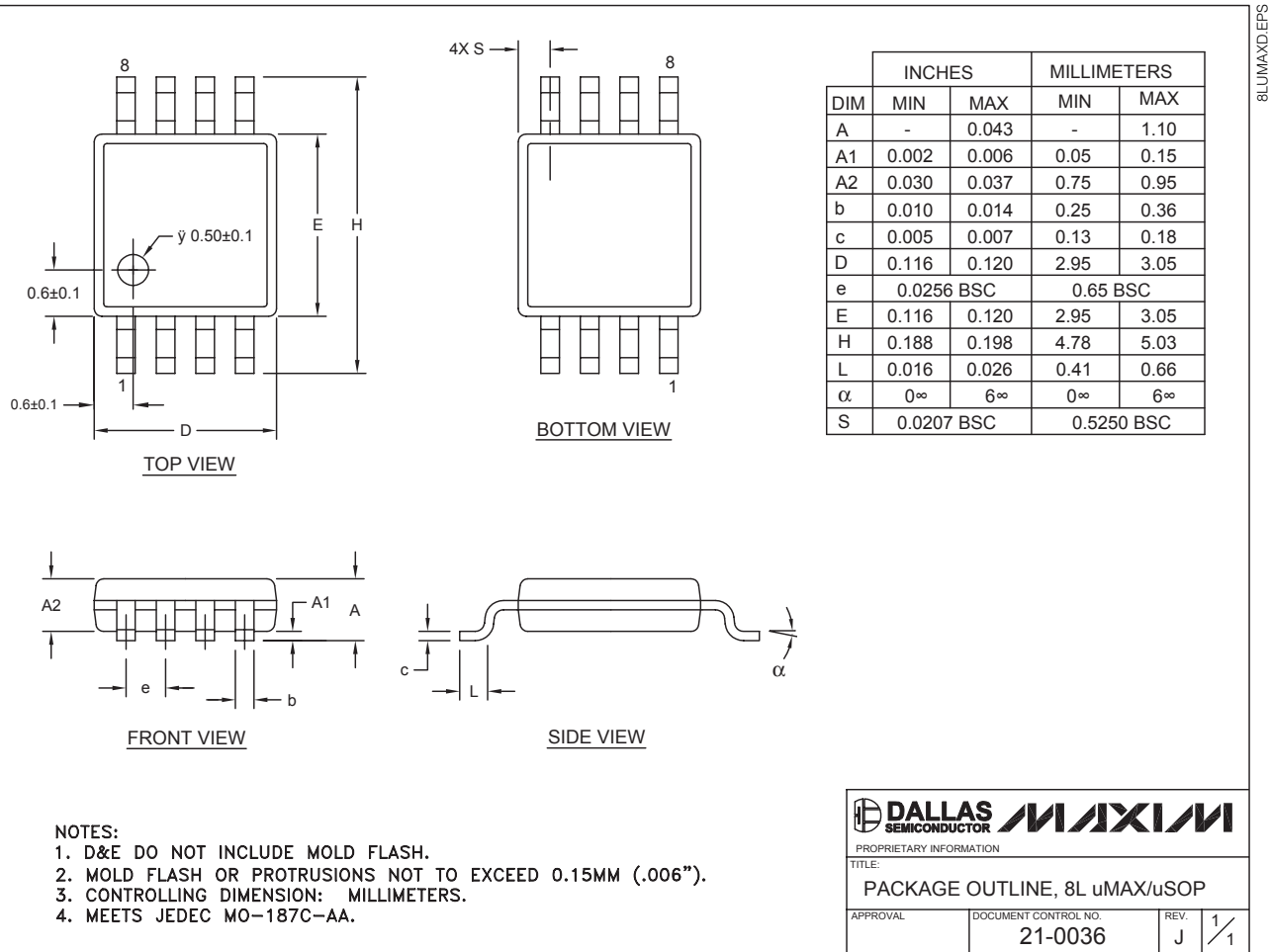
SIDE VIEW

|                                  |                      |      |     |
|----------------------------------|----------------------|------|-----|
| <b>MAXIM</b>                     |                      |      |     |
| PROPRIETARY INFORMATION          |                      |      |     |
| TITLE: PACKAGE OUTLINE, 3×3 UCSP |                      |      |     |
| APPROVAL                         | DOCUMENT CONTROL NO. | REV. | 1/1 |
|                                  | 21-0093              | E    |     |

# 4.5Ω Dual SPST Analog Switches in UCSP

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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