RELIABILITY REPORT

FOR

MAX4649EKA

PLASTIC ENCAPSULATED DEVICES

August 20, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX4649 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation
.....Attachments

I. Device Description

A. General

The MAX4649 is a dual-supply, single-pole/double-throw (SPDT) analog switch. On-resistance is 45 max and flat (7 max) over the specified signal range. The MAX4649 can handle Rail-to-Rail® analog signals, and conducts analog or digital signals equally well in either direction. This switch operates from a single +9V to +36V supply, or from ±4.5V to ±20V dual supplies. The primary application areas are in the switching and routing of signals in telecommunications and test equipment.

The MAX4649 features a switch transition time of 130ns max at +25°C, and a guaranteed break-before-make switching time of 5ns. Off-leakage current is only 2nA max at +25°C.

The MAX4649 is available in a tiny 8-pin SOT23 package.

B. Absolute Maximum Ratings

Item	Rating
V+	-0.3V to +44.0V
V-	-44.0V to +0.3V
V+ to V-	-0.3V to +44.0V
All Other Pins (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into any Terminal	±10mA
Continuous Current (COM, NO, NC)	±30mA
Peak Current (COM, NO, NC) (pulsed at 1ms, 10% duty cycle)	±60mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SOT23	714mW
Derates above +70°C	
8-Pin SOT23	8.9mW/°C

Note 1: Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	Octal 8-Bit Serial DAC with Output Buffer
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	33
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	8-Pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1201-0218
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	57 x 43 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: : Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 100 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5703) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1I**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AH58 die type has been found to have all pins able to withstand a transient pulse of ± 400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4649EKA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

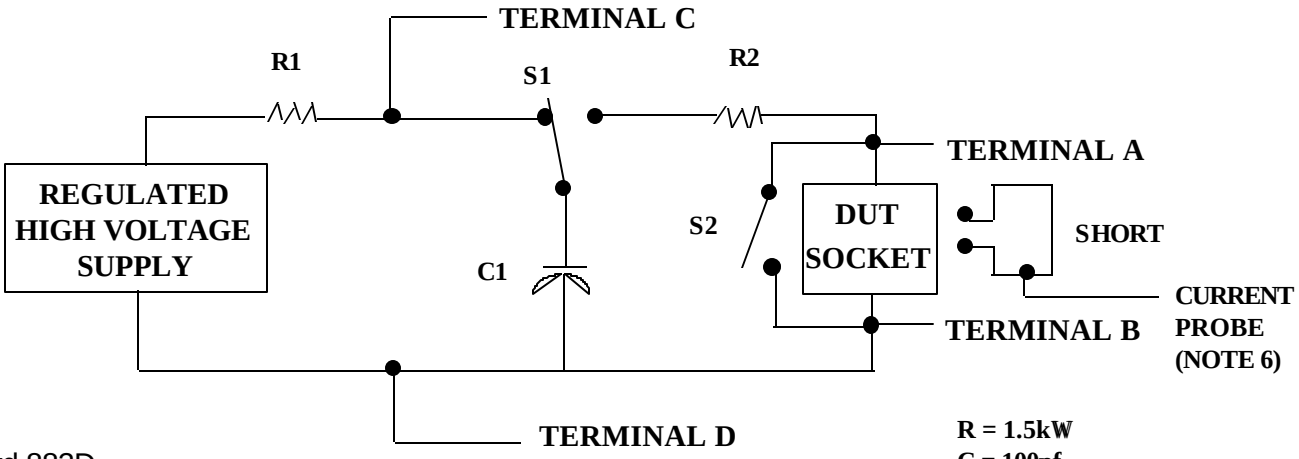
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

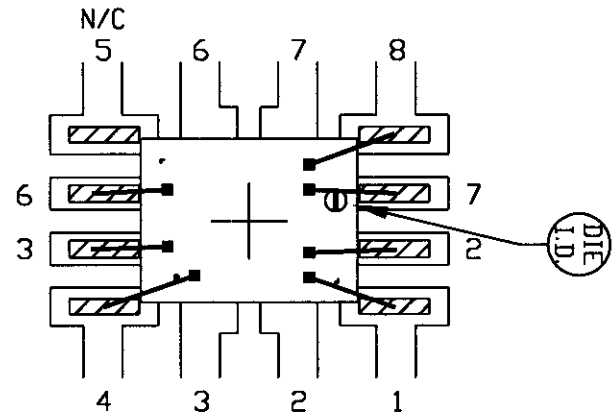
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

Table 1
Reliability Evaluation Test Results



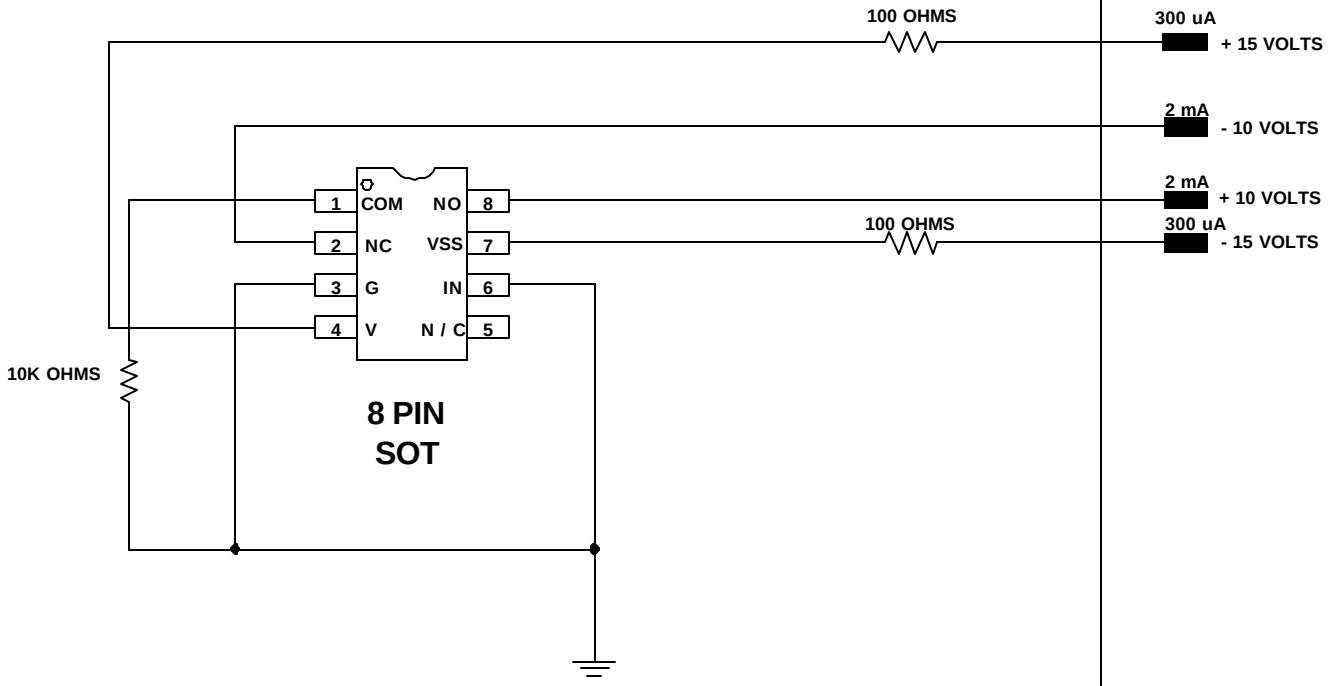
Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: K8C-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: CHIP ON LEAD	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0218	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES : MAX 4649

MAX. EXPECTED CURRENT= (+/- 15V) 300 uA; (+/- 10V) 2 mA

NOTES:

DOCUMENT I.D. 06-5703	**REVISION** A	***MAXIM*** **TITLE: BI Circuit (MAX 4649)**	**PAGE** 2 OF 3