MAX44267

+15V Single-Supply, Dual Op Amp with ±10V Output Range

General Description

The MAX44267 precision, low-noise, low-drift dual operational amplifier offers true-zero output that allows the output to cross zero maximizing the dynamic range of an ADC and increasing resolution. In addition, the input common-mode range extends from +13.5V down to -12V. The MAX44267 integrates charge-pump circuitry that generates the negative voltage rail in conjunction with external capacitors. This allows the amplifier to operate from a single +4.5V to +15V power supply, but it is as effective as a normal dual-rail ±4.5V to ±15V amplifier. The architecture eliminates the need for a negative power-supply rail, saving system cost and size.

The MAX44267 is unity-gain stable with a gain-bandwidth product of 5MHz. The device features low offset voltage of 50µV (max), drift of 0.4µV/°C (max), and 200nV$_{P-P}$ noise from 0.1Hz to 10Hz. The low offset and noise specifications and wide input common-mode range make the device ideal for sensor transmitters and interfaces. Varying the external charge pump capacitors enables the charge-pump noise to be minimized.

The MAX44267 is part of a family of signal chain ICs including amplifiers, multiplexers and ADCs. These ICs eliminate the need for a negative supply to the multiplexer, amplifier and ADC, saving space and cost. See the *Typical Application Circuit* and Table 1 for more information. See the MAX44247 for the same amplifier with internal charge-pump capacitors in a small 8-pin µMAX® package.

The MAX44267 is available in a 14-pin TSSOP package and is specified over the -40°C to +125°C operating temperature range.

***Ordering Information* appears at end of data sheet.**

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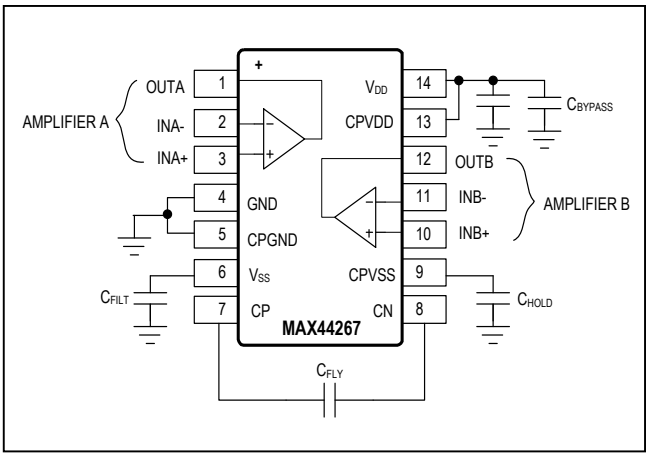
Benefits and Features

- True Bipolar Output Greater than ±10V from a Single +15V Supply Eliminates Space and Cost of Negative Power Supply
  - True Zero Output from a Single Supply
- High-Accuracy Sensing Over Temperature
  - Low Input V_{OS}: 50µV (max)
  - Low 0.4µV/°C (max) of Offset Drift
- 9nV/√Hz Low Input Noise at 1kHz Provides Wide ADC Dynamic Range
- 5MHz Gain-Bandwidth Product Provides Wide Frequency Input Range
- Low 2.4mA (max) Quiescent Current Enables Lower Power Dissipation and Cooler Operation
- Integrated EMI Filter Reduces Sensitivity to Motors and Other High-Frequency Noise Generators
- 14-Pin TSSOP Package with External Charge-Pump Capacitors Enables Noise Optimization

Applications

- PLC Analog I/O Modules
- Sensor Interfaces
- Pressure Sensors
- Bridge Sensors
- Analog Level Shifting/Conditioning

Block Diagram



Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +16.5V
CPVDD to GND.....-0.3V to +16.5V
CP, CN, CPVSS, V_{SS} Input Current .....±20mA
Common-Mode Input Voltage.... ($-V_{DD}$ - 0.3V) to ($+V_{DD}$ + 0.3V)
Differential Input Current .....±20mA
Differential Input Voltage (Note 1).....±1V
OUTA, OUTB to GND..... ($-V_{DD}$ - 0.3V) to ($+V_{DD}$ + 0.3V)
Short-Circuit Duration, OUTA, OUTB to either Supply Rail 1s

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 10mW/°C above +70°C).....796.8mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65ºC to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1V are applied, limit input current to ±20mA.

Package Thermal Characteristics (Note 2)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....100.4°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....30°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, R_L = 5kΩ to GND, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Power-Supply Voltage Input Range	V_{DD}	Guaranteed by PSRR		4.5		15.5	V
Charge-Pump Supply Voltage Input Range (Note 4)	CPV_{DD}			4.5		15.5	V
Charge-Pump Negative Supply Output	CPV_{SS}	V_{DD} = 15V, R_L = ∞			-14.8		V
		V_{DD} = 5V, R_L = ∞			-4.8		
Filtered Negative Supply Output	V_{SS}	V_{DD} = 15V, R_L = 5kΩ			-13		V
		V_{DD} = 5V, R_L = 5kΩ			-3.6		
Power-Supply Rejection Ratio	PSRR		T_A = +25°C	117	137		dB
		+4.5V ≤ V_{DD} ≤ +15.5V	-40°C ≤ T_A ≤ +125°C	112			
Total Quiescent Current	I_{DD}	R_L = ∞	T_A = +25°C		2.4	3.6	mA
			-40°C ≤ T_A ≤ +125°C			4.0	
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	V_{DD} = 15V	-12.0		+13.5	V
			V_{DD} = 5V	-2.0		+3.5	
Common-Mode Rejection Ratio	CMRR	V_{DD} = 15V, V_{CM} = -12V to +13.5V	T_A = +25°C	138	150		dB
			-40°C ≤ T_A ≤ +125°C	122			
		V_{DD} = 5V, V_{CM} = -2V to +3.5V	T_A = +25°C	125	140		dB
			-40°C ≤ T_A ≤ +125°C	118			

Electrical Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, R_L = 5kΩ to GND, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

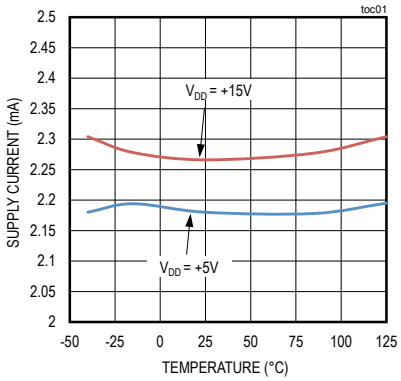
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C			4	45	µV
		-40°C ≤ T_A ≤ +125°C				50	
Input Offset Voltage Drift (Note 5)	TCV_{OS}	-40°C ≤ T_A ≤ +125°C			0.1	0.4	µV/°C
Input Bias Current	I_B	T_A = +25°C			0.5	1.5	nA
		-40°C ≤ T_A ≤ +125°C				2.5	
Input Offset Current	I_{OS}	T_A = +25°C			0.3	1.0	nA
		-40°C ≤ T_A ≤ +125°C				2.0	
Open-Loop Gain	A_{VOL}	V_{DD} = 15V, -11V ≤ V_{OUT} ≤ +13.5V	T_A = +25°C	136	145		dB
			-40°C ≤ T_A ≤ +125°C	129			
		V_{DD} = 5V, -1.3V ≤ V_{OUT} ≤ +3.5V	T_A = +25°C	130	140		
			-40°C ≤ T_A ≤ +125°C	121			
Input Resistance	R_{IN}				50		MΩ
Maximum Output Current	I_{OUT}	Sinking			17		mA
		Sourcing			36		
Output Voltage Swing High (V_{OUT} to GND)	V_{OH}	V_{DD} = 15V, R_L = 5kΩ, both channels driven		13.8	14.8		V
		V_{DD} = 5V, R_L = 5kΩ, both channels driven		3.8	4.9		
Output Voltage Swing Low (V_{OUT} to GND)	V_{OL}	V_{DD} = 15V, R_L = 5kΩ, both channels driven		-11.3	-12.7		V
		V_{DD} = 5V, R_L = 5kΩ,both channels driven		-1.5	-3.5		V
AC SPECIFICATIONS							
Input Voltage-Noise Density	e_N	f = 1kHz			9		nV/√Hz
Input Voltage Noise		0.1Hz < f < 10Hz			200		nV_{P-P}
Input Current-Noise Density	i_N	f = 1kHz			200		fA/√Hz
Gain-Bandwidth Product	GBW				5		MHz
Slew Rate	SR				3		V/µs
Total Harmonic Distortion	THD	f = 1kHz, V_{OUT} = $2V_{P-P}$, A_V = +1V/V			-100		dB
Capacitive Loading	C_L	No sustained oscillation, A_V = +1V/V			300		pF
Charge-Pump Frequency	f_{OSC}				500		kHz
Charge-Pump Feedthrough					2		mV
Crosstalk	X_{talk}	f = 1kHz			-100		dB
Settling Time	t_S				1		µs

Note 3: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 4: CPVDD voltage must be equal to V_{DD} voltage. Connect CPVDD to V_{DD}.
Note 5: Parameter is guaranteed by design.

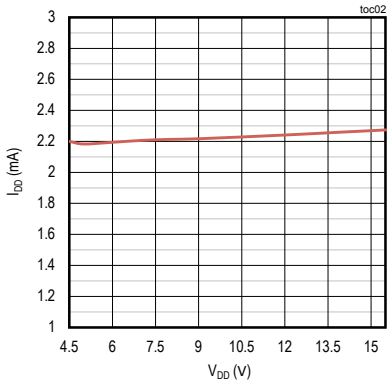
Typical Operating Characteristics

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

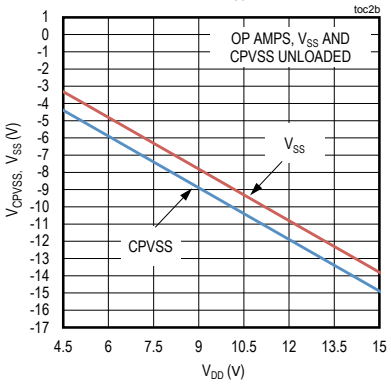
TOTAL SUPPLY CURRENT vs. TEMPERATURE



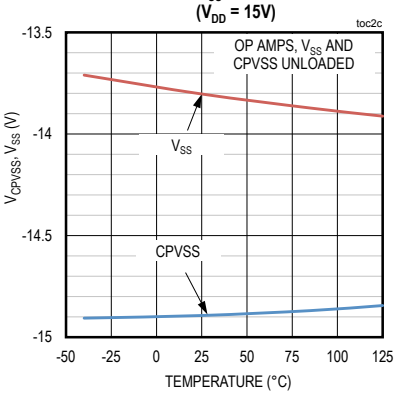
TOTAL SUPPLY CURRENT vs. V_{DD}



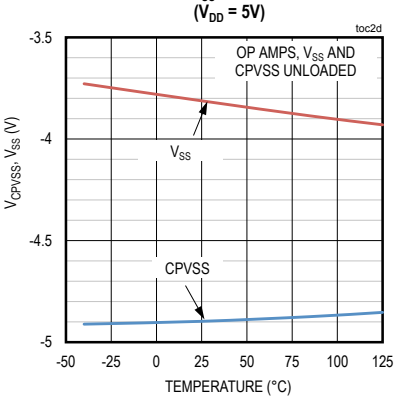
CPVSS AND V_{SS} vs. V_{DD}



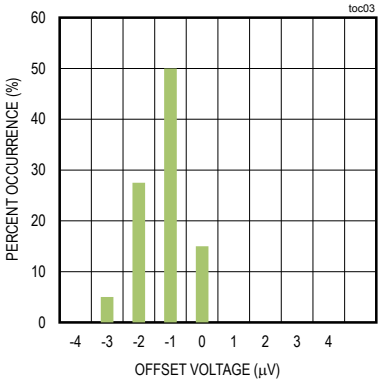
CPVSS AND V_{SS} vs. TEMPERATURE (V_{DD} = 15V)



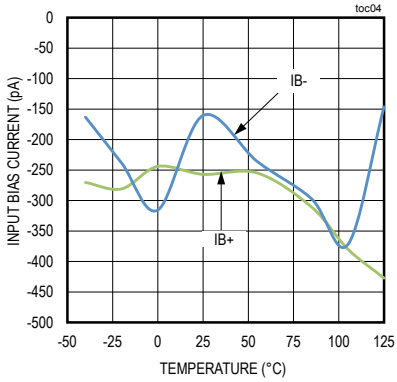
CPVSS AND V_{SS} vs. TEMPERATURE (V_{DD} = 5V)



INPUT OFFSET VOLTAGE HISTOGRAM



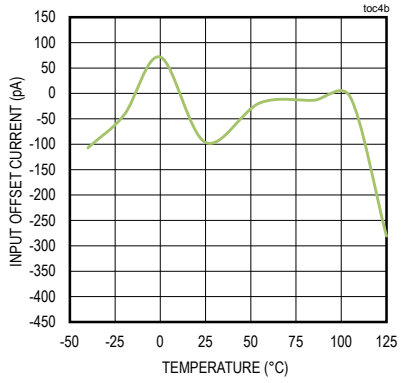
INPUT BIAS CURRENT vs. TEMPERATURE



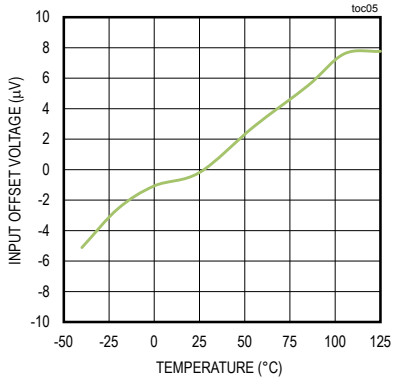
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

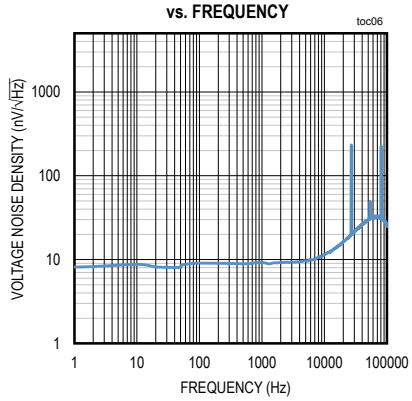
INPUT OFFSET CURRENT vs. TEMPERATURE



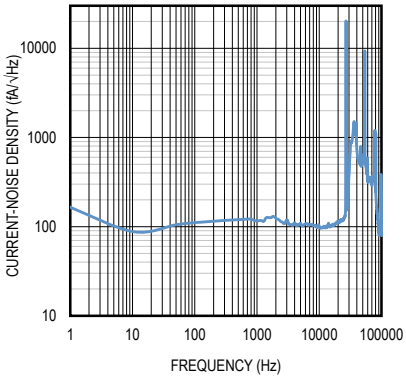
INPUT OFFSET VOLTAGE vs. TEMPERATURE



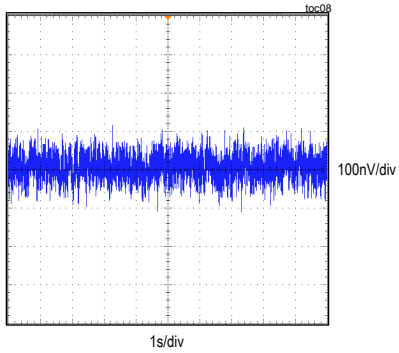
INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY



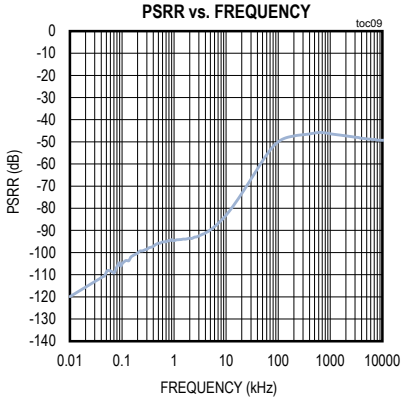
INPUT CURRENT-NOISE DENSITY vs. FREQUENCY



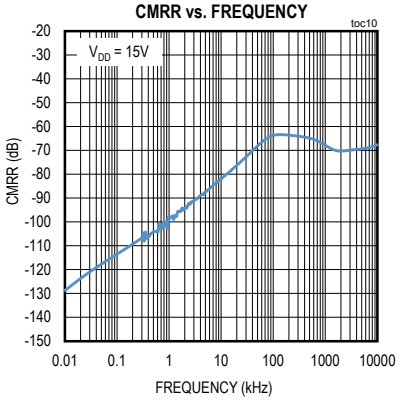
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE



PSRR vs. FREQUENCY



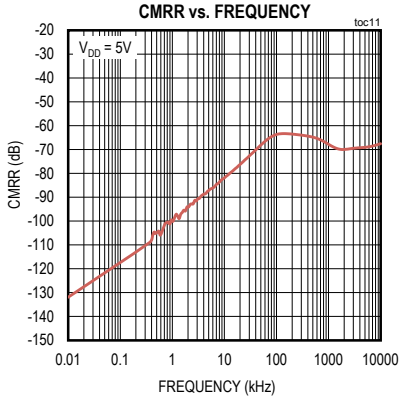
CMRR vs. FREQUENCY



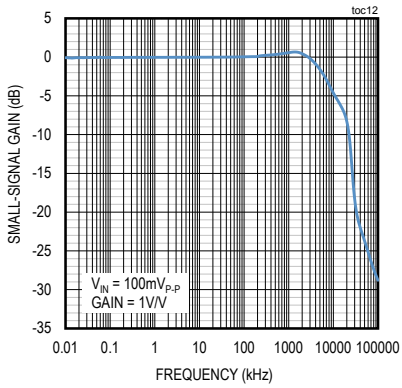
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

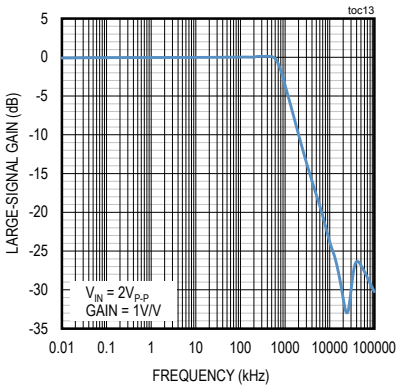
CMRR vs. FREQUENCY



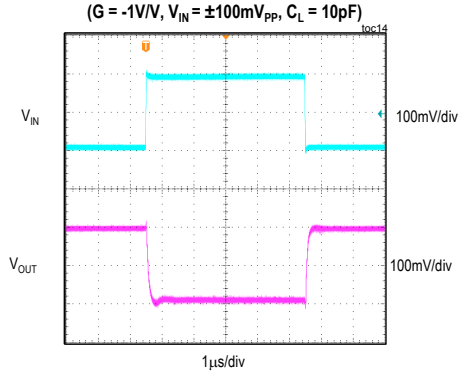
SMALL-SIGNAL GAIN vs. FREQUENCY



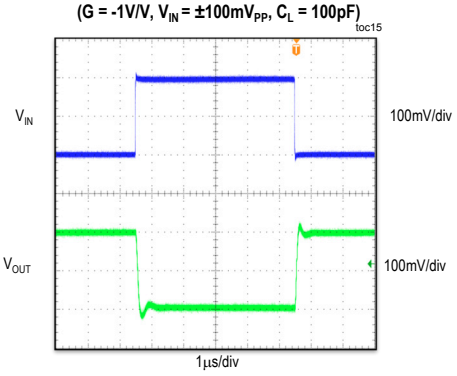
LARGE-SIGNAL GAIN vs. FREQUENCY



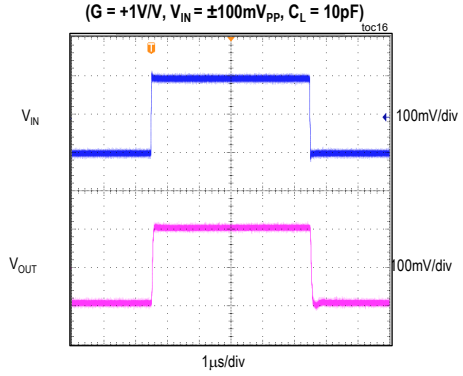
SMALL-SIGNAL STEP RESPONSE
(G = -1V/V, V_{IN} = ±100mV_{PP}, C_L = 10pF)



SMALL-SIGNAL STEP RESPONSE
(G = -1V/V, V_{IN} = ±100mV_{PP}, C_L = 100pF)



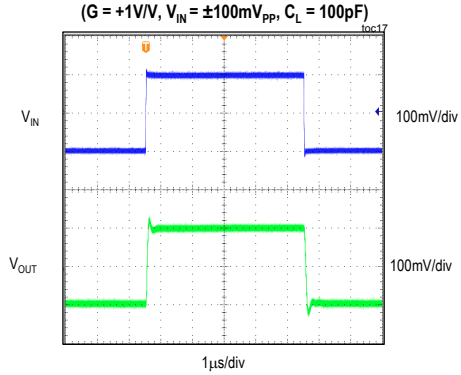
SMALL-SIGNAL STEP RESPONSE
(G = +1V/V, V_{IN} = ±100mV_{PP}, C_L = 10pF)



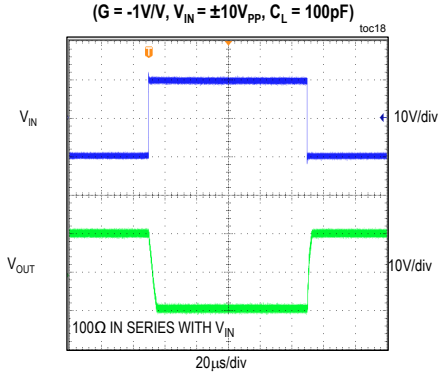
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

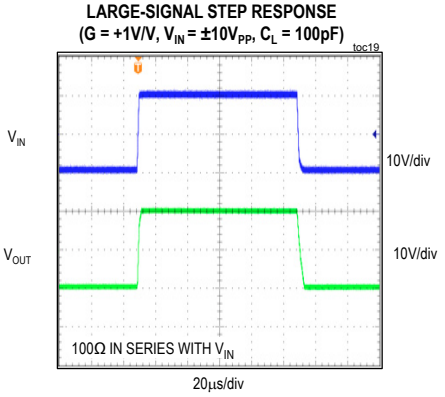
SMALL-SIGNAL STEP RESPONSE
(G = +1V/V, V_{IN} = ±100mV_{PP}, C_L = 100pF)



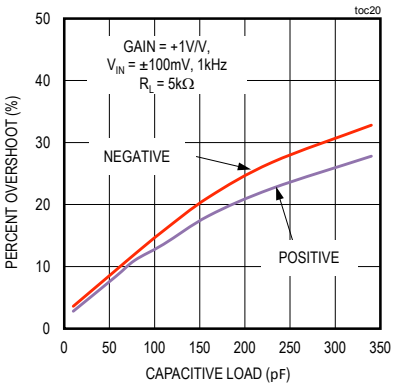
LARGE-SIGNAL STEP RESPONSE
(G = -1V/V, V_{IN} = ±10V_{PP}, C_L = 100pF)



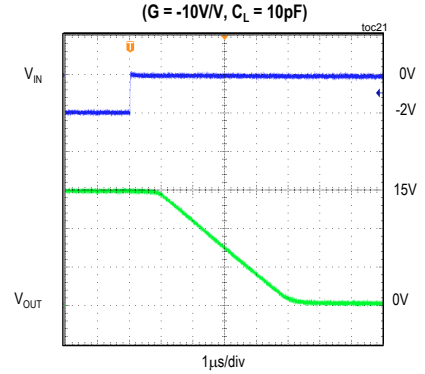
LARGE-SIGNAL STEP RESPONSE
(G = +1V/V, V_{IN} = ±10V_{PP}, C_L = 100pF)



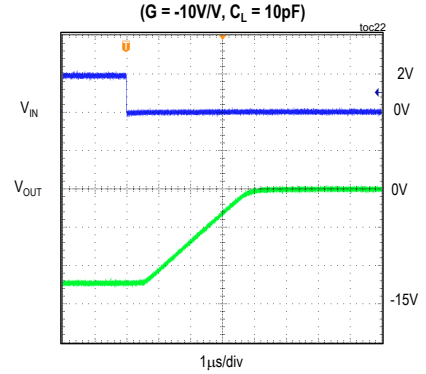
PERCENT OVERSHOOT vs. CAPACITIVE LOAD



NEGATIVE OVERLOAD RECOVERY
(G = -10V/V, C_L = 10pF)



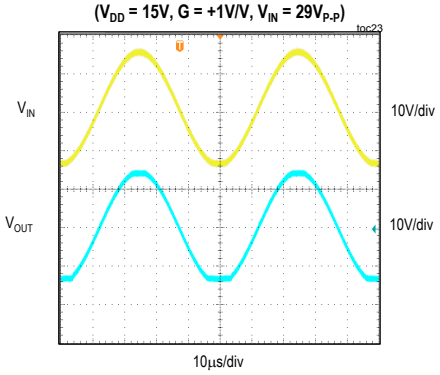
POSITIVE OVERLOAD RECOVERY
(G = -10V/V, C_L = 10pF)



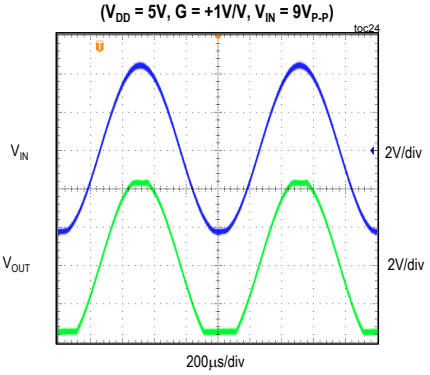
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

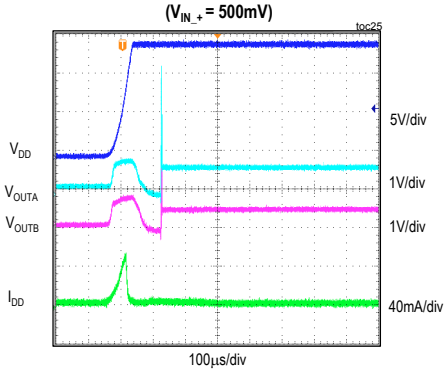
NO PHASE REVERSAL
(V_{DD} = 15V, G = +1V/V, V_{IN} = 29V_{P-P})



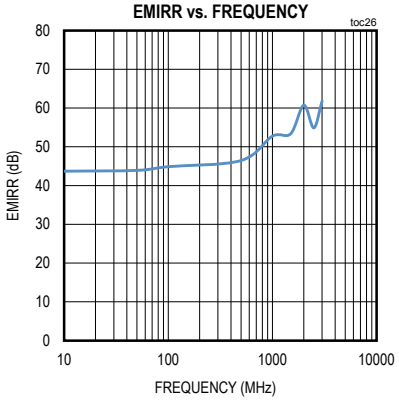
NO PHASE REVERSAL
(V_{DD} = 5V, G = +1V/V, V_{IN} = 9V_{P-P})



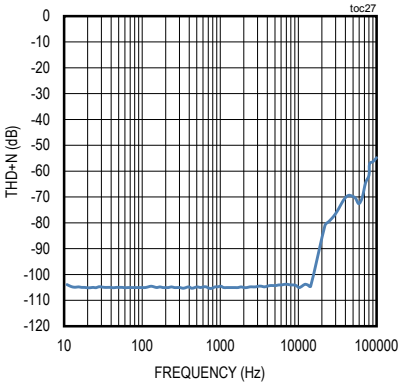
TURN-ON TRANSIENT
(V_{IN_+} = 500mV)



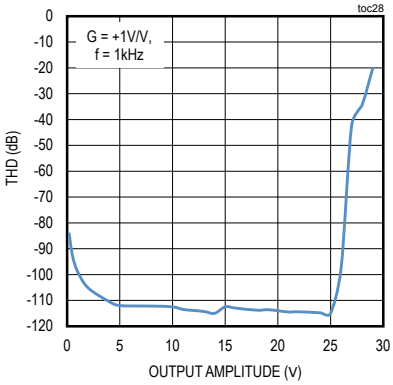
EMIRR vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE
vs. FREQUENCY



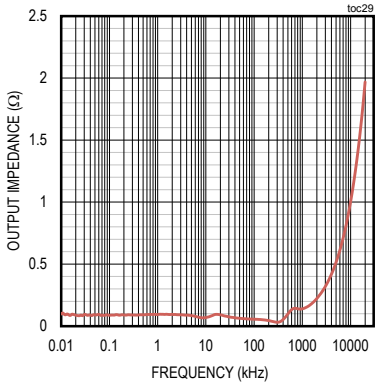
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. OUTPUT AMPLITUDE



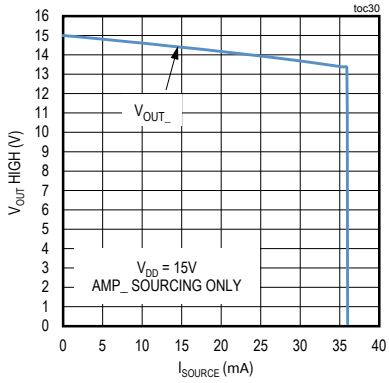
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

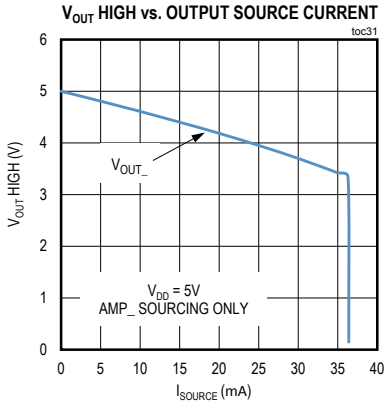
OUTPUT IMPEDANCE vs. FREQUENCY



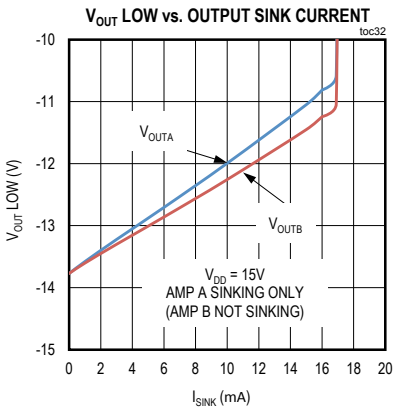
V_{OUT} HIGH vs. OUTPUT SOURCE CURRENT



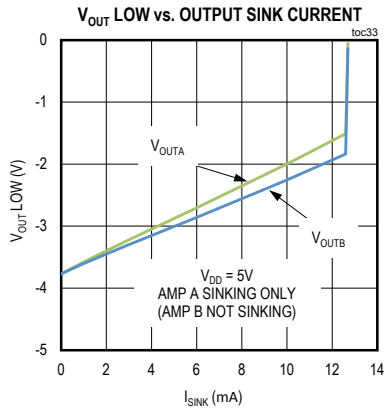
V_{OUT} HIGH vs. OUTPUT SOURCE CURRENT



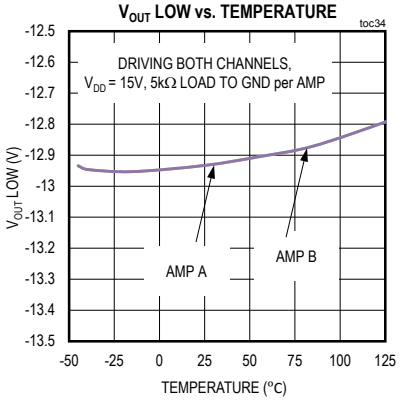
V_{OUT} LOW vs. OUTPUT SINK CURRENT



V_{OUT} LOW vs. OUTPUT SINK CURRENT



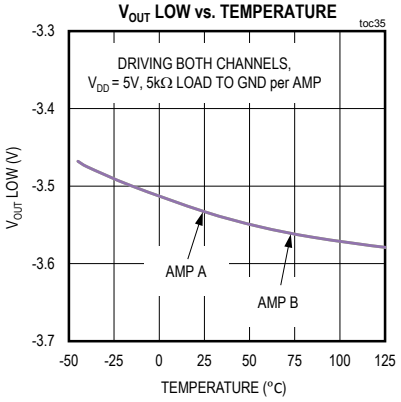
V_{OUT} LOW vs. TEMPERATURE



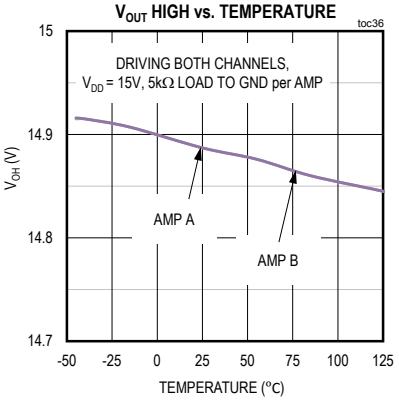
Typical Operating Characteristics (continued)

(V_{DD} = V_{CPVDD} = 15V, V_{GND} = V_{CPGND} = 0V, V_{CM} = 0V, C_{FLY} = 0.022µF, C_{HOLD} = 0.1µF, C_{FILT} = 0.1µF, R_L = 5kΩ and C_L = 10pF to GND, T_A = +25°C, unless otherwise noted.)

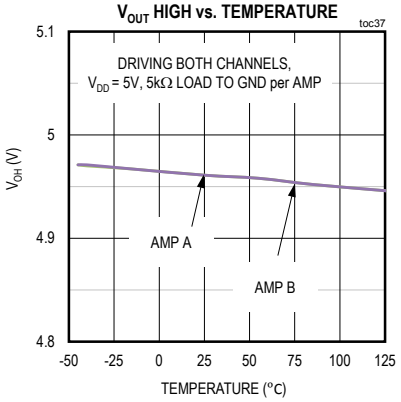
V_{OUT} LOW vs. TEMPERATURE



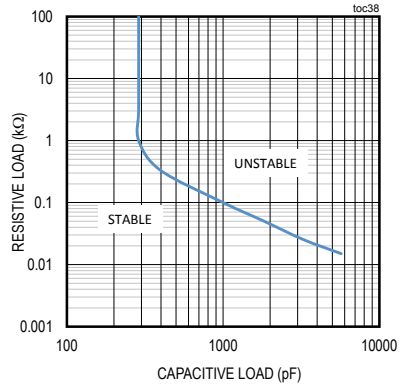
V_{OUT} HIGH vs. TEMPERATURE



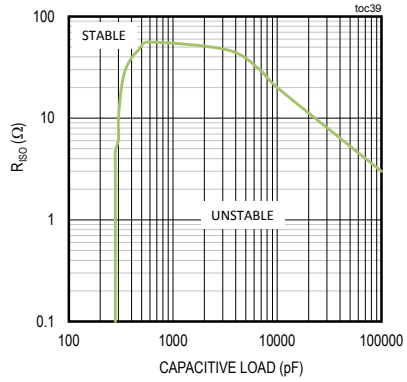
V_{OUT} HIGH vs. TEMPERATURE



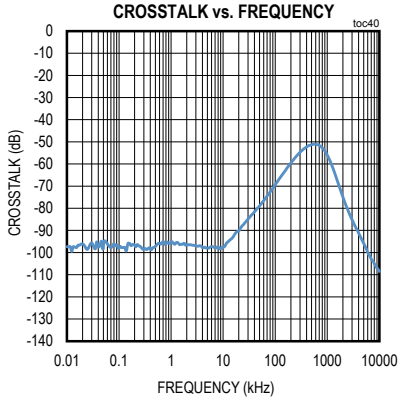
STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTANCE



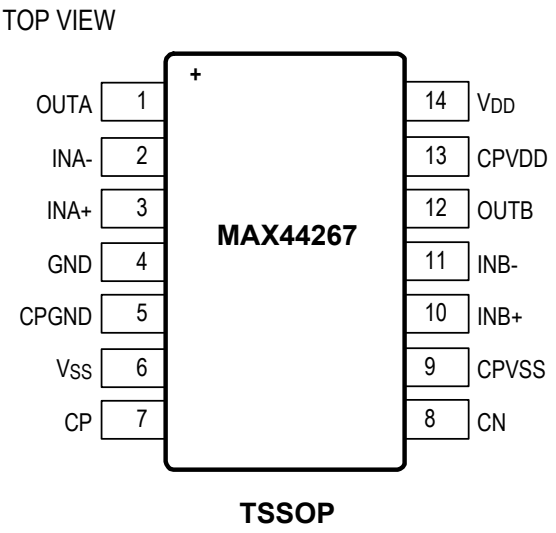
STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTANCE



CROSSTALK vs. FREQUENCY



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	OUTA	Channel A Output
2	INA-	Channel A Negative Input
3	INA+	Channel A Positive Input
4	GND	Ground. Connect GND to a solid ground plane.
5	CPGND	Charge-Pump Ground. Connect CPGND to GND.
6	V_{SS}	Filtered Negative Supply Output. Bypass V_{SS} with a low-ESR capacitor (C_{FILT} = 1µF) to GND.
7	CP	Charge-Pump Positive Capacitor Connection. Capacitor connection only to CN. Do not connect any voltage on CP or CN. Connect a low-ESR capacitor (C_{FLY} = 0.022µF) between CP and CN.
8	CN	Charge-Pump Negative Capacitor Connection. Capacitor connection only to CP. Do not connect any voltage on CN or CP. Connect a low-ESR capacitor (C_{FLY} = 0.022µF) between CP and CN.
9	CPVSS	Charge Pump Negative Supply Output. Bypass CPVSS with a 0.1µF capacitor to CPGND.
10	INB+	Channel B Positive Input
11	INB-	Channel B Negative Input
12	OUTB	Channel B Output
13	CPVDD	Charge-Pump Supply Voltage Input. Connect CPVDD to V_{DD}. Bypass CPVDD with a 0.1µF capacitor to GND.
14	V_{DD}	Device Supply Voltage Input. Bypass V_{DD} with a 0.1µF capacitor to GND.

Detailed Description

The MAX44267 is a high-precision amplifier that provides less than 50µV of maximum input-referred offset and low 1/f noise. These characteristics are achieved by using a combination of proprietary auto-zeroing and chopper-stabilized techniques. This combination of auto-zeroing and chopping ensures that these amplifiers give all the benefits of zero-drift amplifiers, while still ensuring low noise, minimizing chopper spikes, and providing wide bandwidth.

Common Internal Charge Pump

The MAX44267's integrated charge pump produces a negative voltage rail (V_{SS}) that is common to both amplifiers (see Figure 1 for external capacitor connections). The device consumes a total of 4mA (max) of quiescent current (including both the op amps and the charge-pump operation).

The V_{SS} generator acts as a negative supply for the MAX44267, and has limited sink current capability. Attempting to load more than its capability will reduce the negative supply voltage, affecting its driving capability when sinking current. Sinking beyond typically 17mA per channel will result in reduced swing in the negative direction and increased ripple affecting both outputs and degrading output accuracy and performance of both amplifiers.

The output V_{SS} negative supply is common to both amplifier channels. Loading the output of one channel beyond the recommended value will affect the second amplifier channel as mentioned above. The total loading of both channels must be kept below 17mA. If one channel is minimally loaded, for example, only sinking 100µA, the other channel may sink 16.9mA. As shown in Figure 2, when using V_{DD} of +15V the V_{SS} output will be around -13.6V (typ) at no load. As amplifier A is sinking, it causes the V_{SS} rail to rise and this is reflected in V_{OUTB}.

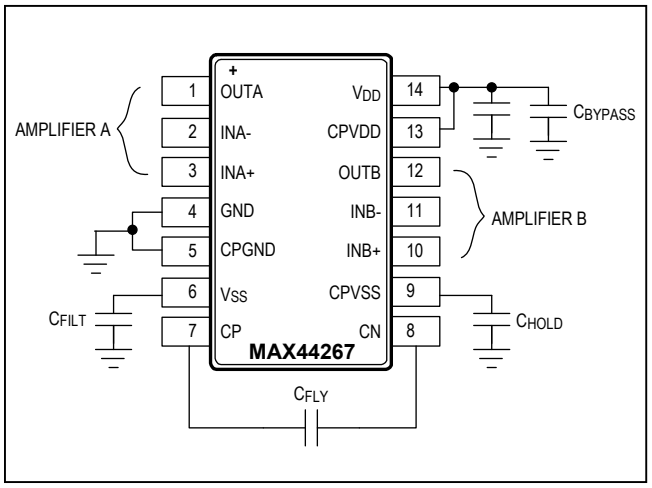


Figure 1. External Capacitor Connections

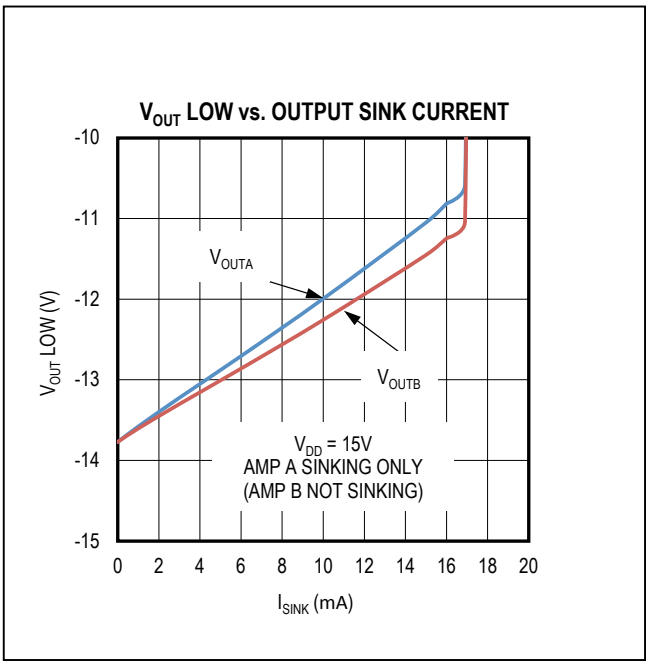


Figure 2. V_{OUT} LOW vs. OUTPUT SINK CURRENT

ESD Networks

The MAX44267 output swing can be well below 0V while all the other circuitry on the board may have 0V as its most negative terminal. Since almost all modern integrated circuits protect their inputs with a network of diode clamps to their power rails, it is possible to discover the driven circuit is clamping the MAX44267's output (Figure 3).

Maxim Integrated has many products that have inputs that can be driven Beyond the Rails: ADCs, multiplexers and current-sensing amplifiers. Other circuitry should be designed such that the MAX44267's output will not be clamped by another circuit's ESD network. A common solution to this problem is to arrange that the output is level-shifted as well as amplified or conditioned by the MAX44267. Be sure not to exceed the absolute maximum ratings on any devices surrounding the MAX44267 amplifier.

Capacitor Selection

The MAX44267 requires three external capacitors (C_{FLY}, C_{HOLD}, and C_{FILT}) to generate the V_{SS} negative supply rail. The charge-pump output resistance is a function of the ESR of C_{FLY}, C_{HOLD}, and C_{FILT}. To maintain the lowest output resistance, use capacitors with low ESR.

Flying Capacitor (C_{FLY})

Increasing the flying capacitor's value reduces the output resistance. Above 0.047µF, increasing C_{FLY}'s capacitance has negligible effect because internal switch resistance and capacitor ESR then dominate the output resistance.

Output Capacitor (C_{HOLD})

Increasing the output capacitor's value reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Lower capacitance values can be

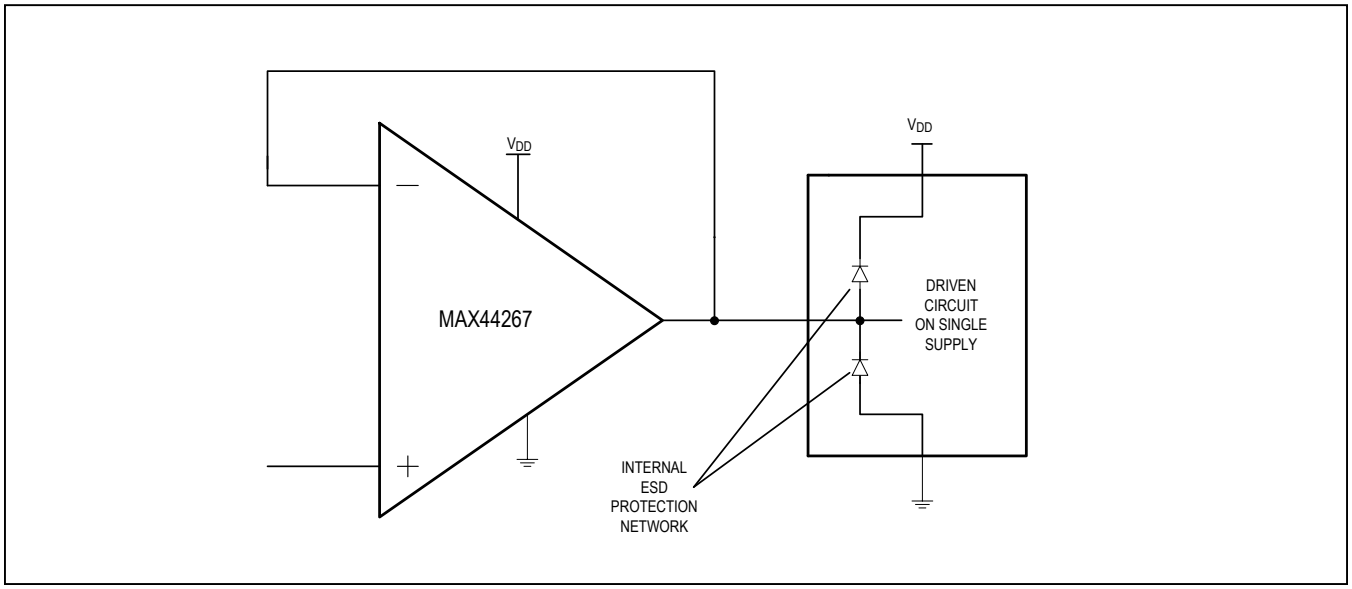


Figure 3. Possibility of Clamping the MAX44267 Output via Another Circuit's ESD Network

used with light loads if higher output ripple can be tolerated. Refer to the following graphs to estimate the peak-to-peak ripple for certain sinking current value.

CPVSS Bypass Capacitor

Bypass the incoming supply (CPVSS) to reduce its AC impedance and the impact of the charge pump's switching noise. Connect a minimum of a 0.1µF low-ESR capacitor from CPVSS to CPGND as close as possible to the IC.

Noise Suppression

Low-frequency noise, inherent in all active devices, is inversely proportional to frequency. Charges at the oxide-silicon interface that are trapped-and-released by oxide and PN junction occur at low frequency more often. The MAX44267 eliminates the 1/f noise internally, thus making it an ideal choice for DC or low frequency, high-precision applications. The 1/f noise appears as a slow varying offset voltage and is eliminated by the chopping technique used.

Electromagnetic interference (EMI) noise occurs at higher frequency that results in malfunction or degradation of electrical equipment. The ICs have an input EMI filter to avoid the output being affected by radio frequency interference. The EMI filter composed of passive devices presents significant higher impedance to higher frequency.

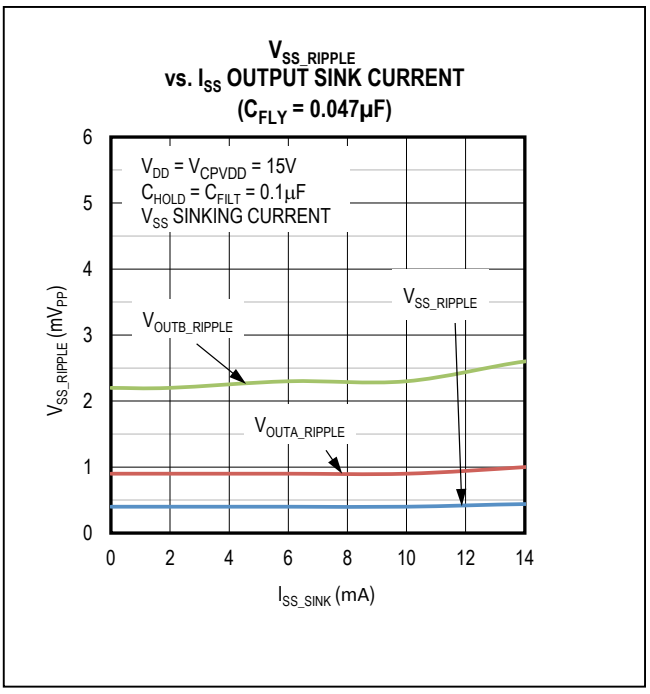


Figure 5. $I_{OUTSINK}$ vs. V_{SS_RIPPLE} (C_{FLY} = 0.047µF, C_{HOLD} = C_{FILT} = 0.1µF)

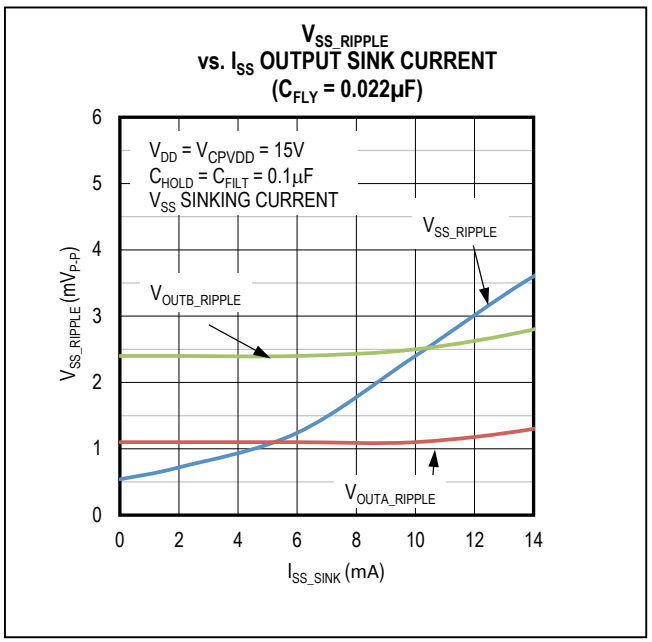


Figure 4. $I_{OUTSINK}$ vs. V_{SS_RIPPLE} (C_{FLY} = 0.022µF, C_{HOLD} = C_{FILT} = 0.1µF)

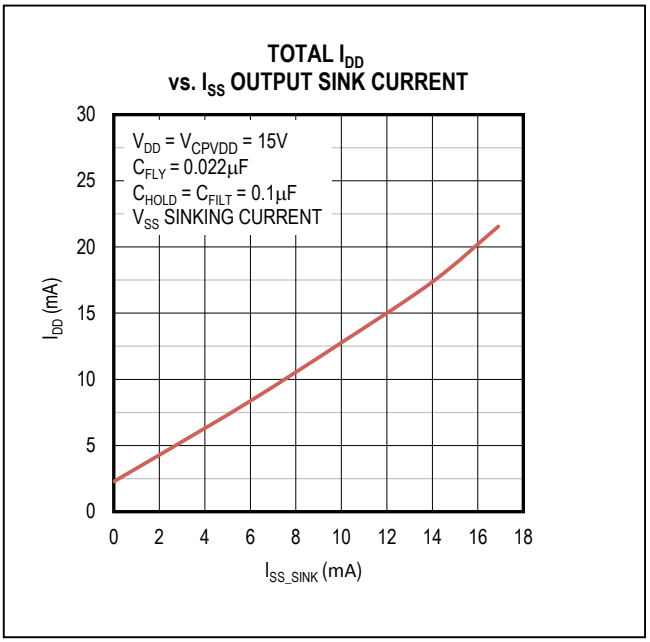


Figure 6. Total Supply Current vs. I_{SINK}

True Zero Output Architecture

The MAX44267 is unique compared to the majority of operational amplifiers. The MAX44267 contains an internal charge pump that generates a negative voltage rail (V_{SS}), shared by both amplifiers. This allows the amplifier input and output ranges to extend substantially below 0V, while powered from only a single positive supply. V_{SS} output supplies both amplifiers and its output load current. V_{SS} can be used to power external circuitry but the additional load current is seen as additional load by the charge pump. This internally generated negative supply can cause currents to flow in unexpected paths—especially through the electrostatic discharge protection networks found in almost all modern integrated circuits (Figure 7).

Near-Zero Source Impedances

The negative voltage generator has a finite current sink capability (typically around 15mA for C_{FLY} = 0.022µF, C_{HOLD} = C_{FILT} = 0.1µF). If the device is overloaded by the output sink current of one or both amplifiers combined, it will lose regulation, limiting output swing in the negative direction. Additionally, if regulation is lost, and the input is forced towards the negative rail, the MAX44267 can enter a latchup condition. This latchup is non-destructive, and the device will recover when the fault conditions are removed.

The MAX44267 is specified with a 5kΩ load on each output channel. This results in a maximum output load current that is well below an overload of the generator, and so the device will not latch up. It is possible to drive even heavier loads, although the total output sink current (of both channels combined) should not be allowed to exceed 15mA peak. (see the V_{OUT} Low vs. Output Sink Current graph in the *Typical Operating Characteristics* for details). When driving loads that may approach the output's limit, it is recommended that the inputs should be high-impedance sources or add a protective 5kΩ series resistor.

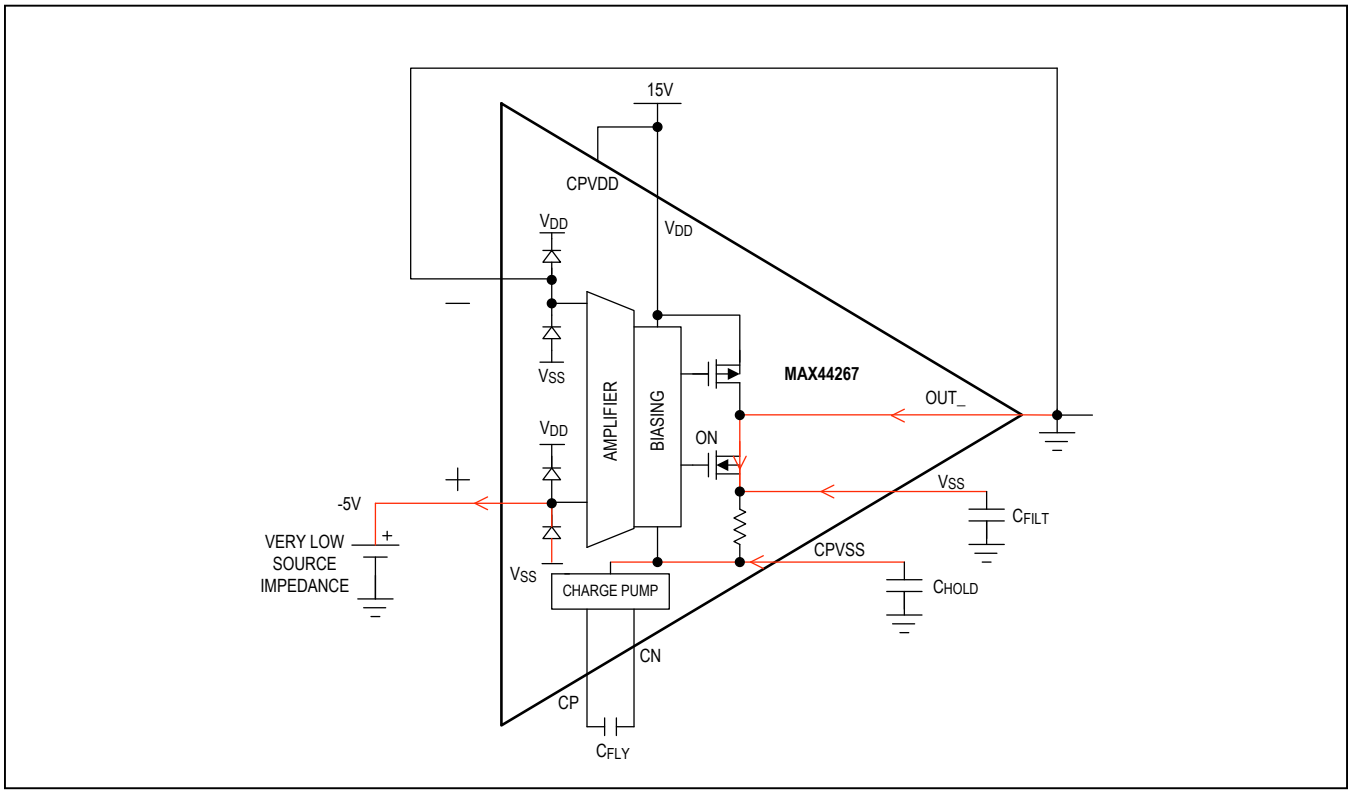


Figure 7. Possible Latchup Due to Overloading the MAX44267

Applications Information

Bridge Measurement Configuration without Instrumentation Amplifier

The MAX44267's low input offset voltage and low noise make it ideal for biasing strain gauges (Figure 8). The strain-gauge bridge is most commonly biased from the reference source and the output from the bridge is then at approximately half the reference voltage. In the case of biasing around ground, a negative supply needs to be available. Hence, the bridge is biased at twice the reference voltage and the center is at 0V (to within the offset voltage of the amplifier X1). Doubling the voltage across the bridge doubles its sensitivity, but of course, the downside is twice the current flows.

Since the bridge's center is now forced to be at 0V, the node "ip" must also be at 0V when no strain is applied, to within the calibration of zero strain of the bridge. Having controlled the zero bias point, the application can use the second amplifier within the dual MAX44267 to take a very large, direct-coupled gain without the usual risk of common-mode errors causing the output to saturate.

A full bridge, as shown, typically produces a differential output with a full scale of approximately 0.1% of the biasing voltage. Doubling the biasing voltage yields a doubling of sensitivity while also removing any common-mode error for the high-gain amplifier. Assuming that RB3 and RB2 are configured to decrease their resistance as the strain increases while RB1 and RB4 increase their resistance, then the full-scale output will be +819.2mV at the output. Capacitor C1 can be sized to roll of any unwanted bandwidth and its associated noise. Assuming the bridge uses resistances of 10kΩ in each leg, the noise will be about 24nV/√Hz, which is then amplified by 100x, along with the signal to give 2.4µV. If the bandwidth is kept down to 100Hz then this is only 24μV_{RMS} or about 300μV_{P-P} yielding a signal to noise ratio of 68dB. This can of course be improved by averaging the readings over a suitably long period of time with an integral number of 60Hz (50Hz) cycles usually offering both improved resolution and reduced sensitivity to the 60Hz power system.

Layout Guidelines

The MAX44267 features ultra-low offset voltage and noise, causing the Seebeck effect error to become significant. Therefore, to get optimum performance follow the following layout guidelines:

Avoid temperature gradients at the junction of two dissimilar metals. The most common dissimilar metals used on a PCB are solder to component lead and solder to board trace. Dissimilar metals create a local thermocouple. A variation in temperature across the board can cause an additional offset due to the Seebeck effect at the solder junctions. To minimize the Seebeck effect, place the amplifier away from potential heat sources on the board, if possible. Orient the resistors such that both the ends are heated equally. It is good practice to match the input signal path to ensure that the type and number of thermoelectric junctions remain the same. For example, consider using dummy 0Ω resistors oriented such that the thermoelectric sources due to the real resistors in the signal path is cancelled. It is recommended to flood the PCB with ground plane. The ground plane ensures that heat is distributed uniformly reducing the potential offset voltage degradation due to Seebeck effect.

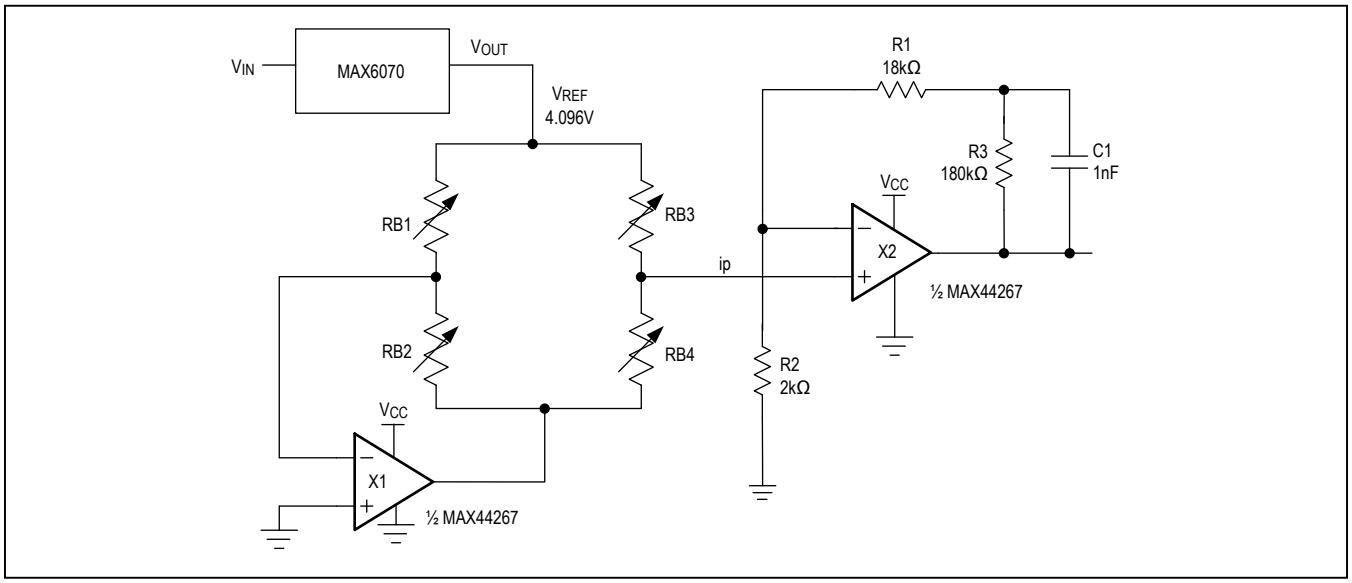


Figure 8. Bridge Measurement Configuration without Instrumentation Amplifier

Typical Application Circuit

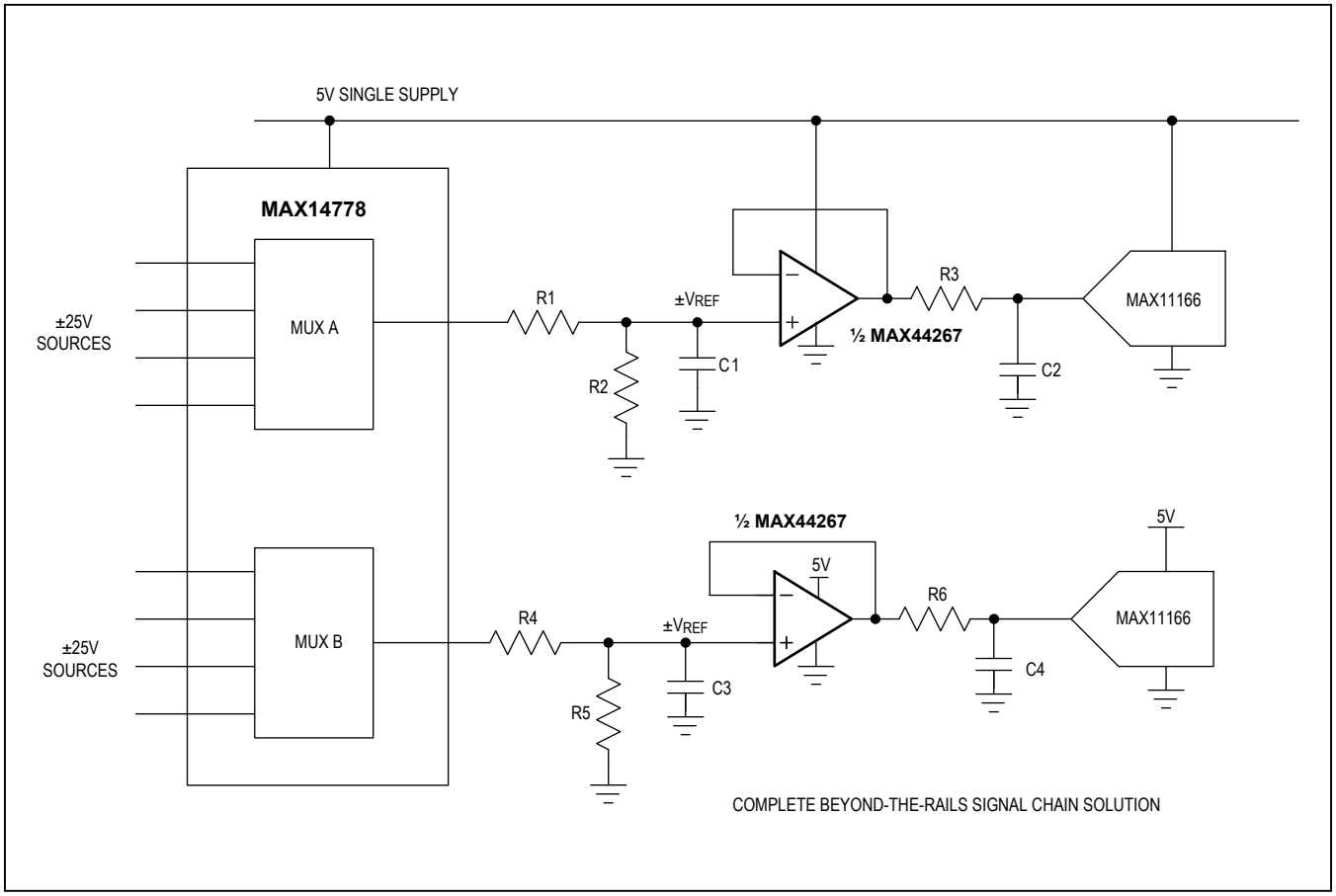


Table 1. Selector Guide for the Typical Operating Circuit

PART NO.	FUNCTION	VOLTAGE SUPPLY RANGE (V)	INPUT VOLTAGE RANGE (V)
MAX44267	Precision amplifier	+4.5 to +15.5	-12.0 to +13.5
MAX14778	4:1 mux	+3 to +5.5	±25
MAX14762	2-channel switch	+3 to +5.5	±25
MAX11167	16-bit ADC	+5	±5

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX44267AUD+	-40°C to + 125°C	14 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	21-0066	90-0113

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/14	Initial release	—

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