19-0868; Rev 0; 7/07

EVALUATION KIT AVAILABLE

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

General Description

The MAX3984 is a single-channel, preemphasis driver with input equalization that operates from 1Gbps to 10.3Gbps. It provides compensation for copper links, such as 8.5Gbps Fibre Channel and 10.3Gbps Ethernet, allowing spans of up to 10m with 24 AWG cable. The driver provides four selectable preemphasis levels, and the selectable input equalizer compensates for up to 10in of FR-4 circuit board material at 10Gbps.

The MAX3984 also features SFP-compliant loss-of-signal (LOS) detection and TX_DISABLE. Selectable output swing reduces EMI and power consumption. The MAX3984 is packaged in a lead-free, 3mm x 3mm, 16-pin thin QFN and operates from a 0°C to +85°C temperature range.

Applications

8.5Gbps Fibre Channel	Active Cable Assemblies
10.3Gbps Ethernet	STM-64

Pin Configuration appears at end of data sheet.

Features

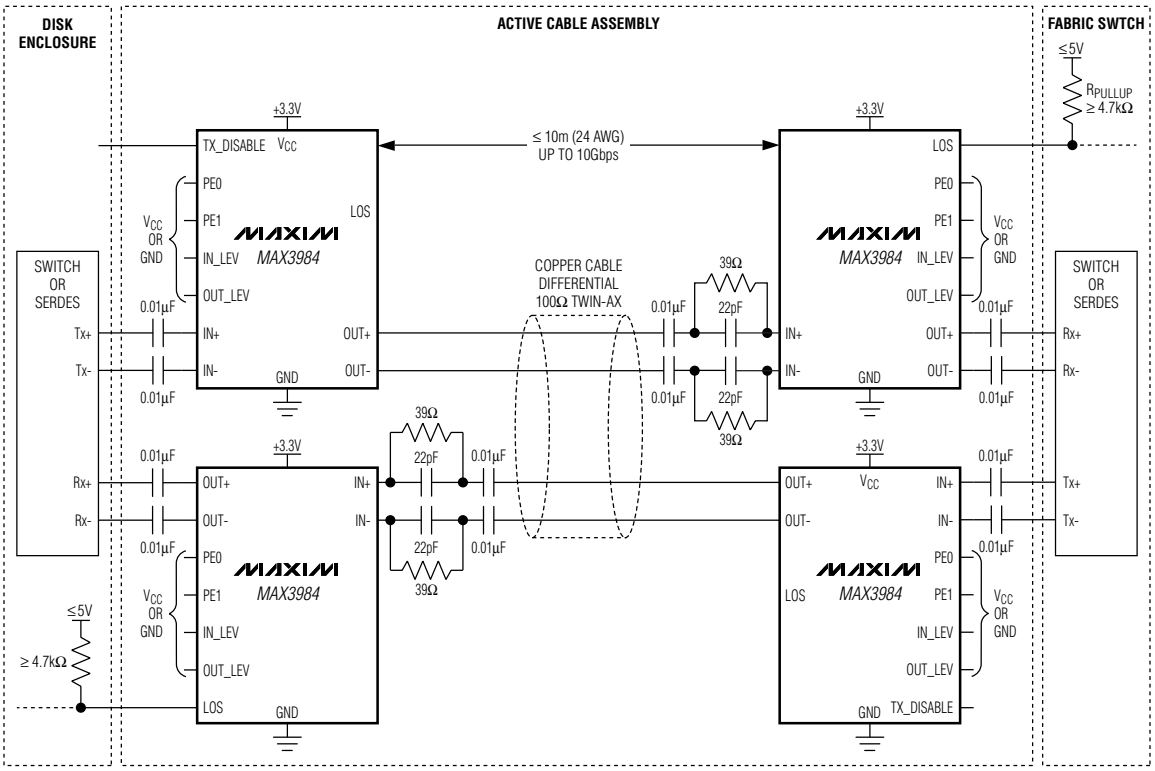
- **Drives Up to 10m of 24 AWG Cable**
- **Drives Up to 30in of FR-4**
- **Selectable 1000mVP-P or 1200mVP-P Differential Output Swing**
- **Selectable Output Preemphasis**
- **Selectable Input Equalization**
- **LOS Detection with Built-In Squelch**
- **Transmit Disable**
- **Hot Pluggable**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3984UTE+	0°C to +85°C	16 Thin QFN-EP*	T1633F-3

+Denotes a lead-free package.
**EP = Exposed pad.*

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}).....-0.5V to +4.1V
Continuous Output Current Range
(OUT+, OUT-) .....-25mA to +25mA
Input Voltage Range (IN+, IN-) .....-0.5V to (V_{CC} + 0.5V)
Logic Inputs Range (PE1, PE0,
TX_DISABLE, IN_LEV, OUT_LEV) .....-0.5V to (V_{CC} + 0.5V)
LOS Open-Collector Supply Voltage Range
(with ≥ 4.7kΩ pullup) .....-0.5V to +5.5V
Storage Ambient Temperature Range (T_{STG}) ...-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Noise Tolerance		1MHz ≤ f < 2GHz		40		mV_{P-P}
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data	1.0	8.5	10.3	Gbps
Consecutive Identical Digits (CID)		CID (bits)			100	Bits
Input Swing (Measured differentially at data source, point A of Figure 2 and 3. Pins LOS and TX_DISABLE are floating.)		IN_LEV = high, Figure 2; 4.25Gbps < data rate ≤ 10.3Gbps	360		1200	mV_{P-P}
		IN_LEV = high, Figure 2; 1.25Gbps < data rate ≤ 4.25Gbps	360		1600	
		IN_LEV = high, Figure 2; 1.0Gbps ≤ data rate ≤ 1.25Gbps	360		2400	
		IN_LEV = low, Figure 3; 1.0Gbps < data rate ≤ 10.3Gbps	100		360	
Time to Reach 50% Mark/Space Ratio					1	µs

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	OUT_LEV = low, TX_DISABLE = low		100	124	mA
		OUT_LEV = high, TX_DISABLE = low		120	148	
Inrush Current		Beyond steady state supply current (Note 1)			10	mA
Power-On Delay		(Note 1)	1		30	ms
EQUALIZER AND DRIVE SPECIFICATIONS						
Input Return Loss	S11	100MHz to 5GHz		10		dB
Input Resistance		Measured differentially (Note 2)	85	100	115	Ω
Different Output Swing (Notes 3, 4)		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high, PE1 = PE0 = high	1000		1300	mV_{P-P}
		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = low, PE1 = PE0 = high	800		1100	
		TX_DISABLE = high, PE1 = PE0 = high			10	
Common-Mode Output (AC) (Note 4)		Measured at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high (Note 5)			25	mV_{RMS}
Output Resistance	R_{OUT}	OUT+ or OUT-, single-ended	42	50	58	Ω
Output Return Loss	S22	100MHz to 5GHz		12		dB
Output Transition Time 20% to 80%	t_r, t_f	20% to 80% (Note 6)		32	40	ps
Random Jitter (Note 4)		Measured at point D in Figure 3 (Note 7)			0.8	ps_{RMS}

Output Preemphasis		Figure 1 (Note 3)	PE1	PE0				dB
			0	0	3.5			
			0	1	6.5			
			1	0	9.5			
			1	1	13			

Residual Output Deterministic Jitter at 1.0Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0			UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	0		0.02	
			5m, 24 AWG	0	1			
			7m, 24 AWG	1	0			
			10m, 24 AWG	1	1			

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
Residual Output Deterministic Jitter at 5.0Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0		0.09	0.12	UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 8.5Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0		0.15	0.20	UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 10Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0		0.18	0.25	UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	1				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 10.0Gbps (Notes 4, 8, and 10)		10in of FR-4 at OUT±; no cable; see Figure 3		PE1	PE0		0.10		UI_{P-P}
				0	0				
Propagation Delay							230		ps
STATUS OUTPUT: LOS									
LOS Deassert		IN_LEV = high (Note 11)						300	mV_{P-P}
		IN_LEV = low (Note 11)						100	
LOS Assert		IN_LEV = high (Note 11)				80			
LOS Hysteresis (Note 4)		IN_LEV = high (Note 11)				20			mV_{P-P}
		IN_LEV = low (Note 11)					10		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOS Open-Collector Current Sink		LOS asserted	0		25	µA
		LOS asserted; $V_{OL} \le 0.4V$	1.0			mA
		(Note 12)	0		25	µA
LOS Response Time (Note 4)		Time from V_{IN} dropping below deassert level or rising above assert level to 50% point of LOS output transition			10	µs
LOS Transition Time		Rise time or fall time (10% to 90%); pullup supply = 5.5V; external pullup R ≥ 4.7kΩ		200		ns
CONTROL INPUTS: TX_DISABLE, PE0, PE1, OUT_LEV, IN_LEV						
Logic-High Voltage	V_{IH}		2.0			V
Logic-Low Voltage	V_{IL}				0.8	V
Logic-High Current	I_{IH}	Current required to maintain logic-high state at V_{IH} > +2.0V			-150	µA
Logic-Low Current	I_{IL}	Current required to maintain logic-low state at V_{IL} < +0.8V			350	µA

Note 1: Supply voltage to reach 90% of final value in less than 100µs, but not less than 10µs. Power-on delay interval measured from the 50% level of the final voltage at the filter's device side to 50% level of final current. The supply is to remain at or above 3V for at least 100ms. Only one full-scale transition is permitted during this interval. Aberrations on the transition are limited to less than 100mV.

Note 2: IN+ and IN- are single-ended, 50Ω terminations to (V_{CC} - 1.5V) ±0.2V.

Note 3: Load is 50Ω ±1% at each side and the pattern is 0000011111 or equivalent pattern at 2.5Gbps.

Note 4: Guaranteed by design and characterization.

Note 5: PE1 = PE0 = logic-high (maximum preemphasis), load is 50Ω ±1% at each side. The pattern is 11001100 (50% edge density) at 10Gbps. AC common-mode output is computed as:

$$V_{ACCM_RMS} = RMS[(V_P + V_N) / 2) - V_{DCCM}]$$

where:
V_P = time-domain voltage measured at OUT+ with at least 10GHz bandwidth.
V_N = time-domain voltage measured at OUT- with at least 10GHz bandwidth.
AC common-mode voltage (V_{ACCM_RMS}) expressed as an RMS value.
DC common-mode voltage (V_{DCCM}) = average DC voltage of (V_P + V_N) / 2.

Note 6: Using 0000011111 or equivalent pattern at 2.5Gbps. PE0 = PE1 = logic-low for minimum preemphasis. Measured within 2in of the output pins with Rogers 4350 dielectric, or equivalent, and ≥ 10-mil line width. For transition time, the 0% reference is the steady state level after four zeros, just before the transition, and the 100% reference level is the steady state level after four consecutive logic ones.

Note 7: Pattern is 0000011111 or equivalent pattern at 10Gbps and 100mV_{P-P} differential swing. IN_LEV = logic-low and PE0 = PE1 = logic-low for minimum preemphasis. Signal transition time is controlled by the 4th-order BT filter (7.5GHz bandwidth) or equivalent. See Figure 3 for setup.

Note 8: Test pattern (464 bits): 100 zeros, 1010, PRBS7, 100 ones, 0101, PRBS7.

Note 9: Input range selection is IN_LEV = logic-high for FR-4 input equalization. Cables are unequalized, Amphenol Spectra-Strip (160-2499-997) 24 AWG or equivalent. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter point D in Figure 2. The deterministic jitter (DJ) at the output of the transmission line must be from media induced loss and not from clock source modulation. DJ is measured at point D of Figure 2.

Note 10: Input range selection is IN_LEV = logic-low. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter point D in Figure 3. The deterministic jitter (DJ) at the output of the transmission line must be from media induced loss and not from clock source modulation. DJ is measured at point D of Figure 3.

Note 11: Measured with 101010… pattern at 10Gbps with less than 1in of FR-4 at the input.

Note 12: True open-collector outputs. V_{CC} = 0 and the external 4.7kΩ pullup resistor is connected to +5.5V.

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

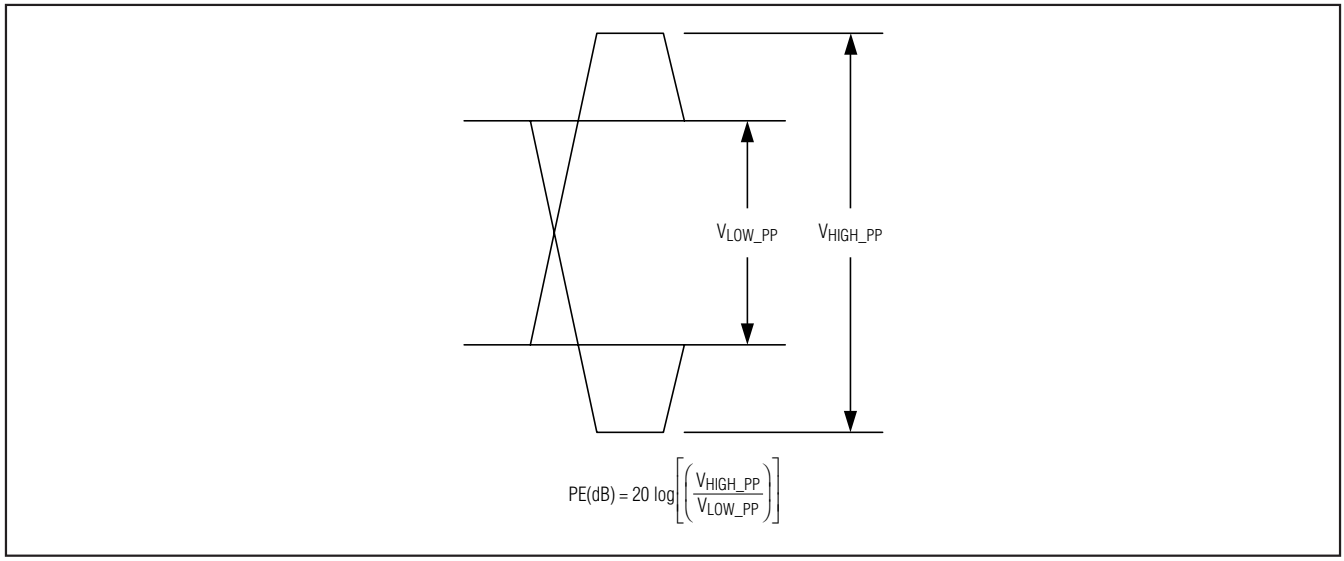


Figure 1. TX Preemphasis in dB

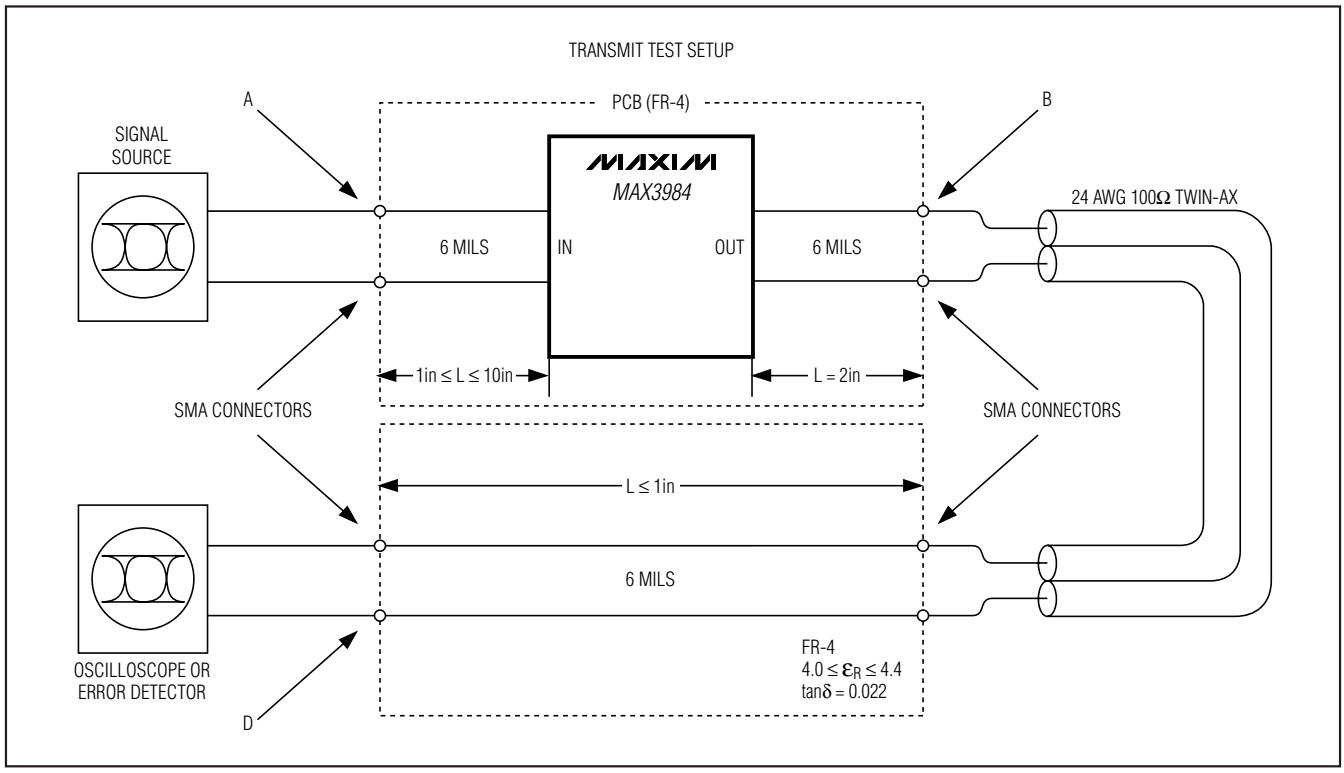


Figure 2. Transmit Test Setup (The points labeled A, B, and D are referenced for AC parameter test conditions. Deterministic jitter and eye diagrams measured at point D.)

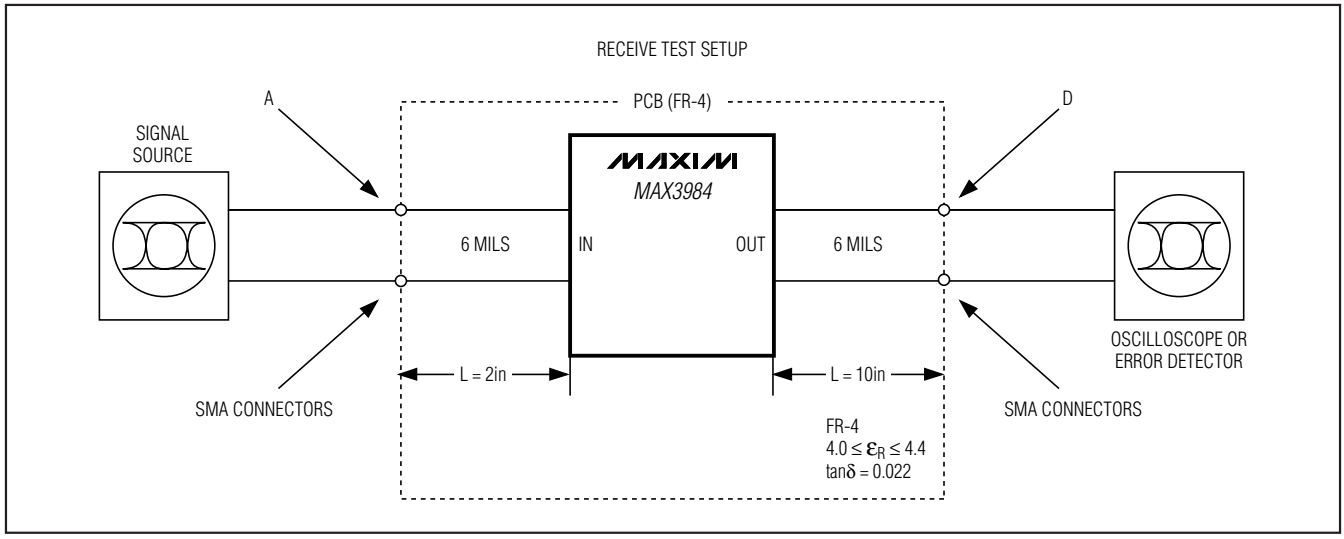
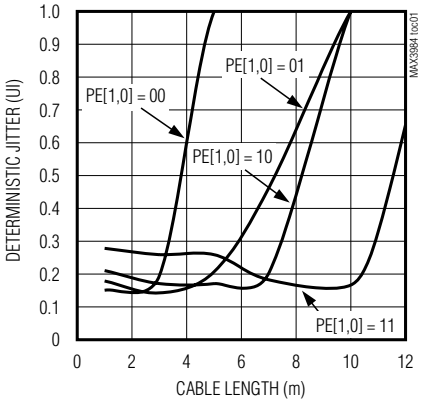


Figure 3. Receive-Side Test Setup (The points labeled A and D are referenced for AC parameter tests.)

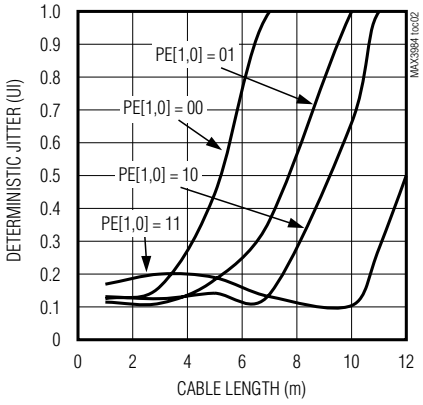
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, PRBS7 + 100 CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101, OUT_LEV = high, 10in of FR-4 at the input, IN_LEV = high, 360mV_{P-P} at input of FR-4, unless otherwise noted.)

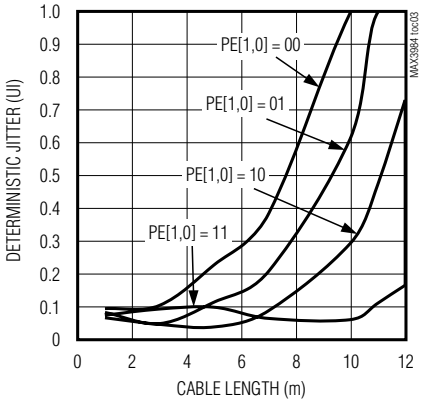
DETERMINISTIC JITTER vs. CABLE LENGTH (10.3Gbps)



DETERMINISTIC JITTER vs. CABLE LENGTH (8.5Gbps)



DETERMINISTIC JITTER vs. CABLE LENGTH (5Gbps)

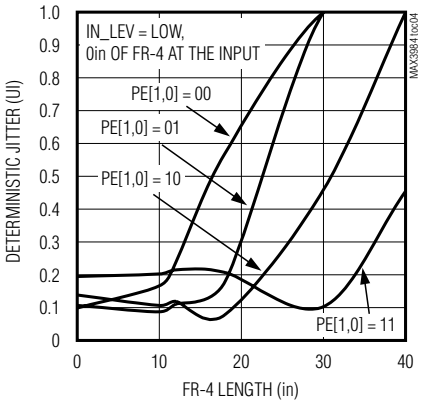


1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

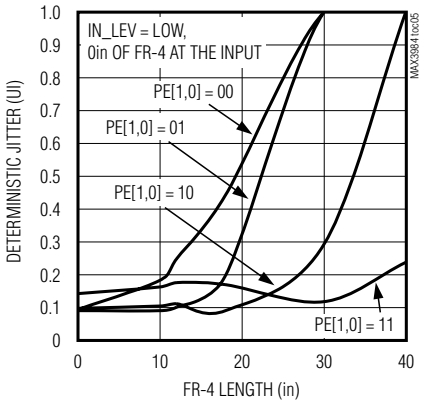
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, PRBS7 + 100 CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101, OUT_LEV = high, 10in of FR-4 at the input, IN_LEV = high, 360mV_{P-P} at input of FR-4, unless otherwise noted.)

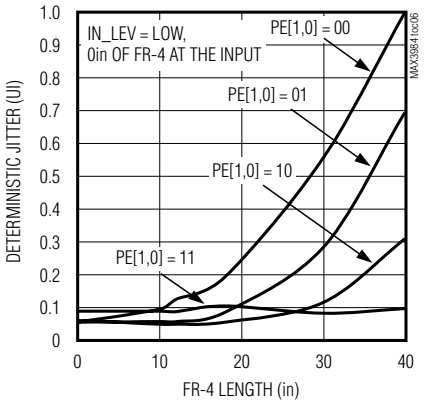
DETERMINISTIC JITTER vs. FR-4 LENGTH (10.3Gbps)



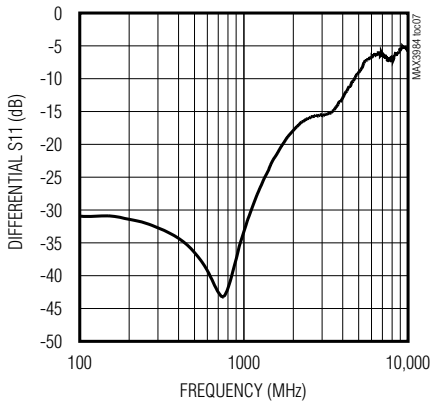
DETERMINISTIC JITTER vs. FR-4 LENGTH (8.5Gbps)



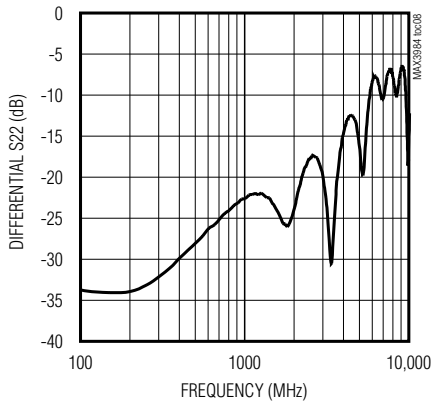
DETERMINISTIC JITTER vs. FR-4 LENGTH (5Gbps)



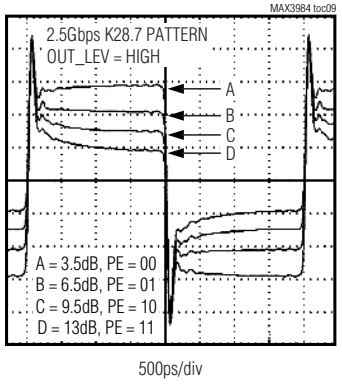
INPUT RETURN LOSS vs. FREQUENCY



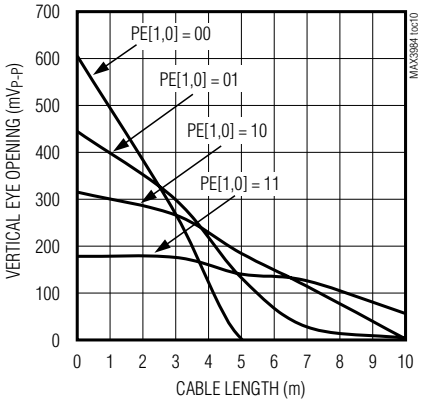
OUTPUT RETURN LOSS vs. FREQUENCY



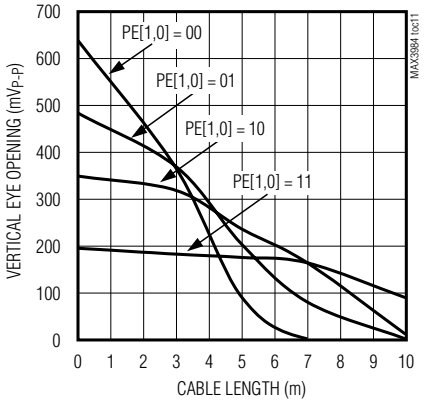
TRANSIENT RESPONSE



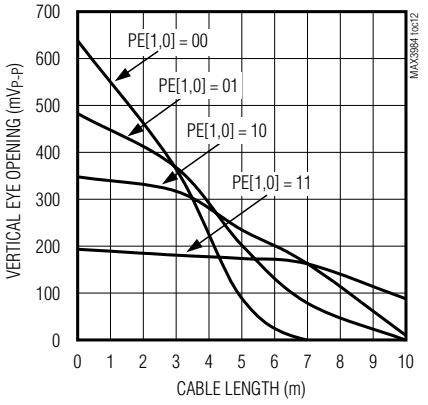
VERTICAL EYE OPENING vs. CABLE LENGTH (10.3Gbps)



VERTICAL EYE OPENING vs. CABLE LENGTH (8.5Gbps)



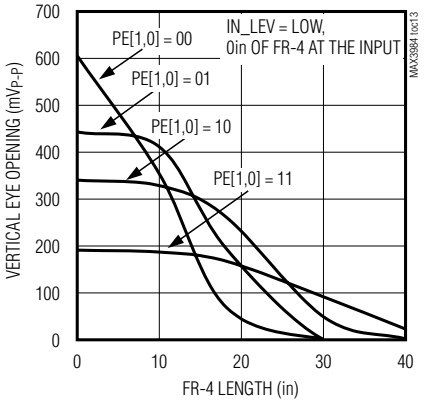
VERTICAL EYE OPENING vs. CABLE LENGTH (5Gbps)



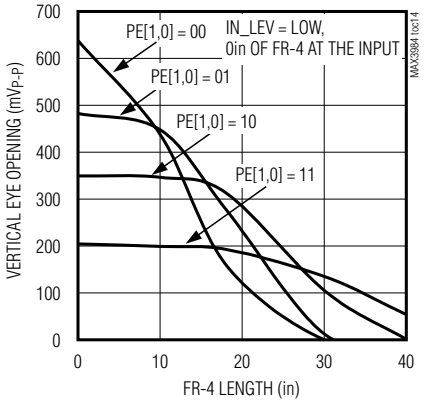
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, PRBS7 + 100 CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101, OUT_LEV = high, 10in of FR-4 at the input, IN_LEV = high, 360mV_{P-P} at input of FR-4, unless otherwise noted.)

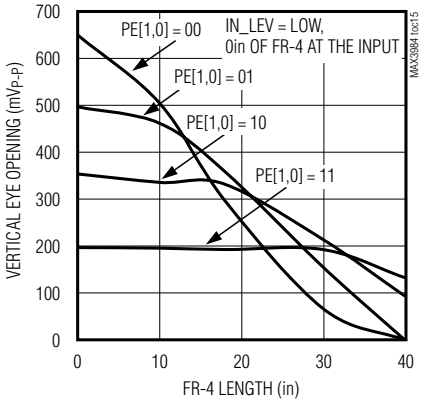
VERTICAL EYE OPENING vs. FR-4 LENGTH (10.3Gbps)



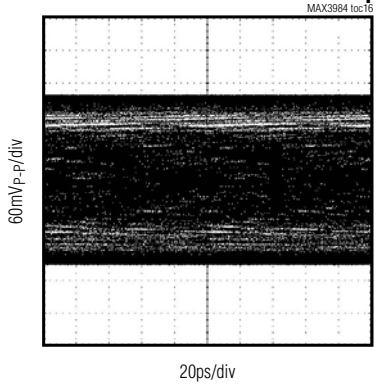
VERTICAL EYE OPENING vs. FR-4 LENGTH (8.5Gbps)



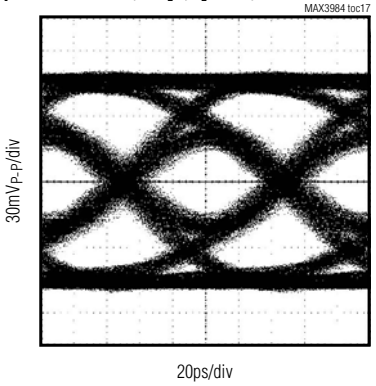
VERTICAL EYE OPENING vs. FR-4 LENGTH (5Gbps)



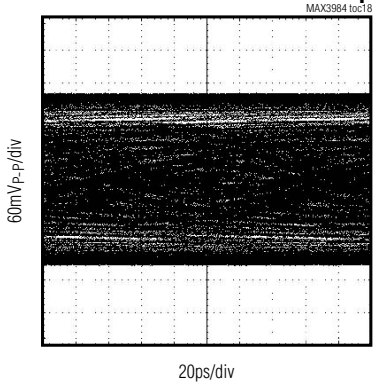
10m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3984 AT 10.3Gbps



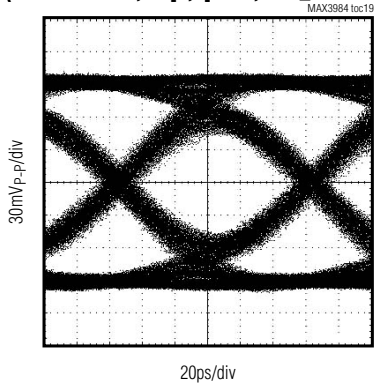
10m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3984 AT 10.3Gbps (PREEMPHASIS, PE[1,0] = 11, OUT_LEV = HIGH)



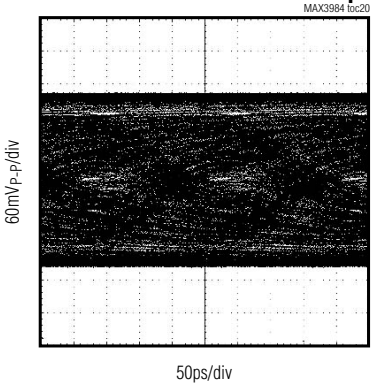
10m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3984 AT 8.5Gbps



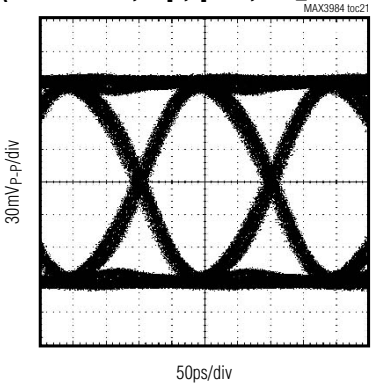
10m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3984 AT 8.5Gbps (PREEMPHASIS, PE[1,0] = 11, OUT_LEV = HIGH)



10m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3984 AT 5Gbps



10m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3984 AT 5Gbps (PREEMPHASIS, PE[1,0] = 11, OUT_LEV = HIGH)



1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

Pin Description

PIN	NAME	FUNCTION
1	V_{CC1}	Power-Supply Connection for Inputs. Connect to +3.3V.
2	IN+	Positive Data Input, CML. This input is internally terminated with 50Ω.
3	IN-	Negative Data Input, CML. This input is internally terminated with 50Ω.
4, 8, 9, 16	GND	Circuit Ground
5	OUT_LEV	Output-Swing Control Input, LVTTL with 20kΩ Internal Pullup. Set to TTL high or open for maximum output swing, or set to TTL low for reduced swing.
6	PE1	Output Preemphasis Control Input, LVTTL with 10kΩ Internal Pullup. This pin is the most significant bit of the 2-bit preemphasis control. Set high or open to assert this pin.
7	PE0	Output Preemphasis Control Input, LVTTL with 10kΩ Internal Pullup. This pin is the least significant bit of the 2-bit preemphasis control. Set high or open to assert this pin.
10	OUT-	Negative Data Output, CML. This output is terminated with 50Ω to V_{CC2}.
11	OUT+	Positive Data Output, CML. This output is terminated with 50Ω to V_{CC2}.
12	V_{CC2}	Power-Supply Connection for Output. Connect to +3.3V.
13	TX_DISABLE	Transmitter Disable Input, LVTTL with 10kΩ Internal Pullup. When high or open, differential output is less than 10mV_{P-P}. Set low for normal operation.
14	LOS	Loss-of-Signal Detect, Open-Collector TTL Output. Requires an external pullup ≥ 4.7kΩ (+5.5V maximum). This output sinks current when the input signal is above the LOS deassert level. To disable squelch pull LOS to ground.
15	IN_LEV	Receive Equalization Control Input, LVTTL 40kΩ Internal Pullup. Set to TTL high or open for higher LOS assert/deassert levels and 10in FR-4 compensation. Set to TTL low for lower LOS assert/deassert levels and to bypass the FR-4 equalization.
—	EP	Exposed Pad. For optimal thermal conductivity, this pad must be soldered to the circuit board ground.

Detailed Description

The MAX3984 is composed of a receiver, a driver, and an LOS detector with selectable threshold. Equalization is provided in the receiver. Selectable preemphasis and selectable output amplitude are included in the transmitter. The MAX3984 also includes transmit disable control for the output.

Receiver

Data is fed into the MAX3984 through a CML input stage and a selectable equalization stage. The fixed equalizer in the receiver corrects for up to 10in of PCB loss on FR-4 material at 10Gbps. The fixed equalizer can be bypassed by setting the IN_LEV pin to a logic-low.

Driver

The driver includes four-state preemphasis to compensate for up to 10m of 24 AWG, 100Ω balanced cable, or 30in of FR-4. The OUT_LEV pin selects the output amplitude. When OUT_LEV is low, the peak-to-peak amplitude is 1000mV_{P-P}. When OUT_LEV is high, the peak-to-peak amplitude is 1200mV_{P-P}.

Loss of Signal (LOS)

Input LOS detection is provided. This is an open-collector output and requires an external pullup resistor (≥ 4.7kΩ). The pullup resistors should be connected from LOS to a supply in the +3.0V to +5.5V range. The LOS output is not valid until power-up is complete.

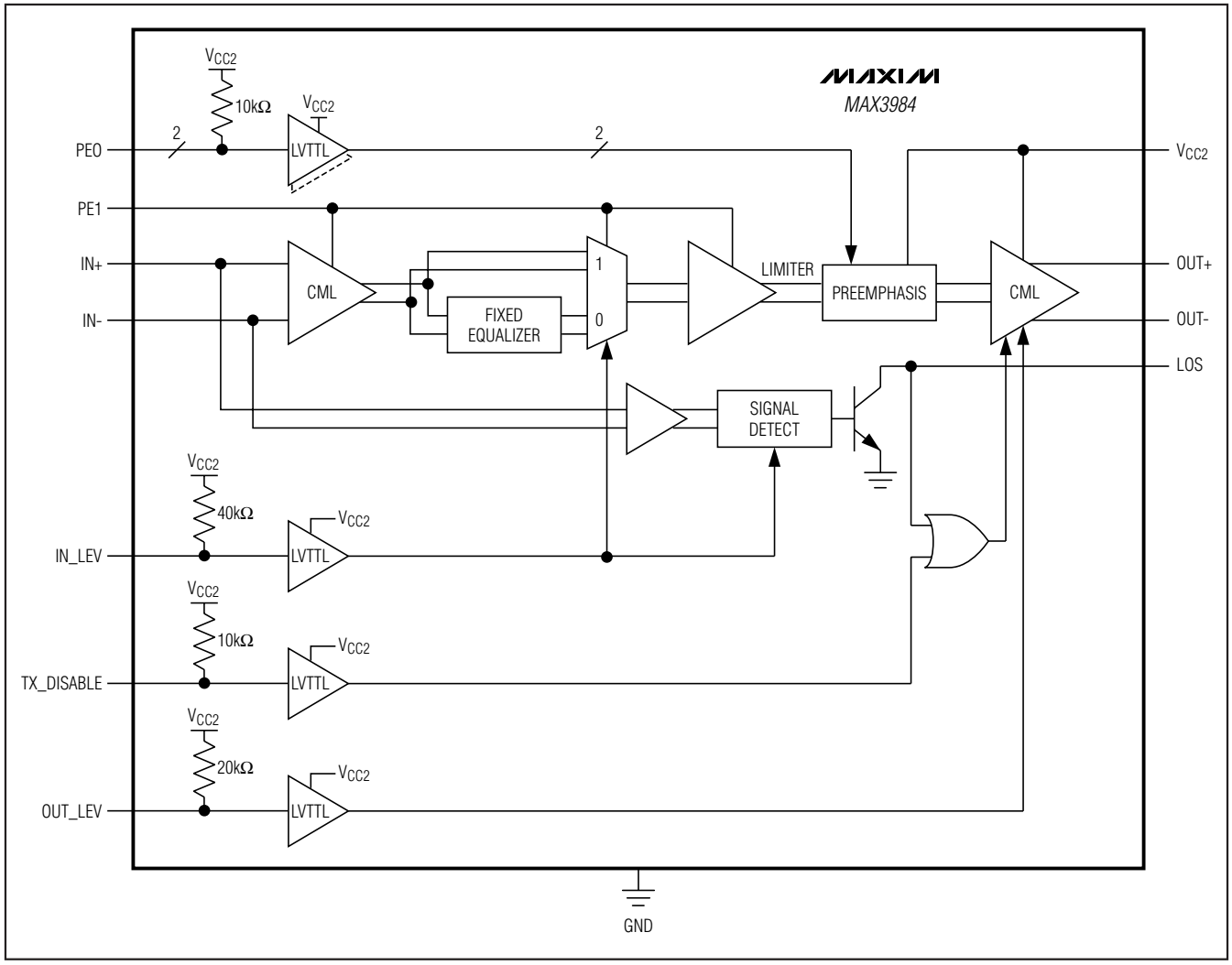


Figure 4. Functional Diagram

The IN_LEV pin sets the LOS assert and deassert levels. When IN_LEV is LVTTL high or open, the LOS assert threshold is 300mV$_{P-P}$. When IN_LEV is LVTTL low, the LOS assert threshold is 100mV$_{P-P}$.

TX_DISABLE provides manual control for turning the output off. The MAX3984 has a squelch function that disables the output when there is an LOS condition. To disable the squelch function, connect LOS to ground (see the *Squelch* section).

Applications Information

Squelch

The MAX3984 can automatically detect an incoming signal and enable or disable the data outputs. To enable squelch, the LOS pin must be connected to a TTL high or V_{CC} with a pullup resistor (≥ 4.7kΩ). Internally, TX_DISABLE and LOS are connected through an OR-gate to control the CML outputs. The outputs are disabled if LOS asserts. To turn off the squelch function, LOS must be pulled to TTL low. The output can also be disabled when TX_DISABLE is forced high.

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

Typical Characteristics at -40°C

The MAX3984 is guaranteed to work from 0°C to +85°C. Table 1 indicates typical performance outside the guaranteed limits.

Table 1. Typical Characteristics at -40°C

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
Different Output Swing (Note 1)		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high, PE1 = PE0 = high					1100		mV_{P-P}
		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = low, PE1 = PE0 = high					920		
		TX_DISABLE = high, PE1 = PE0 = high					3.5		
Common-Mode Output (AC)		Measured at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high (Note 2)					5		mV_{RMS}
Random Jitter		Measured at point D in Figure 3 (Note 3)					0.5		ps_{RMS}
Residual Output Deterministic Jitter at 1.0Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.02		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	0				
			5m, 24 AWG	0	1				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 5.0Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.12		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 8.5Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.2		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				

Table 1. Typical Characteristics at -40°C (continued)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
Residual Output Deterministic Jitter at 10Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.25		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	1				
			10m, 24 AWG	1	1				

Note 1: Load is 50Ω ±1% at each side and the pattern is 0000011111 or equivalent pattern at 2.5Gbps.

Note 2: PE1 = PE0 = logic-high (maximum preemphasis), load is 50Ω ±1% at each side. The pattern is 11001100 (50% edge density) at 10Gbps. AC common-mode output is computed as:

$$V_{ACCM_RMS} = RMS[(V_P + V_N) / 2) - V_{DCCM}]$$

where:

V_P = time-domain voltage measured at OUT+ with at least 10GHz bandwidth.

V_N = time-domain voltage measured at OUT- with at least 10GHz bandwidth.

AC common-mode voltage (V_{ACCM_RMS}) expressed as an RMS value.

DC common-mode voltage (V_{DCCM}) = average DC voltage of ($V_P + V_N$) / 2.

Note 3: Pattern is 0000011111 or equivalent pattern at 10Gbps and 100mV_{P-P} differential swing. IN_LEV = logic-low and PE0 = PE1 = logic-low for minimum preemphasis. Signal transition time is controlled by the 4th-order BT filter (7.5GHz bandwidth) or equivalent. See Figure 3 for setup.

Note 4: Test pattern (464 bits): 100 zeros, 1010, PRBS7, 100 ones, 0101, PRBS7.

Note 5: Input range selection is IN_LEV = logic-high for FR-4 input equalization. Cables are unequalized, Amphenol Spectra-Strip (160-2499-997) 24 AWG or equivalent. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter point D in Figure 2. The deterministic jitter (DJ) at the output of the transmission line must be from media induced loss and not from clock source modulation. DJ is measured at point D of Figure 2.

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

Layout Considerations

Circuit board layout and design can significantly affect the performance of the MAX3984. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on the data signals. Power-supply decoupling should also be placed as close as possible to the V_{CC} pins. Always connect all V_{CC} pins to a power plane. Take care to isolate the input from the output signals to reduce feed through.

Exposed-Pad Package

The exposed-pad, 16-pin thin QFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX3984 must be soldered to the circuit board for proper thermal performance. Refer to Maxim Application Note *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Interface Schematics

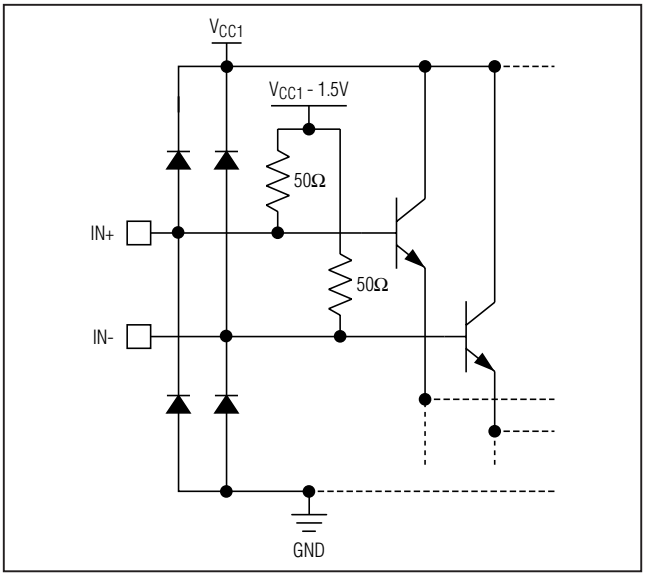


Figure 5. IN+/IN- Equivalent Input Structure

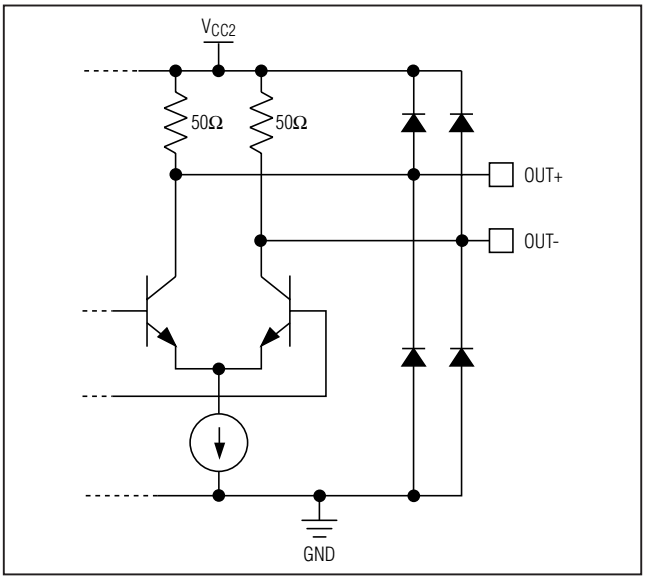
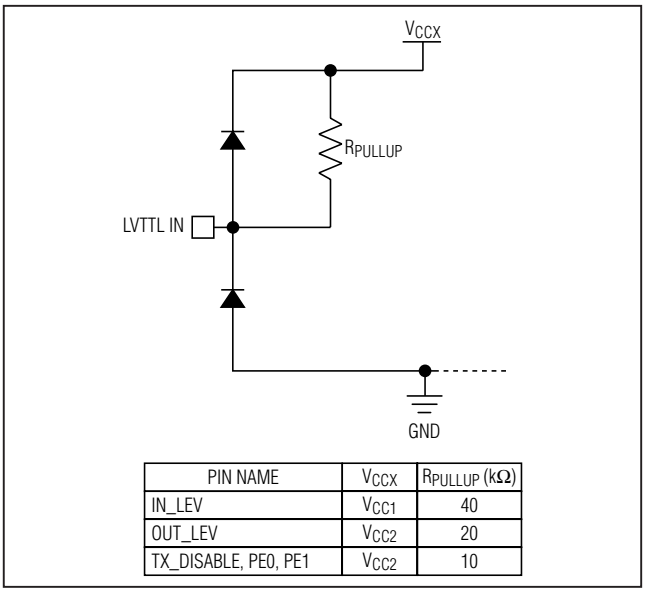


Figure 6. OUT+/OUT- Equivalent Output Structure



PIN NAME	V_{CCX}	R_{PULLUP} (kΩ)
IN_LEV	V_{CC1}	40
OUT_LEV	V_{CC2}	20
TX_DISABLE, PE0, PE1	V_{CC2}	10

Figure 7. LVTTL Equivalent Input Structure

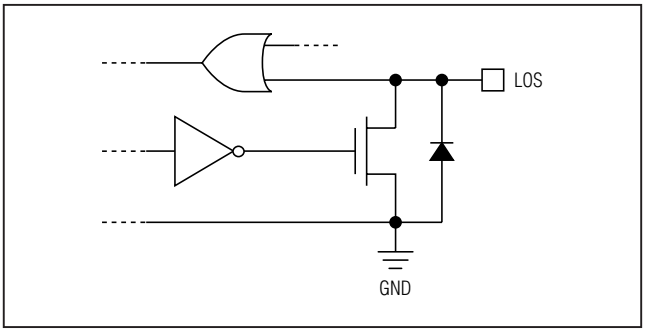
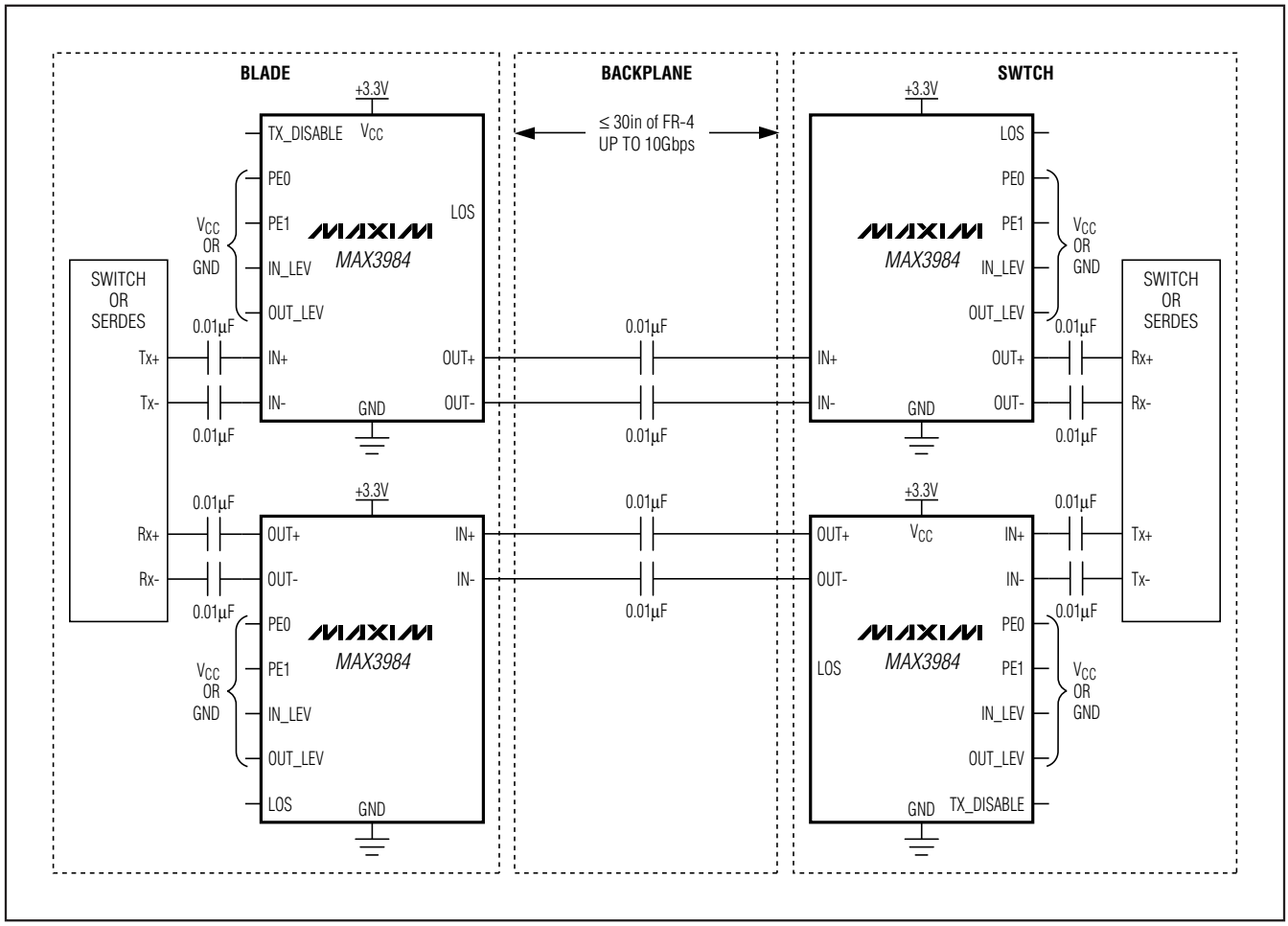


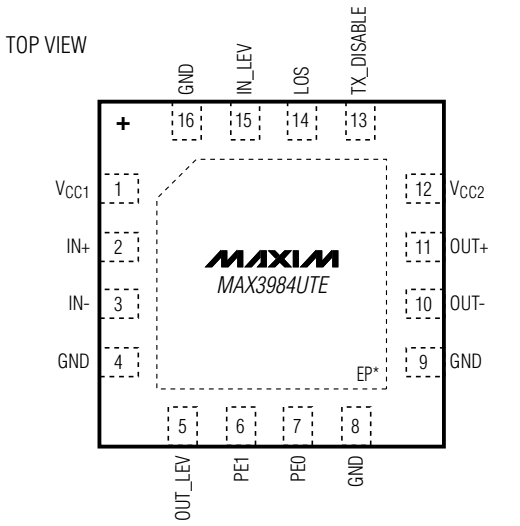
Figure 8. Loss-of-Signal Equivalent Output Structure

Typical Operating Circuits (continued)



1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

Pin Configuration



THIN QFN-EP
(3mm × 3mm)

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL OPERATION OF THE MAX3984.

Chip Information

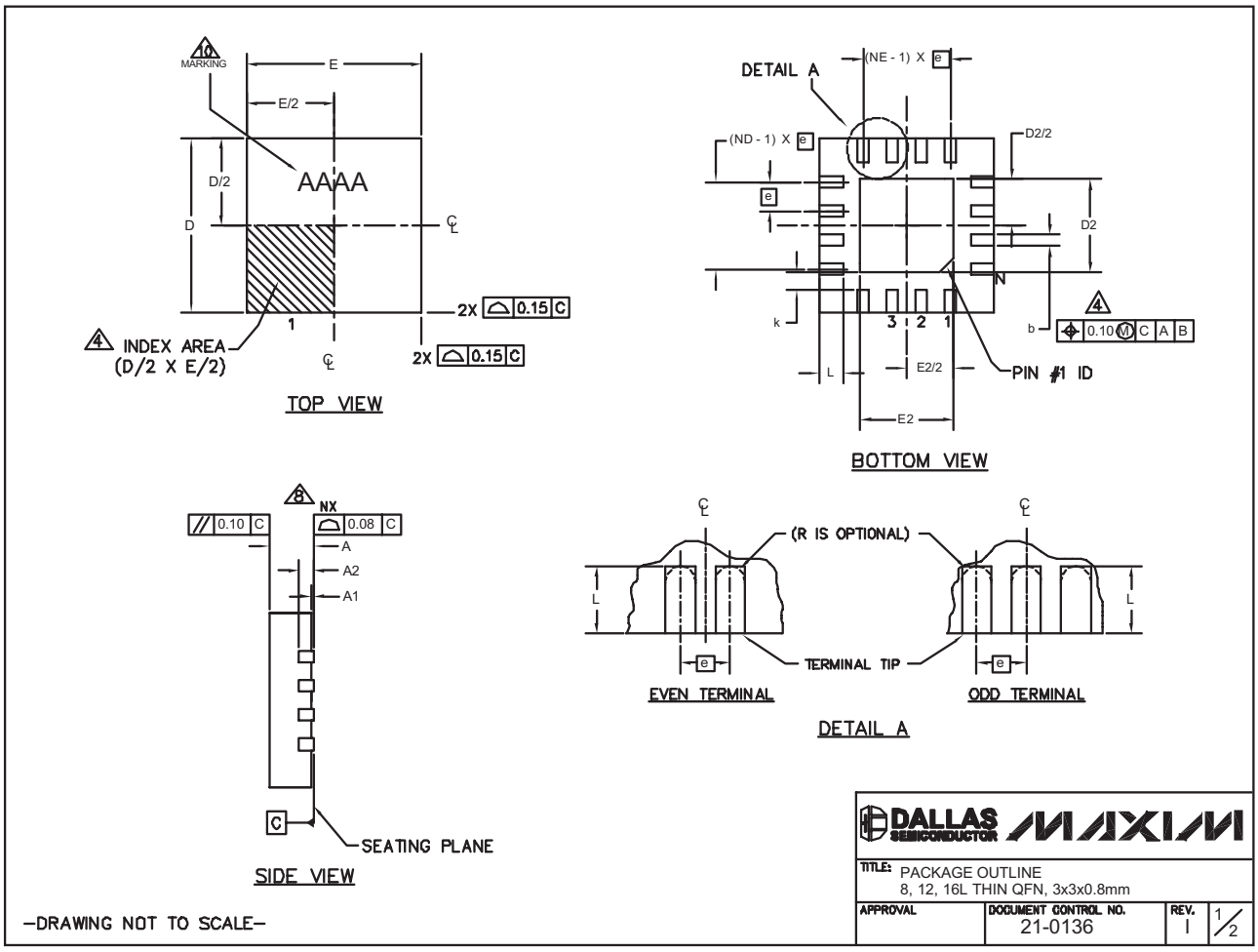
PROCESS: SiGe Bipolar

1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



1Gbps to 10Gbps Preemphasis Driver with Receive Equalizer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. I	2/2

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