maxim integrated™

# MAX3799

# 1Gbps to 14Gbps, SFP+ Multirate Limiting Amplifier and VCSEL Driver

## General Description

The MAX3799 is a highly integrated limiting amplifier and VCSEL driver that operates up to 14Gbps, making it suitable for Ethernet and Fibre Channel applications. By providing a selectable data path with a noise-shaping filter, the MAX3799 enables a module with 10G optics to be fully compliant with both 1000BASE-SR and 10GBASE-SR specifications. Operating from a single +3.3V supply, this low-power integrated limiting amplifier and VCSEL driver IC enables a platform design for SFP MSA as well as for SFP+ MSA-based optical transceivers. The high-sensitivity limiting amplifier limits the differential input signal generated by a transimpedance amplifier into a CML-level differential output signal. The compact VCSEL driver provides a modulation and a bias current for a VCSEL diode. The optical average power is controlled by an average power control (APC) loop implemented by a controller that interfaces to the VCSEL driver through a 3-wire digital interface. All differential I/Os are optimally back-terminated for a 50Ω transmission line PCB design.

The use of a 3-wire digital interface reduces the pin count while enabling advanced Rx (rate selection, LOS threshold, LOS squelch, LOS polarity, CML output level, signal path polarity, deemphasis, and fast mode-select change time) and Tx settings (modulation current, bias current, polarity, and eye safety control) without the need for external components. The MAX3799 provides multiple current and voltage DACs to allow the use of low-cost controller ICs.

The MAX3799 is packaged in a lead-free, 5mm x 5mm, 32-pin TQFN package.

## Applications

1000BASE-SR/10GBASE-SR Multirate SFP+ Optical Transceiver

1x/2x/4x/8x/16x SFF/SFP/SFP+ MSA Fibre Channel (FC) Optical Transceiver

## Features

- **Enables Single-Module Design Compliance with 1000BASE-SR and 10GBASE-SR Specifications**
- **-21.5dBm Optical Sensitivity at 1.25Gbps Using a 10.32Gbps ROSA (-19.7dBm OMA)**
- **Low Power Dissipation of 320mW at 3.3V Power Supply**
- **Typical Electrical Performance of 14.025Gbps on Rx/Tx (Non-Retimed 16x Fibre Channel Solution)**
- **3mV$_{P-P}$ Receiver Sensitivity at 10.32Gbps**
- **4ps$_{P-P}$ DJ at Receiver Output at 8.5Gbps 8B/10B**
- **4ps$_{P-P}$ DJ at Receiver Output at 10.32Gbps $2^{31}$ - 1 PRBS**
- **26ps Rise and Fall Time at Rx/Tx Output**
- **Rate Select for 1Gbps Mode or 10Gbps Mode**
- **CML Output Squelch**
- **Polarity Select for Rx and Tx**
- **LOS Assert Level Adjustment**
- **LOS Polarity Select**
- **Modulation Current Up to 12mA Into 100Ω Differential Load**
- **Bias Current Up to 15mA**
- **Integrated Eye Safety Features**
- **3-Wire Digital Interface**
- **Programmable Deemphasis at Tx Output**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX3799ETJ+ | -40°C to +85°C | 32 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**EP = Exposed pad.*

***Typical Application Circuit and Pin Configuration appear at end of data sheet.***

***For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.***

*19-4695; Rev 2; 10/12*

## ABSOLUTE MAXIMUM RATINGS

$V_{CCR}$, $V_{CCT}$, $V_{CCD}$.....-0.3V to +4.0V
Voltage Range at DISABLE, SDA, SCL, CSEL, RSEL, FAULT, BMON, LOS, CAZ2.....-0.3V to ($V_{CC}$ + 0.3V)
Voltage Range at ROUT+, ROUT- .....($V_{CC}$ - 1V) to ($V_{CC}$ + 0.3V)
Voltage at TIN+, TIN-.....($V_{CC}$ - 2.5V) to ($V_{CC}$ - 0.5V)
Voltage Range at TOUT+, TOUT- .....($V_{CC}$ - 2V) to ($V_{CC}$ + 0.3V)
Voltage at BIAS .....0V to $V_{CC}$
Voltage at RIN+, RIN-.....($V_{CC}$ - 2V) to ($V_{CC}$ - 0.2V)
Current Range into FAULT, LOS.....-1mA to +5mA
Current Range into SDA.....-1mA to +1mA
Current into ROUT+, ROUT- .....40mA
Current into TOUT+, TOUT- .....60mA
Continuous Power Dissipation ($T_A$ = +70°C)
32-Pin TQFN (derate 34.5W/°C above +70°C) .....2759mW
Operating Junction Temperature Range.....-55°C to +150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.85V to 3.63V, $T_A$ = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, $C_{AZ}$ = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, $V_{CC}$ = 3.3V, $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Power-Supply Current | $I_{CC}$ | Includes the CML output current; excludes $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, $V_{DIFF_ROUT}$ = 400m$V_{P-P}$ (Note 1) | | 97 | 150 | mA |
| Power-Supply Voltage | $V_{CC}$ | | 2.85 | | 3.63 | V |
| **GENERAL** | | | | | | |
| Input Data Rate | | | 1.0625 | | 10.32 | Gbps |
| Input/Output SNR | | | 14.1 | | | |
| BER | | | | | 10E-12 | |
| **POWER-ON RESET** | | | | | | |
| High POR Threshold | | | | 2.55 | 2.75 | V |
| Low POR Threshold | | $I_{BIAS}$ = $I_{BIASOFF}$ and $I_{MOD}$ = $I_{MODOFF}$ | 2.3 | 2.45 | | V |
| **Rx INPUT SPECIFICATIONS** | | | | | | |
| Differential Input Resistance RIN+/RIN- | $R_{IN_DIFF}$ | | 75 | 100 | 125 | Ω |
| Input Sensitivity (Note 2) | $V_{INMIN}$ | RATE_SEL = 0 (1.25Gbps) | | 1 | 3 | m$V_{P-P}$ |
| | | RATE_SEL = 1 (10.32Gbps) | | 3 | 8 | |
| Input Overload | $V_{INMAX}$ | | 1.2 | | | $V_{P-P}$ |
| Input Return Loss | SDD11 | DUT is powered on, f ≤ 5GHz | | 14 | | dB |
| | | DUT is powered on, f ≤ 16GHz | | 7 | | |
| Input Return Loss | SCC11 | DUT is powered on, 1GHz < f ≤ 5GHz | | 8 | | dB |
| | | DUT is powered on, 1GHz < f ≤ 16GHz | | 8 | | |
| **Rx OUTPUT SPECIFICATIONS** | | | | | | |
| Differential Output Resistance | $R_{OUTDIFF}$ | | 75 | 100 | 125 | Ω |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.85V to 3.63V, $T_A$ = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, $C_{AZ}$ = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, $V_{CC}$ = 3.3V, $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Return Loss | SDD22 | DUT is powered on, f ≤ 5GHz | | 11 | | dB |
| | | DUT is powered on, f ≤ 16GHz | | 5 | | |
| Output Return Loss | SCC22 | DUT is powered on, 1GHz < f ≤ 5GHz | | 9 | | dB |
| | | DUT is powered on, 1GHz < f ≤ 16GHz | | 7 | | |
| CML Differential Output Voltage High | | $5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[162] | 595 | 800 | 1005 | $mV_{P-P}$ |
| CML Differential Output Voltage Medium | | $10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[80] | 300 | 400 | 515 | $mV_{P-P}$ |
| CML Differential Output DAC Limit | | SET_CML[7:0] | | | 215 | |
| Differential Output Signal When Disabled | | Outputs AC-coupled, $V_{INMAX}$ applied to input $V_{DIFF_ROUT}$ = $800mV_{P-P}$ at 8.5Gbps (Notes 2, 3) | | 6 | 15 | $mV_{P-P}$ |
| Data Output Transition Time (20% to 80%) (Notes 2, 3, 4) | $t_R/t_F$ | $10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 1, $V_{DIFF_ROUT}$ = $400mV_{P-P}$ | | 26 | 35 | ps |
| | | $5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 0, $V_{DIFF_ROUT}$ = $800mV_{P-P}$ | | 60 | 100 | |
| **Rx TRANSFER CHARACTERISTICS** | | | | | | |
| Deterministic Jitter (Notes 2, 3, 5) | DJ | $60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 10.32Gbps, RATE_SEL = 1, $V_{DIFF_ROUT}$ = $400mV_{P-P}$ | | 4 | 12 | $ps_{P-P}$ |
| | | $10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 8.5Gbps, RATE _SEL = 1, $V_{DIFF_ROUT}$ = $400mV_{P-P}$ | | 4 | 12 | |
| | | $5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 1.25Gbps, RATE _SEL = 0, $V_{DIFF_ROUT}$ = $800mV_{P-P}$ | | 20 | | |
| Random Jitter (Notes 2, 3) | RJ | Input = $60mV_{P-P}$ at 1.25Gbps, RATE_SEL = 0, $V_{DIFF_ROUT}$ = $800mV_{P-P}$ | | 1.8 | 2.5 | $ps_{RMS}$ |
| | | Input = $60mV_{P-P}$ at 8.5Gbps, RATE _SEL = 1, $V_{DIFF_ROUT}$ = $400mV_{P-P}$ | | 0.32 | 0.48 | |
| Low-Frequency Cutoff | | $C_{AZ}$ = 0.1µF | | 2 | | kHz |
| | | $C_{AZ}$ = open | | 500 | | |
| **Rx LOS SPECIFICATIONS** | | | | | | |
| LOS Assert Sensitivity Range | | | 14 | | 77 | $mV_{P-P}$ |
| LOS Hysteresis | | 10 x log($V_{DEASSERT}/V_{ASSERT}$) (Note 6) | 1.25 | 2.1 | | dB |
| LOS Assert/Deassert Time | | (Note 7) | 2.3 | | 80 | µs |
| Low Assert Level | | SET_LOS[7] (Notes 2, 6) | 8 | 11 | 14 | $mV_{P-P}$ |
| Low Deassert Level | | SET_LOS[7] (Notes 2, 6) | 14 | 18 | 21 | $mV_{P-P}$ |
| Medium Assert Level | | SET_LOS[32] (Notes 2, 6) | 39 | 48 | 58 | $mV_{P-P}$ |
| Medium Deassert Level | | SET_LOS[32] (Notes 2, 6) | 65 | 81 | 95 | $mV_{P-P}$ |
| High Assert Level | | SET_LOS[63] (Notes 2, 6) | 77 | 94 | 112 | $mV_{P-P}$ |
| High Deassert Level | | SET_LOS[63] (Notes 2, 6) | 127 | 158 | 182 | $mV_{P-P}$ |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.85V to 3.63V, $T_A$ = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, $C_{AZ}$ = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, $V_{CC}$ = 3.3V, $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Tx INPUT SPECIFICATIONS** | | | | | | |
| Differential Input Voltage | $V_{IN}$ | Data rate = 1.0625Gbps | 0.2 | | 2.4 | $V_{P-P}$ |
| | | Data rate = 10.32Gbps | 0.075 | | 0.8 | |
| Common-Mode Input Voltage | $V_{INCM}$ | | | 2.75 | | V |
| Differential Input Resistance | $R_{IN}$ | | 75 | 100 | 125 | Ω |
| Input Return Loss | SDD11 | DUT is powered on, f ≤ 5GHz | | 15 | | dB |
| | | DUT is powered on, f ≤ 16GHz | | 6 | | |
| Input Return Loss | SCC11 | DUT is powered on, 1GHz < f ≤ 5GHz | | 9 | | dB |
| | | DUT is powered on, 1GHz < f ≤ 16GHz | | 5 | | |
| **Tx LASER MODULATOR** | | | | | | |
| Maximum Modulation-On Current into 100Ω Differential Load | $I_{MODMAX}$ | Outputs AC-coupled, $V_{CCTO}$ 2.95V | 12 | | | mA |
| Minimum Modulation-On Current into 100Ω Differential Load | $I_{MODMIN}$ | Outputs AC-coupled | | | 2 | mA |
| Modulation Current DAC Stability | | 2mA ≤ $I_{MOD}$ ≤ 12mA (Note 8) | | | 4 | % |
| Modulation Current Rise Time/ Fall Time | $t_R/t_F$ | 5mA ≤ $I_{MOD}$ ≤ 10mA, 20% to 80%, SET_TXDE[3:0] = 10 (Notes 2, 4) | | 26 | 39 | ps |
| Deterministic Jitter (Notes 2, 9) | DJ | 5mA ≤ $I_{MOD}$ ≤ 12mA, at 10.32Gbps, 250m$V_{P-P}$ ≤ $V_{IN}$ ≤ 800m$V_{P-P}$, SET_TXDE[3:0] = 0 | | 6 | 12 | ps |
| | | 5mA ≤ $I_{MOD}$ ≤ 12mA, at 10.32Gbps, 250m$V_{P-P}$ ≤ $V_{IN}$ ≤ 800m$V_{P-P}$, SET_TXDE[3:0] = 10 | | 6 | 13 | |
| | | 5mA ≤ $I_{MOD}$ ≤ 12mA, at 8.5Gbps, 250m$V_{P-P}$ ≤ $V_{IN}$ ≤ 800m$V_{P-P}$, SET_TXDE[3:0] = 0 | | 6 | 12 | |
| | | 5mA ≤ $I_{MOD}$ ≤ 12mA, at 8.5Gbps, 250m$V_{P-P}$ ≤ $V_{IN}$ ≤ 800m$V_{P-P}$, SET_TXDE[3:0] = 10 | | 6 | 12 | |
| | | 2mA ≤ $I_{MOD}$ ≤ 12mA, at 4.25Gbps | | 5 | | |
| | | 2mA ≤ $I_{MOD}$ ≤ 12mA, at 1.0625Gbps | | 5 | | |
| Random Jitter | | 5mA ≤ $I_{MOD}$ ≤ 12mA, 250m$V_{P-P}$ ≤ $V_{IN}$ ≤ 800m$V_{P-P}$ | | 0.17 | 0.5 | $ps_{RMS}$ |
| Output Return Loss | SDD22 | DUT is powered on, f ≤ 5GHz | | 12 | | dB |
| | | DUT is powered on, f ≤ 16GHz | | 5 | | |
| **Tx BIAS GENERATOR** | | | | | | |
| Maximum Bias-On Current | $I_{BIASMAX}$ | Current into BIAS pin | 15 | | | mA |
| Minimum Bias-On Current | $I_{BIASMIN}$ | Current into BIAS pin | | | 2 | mA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.85V to 3.63V, $T_A$ = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, $C_{AZ}$ = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, $V_{CC}$ = 3.3V, $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| BIAS Current DAC Stability | | 2mA ≤ $I_{BIAS}$ ≤ 15mA (Notes 2, 10) | | | 4 | % |
| Compliance Voltage at BIAS | $V_{BIAS}$ | | 0.9 | | 2.1 | V |
| BIAS Current Monitor Current Gain | $I_{BMON}$ | External resistor to GND defines the voltage gain | | 16 | | mA/A |
| Compliance Voltage at BMON | $V_{BMON}$ | | 0 | | 1.8 | V |
| BIAS Current Monitor Current Gain Stability | $I_{BMON}$ | 2mA ≤ $I_{BIAS}$ ≤ 15mA (Note 10) | | | 5 | % |
| **Tx SAFETY FEATURES** | | | | | | |
| Excessive Voltage at BMON | $V_{BMON}$ | Average voltage, FAULT warning always occurs for $V_{BMON}$ $V_{CC}$ - 0.55V, FAULT warning never occurs for $V_{BMON}$ ≤ $V_{CC}$ - 0.65V | $V_{CC}$ - 0.65V | $V_{CC}$ - 0.6V | $V_{CC}$ - 0.55V | V |
| Excessive Voltage at BIAS | $V_{BIAS}$ | Average voltage, FAULT always occurs for $V_{BIAS}$ ≤ 0.44V, FAULT never occurs for $V_{BIAS}$ 0.65V | 0.44 | 0.48 | 0.65 | V |
| Maximum VCSEL Current in Off State | $I_{OFF}$ | FAULT or DISABLE, $V_{BIAS}$ = $V_{CC}$ | | | 25 | µA |
| **SFP TIMING REQUIREMENTS** | | | | | | |
| DISABLE Assert Time | $t_{OFF}$ | Time from rising edge of DISABLE input signal to $I_{BIAS}$ = $I_{BIASOFF}$ and $I_{MOD}$ = $I_{MODOFF}$ | | | 1 | µs |
| DISABLE Negate Time | $t_{ON}$ | Time from falling edge of DISABLE to $I_{BIAS}$ and $I_{MOD}$ at 90% of steady state when FAULT = 0 before reset | | | 500 | µs |
| FAULT Reset Time of Power-On Time | $t_{INIT}$ | Time from power-on or negation of FAULT using DISABLE | | | 100 | ms |
| FAULT Reset Time | $t_{FAULT}$ | Time from fault to FAULT on, $C_{FAULT}$ ≤ 20pF, $R_{FAULT}$ = 4.7kΩ | | | 10 | µs |
| DISABLE to Reset | | Time DISABLE must be held high to reset FAULT | 5 | | | µs |
| **OUTPUT_LEVEL VOLTAGE DAC (SET_CML)** | | | | | | |
| Full-Scale Voltage | $V_{FS}$ | 100Ω differential resistive load | | 1200 | | $mV_{P-P}$ |
| Resolution | | | | 5 | | $mV_{P-P}$ |
| Integral Nonlinearity | INL | 5mA ≤ $I_{CML_LEVEL}$ ≤ 20mA | | ±0.9 | | LSB |
| **LOS THRESHOLD VOLTAGE DAC (SET_LOS)** | | | | | | |
| Full-Scale Voltage | $V_{FS}$ | | | 94 | | $mV_{P-P}$ |
| Resolution | | | | 1.5 | | $mV_{P-P}$ |
| Integral Nonlinearity | INL | 11$mV_{P-P}$ ≤ $V_{TH_LOS}$ ≤ 94$mV_{P-P}$ | | ±0.7 | | LSB |
| **BIAS CURRENT DAC (SET_IBIAS)** | | | | | | |
| Full-Scale Current | $I_{FS}$ | | | 21 | | mA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.85V to 3.63V, $T_A$ = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, $C_{AZ}$ = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, $V_{CC}$ = 3.3V, $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution | | | | 40 | | µA |
| Integral Nonlinearity | INL | 1mA ≤ $I_{BIAS}$ ≤ 15mA | | ±1 | | LSB |
| Differential Nonlinearity | DNL | 1mA ≤ $I_{BIAS}$ ≤ 15mA, guaranteed monotonic at 8-bit resolution (SET_IBIAS[8:1]) | | ±1 | | LSB |
| **MODULATION CURRENT DAC (SET_IMOD)** | | | | | | |
| Full-Scale Current | $I_{FS}$ | | | 21 | | mA |
| Resolution | | | | 40 | | µA |
| Integral Nonlinearity | INL | 2mA ≤ $I_{MOD}$ ≤ 12mA | | ±1 | | LSB |
| Differential Nonlinearity | DNL | 2mA ≤ $I_{MOD}$ ≤ 12mA, guaranteed monotonic at 8-bit resolution (SET_IMOD[8:1]) | | ±1 | | LSB |
| **CONTROL I/O SPECIFICATIONS** | | | | | | |
| RSEL Input Current | $I_{IH}$, $I_{IL}$ | | | | 150 | µA |
| RSEL Input High Voltage | $V_{IH}$ | | 1.8 | | $V_{CC}$ | V |
| RSEL Input Low Voltage | $V_{IL}$ | | 0 | | 0.8 | V |
| RSEL Input Impedance | $R_{PULL}$ | Internal pulldown resistor | 40 | 75 | 110 | kΩ |
| DISABLE Input Current | $I_{IH}$ | | | | 12 | µA |
| | $I_{IL}$ | Dependency on pullup resistance | | 420 | 800 | |
| DISABLE Input High Voltage | $V_{IH}$ | | 1.8 | | $V_{CC}$ | V |
| DISABLE Input Low Voltage | $V_{IL}$ | | 0 | | 0.8 | V |
| DISABLE Input Impedance | $R_{PULL}$ | Internal pullup resistor | 4.7 | 8 | 10 | kΩ |
| LOS, FAULT Output High Voltage | $V_{OH}$ | $R_{LOS}$ = 4.7kΩ - 10kΩ to $V_{CC}$, $R_{FAULT}$ = 4.7kΩ - 10kΩ to $V_{CC}$ | $V_{CC}$ - 0.5 | | $V_{CC}$ | V |
| LOS, FAULT Output Low Voltage | $V_{OL}$ | $R_{LOS}$ = 4.7kΩ - 10kΩ to $V_{CC}$, $R_{FAULT}$ = 4.7kΩ - 10kΩ to $V_{CC}$ | 0 | | 0.4 | V |
| **3-WIRE DIGITAL I/O SPECIFICATIONS (SDA, CSEL, SCL)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2.0 | | $V_{CC}$ | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input Hysteresis | $V_{HYST}$ | | | 0.082 | | V |
| Input Leakage Current | $I_{IL}$, $I_{IH}$ | $V_{IN}$ = 0V or $V_{CC}$; internal pullup or pulldown (75kΩ typ) | | | 150 | µA |
| Output High Voltage | $V_{OH}$ | External pullup of 4.7kΩ to $V_{CC}$ | $V_{CC}$ - 0.5 | | | V |
| Output Low Voltage | $V_{OL}$ | External pullup of 4.7kΩ to $V_{CC}$ | | | 0.4 | V |
| **3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (See Figure 4)** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | | 400 | 1000 | kHz |
| SCL Pulse-Width High | $t_{CH}$ | | 0.5 | | | µs |
| SCL Pulse-Width Low | $t_{CL}$ | | 0.5 | | | µs |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 2.85V to 3.63V, $T_A$ = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, $C_{AZ}$ = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, $V_{CC}$ = 3.3V, $I_{BIAS}$ = 6mA, $I_{MOD}$ = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SDA Setup Time | $t_{DS}$ | | | 100 | | ns |
| SDA Hold Time | $t_{DH}$ | | | 100 | | ns |
| SCL Rise to SDA Propagation Time | $t_D$ | | | 5 | | ns |
| CSEL Pulse-Width Low | $t_{CSW}$ | | 500 | | | ns |
| CSEL Leading Time Before the First SCL Edge | $t_L$ | | | 500 | | ns |
| CSEL Trailing Time After the Last SCL Edge | $t_T$ | | | 500 | | ns |
| SDA, SCL External Load | $C_B$ | Total bus capacitance on one line with 4.7kΩ pullup to $V_{CC}$ | | | 20 | pF |

**Note 1:** Supply current is measured with unterminated receiver CML output or with AC-coupled Rx output termination. The Tx output and the bias current output must be connected to a separate supply to remove the modulation/bias current portion from the supply current. BIAS must be connected to 2.0V. TOUT+/- must be connected through 50Ω load resistors to a separate supply voltage.

**Note 2:** Guaranteed by design and characterization, $T_A$ = -40°C to +95°C.

**Note 3:** The data input transition time is controlled by a 4th-order Bessel filter with -3dB frequency = 0.75 x data rate. The deterministic jitter caused by this filter is not included in the DJ generation specifications.

**Note 4:** Test pattern is 00001111 at 1.25Gbps for RATE_SEL = 0. Test pattern is 00001111 at 8.5Gbps for RATE_SEL = 1.

**Note 5:** Receiver deterministic jitter is measured with a repeating $2^{31}$ - 1 PRBS equivalent pattern at 10.32Gbps. For 1.25Gbps to 8.5Gbps, a repeating K28.5 pattern [00111110101100000101] is used. Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ).

**Note 6:** Measured with a k28.5 pattern from 1.0625Gbps to 8.5Gbps. Measured with $2^{31}$ - 1 PRBS at 10.32Gbps.

**Note 7:** Measurement includes an input AC-coupling capacitor of 100nF and $C_{CAZ}$ of 100nF. The signal at the input is switched between two amplitudes: Signal_ON and Signal_OFF.

1) Receiver operates at sensitivity level plus 1dB power penalty.
   a) Signal_OFF = 0
      Signal_ON = (+8dB) + 10log(min_assert_level)
   b) Signal_ON = (+1dB) + 10log(max_deassert_level)
      Signal_OFF = 0
2) Receiver operates at overload.
   Signal_OFF = 0
   Signal_ON = $1.2V_{P-P}$

max_deassert_level and the min_assert_level are measured for one LOS_THRESHOLD setting.

**Note 8:** Gain stability is defined as [(I_measured) - (I_reference)]/(I_reference) over the listed current range, temperature, and $V_{CC}$ from +2.95V to +3.63V. Reference current measured at $V_{CC}$ = +3.2V, $T_A$ = +25°C.

**Note 9:** Transmitter deterministic jitter is measured with a repeating $2^7$ - 1 PRBS, 72 0s, $2^7$ - 1 PRBS, and 72 1s pattern at 10.32Gbps. For 1.0625Gbps to 8.5Gbps, a repeating K28.5 pattern [00111110101100000101] is used. Deterministic jitter is defined as the arithmetic sum of PWD and PDJ.

**Note 10:** Gain stability is defined as [(I_measured) - (I_reference)]/(I_reference) over the listed current range, temperature, and $V_{CC}$ from +2.85V to +3.63V. Reference current measured at $V_{CC}$ = +3.3V, $T_A$ = +25°C.

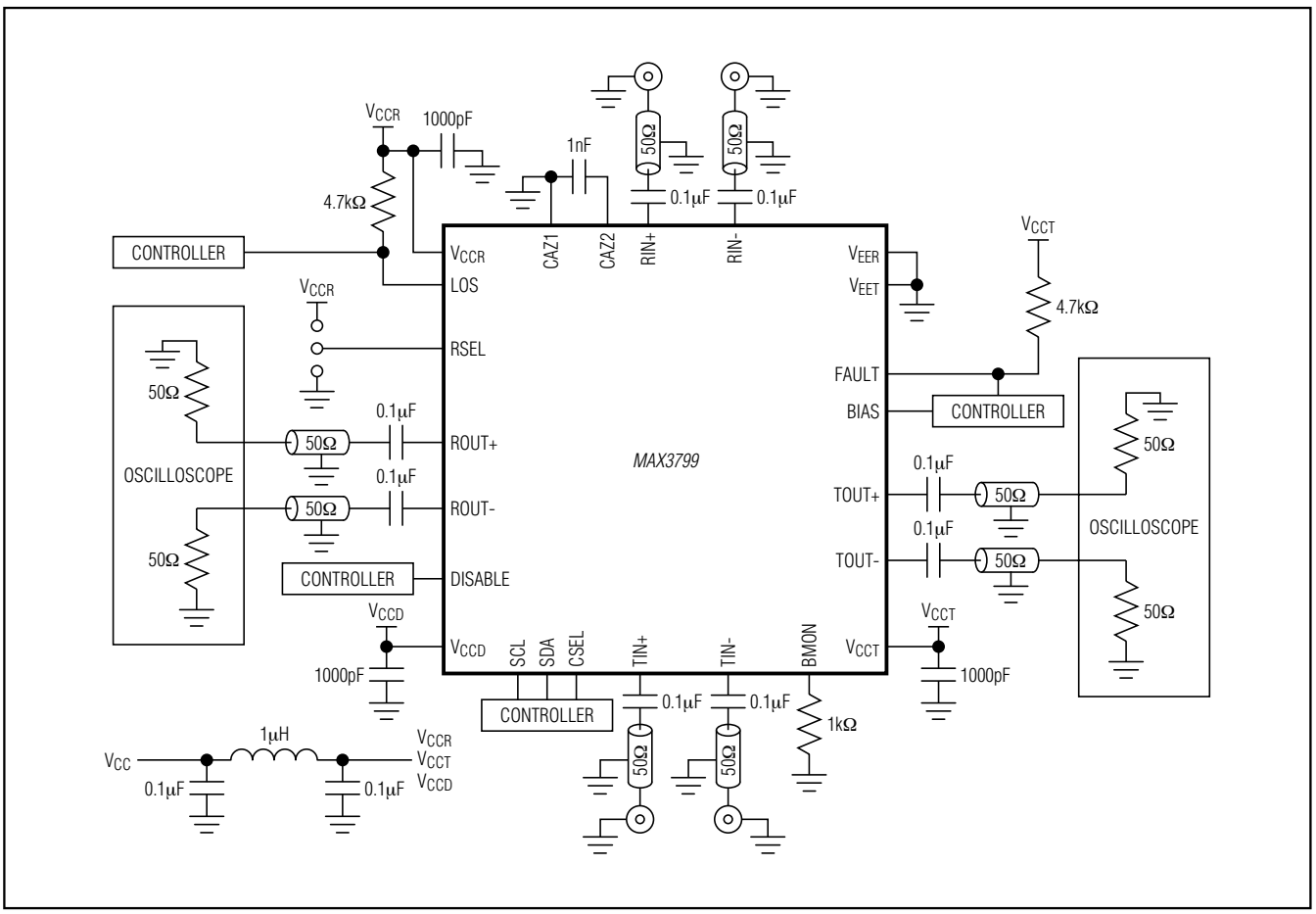
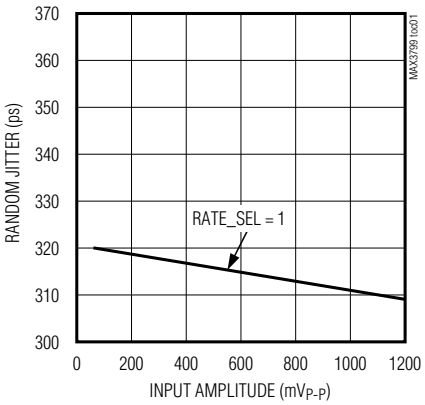



*Figure 1. Test Circuit for VCSEL Driver Characterization*

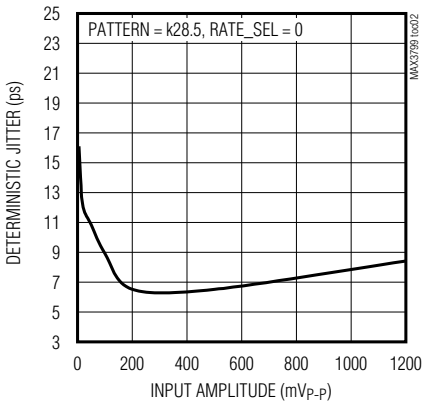
## Typical Operating Characteristics—Limiting Amplifier

($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

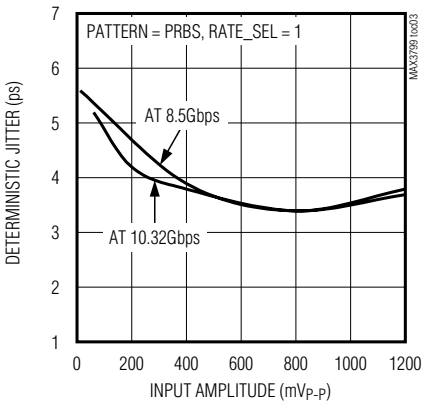
**RANDOM JITTER vs. INPUT AMPLITUDE**



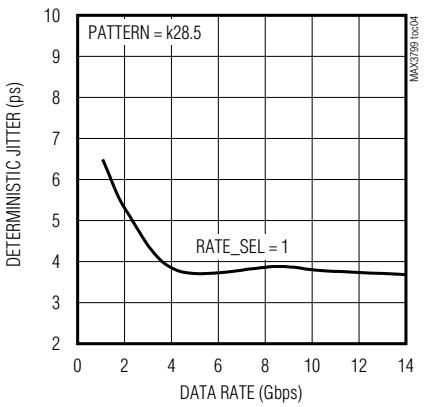

**DETERMINISTIC JITTER vs. INPUT AMPLITUDE AT 1.25Gbps**



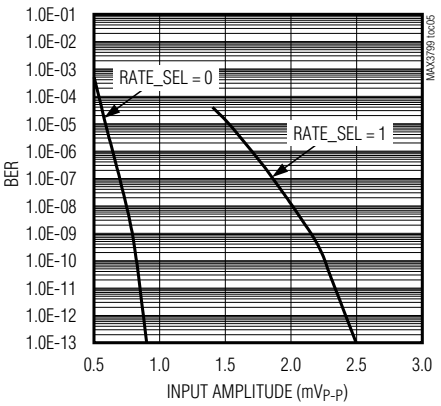

**DETERMINISTIC JITTER vs. INPUT AMPLITUDE**



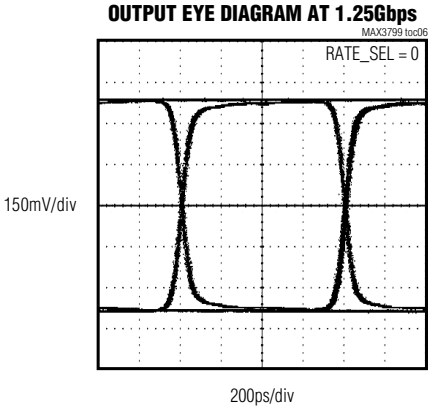

**DETERMINISTIC JITTER vs. DATA RATE**



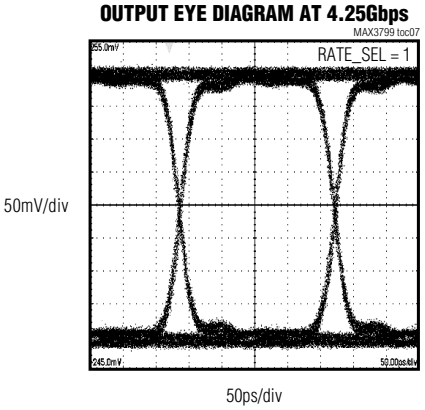

**BER vs. INPUT AMPLITUDE**



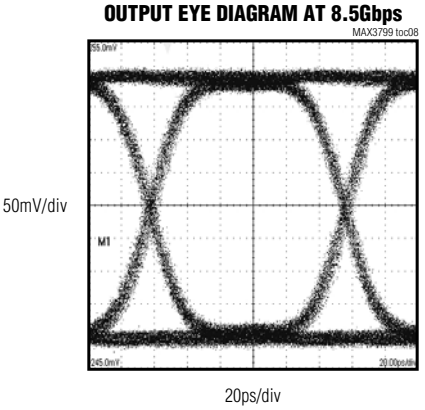

**OUTPUT EYE DIAGRAM AT 1.25Gbps**



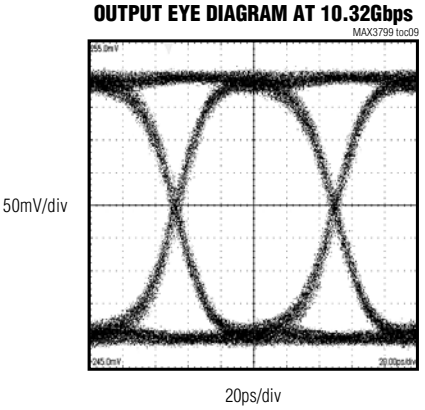

**OUTPUT EYE DIAGRAM AT 4.25Gbps**




**OUTPUT EYE DIAGRAM AT 8.5Gbps**



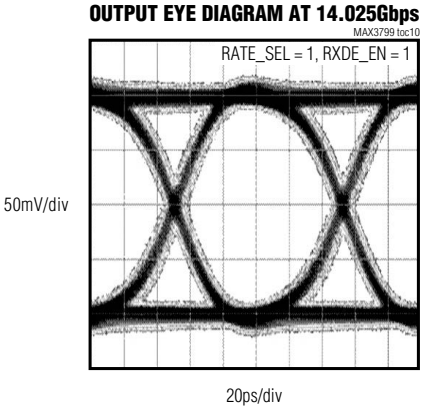

**OUTPUT EYE DIAGRAM AT 10.32Gbps**



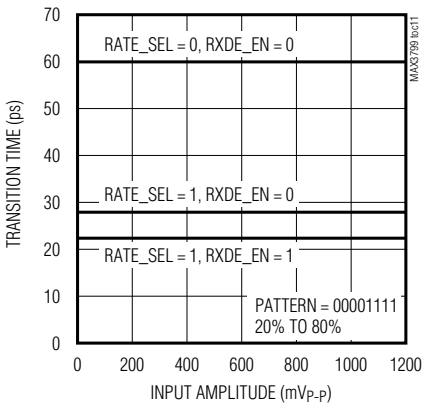
## Typical Operating Characteristics—Limiting Amplifier (continued)

($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

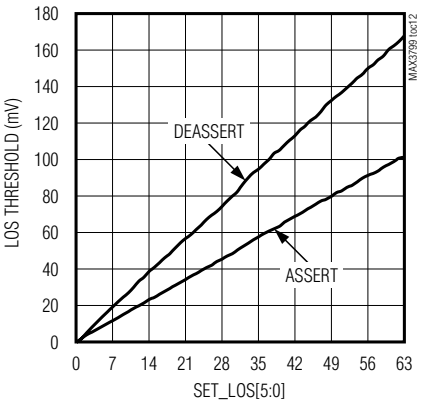
**OUTPUT EYE DIAGRAM AT 14.025Gbps**



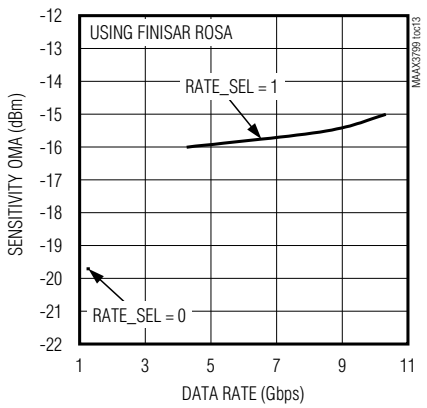

**TRANSITION TIME vs. INPUT AMPLITUDE**



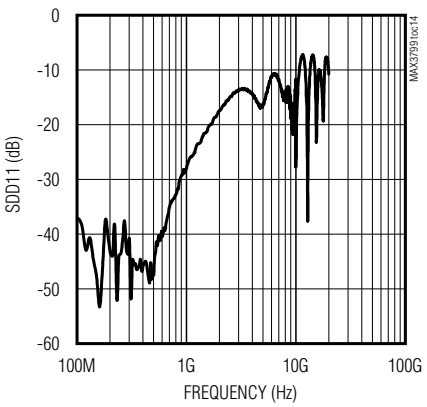

**LOS THRESHOLD vs. DAC SETTING**



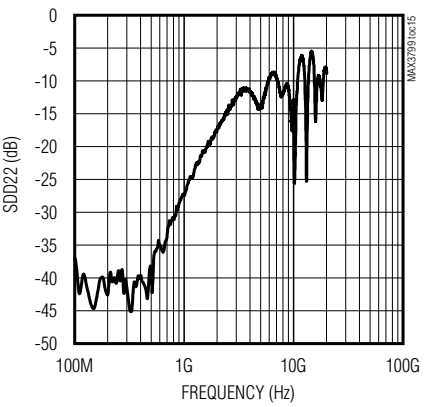

**SENSITIVITY vs. DATA RATE**



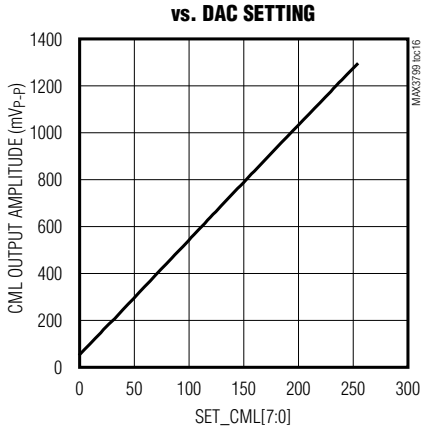

**Rx INPUT RETURN LOSS**



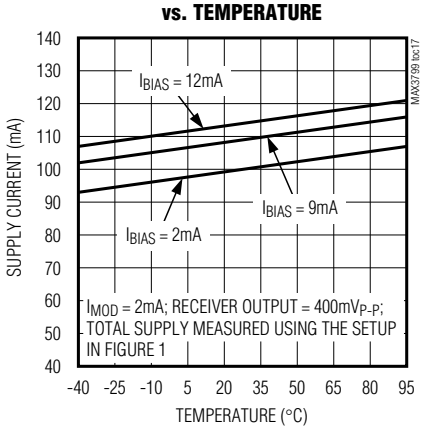

**Rx OUTPUT RETURN LOSS**



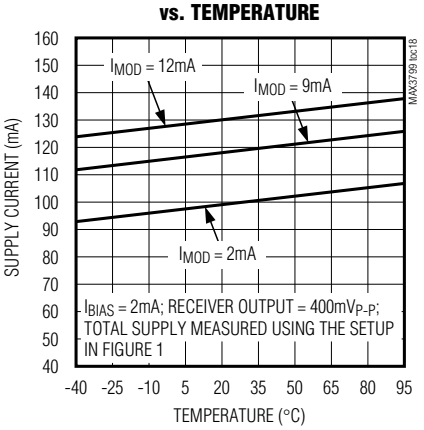

**CML OUTPUT AMPLITUDE vs. DAC SETTING**




**TOTAL SUPPLY CURRENT vs. TEMPERATURE**




**TOTAL SUPPLY CURRENT vs. TEMPERATURE**

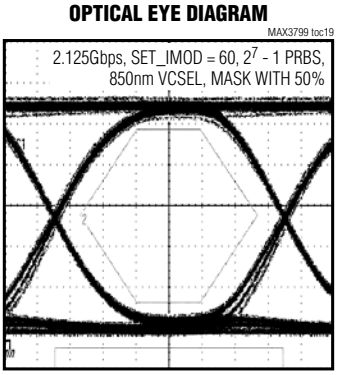


# 1Gbps to 14Gbps, SFP+ Multirate Limiting Amplifier and VCSEL Driver

## Typical Operating Characteristics—VCSEL Driver (continued)

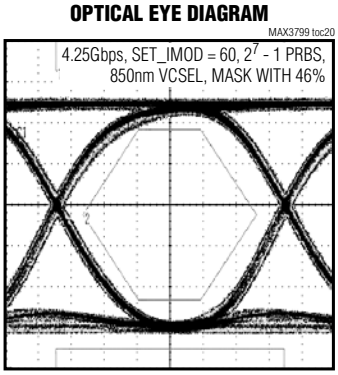
($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

**OPTICAL EYE DIAGRAM**



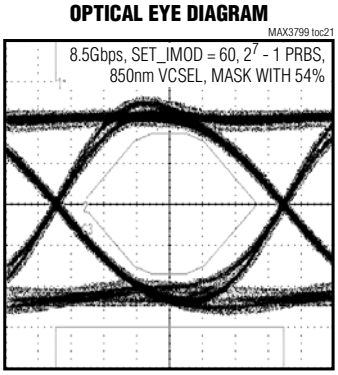

68ps/div

**OPTICAL EYE DIAGRAM**



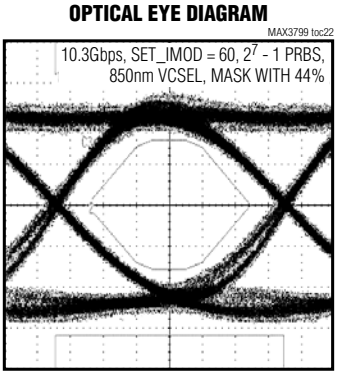

34ps/div

**OPTICAL EYE DIAGRAM**



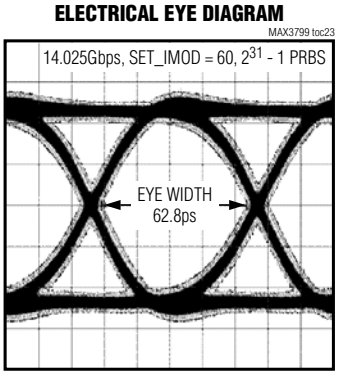

17ps/div

**OPTICAL EYE DIAGRAM**



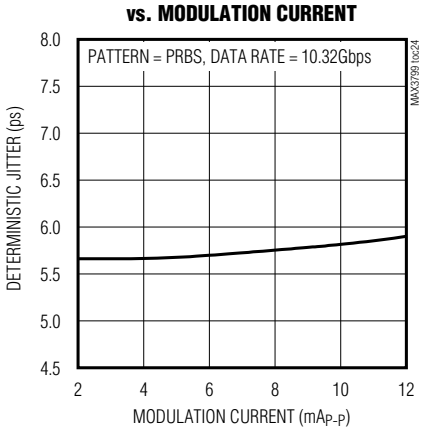

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**ELECTRICAL EYE DIAGRAM**

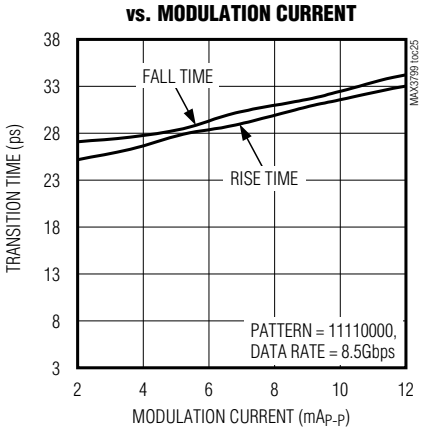



14ps/div

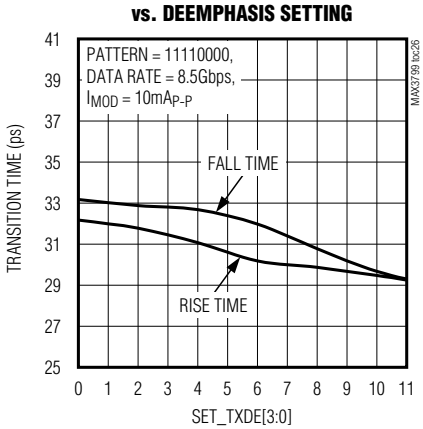
**DETERMINISTIC JITTER vs. MODULATION CURRENT**



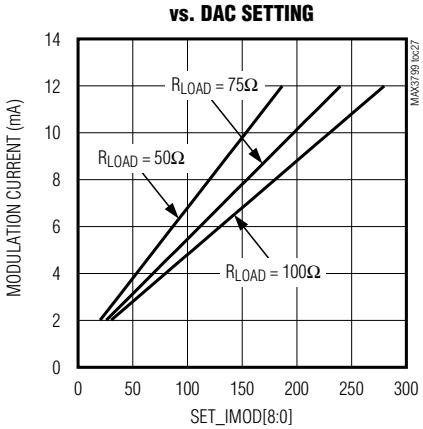

**TRANSITION TIME vs. MODULATION CURRENT**




**TRANSITION TIME vs. DEEMPHASIS SETTING**



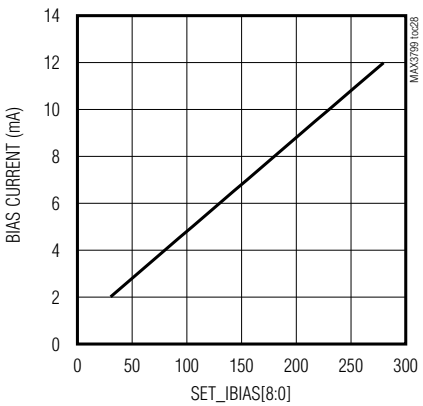

**MODULATION CURRENT vs. DAC SETTING**



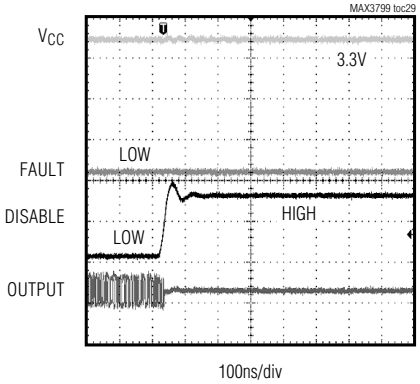
## Typical Operating Characteristics—VCSEL Driver (continued)

($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

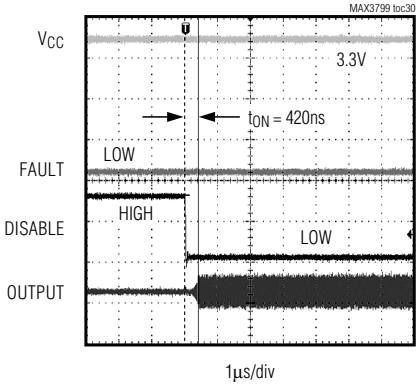
**BIAS CURRENT vs. DAC SETTING**



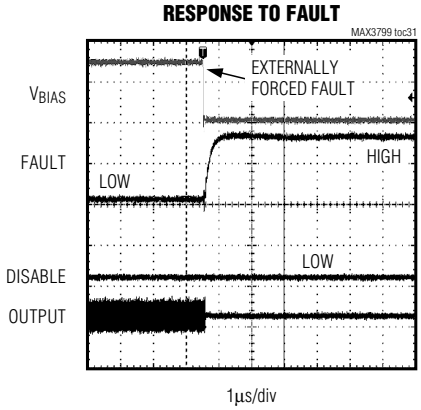

**TRANSMITTER DISABLE**



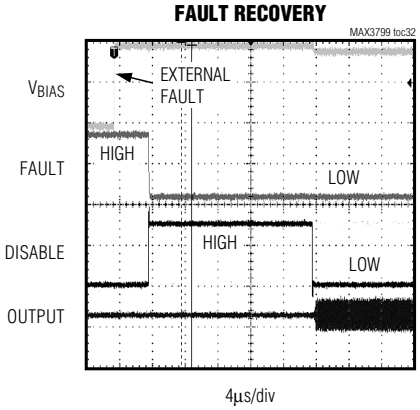

**TRANSMITTER ENABLE**



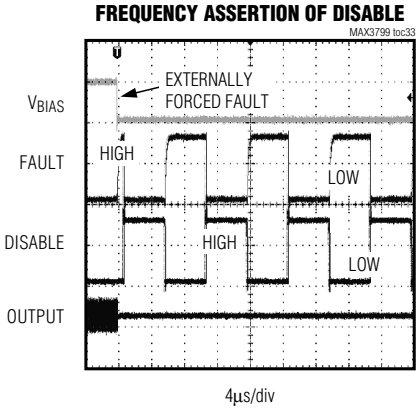

**RESPONSE TO FAULT**



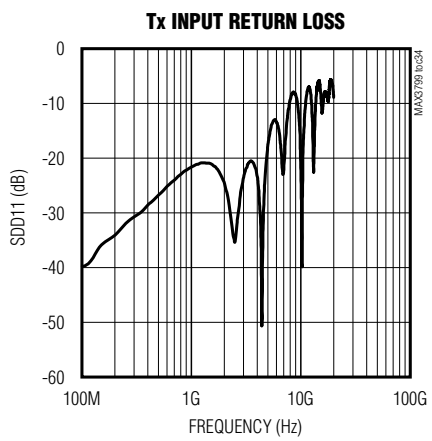

**FAULT RECOVERY**



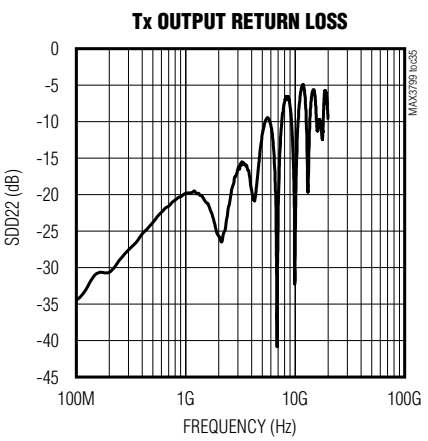

**FREQUENCY ASSERTION OF DISABLE**




**Tx INPUT RETURN LOSS**



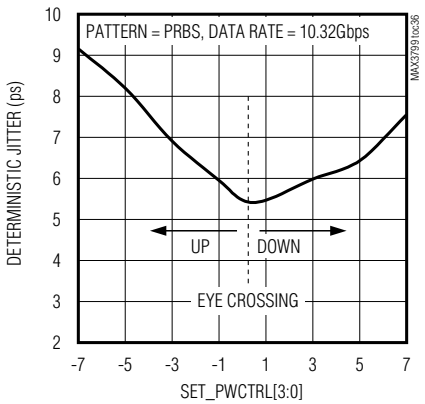

**Tx OUTPUT RETURN LOSS**



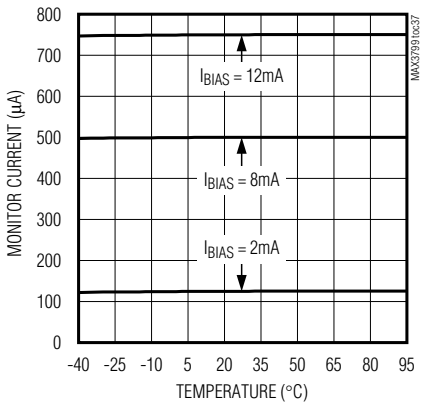
## Typical Operating Characteristics—VCSEL Driver (continued)

($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

**DETERMINISTIC JITTER vs. PULSE-WIDTH SETTING**




**BIAS MONITOR CURRENT vs. TEMPERATURE**




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | LOS | Loss-of-Signal Output, Open Drain. The default polarity of LOS is high when the level of the input signal is below the preset threshold set by the SET_LOS DAC. Polarity of the LOS function can be inverted by setting LOS_POL = 0. The LOS circuitry can be disabled by setting the bit LOS_EN = 0. |
| 2 | RSEL | Mode-Select Input, TTL/CMOS. Set the RSEL pin or RATE_SEL bit (set by the 3-wire digital interface) to logic-high for high-bandwidth mode. Setting RSEL and RATE_SEL logic-low for high-gain mode. The RSEL pin is internally pulled down by a 75kΩ resistor to ground. |
| 3, 6, 27, 30 | $V_{CCR}$ | Power Supply. Provides supply voltage to the receiver block. |
| 4 | ROUT+ | Noninverted Receive Data Output, CML. Back-terminated for 50Ω load. |
| 5 | ROUT- | Inverted Receive Data Output, CML. Back-terminated for 50Ω load. |
| 7 | $V_{CCD}$ | Power Supply. Provides supply voltage for the digital block. |
| 8 | DISABLE | Transmitter Disable Input, TTL/CMOS. Set to logic-low for normal operation. Logic-high or open disables both the modulation and bias current. Internally pulled up by an 8kΩ resistor to $V_{CCT}$. |
| 9 | SCL | Serial-Clock Input, TTL/CMOS. This pin has a 75kΩ internal pulldown. |
| 10 | SDA | Serial-Data Bidirectional Input, TTL/CMOS. Open-drain output. This pin has a 75kΩ internal pullup, but it requires an external 4.7kΩ pullup resistor to meet the 3-wire digital timing specification. (Data line collision protection is implemented.) |
| 11 | CSEL | Chip-Select Input, TTL/CMOS. Setting CSEL to logic-high starts a cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled down by a 75kΩ resistor to ground. |
| 12, 15, 18, 21, 24, 25 | $V_{CCT}$ | Power Supply. Provides supply voltage to the transmitter block. |
| 13 | TIN+ | Noninverted Transmit Data Input, CML |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 14 | TIN- | Inverted Transmit Data Input, CML |
| 16 | BMON | Bias Current Monitor Output. Current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the laser bias current. |
| 17 | $V_{EET}$ | Ground. Provides ground for the transmitter block. |
| 19 | TOUT- | Inverted Modulation Current Output. Back-termination of 50Ω to $V_{CCT}$. |
| 20 | TOUT+ | Noninverted Modulation Current Output. Back-termination of 50Ω to $V_{CCT}$. |
| 22 | BIAS | VCSEL Bias Current Output |
| 23 | FAULT | Transmitter Fault Output, Open Drain. Logic-high indicates a fault condition. FAULT remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by the DISABLE signal. |
| 26 | $V_{EER}$ | Ground. Provides ground for the receiver block. |
| 28 | RIN- | Inverted Receive Data Input, CML |
| 29 | RIN+ | Noninverted Receive Data Input, CML |
| 31 | CAZ2 | Offset Correction Loop Capacitor. A capacitor connected between this pin and CAZ1 sets the time constant of the offset correction loop. The offset correction can be disabled through the digital interface by setting the bit AZ_EN = 0. |
| 32 | CAZ1 | Offset Correction Loop Capacitor. Counterpart to CAZ2, internally connected to $V_{EER}$. |
| — | EP | Exposed Pad. Ground. Must be soldered to circuit board ground for proper thermal and electrical performance (see the *Exposed-Pad Package* section). |

## Detailed Description

The MAX3799 SFP+ transceiver combines a limiting amplifier receiver with loss-of-signal detection and a VCSEL laser driver transmitter with fault protection. Configuration of the advanced Rx and Tx settings of the MAX3799 is performed by a controller through the 3-wire interface. The MAX3799 provides multiple current and voltage DACs to allow the use of low-cost controller ICs.

### Limiting Amplifier Receiver

The limiting amplifier receiver inside the MAX3799 is designed to operate from 1.0625Gbps to 10.32Gbps. The receiver includes a dual path limiter, offset correction circuitry, CML output stage with deemphasis, and loss-of-signal circuitry. The functions of the receiver can be controlled through the on-chip 3-wire interface. The registers that control the receiver functionality are RXCTRL1, RXCTRL2, RXSTAT, MODECTRL, SET_CML, and SET_LOS.

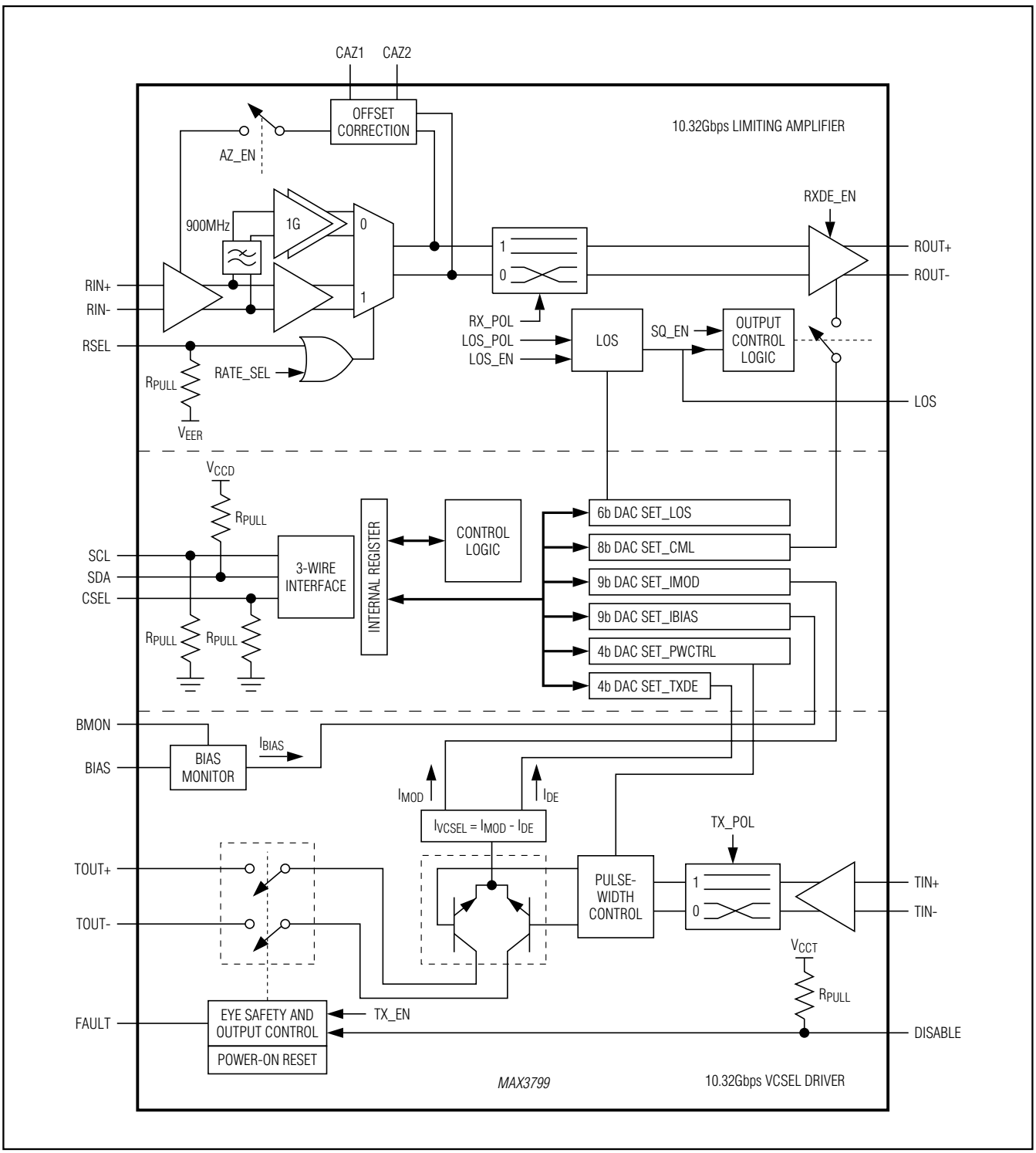



*Figure 2. Functional Diagram*

### Dual Path Limiter

The limiting amplifier features a low data-rate mode (1.25Gbps) and a high data-rate mode (up to 10.32Gbps), allowing for overall system optimization. Either the RSEL pin or the RATE_SEL bit can perform the rate selection. For operating up to 1.25Gbps, the low data-rate mode (RATE_SEL = 0) is recommended. For operation up to 14.025Gbps, the high data-rate mode (RATE_SEL = 1) is recommended. The polarity of the ROUT+/ROUT- relative to RIN+/RIN- is programmed by the RX_POL bit.

### Offset Correction Circuitry

The offset correction circuit is enabled to remove pulse-width distortion caused by intrinsic offset voltages within the differential amplifier stages. An external capacitor ($C_{AZ}$) connected between the CAZ1 and CAZ2 pins is used to set the offset correction loop cutoff frequency. The offset loop can be disabled using the AZ_EN bit.

### CML Output Stage with Deemphasis and Slew-Rate Control

The CML output stage is optimized for differential 100Ω loads. The RXDE_EN bit adds analog deemphasis compensation to the limited differential output signal for SFP connector losses. The output stage is controlled by a combination of the RX_EN and SQ_EN bits and the LOS pin. See Table 1.

Amplitude of the CML output stage is controlled by an 8-bit DAC register (SET_CML). The differential output amplitude range is from $40mV_{P-P}$ up to $1200mV_{P-P}$ with $4.6mV_{P-P}$ resolution (assuming an ideal 100Ω differential load).

### Loss-of-Signal (LOS) Circuitry

The input data amplitude is compared to a preset threshold controlled by the 6-bit DAC register SET_LOS. The LOS assert level can be programmed from $14mV_{P-P}$ up to $77mV_{P-P}$ with $1.5mV_{P-P}$ resolution (assuming an ideal 100Ω differential source). LOS is enabled through the LOS_EN bit and the polarity of the LOS is controlled with the LOS_POL bit.

## VCSEL Driver

The VCSEL driver inside the MAX3799 is designed to operate from 1.0625Gbps to 10.32Gbps. The transmitter contains a differential data path with pulse-width adjustment, bias current and modulation current DACs, output driver with programmable deemphasis, power-on reset circuitry, BIAS monitor, VCSEL current limiter, and eye safety circuitry. A 3-wire digital interface is used to control the transmitter functions. The registers that control the transmitter functionality are TXCTRL, TXSTAT1, TXSTAT2, SET_IBIAS, SET_IMOD, IMODMAX, IBIASMAX, MODINC, BIASINC, MODECTRL, SET_PWCTRL, and SET_TXDE.

### Differential Data Path

The CML input buffer is optimized for AC-coupled signals and is internally terminated with a differential 100Ω. Differential input data is equalized for high-frequency losses due to SFP connectors. The TX_POL bit in the TXCTRL register controls the polarity of TOUT+ and TOUT- vs. TIN+ and TIN-. The SET_PWCTRL register controls the output eye-crossing adjustment. A status indicator bit (TXED) monitors the presence of an AC input signal.

**Table 1. CML Output Stage Operation Mode**

| RX_EN | SQ_EN | LOS | OPERATION MODE DESCRIPTION |
|---|---|---|---|
| 0 | X | X | CML output disabled. |
| 1 | 0 | X | CML output enabled. |
| 1 | 1 | 0 | CML output enabled. |
| 1 | 1 | 1 | CML output disabled. |

**Table 2. Slew-Rate Control for CML Output Stage**

| RATE_SEL | OPERATION MODE DESCRIPTION |
|---|---|
| 0 | 1.25Gbps operation with reduced output edge speed. |
| 1 | Up to 10.32Gbps operation. |

### Bias Current DAC

The bias current from the MAX3799 is optimized to provide up to 15mA of bias current into a 50Ω to 75Ω VCSEL load with 40µA resolution. The bias current is controlled through the 3-wire digital interface using the SET_IBIAS, IBIASMAX, and BIASINC registers.

For VCSEL operation, the IBIASMAX register is first programmed to a desired maximum bias current value (up to 15mA). The bias current to the VCSEL then can range from zero to the value programmed into the IBIASMAX register. The bias current level is stored in the 9-bit SET_IBIAS register. Only bits 1 to 8 are written to. The LSB (bit 0) of SET_IBIAS is initialized to zero and is updated through the BIASINC register.

The value of the SET_IBIAS DAC register is updated when the BIASINC register is addressed through the 3-wire interface. The BIASINC register is an 8-bit register where the first 5 bits contain the increment information in two's complement notation. Increment values range from -8 to +7 LSBs. If the updated value of SET_IBIAS[8:1] exceeds IBIASMAX[7:0], the IBIASERR warning flag is set and SET_IBIAS[8:0] remains unchanged.

### Modulation Current DAC

The modulation current from the MAX3799 is optimized to provide up to 12mA of modulation current into a 100Ω differential load with 40µA resolution. The modulation current is controlled through the 3-wire digital interface using the SET_IMOD, IMODMAX, MODINC, and SET_TXDE registers.

For VCSEL operation, the IMODMAX register is first programmed to a desired maximum modulation current value (up to 12mA into a 100Ω differential load). The modulation current to the VCSEL then can range from zero to the value programmed into the IMODMAX register. The modulation current level is stored in the 9-bit SET_IMOD register. Only bits 1 to 8 are written to. The LSB (bit 0) of SET_IMOD is initialized to zero and is updated through the MODINC register.

The value of the SET_IMOD DAC register is updated when the MODINC register is addressed through the 3-wire interface. The MODINC register is an 8-bit register where the first 5 bits contain the increment information in two's complement notation. Increment values range from -8 to +7 LSBs. If the updated value of SET_IMOD[8:1] exceeds IMODMAX[7:0], the IMODERR warning flag is set and SET_IMOD[8:0] remains unchanged.

### Output Driver

The output driver is optimized for an AC-coupled 100Ω differential load. The output stage also features programmable deemphasis that allows the deemphasis amplitude to be set as a percentage of the modulation current. The deemphasis function is enabled by the TXDE_EN bit. At initial setup, the required amount of deemphasis can be set using the SET_TXDE register. During the system operation, it is advised to use the incremental mode that updates the deemphasis (SET_TXDE) and the modulation current DAC (SET_IMOD) simultaneously through the MODINC register.

### Power-On Reset (POR)

Power-on reset ensures that the laser is off until the supply voltage has reached a specified threshold (2.55V). After power-on reset, bias current and modulation current ramp up slowly to avoid an overshoot. In the case of a POR, all registers are reset to their default values.

### Bias Current Monitor

Current out of the BMON pin is typically 1/16th the value of $I_{BIAS}$. A resistor to ground at BMON sets the voltage gain. An internal comparator latches a SOFT FAULT if the voltage on BMON exceeds the value of $V_{CC}$ - 0.55V.

### Eye Safety and Output Control Circuitry

The safety and output control circuitry contains a disable pin (DISABLE) and disable bit (TX_EN), along with a FAULT indicator and fault detectors (Figure 3). The MAX3799 has two types of faults, HARD FAULT and SOFT FAULT. A HARD FAULT triggers the FAULT pin and the output to the VCSEL is disabled. A SOFT FAULT operates more like a warning and the outputs are not disabled. Both types of faults are stored in the TXSTAT1 and TXSTAT2 registers.

The FAULT pin is a latched output that can be cleared by toggling the DISABLE pin. Toggling the DISABLE pin also clears the TXSTAT1 and TXSTAT2 registers. A single-point fault can be a short to $V_{CC}$ or GND. Table 3 shows the circuit response to various single-point failures.

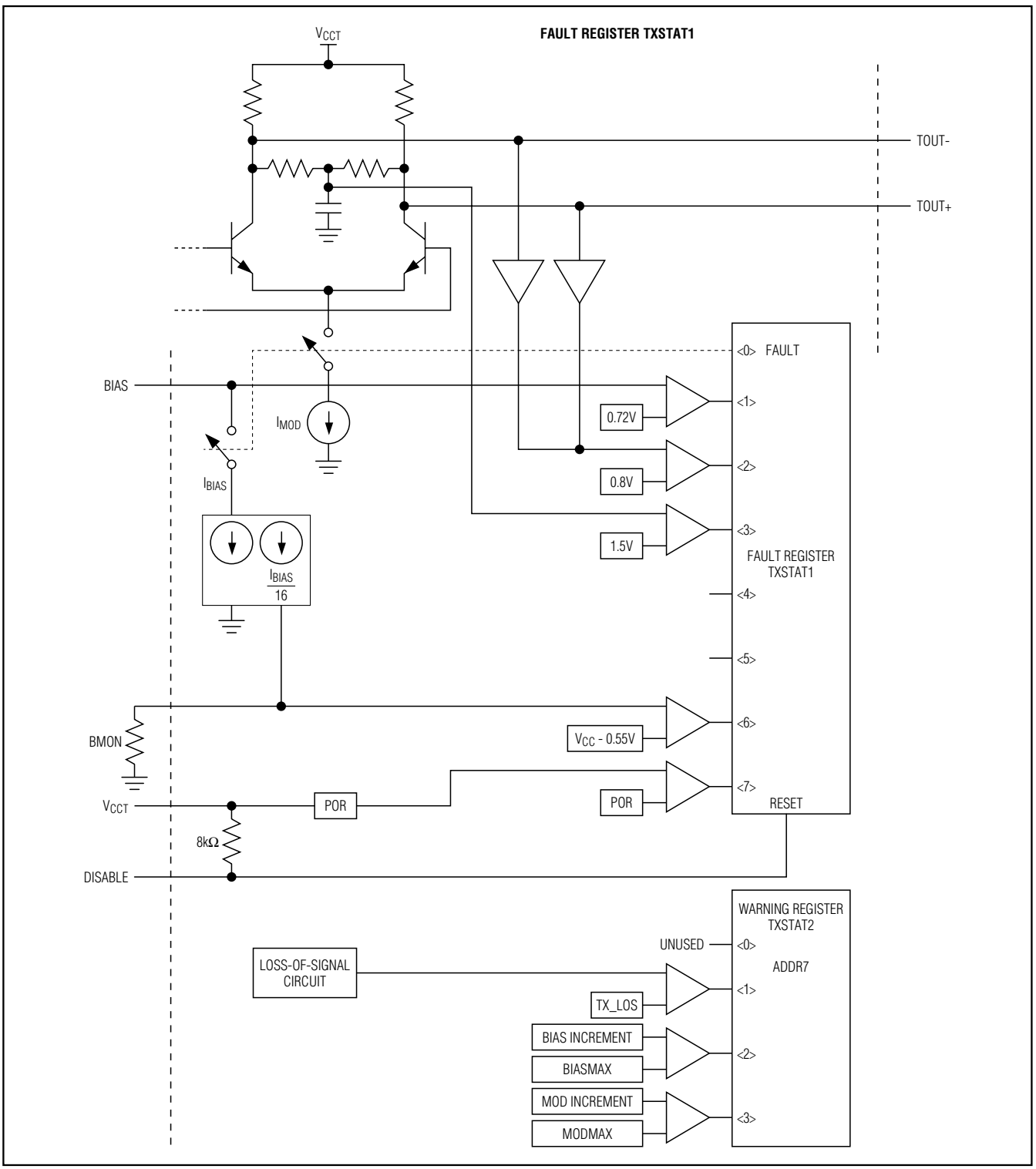



*Figure 3. Eye Safety Circuitry*

## Table 3. Circuit Response to Single-Point Faults

| PIN | NAME | SHORT TO $V_{CC}$ | SHORT TO GND | OPEN |
|---|---|---|---|---|
| 1 | LOS | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 2 | RSEL | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 3 | $V_{CCR}$ | Normal | Disabled—HARD FAULT (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 4 | ROUT+ | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 5 | ROUT- | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 6 | $V_{CCR}$ | Normal | Disabled—HARD FAULT (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 7 | $V_{CCD}$ | Normal | Disabled—HARD FAULT | Disabled—HARD FAULT |
| 8 | DISABLE | Disabled | Normal (Note 1). Can only be disabled with other means. | Disabled |
| 9 | SCL | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 10 | SDA | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 11 | CSEL | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 12 | $V_{CCT}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 13 | TIN+ | SOFT FAULT | SOFT FAULT | Normal (Note 1) |
| 14 | TIN- | SOFT FAULT | SOFT FAULT | Normal (Note 1) |
| 15 | $V_{CCT}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 16 | BMON | Disabled—HARD FAULT | Normal (Note 1) | Disabled—HARD FAULT |
| 17 | $V_{EET}$ | Disabled—Fault (external supply shorted) (Note 2) | Normal | Disabled—HARD FAULT |
| 18 | $V_{CCT}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 19 | TOUT- | $I_{MOD}$ is reduced | Disabled—HARD FAULT | $I_{MOD}$ is reduced |
| 20 | TOUT+ | $I_{MOD}$ is reduced | Disabled—HARD FAULT | $I_{MOD}$ is reduced |
| 21 | $V_{CCT}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 22 | BIAS | $I_{BIAS}$ is on—No Fault | Disabled—HARD FAULT | Disabled—HARD FAULT |
| 23 | FAULT | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 24 | $V_{CCT}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 25 | $V_{CCT}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 26 | $V_{EER}$ | Disabled—Fault (external supply shorted) (Note 2) | Normal | Normal (Note 3)—Redundant path |
| 27 | $V_{CCR}$ | Normal | Disabled—HARD FAULT (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 28 | RIN- | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 29 | RIN+ | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |

## Table 3. Circuit Response to Single-Point Faults (continued)

| PIN | NAME | SHORT TO $V_{CC}$ | SHORT TO GND | OPEN |
|---|---|---|---|---|
| 30 | $V_{CCR}$ | Normal | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path |
| 31 | CAZ2 | Normal (Note 1) | Normal (Note 1) | Normal (Note 1) |
| 32 | CAZ1 ($V_{EER}$) | Disabled—Fault (external supply shorted) (Note 2) | Normal (Note 3)—Redundant path | Normal (Note 3)—Redundant path |

**Note 1:** Normal—Does not affect laser power.
**Note 2:** Supply-shorted current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.
**Note 3:** Normal in functionality, but performance could be affected.
**Warning:** Shorted to $V_{CC}$ or shorted to ground on some pins can violate the *Absolute Maximum Ratings*.

### 3-Wire Digital Communication

The MAX3799 implements a proprietary 3-wire digital interface. An external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. The master starts to generate a clock signal after the CSEL pin has been set to 1. All data transfers are most significant bit (MSB) first.

#### Protocol

Each operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the MAX3799. The RWN bit determines if the cycle is read or write. See Table 4.

#### Register Addresses

The MAX3799 contains 17 registers available for programming. Table 5 shows the registers and addresses.

#### Write Mode (RWN = 0)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 4 shows the interface timing.

#### Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 4 shows the interface timing.

#### Mode Control

Normal mode allows read-only instruction for all registers except MODINC and BIASINC. The MODINC and BIASINC registers can be updated during normal mode. Doing so speeds up the laser control update through the 3-wire interface by a factor of two. The normal mode is the default mode.

Setup mode allows the master to write unrestricted data into any register except the status (TXSTAT1, TXSTAT2, and RXSTAT) registers. To enter the setup mode, the MODECTRL register (address = H0x0E) must be set to H0x12. After the MODECTRL register has been set to H0x12, the next operation is unrestricted. The setup mode is automatically exited after the next operation is finished. This sequence must be repeated if further unrestricted settings are necessary.

## Table 4. Digital Communication Word Structure

| BIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register Address | | | | | | | RWN | Data that is written or read. | | | | | | | |

## Table 5. Register Descriptions and Addresses

| ADDRESS | NAME | FUNCTION |
|---|---|---|
| H0x00 | RXCTRL1 | Receiver Control Register 1 |
| H0x01 | RXCTRL2 | Receiver Control Register 2 |
| H0x02 | RXSTAT | Receiver Status Register |
| H0x03 | SET_CML | Output CML Level Setting Register |
| H0x04 | SET_LOS | LOS Threshold Level Setting Register |
| H0x05 | TXCTRL | Transmitter Control Register |
| H0x06 | TXSTAT1 | Transmitter Status Register 1 |
| H0x07 | TXSTAT2 | Transmitter Status Register 2 |
| H0x08 | SET_IBIAS | Bias Current Setting Register |
| H0x09 | SET_IMOD | Modulation Current Setting Register |
| H0x0A | IMODMAX | Maximum Modulation Current Setting Register |
| H0x0B | IBIASMAX | Maximum Bias Current Setting Register |
| H0x0C | MODINC | Modulation Current Increment Setting Register |
| H0x0D | BIASINC | Bias Current Increment Setting Register |
| H0x0E | MODECTRL | Mode Control Register |
| H0x0F | SET_PWCTRL | Transmitter Pulse-Width Control Register |
| H0x10 | SET_TXDE | Transmitter Deemphasis Control Register |

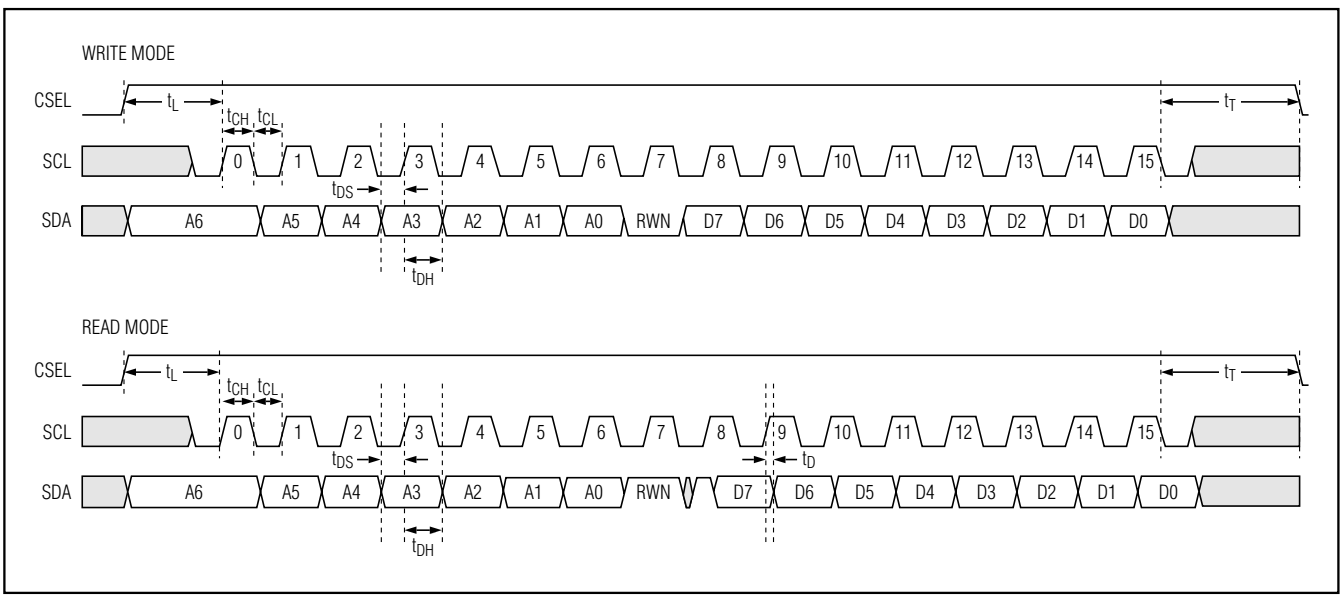



*Figure 4. Timing for 3-Wire Digital Interface*

## Register Descriptions

### Receiver Control Register 1 (RXCTRL1)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | X | X | X | X | RATE_SEL | X | H0x00 |
| Default Value | X | X | X | X | X | X | 0 | X | |

**Bit 1: RATE_SEL.** RATE_SEL combined with the RSEL pin through a logic-OR function selects between the low data-rate mode (1.25Gbps) or high data-rate mode (up to 10.32Gbps).

Logic-OR output 0 = 1Gbps mode

Logic-OR output 1 = 10Gbps mode

### Receiver Control Register 2 (RXCTRL2)

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | LOS_EN | LOS_POL | RX_POL | SQ_EN | RX_EN | RXDE_EN | AZ_EN | H0x01 |
| Default Value | X | 1 | 1 | 1 | 0 | 1 | 0 | 1 | |

**Bit 6: LOS_EN.** Controls the LOS circuitry. When RX_EN is set to 0, the LOS detector is also disabled.

0 = disabled

1 = enabled

**Bit 5: LOS_POL.** Controls the output polarity of the LOS pin.

0 = inverse

1 = normal

**Bit 4: RX_POL.** Controls the polarity of the receiver signal path.

0 = inverse

1 = normal

**Bit 3: SQ_EN.** When SQ_EN = 1, the LOS controls the output circuitry.

0 = disabled

1 = enabled

**Bit 2: RX_EN.** Enables or disables the receive circuitry.

0 = disabled

1 = enabled

**Bit 1: RXDE_EN.** Enables or disables the deemphasis on the receiver output.

0 = disabled

1 = enabled

**Bit 0: AZ_EN.** Enables or disables the autozero circuitry. When RX_EN is set to 0, the autozero circuitry is also disabled.

0 = disabled

1 = enabled

***Receiver Status Register (RXSTAT)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 (STICKY) | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | X | X | X | X | X | LOS | H0x02 |
| Default Value | X | X | X | X | X | X | X | X | |

**Bit 0: LOS.** Copy of the LOS output circuitry. This is a sticky bit, which means that it is cleared on a read. The first 0-to-1 transition gets latched until the bit is read by the master or POR occurs.

***Output CML Level Setting Register (SET_CML)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | SET_CML[7] (MSB) | SET_CML[6] | SET_CML[5] | SET_CML[4] | SET_CML[3] | SET_CML[2] | SET_CML[1] | SET_CML[0] (LSB) | H0x03 |
| Default Value | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | |

**Bits 7 to 0: SET_CML[7:0].** The SET_CML register is an 8-bit register that can be set up to 255, corresponding to an output up to 1000mV$_{P-P}$. See the *Typical Operating Characteristics* section for a typical CML output voltage vs. DAC code graph.

***LOS Threshold Level Setting Register (SET_LOS)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | SET_LOS[5] (MSB) | SET_LOS[4] | SET_LOS[3] | SET_LOS[2] | SET_LOS[1] | SET_LOS[0] (LSB) | H0x04 |
| Default Value | X | X | 0 | 0 | 1 | 1 | 0 | 0 | |

**Bits 5 to 0: SET_LOS[5:0].** The SET_LOS register is a 6-bit register used to program the LOS threshold. See the *Typical Operating Characteristics* section for a typical LOS threshold voltage vs. DAC code graph.

***Transmitter Control Register (TXCTRL)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | X | X | TXDE_EN | SOFTRES | TX_POL | TX_EN | H0x05 |
| Default Value | X | X | X | X | 0 | 0 | 1 | 1 | |

**Bit 3: TXDE_EN.** Enables or disables the transmit output deemphasis circuitry.

0 = disabled

1 = enabled

**Bit 2: SOFTRES.** Resets all registers to their default values.

0 = normal

1 = reset

**Bit 1: TX_POL.** Controls the polarity of the transmit signal path.

0 = inverse

1 = normal

**Bit 0: TX_EN.** Enables or disables the transmit circuitry.

0 = disabled

1 = enabled

***Transmitter Status Register 1 (TXSTAT1)***

| Bit # | 7 (STICKY) | 6 (STICKY) | 5 (STICKY) | 4 (STICKY) | 3 (STICKY) | 2 (STICKY) | 1 (STICKY) | 0 (STICKY) | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | FST[7] | FST[6] | X | X | FST[3] | FST[2] | FST[1] | TX_FAULT | H0x06 |
| Default Value | X | X | X | X | X | X | X | X | |

**Bit 7: FST[7].** When the $V_{CCT}$ supply voltage is below 2.45V, the POR circuitry reports a FAULT. Once the $V_{CCT}$ supply voltage is above 2.55V, the POR resets all registers to their default values and the FAULT is cleared.

**Bit 6: FST[6].** When the voltage at BMON is above $V_{CC}$ - 0.55V, a SOFT FAULT is reported.

**Bit 3: FST[3].** When the common-mode voltage at $V_{TOUT}$+/- goes below 1.5V, a SOFT FAULT is reported.

**Bit 2: FST[2].** When the voltage at $V_{TOUT}$+/- goes below 0.8V, a HARD FAULT is reported.

**Bit 1: FST[1].** When the BIAS voltage goes below 0.44V, a HARD FAULT is reported.

**Bit 0: TX_FAULT.** Copy of a FAULT signal in FST[7] to FST[1]. A POR resets FST[7:1] to 0.

***Transmitter Status Register 2 (TXSTAT2)***

| Bit # | 7 | 6 | 5 | 4 | 3 (STICKY) | 2 (STICKY) | 1 (STICKY) | 0 (STICKY) | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | X | X | IMODERR | IBIASERR | TXED | X | H0x07 |
| Default Value | X | X | X | X | X | X | X | X | |

**Bit 3: IMODERR.** When the modulation-incremented result is greater than IMODMAX, a SOFT FAULT is reported. See the *Programming Modulation Current* section.

**Bit 2: IBIASERR.** When the bias incremented result is greater than IBIASMAX, then a SOFT FAULT is reported. See the *Programming Bias Current* section.

**Bit 1: TXED.** This only indicates the absence of an AC signal at the transmit input. This is not an LOS indicator.

***Bias Current Setting Register (SET_IBIAS)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | SET_IBIAS [8] (MSB) | SET_IBIAS [7] | SET_IBIAS [6] | SET_IBIAS [5] | SET_IBIAS [4] | SET_IBIAS [3] | SET_IBIAS [2] | SET_IBIAS [1] | H0x08 |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | |

**Bits 7 to 0: SET_IBIAS[8:1].** The bias current DAC is controlled by a total of 9 bits. The SET_IBIAS[8:1] bits are used to set the bias current with even denominations from 0 to 510 bits. The LSB (SET_IBIAS[0]) bit is controlled by the BIASINC register and is used to set the odd denominations in the SET_IBIAS[8:0].

***Modulation Current Setting Register (SET_IMOD)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | SET_IMOD [8] (MSB) | SET_IMOD [7] | SET_IMOD [6] | SET_IMOD [5] | SET_IMOD [4] | SET_IMOD [3] | SET_IMOD [2] | SET_IMOD [1] | H0x09 |
| Default Value | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | |

**Bits 7 to 0: SET_IMOD[8:1].** The modulation current DAC is controlled by a total of 9 bits. The SET_IMOD[8:1] bits are used to set the modulation current with even denominations from 0 to 510 bits. The LSB (SET_IMOD[0]) bit is controlled by the MODINC register and is used to set the odd denominations in the SET_IMOD[8:0].

***Maximum Modulation Current Setting Register (IMODMAX)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | IMODMAX [7] (MSB) | IMODMAX [6] | IMODMAX [5] | IMODMAX [4] | IMODMAX [3] | IMODMAX [2] | IMODMAX [1] | IMODMAX [0] (LSB) | H0x0A |
| Default Value | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |

**Bits 7 to 0: IMODMAX[7:0].** The IMODMAX register is an 8-bit register that can be used to limit the maximum modulation current. IMODMAX[7:0] is continuously compared to the SET_IMOD[8:1].

***Maximum Bias Current Setting Register (IBIASMAX)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | IBIASMAX [7] (MSB) | IBIASMAX [6] | IBIASMAX [5] | IBIASMAX [4] | IBIASMAX [3] | IBIASMAX [2] | IBIASMAX [1] | IBIASMAX [0] (LSB) | H0x0B |
| Default Value | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | |

**Bits 7 to 0: IBIASMAX[7:0].** The IBIASMAX register is an 8-bit register that can be used to limit the maximum bias current. IBIASMAX[7:0] is continuously compared to the SET_IBAS[8:1].

***Modulation Current Increment Setting Register (MODINC)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | SET_IMOD [0] | X | DE_INC | MODINC[4] (MSB) | MODINC[3] | MODINC[2] | MODINC[1] | MODINC[0] (LSB) | H0x0C |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 7: SET_IMOD[0].** This is the LSB of the SET_IMOD[8:0] bits. This bit can only be updated by the use of MODINC[4:0].

**Bit 5: DE_INC.** When this bit is set to 1 and the deemphasis on the transmit output is enabled, the SET_TXDE[3:0] is incremented or decremented by 1 LSB. The increment or decrement is determined by the sign bit of the MODINC[4:0] string of bits.

**Bits 4 to 0: MODINC[4:0].** This string of bits is used to increment or decrement the modulation current. When written to, the SET_IMOD[8:0] bits are updated. MODINC[4:0] are a two's complement string.

***Bias Current Increment Setting Register (BIASINC)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | SET_IBIAS [0] | X | X | BIASINC[4] (MSB) | BIASINC[3] | BIASINC[2] | BIASINC[1] | BIASINC[0] (LSB) | H0x0D |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 7: SET_IBIAS[0].** This is the LSB of the SET_IBIAS[8:0] bits. This bit can only be updated by the use of BIASINC[4:0].

**Bits 4 to 0: BIASINC[4:0].** This string of bits is used to increment or decrement the bias current. When written to, the SET_IBIAS[8:0] bits are updated. BIASINC[4:0] are a two's complement string.

***Mode Control Register (MODECTRL)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | MODECTRL [7] (MSB) | MODECTRL [6] | MODECTRL [5] | MODECTRL [4] | MODECTRL [3] | MODECTRL [2] | MODECTRL [1] | MODECTRL [0] (LSB) | H0x0E |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bits 7 to 0: MODECTRL[7:0].** The MODECTRL register enables a switch between normal and setup modes. The setup mode is achieved by setting this register to H0x12. MODECTRL must be updated before each write operation. Exceptions are MODINC and BIASINC, which can be updated in normal mode.

***Transmitter Pulse-Width Control Register (SET_PWCTRL)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | X | X | SET_ PWCTRL[3] (MSB) | SET_ PWCTRL[2] | SET_ PWCTRL[1] | SET_ PWCTRL[0] (LSB) | H0x0F |
| Default Value | X | X | X | X | 0 | 0 | 0 | 0 | |

**Bits 3 to 0: SET_PWCTRL[3:0].** This is a 4-bit register used to control the eye crossing by adjusting the pulse width.

***Transmitter Deemphasis Control Register (SET_TXDE)***

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDRESS |
|---|---|---|---|---|---|---|---|---|---|
| Name | X | X | X | X | SET_TXDE [3] (MSB) | SET_TXDE [2] | SET_TXDE [1] | SET_TXDE [0] (LSB) | H0x10 |
| Default Value | X | X | X | X | 0 | 0 | 0 | 0 | |

**Bits 3 to 0: SET_TXDE[3:0].** This is a 4-bit register used to control the amount of deemphasis on the transmitter output. When calculating the total modulation current, the amount of deemphasis must be taken into account. The deemphasis is set as a percentage of modulation current.

## Design Procedure

### Programming Bias Current

1) IBIASMAX[7:0] = Maximum_Bias_Current_Value

2) $SET_IBIAS_i[8:1]$ = Initial_Bias_Current_Value

**Note:** The total bias current value is calculated using the SET_IBIAS[8:0] register. SET_IBIAS[8:1] are the bits that can be manually written. SET_IBIAS[0] can only be updated using the BIASINC[4:0] register.

When implementing an APC loop, it is recommended to use the BIASINC[4:0] register, which guarantees the fastest bias current update.

3) $BIASINC_i[4:0]$ = New_Increment_Value

4) If ($SET_IBIAS_i[8:1] \le$ IBIASMAX[7:0]), then ($SET_IBIAS_i[8:0] = SET_IBIAS_{i-1}[8:0] + BIASINC_i[4:0]$)

5) Else ($SET_IBIAS_i[8:0] = SET_IBIAS_{i-1}[8:0]$)

The total bias current can be calculated as follows:

6) $I_{BIAS} = [SET_IBIAS_i[8:0] + 20] \times 40\mu A$

### Programming Modulation Current

1) IMODMAX[7:0] = Maximum_Modulation_Current_Value

2) $SET_IMOD_i[8:1]$ = Initial_Modulation_Current_Value

**Note:** The total modulation current value is calculated using the SET_IMOD[8:0] register. SET_IMOD[8:1] are the bits that can be manually written. SET_IMOD[0] can only be updated using the MODINC[4:0] register.

When implementing modulation compensation, it is recommended to use the MODINC[4:0] register, which guarantees the fastest modulation current update.

3) $MODINC_i[4:0]$ = New_Increment_Value

4) If ($SET_IMOD_i[8:1] \le$ IMODMAX[7:0]), then ($SET_IMOD_i[8:0] = SET_IMOD_{i-1}[8:0] + MODINC_i[4:0]$)

5) Else ($SET_IMOD_i[8:0] = SET_IMOD_{i-1}[8:0]$)

The following equation is valid with assumption of 100Ω on-chip and 100Ω external differential load (Rextd). The maximum value that can be set for SET_TXDE[3:0] = 11.

6) $$I_{MOD(Rextd=100\Omega)} = [(20 + SET_IMOD_i[8:0]) \times 40\mu A] \times \left[1 - \frac{2 + SET_TXDE[3:0]}{64}\right]$$

For general Rextd, the modulation current that is achieved using the same setting of $SET_IMOD_i[8:0]$ as for Rextd = 100Ω is shown below. It can be written as a function of $I_{MOD(Rextd=100\Omega)}$, still assuming a 100Ω on-chip load.

7) $$I_{MOD(Rextd)} = 2 \times I_{MOD(Rextd=100\Omega)} \left[\frac{Rext}{Rext + 100}\right]$$

### Programming LOS Threshold

$$LOS_{TH} = (SET_LOS[5:0] \times 1.5mV_{P-P})$$

### Programming Transmit Output Deemphasis

The TXDE_EN bit must be set to 1 to enable the deemphasis function. The SET_TXDE register value is used to set the amount of deemphasis, which is a percentage of the modulation current. Deemphasis percentage is determined as:

$$DE(\%) = \frac{100 \times (2 + SET_TXDE[3:0])}{64}$$

where the maximum SET_TXDE[3:0] = 11.

For an $I_{MOD}$ value of 10mA, the maximum achievable deemphasis value is approximately 20%. Maximum deemphasis achievable for full $I_{MOD}$ range of 12mA is limited to 15%.

With deemphasis enabled, the value of the modulation current amplitude is reduced by the calculated deemphasis percentage. To maintain the modulation current amplitude constant, the SET_IMOD[8:0] register must be increased by the deemphasis percentage. If the system conditions like temperature, required $I_{MOD}$ value, etc., change during the transmit operation, the deemphasis setting might need to be readjusted. For such an

impromptu deemphasis adjustment, it is recommended that the DE_INC (MODINC[5]) bit is used. Use of this bit increments or decrements the deemphasis code setting by 1 LSB based on the sign of increment in the MODINC[4:0] and, hence, the SET_IMOD[8:0] setting. This helps maintain the BER while having the flexibility to improve signal quality by adjusting deemphasis while the transmit operation continues. This feature enables glitchless deemphasis adjustment while maintaining excellent BER performance.

### Activating Receiver Output Deemphasis

The RXDE_EN bit must be set to 1 to enable the deemphasis function. Deemphasis decreases the output amplitude at ROUT+/ROUT- by 25%. To maintain the same output amplitude as before the activation of deemphasis, the SET_CML register value needs to be increased by 25%. When deemphasis is enabled, the limiting amplifier AC performance is guaranteed up to 800mV$_{P-P}$ typical output amplitude. The SET_CML register can be set from 0 to 255 bits, but it is important to note that performance is guaranteed up to 215 bits.

### Programming Pulse-Width Control

The eye crossing at the Tx output can be adjusted using the SET_PWCTRL register. Table 6 shows these settings.

The sign of the number specifies the direction of pulse-width distortion. The code of 1111 corresponds to a balanced state for differential output. The pulse-width distortion is bidirectional around the balanced state (see the *Typical Operating Characteristics* section).

### Programming CML Output Settings

Amplitude of the CML output stage is controlled by an 8-bit DAC register (SET_CML). The differential output amplitude is up to 1000mV$_{P-P}$ with 4.6mV$_{P-P}$ resolution (assuming an ideal 100Ω differential load). The guaranteed output CML DAC range is up to 215.

$$\text{Output Voltage } R_{OUT} \text{ (mV}_{P-P}\text{)} = 40 + 4.55 \text{ (SET_CML)}$$

### Select the Coupling Capacitor

For AC-coupling, the coupling capacitors $C_{IN}$ and $C_{OUT}$ should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff ($f_{IN}$) is decreased.

$$f_{IN} = 1/[2\pi(50)(C_{IN})]$$

The recommended $C_{IN}$ and $C_{OUT}$ is 0.1µF for the MAX3799.

### Select the Offset-Correction Capacitor

The capacitor between CAZ1 and CAZ2 determines the time constant of the signal path DC-offset cancellation loop. To maintain stability, it is important to keep at least a one-decade separation between $f_{IN}$ and the low-frequency cutoff ($f_{OC}$) associated with the DC-offset cancellation circuit. A 1nF capacitor between CAZ1 and CAZ2 is recommended for the MAX3799.

## Applications Information

### Layout Considerations

To minimize inductance, keep the connections between the MAX3799 output pins and laser diode as close as possible. Optimize the laser diode performance by placing a bypass capacitor as close as possible to the laser anode. Use good high-frequency layout techniques and multiple-layer boards with uninterrupted ground planes to minimize EMI and crosstalk.

### Exposed-Pad Package

The exposed pad on the 32-pin TQFN provides a very low-thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3799 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

### Laser Safety and IEC 825

Using the MAX3799 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each user must determine the level of fault tolerance required by the application, recognizing that Maxim products are neither designed nor authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application in which the failure of a Maxim product could create a situation where personal injury or death could occur.

**Table 6. Eye-Crossing Settings for SET_PWCTRL**

| SET_PWCTRL[3:0] | PWD | SET_PWCTRL[3:0] | PWD |
|---|---|---|---|
| 1000 | -7 | 0111 | 8 |
| 1001 | -6 | 0110 | 7 |
| 1010 | -5 | 0101 | 6 |
| 1011 | -4 | 0100 | 5 |
| 1100 | -3 | 0011 | 4 |
| 1101 | -2 | 0010 | 3 |
| 1110 | -1 | 0001 | 2 |
| 1111 | 0 | 0000 | 1 |

## Table 7. Register Summary

| REGISTER FUNCTION/ ADDRESS | REGISTER NAME | NORMAL MODE | SETUP MODE | BIT NUMBER /TYPE | BIT NAME | DEFAULT VALUE | NOTES |
|---|---|---|---|---|---|---|---|
| Receiver Control Register 1 **Address = H0x00** | RXCTRL1 | R | RW | 1 | RATE_SEL | 0 | Mode-select 0: high-gain mode, 1: high-bandwidth mode |
| Receiver Control Register 2 **Address = H0x01** | RXCTRL2 | R | RW | 6 | LOS_EN | 1 | LOS control 0: disable, 1: enable (always 0 when RX_EN = 0) |
| | | R | RW | 5 | LOS_POL | 1 | LOS polarity 0: inverse, 1: normal |
| | | R | RW | 4 | RX_POL | 1 | Rx polarity 0: inverse, 1: normal |
| | | R | RW | 3 | SQ_EN | 0 | Squelch 0: disable, 1: enable |
| | | R | RW | 2 | RX_EN | 1 | Rx control 0: disable, 1: enable |
| | | R | RW | 1 | RXDE_EN | 0 | Rx deemphasis 0: disable, 1: enable |
| | | R | RW | 0 | AZ_EN | 1 | Rx autozero control 0: disable, 1: enable (always 0 when RX_EN = 0) |
| Receiver Status Register **Address = H0x02** | RXSTAT | R | R | 0 (sticky) | LOS | X | Copy of LOS output signal |
| Output CML Level Setting Register **Address = H0x03** | SET_CML | R | RW | 7 | SET_CML[7] | 0 | MSB output level DAC |
| | | R | RW | 6 | SET_CML[6] | 1 | |
| | | R | RW | 5 | SET_CML[5] | 0 | |
| | | R | RW | 4 | SET_CML[4] | 1 | |
| | | R | RW | 3 | SET_CML[3] | 0 | |
| | | R | RW | 2 | SET_CML[2] | 0 | |
| | | R | RW | 1 | SET_CML[1] | 1 | |
| | | R | RW | 0 | SET_CML[0] | 1 | LSB output level DAC |
| LOS Threshold Level Setting Register **Address = H0x04** | SET_LOS | R | RW | 5 | SET_LOS[5] | 0 | MSB LOS threshold DAC |
| | | R | RW | 4 | SET_LOS[4] | 0 | |
| | | R | RW | 3 | SET_LOS[3] | 1 | |
| | | R | RW | 2 | SET_LOS[2] | 1 | |
| | | R | RW | 1 | SET_LOS[1] | 0 | |
| | | R | RW | 0 | SET_LOS[0] | 0 | LSB LOS threshold DAC |

## Table 7. Register Summary (continued)

| REGISTER FUNCTION/ ADDRESS | REGISTER NAME | NORMAL MODE | SETUP MODE | BIT NUMBER /TYPE | BIT NAME | DEFAULT VALUE | NOTES |
|---|---|---|---|---|---|---|---|
| Transmitter Control Register **Address = H0x05** | TXCTRL | R | RW | 3 | TXDE_EN | 0 | Tx deemphasis 0: disable, 1: enable |
| | | R | RW | 2 | SOFTRES | 0 | Global digital reset |
| | | R | RW | 1 | TX_POL | 1 | Tx polarity 0: inverse, 1: normal |
| | | R | RW | 0 | TX_EN | 1 | Tx control 0: disable, 1: enable |
| Transmitter Status Register 1 **Address = H0x06** | TXSTAT1 | R | R | 7 (sticky) | FST[7] | X | TX_POR → TX_VCC low-limit violation |
| | | R | R | 6 (sticky) | FST[6] | X | BMON open/shorted to $V_{CC}$ |
| | | R | R | 5 (sticky) | X | X | |
| | | R | R | 4 (sticky) | X | X | |
| | | R | R | 3 (sticky) | FST3] | X | $V_{TOUT+/-}$ common-mode low-limit violation |
| | | R | R | 2 (sticky) | FST[2] | X | $V_{TOUT+/-}$ low-limit violation |
| | | R | R | 1 (sticky) | FST[1] | X | BIAS open or shorted to GND |
| | | R | R | 0 (sticky) | TX_FAULT | X | Copy of FAULT signal in case POR bits 6 to 1 reset to 0 |
| Transmitter Status Register 2 **Address = H0x07** | TXSTAT2 | R | R | 3 (sticky) | IMODERR | X | Warning increment result > IMODMAX |
| | | R | R | 2 (sticky) | IBIASERR | X | Warning increment result > IBIASMAX |
| | | R | R | 1 (sticky) | TXED | X | Tx edge detection |
| | | R | R | 0 (sticky) | Unused | X | Unused |
| Bias Current Setting Register **Address = H0x08** | SET_IBIAS | R | RW | 8 | SET_IBIAS[8] | 0 | MSB bias DAC |
| | | R | RW | 7 | SET_IBIAS[7] | 0 | |
| | | R | RW | 6 | SET_IBIAS[6] | 0 | |
| | | R | RW | 5 | SET_IBIAS[5] | 0 | |
| | | R | RW | 4 | SET_IBIAS[4] | 0 | |
| | | R | RW | 3 | SET_IBIAS[3] | 1 | |
| | | R | RW | 2 | SET_IBIAS[2] | 0 | |
| | | R | RW | 1 | SET_IBIAS[1] | 0 | |
| | | Accessible through REG_ADDR = 13 | | 0 | SET_IBIAS[0] | 0 | LSB bias DAC |

**Table 7. Register Summary (continued)**

| REGISTER FUNCTION/ ADDRESS | REGISTER NAME | NORMAL MODE | SETUP MODE | BIT NUMBER /TYPE | BIT NAME | DEFAULT VALUE | NOTES |
|---|---|---|---|---|---|---|---|
| Modulation Current Setting Register **Address = H0x09** | SET_IMOD | R | RW | 8 | SET_IMOD[8] | 0 | MSB modulation DAC |
| | | R | RW | 7 | SET_IMOD[7] | 0 | |
| | | R | RW | 6 | SET_IMOD[6] | 0 | |
| | | R | RW | 5 | SET_IMOD[5] | 1 | |
| | | R | RW | 4 | SET_IMOD[4] | 0 | |
| | | R | RW | 3 | SET_IMOD[3] | 0 | |
| | | R | RW | 2 | SET_IMOD[2] | 1 | |
| | | R | RW | 1 | SET_IMOD[1] | 0 | |
| | | Accessible through REG_ADDR = 12 | | 0 | SET_IMOD[0] | 0 | LSB modulation DAC |
| Maximum Modulation Current Setting Register **Address = H0x0A** | IMODMAX | R | RW | 7 | IMODMAX[7] | 0 | MSB modulation limit |
| | | R | RW | 6 | IMODMAX[6] | 0 | |
| | | R | RW | 5 | IMODMAX[5] | 1 | |
| | | R | RW | 4 | IMODMAX[4] | 1 | |
| | | R | RW | 3 | IMODMAX[3] | 0 | |
| | | R | RW | 2 | IMODMAX[2] | 0 | |
| | | R | RW | 1 | IMODMAX[1] | 0 | |
| | | R | RW | 0 | IMODMAX[0] | 0 | LSB modulation limit |
| Maximum Bias Current Setting Register **Address = H0x0B** | IBIASMAX | R | RW | 7 | IBIASMAX[7] | 0 | MSB bias limit |
| | | R | RW | 6 | IBIASMAX[6] | 0 | |
| | | R | RW | 5 | IBIASMAX[5] | 0 | |
| | | R | RW | 4 | IBIASMAX[4] | 1 | |
| | | R | RW | 3 | IBIASMAX[3] | 0 | |
| | | R | RW | 2 | IBIASMAX[2] | 0 | |
| | | R | RW | 1 | IBIASMAX[1] | 1 | |
| | | R | RW | 0 | IBIASMAX[0] | 0 | LSB bias limit |
| Modulation Current Increment Setting Register **Address = H0x0C** | MODINC | R | R | 7 | SET_IMOD[0] | 0 | LSB of SET_IMOD DAC register address = H0x09 |
| | | R | R | 6 | X | 0 | |
| | | R | R | 5 | DE_INC | 0 | Deemphasis increment 0: no update, 1: SET_TXDE updates ±1 LSB |
| | | RW | RW | 4 | MODINC[4] | 0 | MSB MOD DAC two's complement |
| | | RW | RW | 3 | MODINC[3] | 0 | |
| | | RW | RW | 2 | MODINC[2] | 0 | |
| | | RW | RW | 1 | MODINC[1] | 0 | |
| | | RW | RW | 0 | MODINC[0] | 0 | LSB MOD DAC two's complement |

## Table 7. Register Summary (continued)

| REGISTER FUNCTION/ ADDRESS | REGISTER NAME | NORMAL MODE | SETUP MODE | BIT NUMBER /TYPE | BIT NAME | DEFAULT VALUE | NOTES |
|---|---|---|---|---|---|---|---|
| Bias Current Increment Setting Register **Address = H0x0D** | BIASINC | R | R | 7 | SET_IBIAS[0] | 0 | LSB of SET_IBIAS DAC register address = H0x08 |
| | | R | R | 6 | X | 0 | |
| | | R | R | 5 | X | 0 | |
| | | RW | RW | 4 | BIASINC[4] | 0 | MSB bias DAC two's complement |
| | | RW | RW | 3 | BIASINC[3] | 0 | |
| | | RW | RW | 2 | BIASINC[2] | 0 | |
| | | RW | RW | 1 | BIASINC[1] | 0 | |
| | | RW | RW | 0 | BIASINC[0] | 0 | LSB bias DAC two's complement |
| Mode Control Register **Address = H0x0E** | MODECTRL | RW | RW | 7 | MODECTRL[7] | 0 | MSB mode control |
| | | RW | RW | 6 | MODECTRL[6] | 0 | |
| | | RW | RW | 5 | MODECTRL[5] | 0 | |
| | | RW | RW | 4 | MODECTRL[4] | 0 | |
| | | RW | RW | 3 | MODECTRL[3] | 0 | |
| | | RW | RW | 2 | MODECTRL[2] | 0 | |
| | | RW | RW | 1 | MODECTRL[1] | 0 | |
| | | RW | RW | 0 | MODECTRL[0] | 0 | LSB mode control |
| Transmitter Pulse-Width Control Register **Address = H0x0F** | SET_ PWCTRL | R | RW | 3 | SET_PWCTRL[3] | 0 | MSB Tx pulse-width control |
| | | R | RW | 2 | SET_PWCTRL[2] | 0 | |
| | | R | RW | 1 | SET_PWCTRL[1] | 0 | |
| | | R | RW | 0 | SET_PWCTRL[0] | 0 | LSB Tx pulse-width control |
| Transmitter Deemphasis Control Register **Address = H0x10** | SET_TXDE | R | RW | 3 | SET_TXDE[3] | 0 | MSB Tx deemphasis |
| | | R | RW | 2 | SET_TXDE[2] | 0 | |
| | | R | RW | 1 | SET_TXDE[1] | 0 | |
| | | R | RW | 0 | SET_TXDE[0] | 0 | LSB Tx deemphasis |

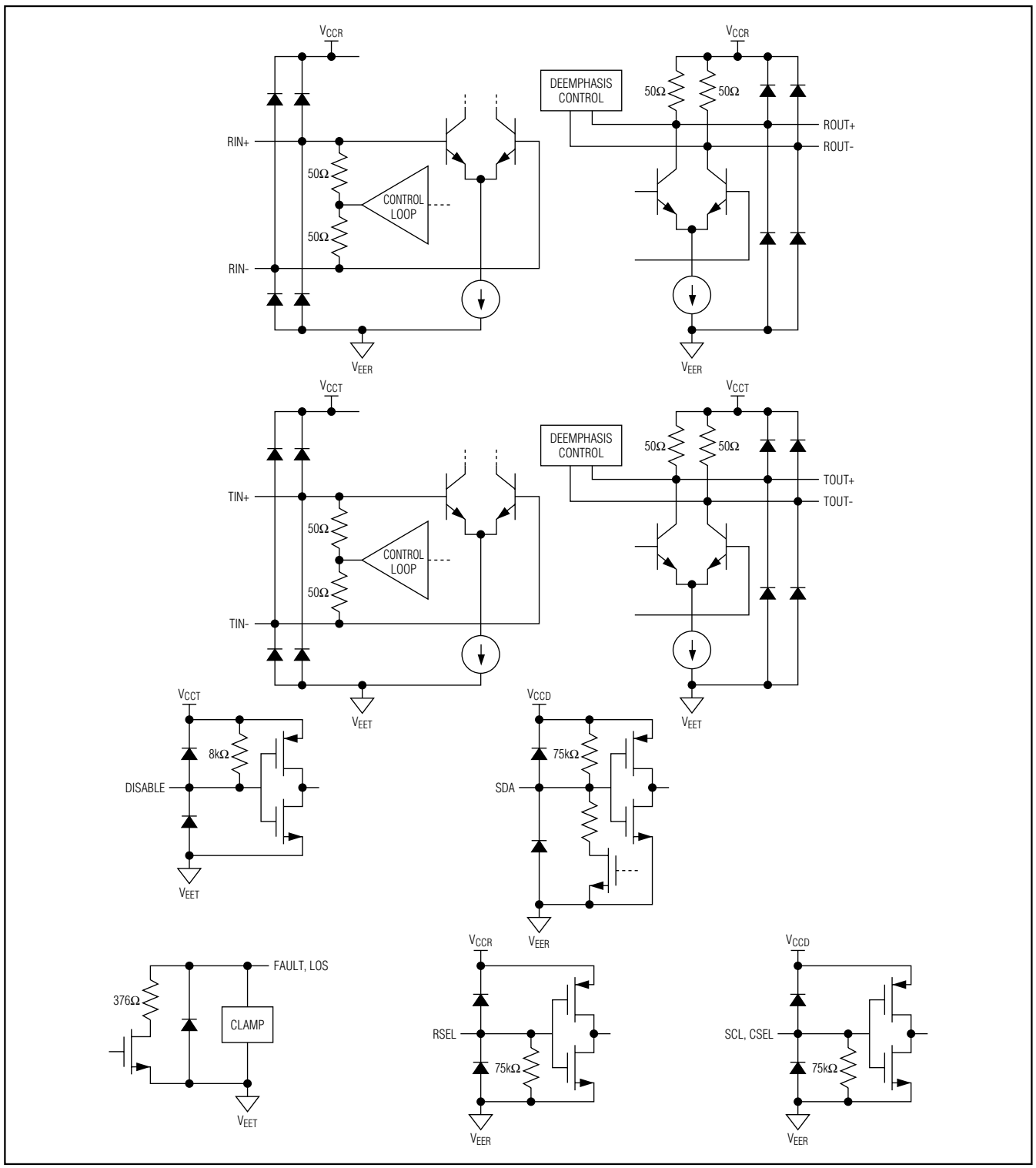
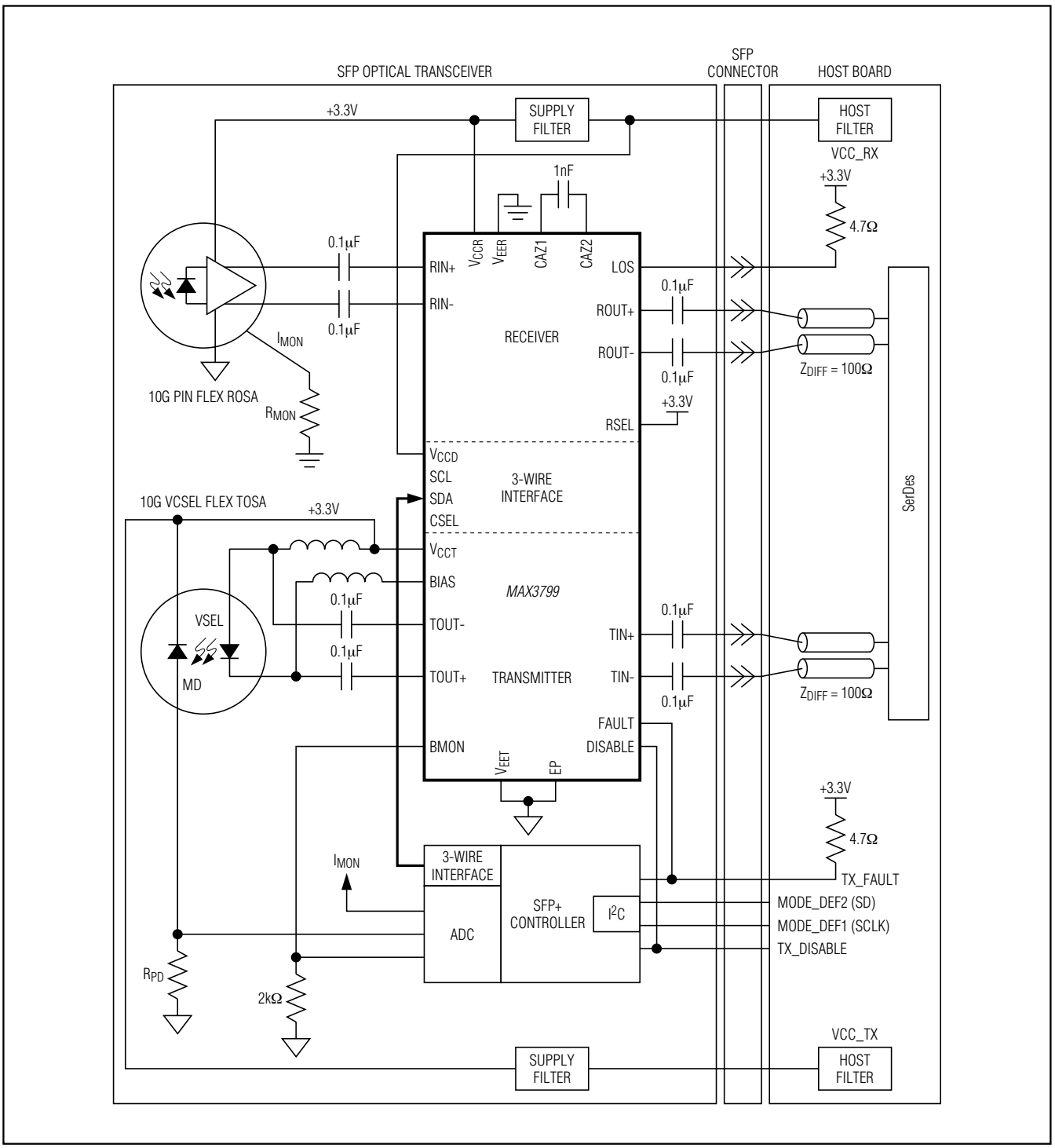


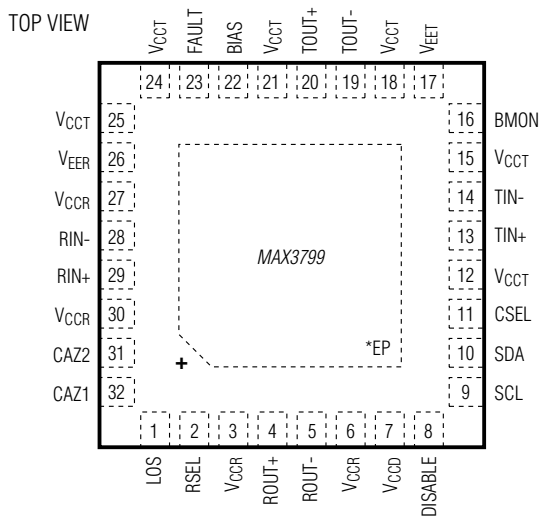

*Figure 5. Simplified I/O Structures*

### Typical Application Circuit



# 1Gbps to 14Gbps, SFP+ Multirate Limiting Amplifier and VCSEL Driver

## Pin Configuration




**THIN QFN**
**(5mm × 5mm)**

*THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

## Chip Information

PROCESS: SiGe BiPOLAR

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 32 TQFN-EP | T3255+5 | 21-0140 | 90-0001 |

# 1Gbps to 14Gbps, SFP+ Multirate Limiting Amplifier and VCSEL Driver

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 8/09 | Initial release | — |
| 1 | 6/10 | Added the dice package and pad configuration to the *Ordering Information* and *Pad Configuration* sections | 1, 35 |
| 2 | 10/12 | Removed references to dice package. | 1, 35 |

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