Click here for production status of specific part numbers.

MAX3523

Low-Power DOCSIS 3.1 Programmable-Gain Amplifier

General Description

The MAX3523 is a programmable gain amplifier (PGA) designed to exceed the DOCSIS 3.1 upstream transmit requirements. The PGA meets the DOCSIS 3.1 spurious limits while transmitting a combined output power of 68dBmV over the RF bandwidth of 5MHz to 204MHz. The gain is controlled in 1dB steps over a 60dB range using an SPI 3-wire interface. The use of Maxim's high-voltage CMOS process enables the device to deliver high dynamic range while minimizing power dissipation under a +5V supply rail.

The MAX3523 is available in a 20-pin 5mm x 5mm x 0.75mm TQFN package, and operates over temperature range of 0ºC to +70ºC.

Applications

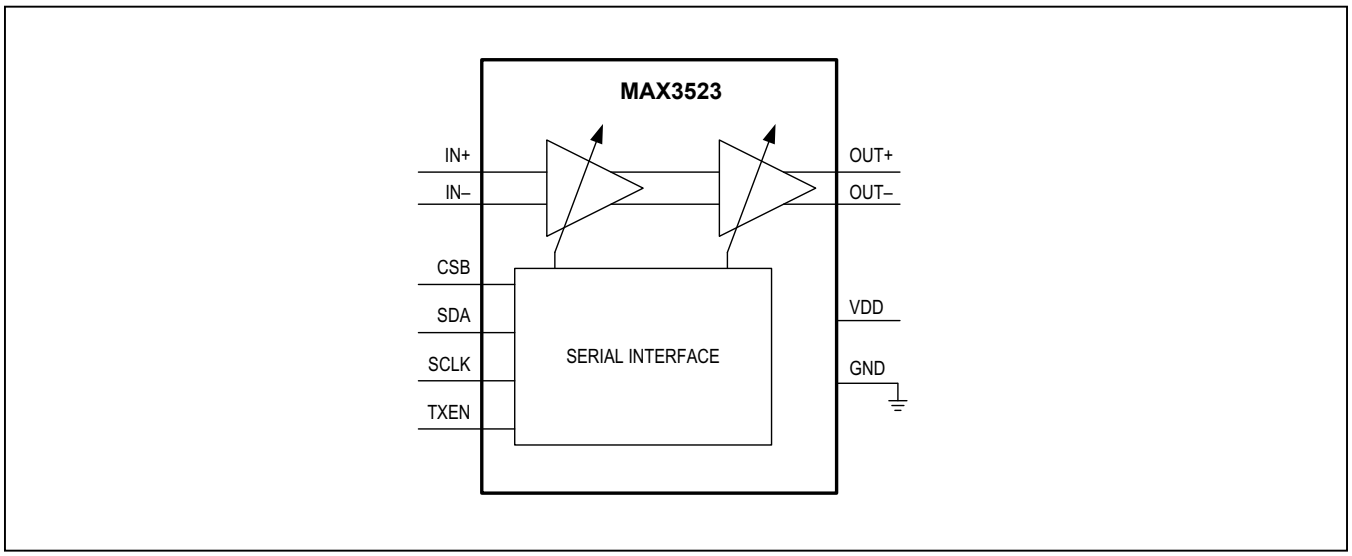
- DOCSIS 3.1 Upstream (D3.1 US)
- Cable Modem (CM)
- Customer Premises Equipment (CPE)

Benefits and Features

- Delivers +68dBmV Output Power While Meeting DOCSIS 3.1 Requirements
- Covers 5MHz–204MHz Output Bandwidth
- 3.5W Power Consumption with 5V Supply Voltage
- Programmable Power Codes Allow Operation at Reduced Power Dissipation
- Exceeds Spurious Requirements with Fully Loaded OFDM Allocation at +65dBmV at Modem Output
- 20L 5mm x 5mm x 0.75mm TQFN Package with Exposed Paddle

Ordering Information *appears at end of data sheet.*

Simplified Block Diagram



19-100360; Rev 0; 6/18

maxim integrated™

Absolute Maximum Ratings

VDD to GND .....-0.3V to +6.0V
TXEN, SDA, SCLK, CSB .....-0.3V to +6.0V
IN+, IN- .....V_{DD} - 2.1V to 6V
OUT+, OUT- to GND .....-0.3V to V_{DD} + 5V
RF Input Power .....+10dBm
Continuous Power Dissipation (T_A = 70°C)
(derate 54mW/°C above T_A = 70°C).....3500mW

Operating Junction Temperature (Note 4)..... -40°C to +150°C
Storage Temperature Range..... -65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20 TQFN-EP

PACKAGE CODE	T2055+5
Outline Number	21-0140
Land Pattern Number	90-0010
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	PCB must be designed for a θ_{JA} of 18.5°C/W or lower
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{DD} = 4.75V to 5.25V, V_{GND} = 0V, Z_{OUT} = 75Ω, TXEN = high, Gain Code = 63, Power code = 3, P_{OUT} = 68dBmV, T_A = 0°C to 70°C, Typical values are at V_{DD} = 5V, T_A = +25°C, unless otherwise noted. *Typical Application Circuit* as shown. Note 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS							
Supply Voltage	V_{DD}			4.75	5.0	5.25	V
Supply Current Transmit Mode	I_{DD}	Gain code = 63, power code = 3			700	730	mA
		Gain code = 63, power code = 2			635		
		Gain code = 63, power code = 1			570		
Supply Current Transmit Disable Mode	I_{DD}	TXEN = low			2.5	3.5	mA
Input High Voltage	V_{INH}			2		V_{DD}	V
Input Low Voltage	V_{INL}					0.7	V
Input High Current	I_{BIASH}				1		µA
Input Low Current	I_{BIASL}				-1		µA
AC ELECTRICAL SPECIFICATIONS							
Voltage Gain	A_V	Z_{IN} = 100Ω (Note 3), Power Code = 3, F_{IN} = 10MHz	Gain code = 63	36.3	37.3	38.3	dB
			Gain code = 53	26.3	27.3	28.3	
			Gain code = 43	16.3	17.3	18.3	
			Gain code = 33	6.3	7.3	8.3	
			Gain code = 23	-3.7	-2.7	-1.7	
			Gain code = 13	-14	-13	-12	
			Gain code = 03		-23		
Voltage Gain Variation with Power Code, Any Gain Code	Δ_{AV}				±0.1		dB
Gain Rolloff		Voltage gain = -16dB to +37dB, f_{IN} = 5MHz to 204MHz			-0.5		dB
Gain Step Size		Voltage gain = -16dB to +37dB, f_{IN} = 10MHz		0.6	1	1.4	dB
Transmit-Disable Mode Noise		BW = 160kHz, 5MHz to 204MHz, TXEN = LOW			-66		dBmV
Isolation in Transmit-Disable Mode		TXEN = LOW			80		dB
Noise Figure	NF	Transmit mode, voltage gain = +11dB to +37dB			14		dB
Noise Figure Slope		Transmit mode, voltage gain = -16dB to +37dB			-1		dB/dB
Transmit-Disable/Transmit-Enable Transient Duration		TXEN input rise/fall time < 0.1µs			4		µs
Transmit-Disable/Transmit-Enable Transient Amplitude		Gain = 37dB			20		mV_{pp}
		Gain = 3dB			1		
Internal Input Impedance		Differential balanced			200		Ω
Output Return Loss	S22	5MHz - 204MHz, TXEN = high (Note 2)			13		dB

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{GND} = 0V, Z_{OUT} = 75Ω, TXEN = high, Gain Code = 63, Power code = 3, P_{OUT} = 68dBmV, T_A = 0°C to 70°C, Typical values are at V_{DD} = 5V, T_A = +25°C, unless otherwise noted. *Typical Application Circuit* as shown. Note 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Return Loss in Transmit-Disable Mode	S22	5MHz - 204MHz, TXEN = low (Note 2)			14		dB
2nd Harmonic Distortion	HD2	f_{IN} = 100MHz, V_{OUT} = +68dBmV			-65		dBc
Two-Tone 2nd-Order Distortion ($f_1 + f_2$)	IM2	f_1 = 100MHz, f_2 = 105MHz, V_{OUT} = +65dBmV/tone			-62		dBc
3rd Harmonic Distortion	HD3	f_{IN} = 65MHz, V_{OUT} = +68dBmV			-60		dBc
Two-Tone 3rd-Order Distortion	IM3	f_1 = 195MHz, f_2 = 200MHz, V_{OUT} = +65dBmV/tone			-55		dBc
Output Compression at Peak Output		f = 100MHz, GC = 63, output power = +79dBmV			0.3		dB
Modulation Error Ratio	MER	4k FFT, 1024QAM, f_{IN} = 150MHz, BW = 96MHz	V_{OUT} = +67dBmV		49		dB
			V_{OUT} = +68dBmV		47		
		4k FFT, 1024QAM, f_{IN} = 192MHz, BW = 24MHz	V_{OUT} = +67dBmV		51		
			V_{OUT} = +68dBmV		46		
CSB to SCLK Rise Setup Time	t_{SENS}				20		ns
CSB to SCLK Rise Hold Time	t_{SENH}				10		ns
SDA to SCLK Setup Time	t_{SDAS}				20		ns
SDA to SCLK Hold Time	t_{SDAH}				10		ns
SCLK Pulse-Width High	t_{SCLKH}				50		ns
SCLK Pulse-Width Low	t_{SCLKL}				50		ns
Maximum SCLK Frequency	f_{SCLK}				20		MHz

Note 1: Limits are tested at T_A = +70°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Output return loss is measured with the LC matching network, as shown in the Typical Application Circuit.

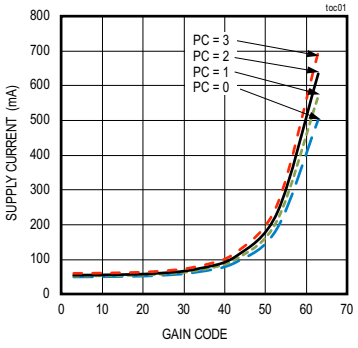
Note 3: Effective input impedance with external 200Ω resistance in parallel with internal 200Ω resistance

Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours plus T_J = +150°C for 5,000 hours.

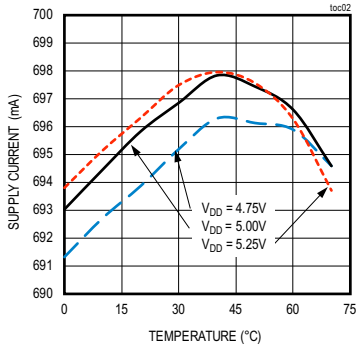
Typical Operating Characteristics

(T_A = 25°C, P_{OUT} = 68dBmV, TXEN = high, Gain Code = 63, Power Code = 3, V_{DD} = 5V, unless otherwise noted.)

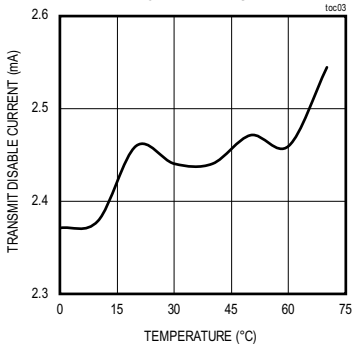
SUPPLY CURRENT vs. GAIN CODE



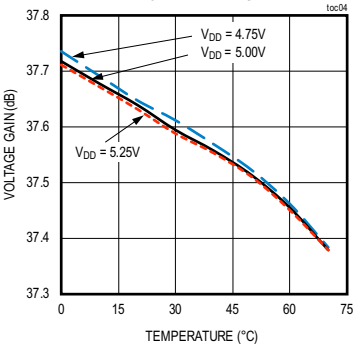
SUPPLY CURRENT vs. TEMPERATURE



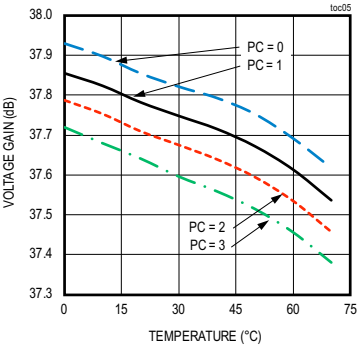
TRANSMIT DISABLE CURRENT vs. TEMPERATURE



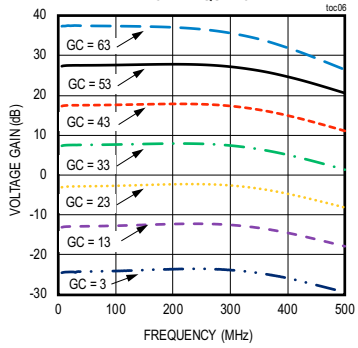
VOLTAGE GAIN vs. TEMPERATURE



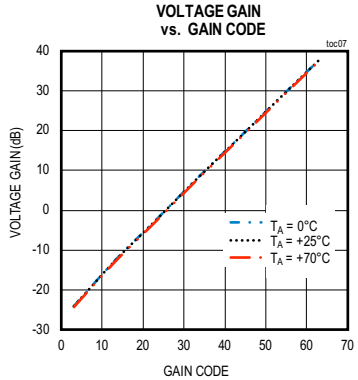
VOLTAGE GAIN vs. TEMPERATURE



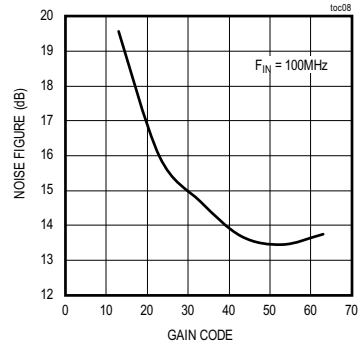
VOLTAGE GAIN vs. FREQUENCY



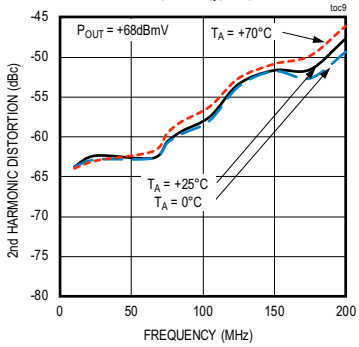
VOLTAGE GAIN vs. GAIN CODE



NOISE FIGURE vs. GAIN CODE



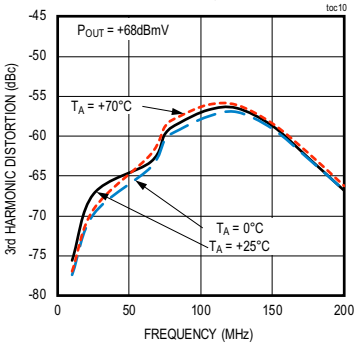
2nd HARMONIC DISTORTION vs. FREQUENCY



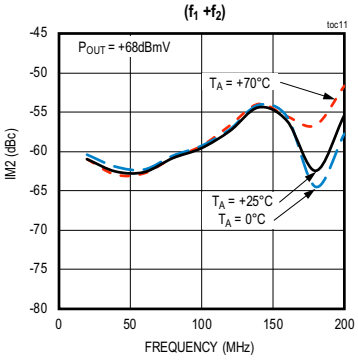
Typical Operating Characteristics (continued)

(T_A = 25°C, P_{OUT} = 68dBmV, TXEN = high, Gain Code = 63, Power Code = 3, V_{DD} = 5V, unless otherwise noted.)

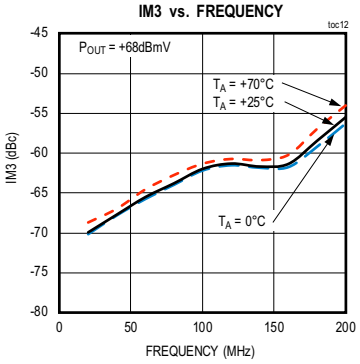
3rd HARMONIC DISTORTION vs. FREQUENCY



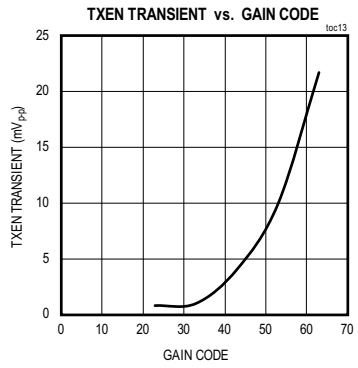
IM2 vs. FREQUENCY (f_1 +f_2)



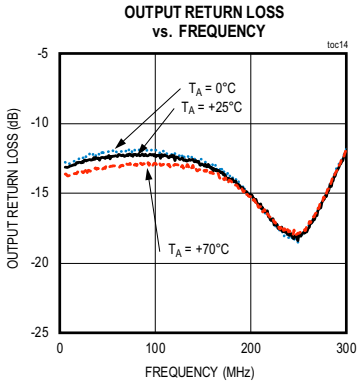
IM3 vs. FREQUENCY



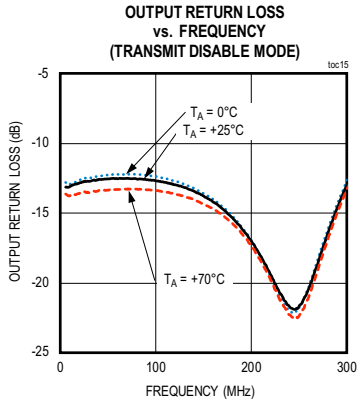
TXEN TRANSIENT vs. GAIN CODE



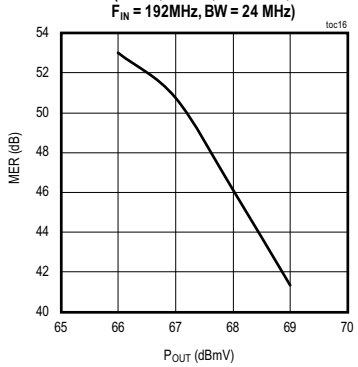
OUTPUT RETURN LOSS vs. FREQUENCY



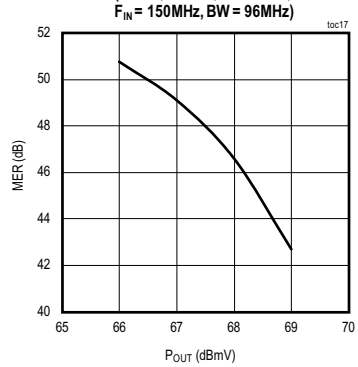
OUTPUT RETURN LOSS vs. FREQUENCY (TRANSMIT DISABLE MODE)



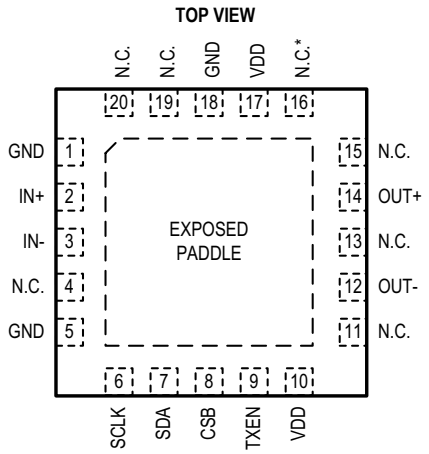
MER vs. P_{OUT} (OFDM, 4k FFT, 1024 QAM, F_{IN} = 192MHz, BW = 24 MHz)



MER vs. P_{OUT} (OFDM, 4k FFT, 1024 QAM, F_{IN} = 150MHz, BW = 96MHz)



Pin Configuration



NOTES:
1. CONNECT N.C. PINS TO PCB GND FOR IMPROVED HEAT DISSIPATION.
2. N.C.* PIN MUST BE LEFT UNCONNECTED.

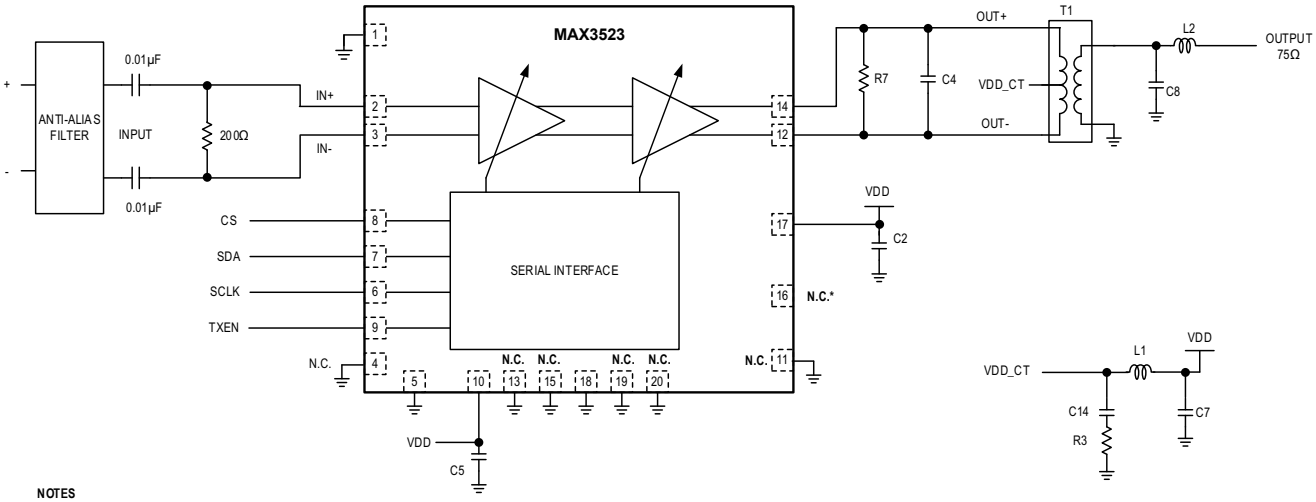
Pin Description

PIN	NAME	FUNCTION
10, 17	VDD	+5V Supply. Connect a 0.1µF capacitor to GND.
2	IN+	Positive Input
3	IN-	Negative Input
8	CSB	Chip Select. Active-low.
7	SDA	Serial Data
6	SCLK	Clock
9	TXEN	Transmit Enable/Disable
4, 11, 13, 15, 19, 20	N.C.	Connect to PCB GND for Improved Heat Dissipation
12	OUT-	PA Negative Output
14	OUT+	PA Positive Output
1, 5, 18	GND	Ground
16	N.C.*	Leave Open
Paddle	GND	Ground

Recommended Operating Conditions

PARAMETER	CONDITIONS
Ambient Temperature Range	0°C to +70°C

Typical Application Circuit



NOTES
1. N.C. PINS TO BE LEFT OPEN OR CONNECTED TO PCB GROUND FOR IMPROVED HEAT DISSIPATION.
2. N.C.* PINS MUST BE LEFT UNCONNECTED.
3. FOR COMPONENT VALUES, PLEASE REFER TO THE MAX3523 EV KIT DATA SHEET.

Detailed Description

Programmable-Gain Amplifier

The programmable-gain amplifier (PGA) provides 60dB of output level control in 1dB steps. The gain of the PGA is determined by a 6-bit gain code (GC5–GC0) programmed through the serial-data interface (see *Register Map*). Specified performance is achieved when the input is driven differentially.

Four power codes (PC1–PC0) allow the PGA to be used with reduced bias current when distortion performance can be relaxed. In addition, for each power code, bias current is automatically reduced with gain code for maximum efficiency.

The PGA features a differential Class A output stage capable of driving an +68dBmV OFDMA signal from 5MHz–85MHz or two 96MHz +65dBmV OFDMA signals from 5MHz–204MHz into a 75Ω load. This architecture features a differential output that provides superior even-order distortion performance. This requires that a transformer be used to convert to a single-ended output. In transmit-disable mode, the output amplifiers are powered down, resulting in low output noise while maintaining the impedance match.

3-Wire Serial Programmable Interface (SPI) and Control Registers

The MAX3523 includes a user-programmable register for initializing the part and setting the gain and power consumption. The four MSBs are address bits; the eight least significant bits (LSBs) are used for register data. Data is shifted MSB first.

The serial interface should only be written to when TXEN = low, as is the case between transmit bursts in a DOCSIS environment. Once a new set of register data is clocked in, the corresponding power code and/or gain code does not take effect until the 12th rising edge of SCLK.

Note: *The registers must be written no earlier than 100µs after the device is powered up.*

SPI Read

Figure 1 shows a single-byte read transaction. In this example, a single byte is read from the slave by the master. The master first asserts CSB, begins driving SDA with the R/Wb bit having value of 1 indicating this a read transaction and starts toggling SCLK. The slave samples the bits on SDA on the rising edge of SCLK. After the R/Wb bit, the master outputs the 3-bit register addresses starting with the most significant bit following which the master releases the SDA line. The slave then starts driving SDA and outputs the single byte that was requested by the master. After the last bit has been output, the slave three-states SDA on the rising edge of CSB that ends the transaction.

SPI Write

Figure 2 shows a single-byte write transaction. In this example, a single byte is written to the slave by the master. The master first asserts CSB, begins driving SDA with the R/Wb bit having value of 0 indicating this a write transaction and starts toggling SCLK. The slave samples the bits on SDA on the rising edge of SCLK. After the R/Wb bit, the master outputs the 3-bit register addresses starting with the most significant bit and then the 8-bit data starting with the most significant bit. The internal registers are updated on the 12th rising edge of SCLK.

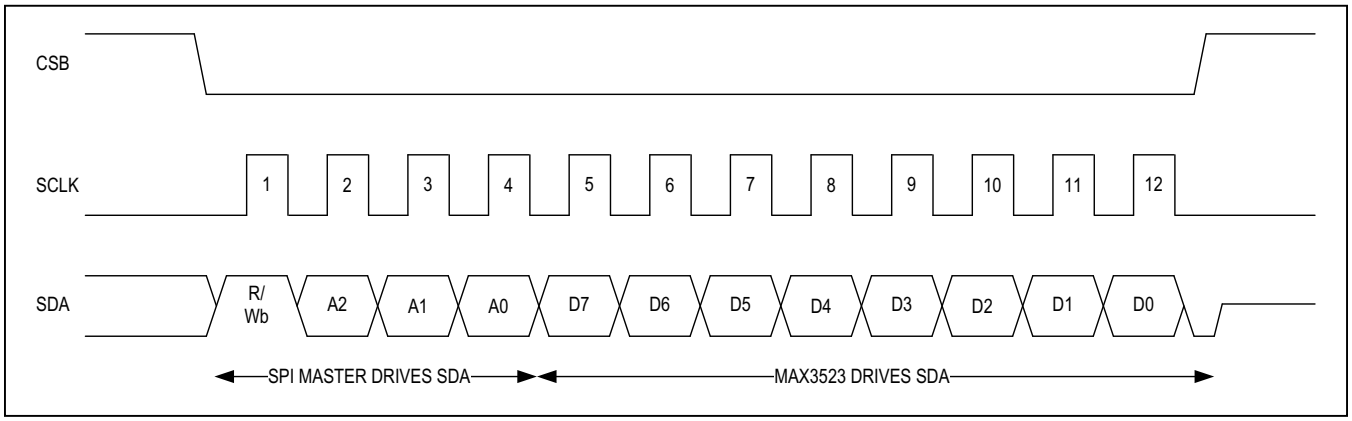


Figure 1. SPI Read Transaction

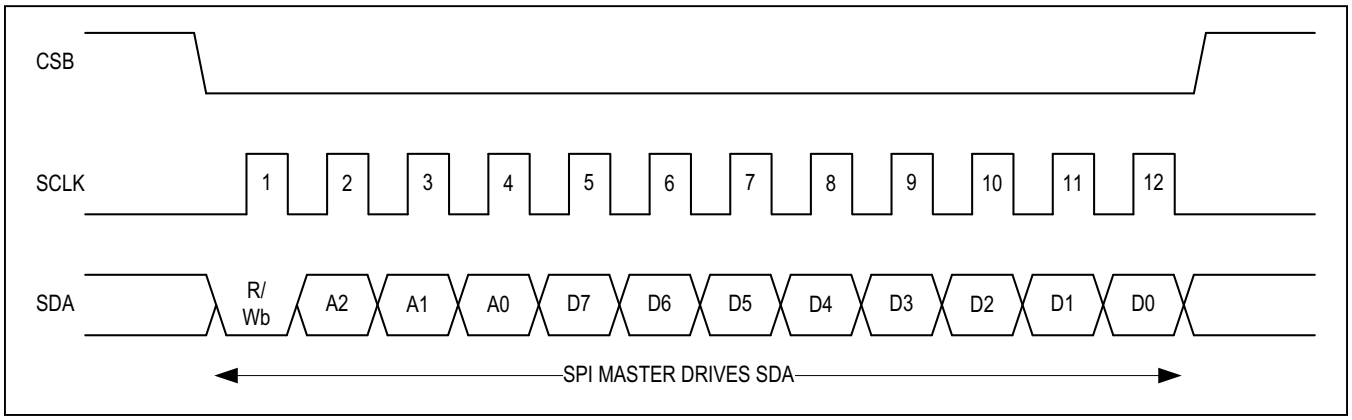


Figure 2. SPI Write Transaction

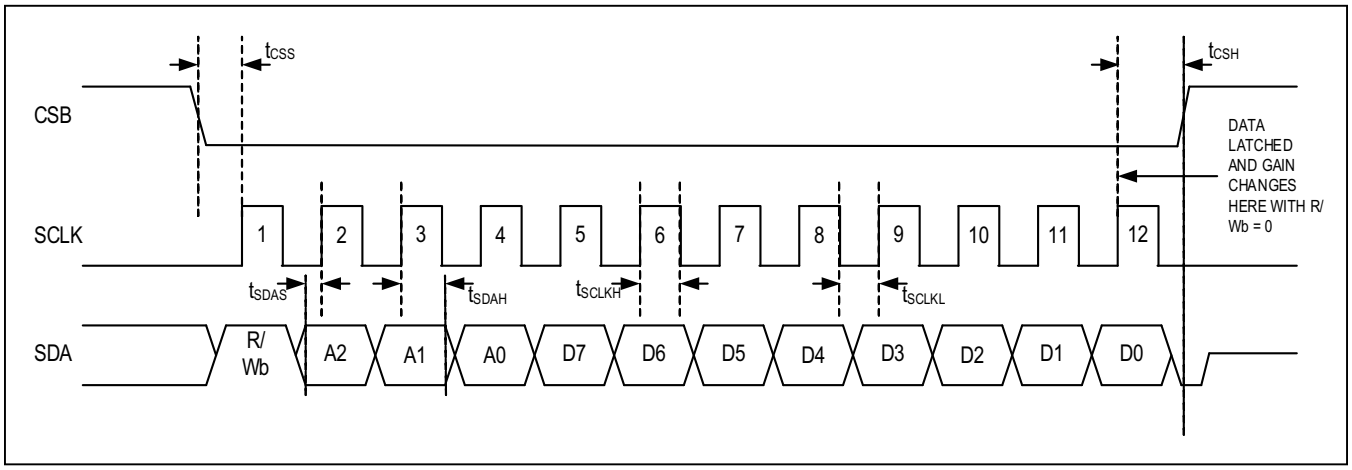


Figure 3. SPI Timing Diagram

Register Map

ADDRESS	NAME	MSB							LSB
MAIN									
0x00	GAIN[7:0]	PC[1:0]		GC[5:0]					

Register Details

GAIN (0x0)

BIT	7	6	5	4	3	2	1	0
Field	PC[1:0]		GC[5:0]					
Reset	0x0		0x0					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PC	7:6	Power Code	0x0: MIN POWER 0x3: MAX POWER
GC	5:0	Gain Code	0x0: MIN GAIN 0x3F: MAX GAIN

Applications Information

Power Codes

The device is designed to exceed the stringent linearity requirements of DOCSIS 3.1 using power code (PC 3). Using lower power codes (PC = 2, 1 or 0) allows for operation at reduced current levels. The full range of gain codes can be used in any power code. The gain difference between power codes is typically less than 0.1dB.

Transmit Disable Mode

Between bursts in a DOCSIS system, the MAX3523 can be put in transmit-disable mode by setting TXEN low. The output transient on the cable is kept well below the DOCSIS 3.1 requirement during the TXEN transitions.

If a gain code or power code change is required, the new values of PC and GC should be clocked in during transmit-disable mode (TXEN low). The new operating point of the MAX3523 is set on the 12th rising edge of SCLK. This should be done between transmission bursts.

Output Circuit

The output circuit is an open-drain differential amplifier. The outputs should be resistively terminated, as shown in the Typical Application Circuit. A 50:75 impedance ratio transformer should be used as the interface between the differential output of the device and the unbalanced 75Ω load.

Amplifier performance depends on the value of the termination resistors. Rated performance is obtained using the R7 termination resistor as shown in the Typical Application Circuit. Increasing the value of this resistor will increase gain and improve SNR at the expense of output return loss.

Transformer core inductance may vary with temperature. Adequate primary inductance must be present to sustain broadband output capability as temperatures vary.

Input Circuit

The differential input impedance of the MAX3523 is 200Ω. In a typical application, however, it is driven from a 100Ω differential source, requiring an external 200Ω matching resistor, as shown in the Typical Application Circuit.

The device has sufficient gain and linearity to produce an output level of +68dBmV when driven with a +31dBmV input signal. If an input level greater than +31dBmV is used, the 3rd-order distortion performance degrades.

Layout Issues

A well-designed printed circuit board (PCB) is an essential part of an RF circuit. For best performance, pay attention to power-supply layout issues as well as the output circuit layout. The MAX3523 evaluation (EV) board layout can be utilized as a guide during PCB design. Its electrical performance has been thoroughly tested, making it an excellent reference. Refer to the MAX3523 EV kit for additional information.

Output Circuit Layout

Keep the length of the output traces as short as possible. Series inductance between the part and the transformer will degrade the performance at the higher end of the operating frequency range. To maintain the balance of the output network, match the length of the differential traces as closely as possible.

Power-Supply Layout

For minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the circuit. At the end of each of these traces is a decoupling capacitor that provides a very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin. The power-supply traces must be capable of carrying the maximum current without significant voltage drop.

Exposed Pad Thermal Considerations

The exposed pad (EP) of the MAX3523's 20-pin TQFN package provides a low thermal resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from this contact. In addition, the EP should be provided with a low-inductance path to electrical ground. The MAX3523 EV board is an example of a layout that provides optimal thermal and electrical performance.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX3523ETP+	0°C to +70°C	20 TQFN-EP*
MAX3523ETP+T	0°C to +70°C	20 TQFN-EP*

** EP = Exposed pad.*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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