Click here for production status of specific part numbers.

MAX2771

Multiband Universal GNSS Receiver

General Description

The MAX2771 is a next-generation Global Navigation Satellite System (GNSS) receiver covering E5/L5, L2, E6, E1/L1 bands and GPS, GLONASS, Galileo, QZSS, IRNSS, and BeiDou navigation satellite systems on a single chip.

Designed on Maxim's advanced, low-power SiGe BiCMOS process technology, the MAX2771 offers the highest performance and integration at a low cost. Incorporated on the chip is the complete receiver chain, including a dual-input LNA and mixer, followed by filter, PGA, and multi-bit ADC, along with a fractional-N frequency synthesizer, and crystal oscillator. The total cascaded noise figure of this receiver is as low as 1.4dB.

The MAX2771 completely eliminates the need for external IF filters by implementing on-chip monolithic filters and requires only a few external components to form a complete, low-cost GNSS RF receiver solution.

The MAX2771 is the most flexible receiver on the market. The integrated delta-sigma fractional-N frequency synthesizer allows programming of the IF frequency within a ±30Hz (f_{XTAL} = 32MHz) accuracy while operating with any reference or crystal frequencies that are available in the host system. The ADC outputs CMOS logic levels with one or two quantized bits for both I and Q channels, or up to 3 quantized bits for the I channel. The on-chip ADCs can be bypassed and the analog I and Q signals output for sampling with external ADCs. An analog monitoring feature is provided that allows simultaneous output of the on-chip ADC samples and the I analog signal.

The MAX2771 is packaged in a 5mm x 5mm, 28-pin, TQFN package with an exposed paddle.

Applications

- Location-Enabled Mobile Handsets
- PNDs (Personal Navigation Devices)
- Telematics (Asset Tracking, Inventory Management)
- Marine/Avionics Navigation
- Software GPS
- Laptops and Netbooks
- Surveying Equipment
- Digital Still Cameras and Camcorders
- Vehicle Tracking and Fleet Management

Benefits and Features

- Multi-Constellation Support
  - GPS, Galileo, GLONASS, BeiDou, IRNSS, QZSS, SBAS
- Multiband Support
  - L1, L2, L5, E1, E5, E6, B1, B2, B3
- Programmable IF Bandwidths of 2.5MHz, 4.2MHz, 8.7MHz, 16.4MHz, 23.4MHz, 36MHz
  - Supports Wide-Band Carriers for Precision Applications (e.g., GPS L5, Galileo E5)
- Operates in Low IF or Zero IF Mode
  - Programmable IF Center Frequency
- Fractional-N Synthesizer with Integrated VCO Supports Wide Range of Reference Frequencies
- On-Chip LNAs to Support Multiple Bands
- 1.4dB Cascaded Noise Figure and 110dB of Cascaded Gain with Gain Control Range of 59dB from PGA
- Integrated Crystal Oscillator
- Supply Voltage Range: 2.7V to 3.3V
- 28-Pin, RoHS-Compliant, Thin QFN Lead-Free Package (5mm x 5mm)

Ordering Information *appears at end of data sheet.*

19-100378; Rev 0; 7/18

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Block Diagram

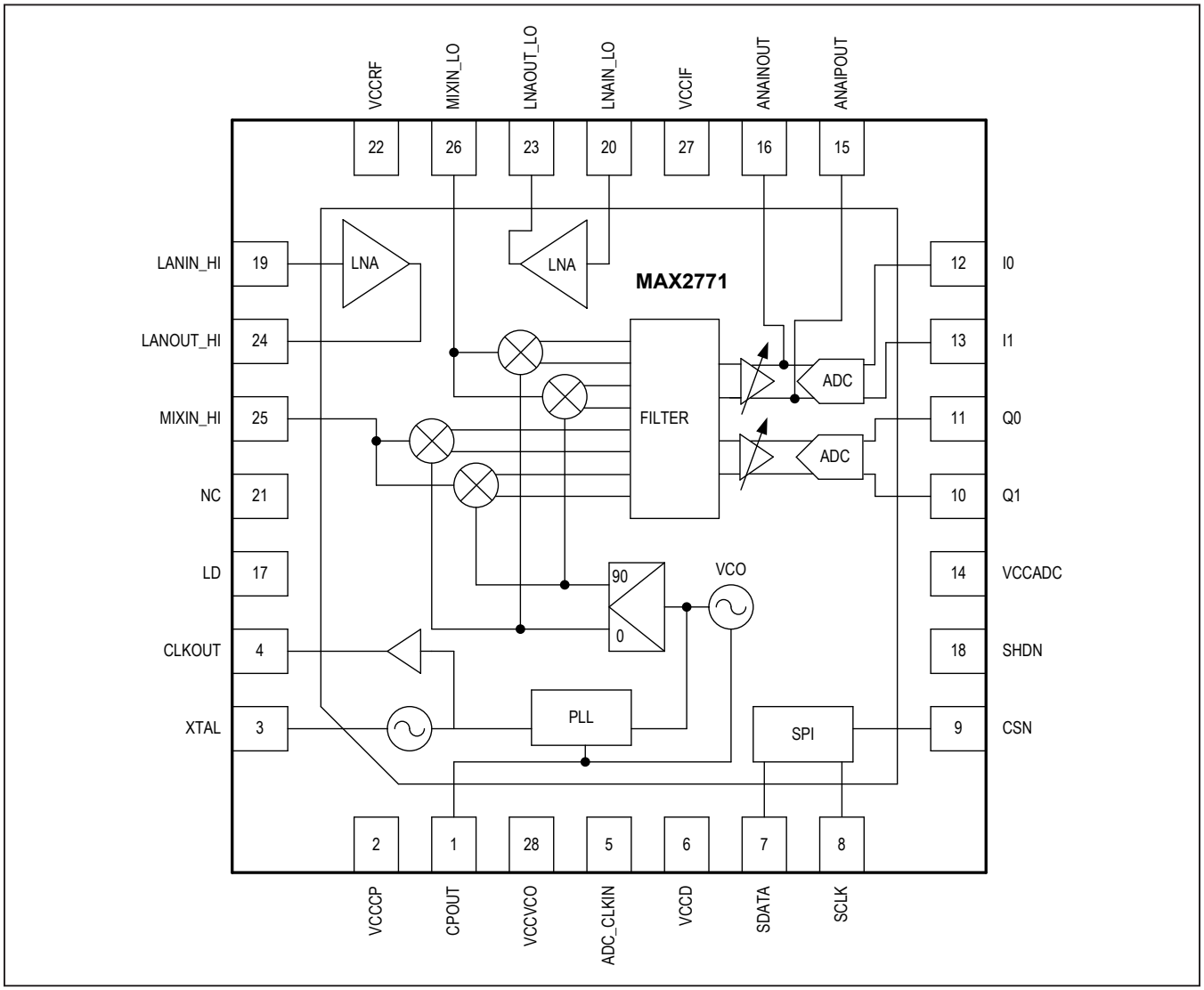


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Absolute Maximum Ratings

VCC to GND .....-0.3V to +4.2V
MIXIN_ to GND .....-0.3V to +0.3V
Other Pins to GND (Note 1) .....-0.3V to V_{CC} + 0.3V
Maximum RF Input Power.....+15dBm
Continuous Power Dissipation
(T_A = +70°C, derate 27 mW/°C above +70°C.) 2500mW

Operating Temperature Range.....-40°C to 85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (Soldering, 10 seconds).....+300°C

Note 1: Except for LNAIN_HI, LNAIN_LO, MIXIN_HI, MIXIN_LO, XTAL, LNAOUT_HI and LNAOUT_LO

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 TQFN-EP

Package Code	T2855+8
Outline Number	**21-0140**
Land Pattern Number	**90-0023**

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the specified default states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 through SPI interface, unless otherwise noted. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Supply Voltage	VCC		2.7	2.85	3.3	V
Supply Current		Default mode, high-band LNA and mixer input is active (Note 2)		26		mA
		Default mode, low-band LNA and mixer input is active (Note 2)		27		
		Idle Mode™, IDLE bit is 1, $\overline{SHDN}$ = high		5		
		Shutdown mode, $\overline{SHDN}$= low		200		µA
Digital Input Logic-High	V_{IH}	Measure at the $\overline{SHDN}$ pin	1.5			V
Digital Input Logic-Low	V_{IL}	Measure at $\overline{SHDN}$ pin			0.4	V

Idle Mode is a trademark of Maxim Integrated Products, Inc.

Electrical Characteristics (continued)

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the specified default states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 through SPI interface, unless otherwise noted. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS/ASCADED RF PERFORMANCE						
RF Frequency		L1 band		1575.42		MHz
RF Frequency - L2/L5 Band		L2/L5 band		1227.6		MHz
Noise Figure		High band LNA input active, default mode (Note 3)		1.4		dB
Noise Figure - L2/L5 Band		L2/L5 band (Note 6). Low-band LNA input active, default mode (Note 3)		1.6		dB
Noise Figure		Measured at the high-band mixer input		10.3		dB
Noise Figure - L2/L5 Band		L2/L5 band (Note 6). Measured at the low-band mixer input		10.3		dB
Out-of-Band 3rd-Order Input Intercept Point		Measured at the high-band mixer input (Note 4)		-9		dBm
Out-of-Band 3rd-Order Input Intercept Point - L2/L5 Band		L2/L5 band (Note 6). Measured at the low-band mixer input (Note 4)		-9		dBm
In-Band Mixer Input Referred 1dB Compression Point		Measured at the high-band mixer input		-85		dBm
In-Band Mixer Input Referred 1dB Compression Point – L2/L5 Band		L2/L5 band (Note 6). Measured at the low-band mixer input		-85		dBm
Mixer Input Return Loss		Measured at high-band mixer input		10		dB
Mixer Input Return Loss - L2/L5 Band		Measured at low-band mixer input		8		dB
Image Rejection				25		dB
Image Rejection - L2/L5 Band		L2/L5 band (Note 6)		25		dB
Spurs at High-Band LNA Input		LO leakage		-101		dBm
Spurs at Low-Band LNA Input		L2/L5 band (Note 6). LO leakage		-101		dBm
Spurs at High-Band LNA Input		Reference harmonics leakage		-103		dBm
Spurs at Low-Band LNA Input		L2/L5 band (Note 6). Reference harmonics leakage		-103		dBm
Maximum Voltage Gain		Measured from the high-band mixer input to the baseband analog output	89	96	104	dB
Maximum Voltage Gain - L2/L5 Band		L2/L5 band (Note 6). Measured from the low-band mixer input to the baseband analog output	89	96	104	dB
Variable Gain Range		Measured at high-band mixer input	53	59		dB

Electrical Characteristics (continued)

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the specified default states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 through SPI interface, unless otherwise noted. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS/FILTER RESPONSE						
Passband Center Frequency		FBW = 000, FCEN = 1011000 (Note 7)		3.9		MHz
		FBW = 010, FCEN = 1011000 (Note 7)		7.1		
		FBW = 001, FCEN = 1101001 (Note 7)		7.6		
Passband 3dB Bandwidth		FBW = 000 (Note 7)		2.5		MHz
		FBW = 010 (Note 7)		4.2		
		FBW = 001 (Note 7)		8.7		
Lowpass 3dB Bandwidth		FBW = 011, single-sided BW (Note 7)		11.7		MHz
		FBW = 111, single-sided BW (Note 7)		8.2		
		FBW = 100, single-sided BW (Note 7)		18		
Stopband Attenuation		3rd-order filter, bandwidth = 2.5MHz, measured at 4MHz offset (Note 7)		30		dB
		5th-order filter, bandwidth = 2.5MHz, measured at 4MHz offset (Note 7)		50		
Passband Flatness		FBW = 001, Filter center frequency = 8.9MHz, 5th-order BPF, |response magnitude at 5.1MHz - response magnitude at 11.6MHz| (Note 7)		3		dB
AC ELECTRICAL CHARACTERISTICS/HIGH-BAND LNA						
Power Gain				18		dB
Noise Figure				0.9		dB
Input IP3		(Note 5)		-1.1		dBm
Output Return Loss				10		dB
Input Return Loss		With external matching circuit components of 5.6nH series inductor and 1.7pF shunt capacitor.		10		dB
AC ELECTRICAL CHARACTERISTICS/LOW-BAND LNA						
Power Gain				18		dB
Noise Figure				0.9		dB
Input IP3		(Note 5)		-1.1		dBm
Output Return Loss				10		dB
Input Return Loss		With external matching circuit components of 8.4nH series inductor and 1.1pF shunt capacitor.		8		dB

Electrical Characteristics (continued)

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the specified default states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 through SPI interface, unless otherwise noted. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS/FREQUENCY SYNTHESIZER						
LO Frequency Range		0.2V < V_{TUNE} < (V_{CC} - 0.25V), LOBAND = 0	1525		1610	MHz
LO Frequency Range—L2/L5 Band		0.2V < V_{TUNE} < (V_{CC} - 0.25V), LOBAND = 1	1160		1290	MHz
LO Tuning Gain				70		MHz/V
LO Tuning Gain - L2/L5 Band				76		MHz/V
Reference Input Frequency			8		44	MHz
Main Divider Ratio			36		32,767	—
Reference Divider Ratio			1		1023	—
Charge-Pump Current		ICP = 0		0.5		mA
		ICP = 1		1		
AC ELECTRICAL CHARACTERISTICS/TXCO INPUT BUFFER/OUTPUT CLOCK BUFFER						
Frequency Range		Load = 10kΩ||10pF	8		44	MHz
Output High Level		With respect to ground, I_{OH} = 10µA (DC-coupled)	2			V
Output Low Level		With respect to ground, I_{OL} = 10µA (DC-coupled)			0.8	V
Capacitive Slew Current		Load = 10KΩ||10pF, f_{CLKOUT} = 44MHz		11		mA
Output Load					10||10	KΩ||pF
Reference Input Level		Sine wave	0.5			V_{P-P}
Clock Output Multiply/Divide Range		x2: max input frequency of 22MHz, x4: max input frequency of 11MHz	/4		x4	—
AC ELECTRICAL CHARACTERISTICS/ADC						
ADC Differential Nonlinearity		AGC enabled, 3-bit output		±0.1		LSB
ADC Integral Nonlinearity		AGC enabled, 3-bit output		±0.1		LSB

Note 1: MAX2771 is production tested at T_A = 25ºC. User must program the registers to the specified default settings upon power-up.

Note 2: Default mode of the IC. PLL is an an integer-N mode with $f_{COMP} = f_{TCXO}/16$ = 1.023MHz and I_{CP} = 0.5mA. The complex IF filter is configured as a 5th-order Butterworth filter with a center frequency of 4MHz and bandwidth of 2.5MHz. Output data is in a 2-bit sign/magnitude format at CMOS logic levels in the I channel only.

Note 3: The LNA output connects to the mixer input without a SAW filter between them.

Note 4: Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz or 1227.6MHz depending on band. Passive pole at the mixer output is programmed to be 13MHz.

Note 5: Measured from the LNA input to the LNA output. Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz or 1227.6MHz depending on band.

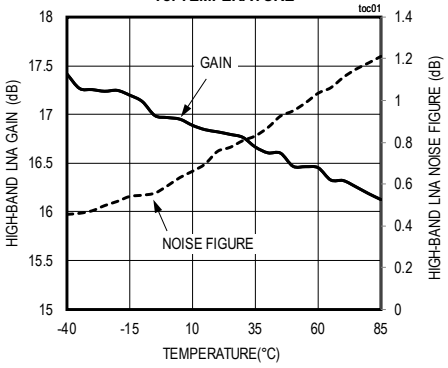
Note 6: Same global conditions except tune LO to 1223.508 MHz which means change PLL integer divider ratio to 1196 and program LOBAND bit to 1.

Note 7: Filter response measured with PGA gain setting of GAININ = 000100, and mixer pole set to 36 MHz (MIXPOLE = 1).

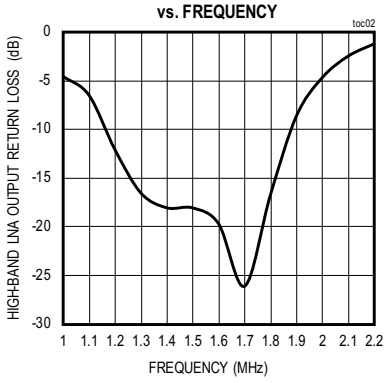
Typical Operating Characteristics

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. LNA input has specified external matching circuit. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 except for IF filter response plots in which case it is set to GAININ = 000100. For IF filter response plots, MIXPOLE = 1. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

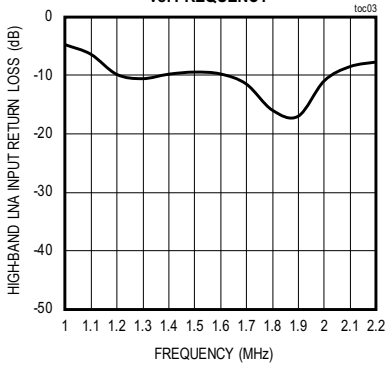
HIGH-BAND LNA GAIN AND NOISE FIGURE vs. TEMPERATURE



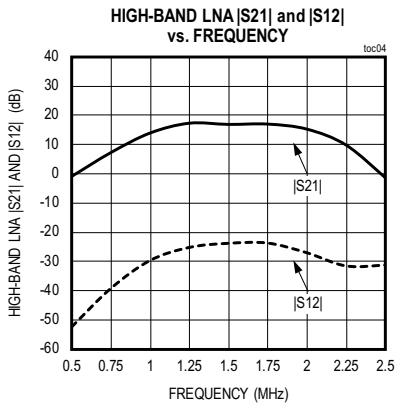
HIGH-BAND LNA OUTPUT RETURN LOSS vs. FREQUENCY



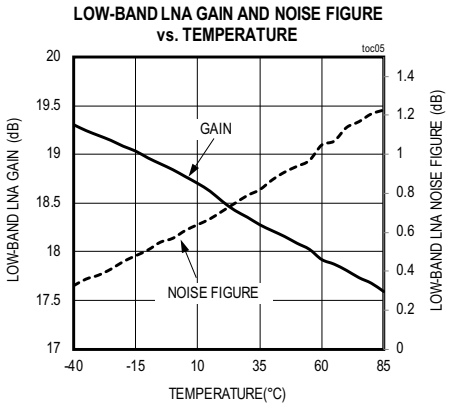
HIGH-BAND LNA INPUT RETURN LOSS vs. FREQUENCY



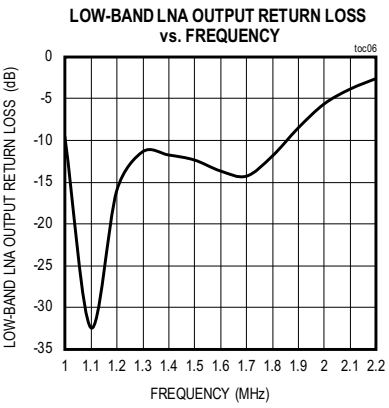
HIGH-BAND LNA |S21| and |S12| vs. FREQUENCY



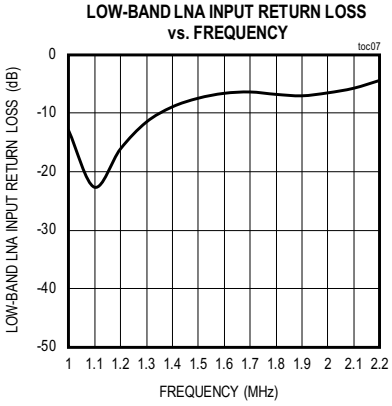
LOW-BAND LNA GAIN AND NOISE FIGURE vs. TEMPERATURE



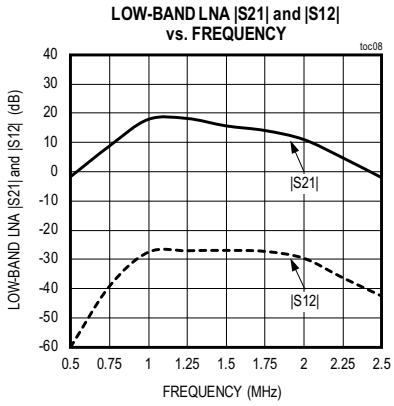
LOW-BAND LNA OUTPUT RETURN LOSS vs. FREQUENCY



LOW-BAND LNA INPUT RETURN LOSS vs. FREQUENCY



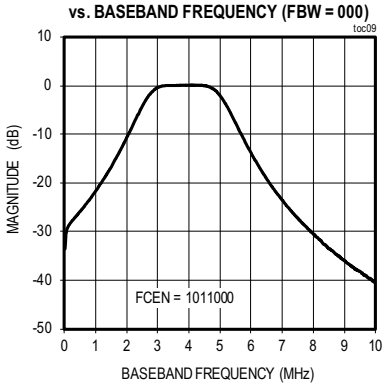
LOW-BAND LNA |S21| and |S12| vs. FREQUENCY



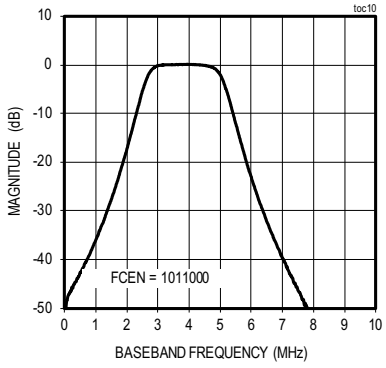
Typical Operating Characteristics (continued)

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. LNA input has specified external matching circuit. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 except for IF filter response plots in which case it is set to GAININ = 000100. For IF filter response plots, MIXPOLE = 1. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

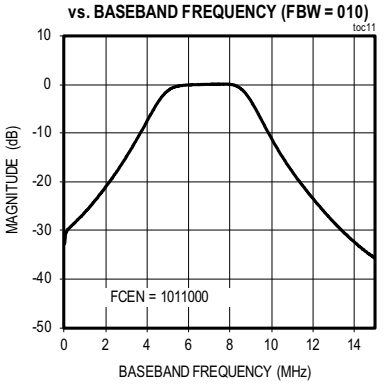
3RD-ORDER POLYPHASE FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 000)



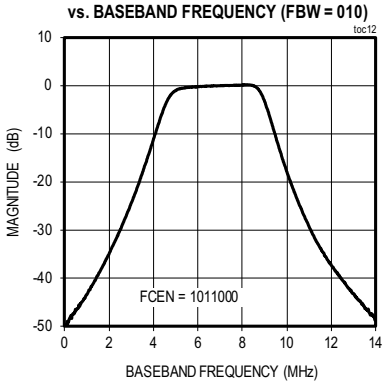
5TH-ORDER POLYPHASE FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 000)



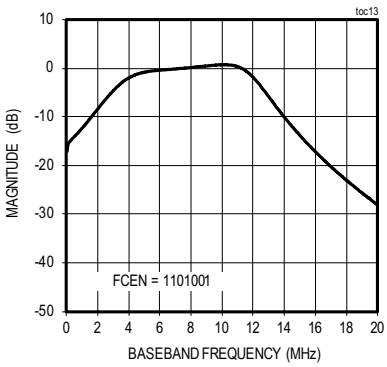
3RD-ORDER POLYPHASE FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 010)



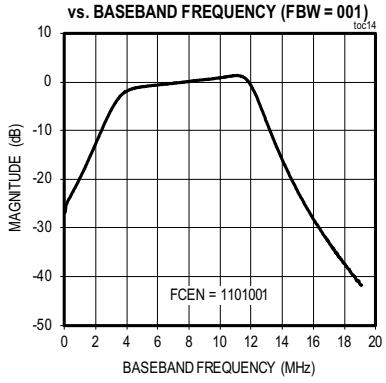
5TH-ORDER POLYPHASE FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 010)



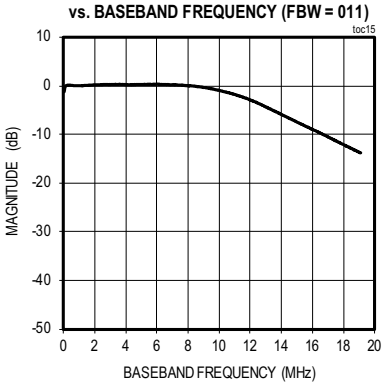
3RD-ORDER POLYPHASE FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 001)



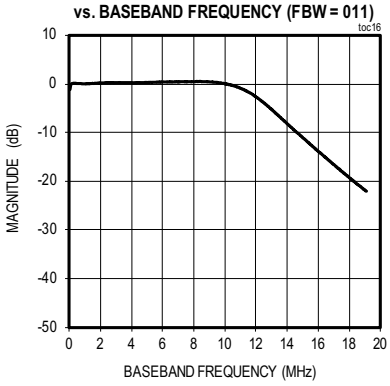
5TH-ORDER POLYPHASE FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 001)



3RD-ORDER LOW-PASS FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 011)



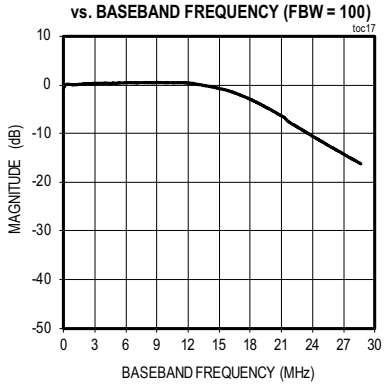
5TH-ORDER LOW-PASS FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 011)



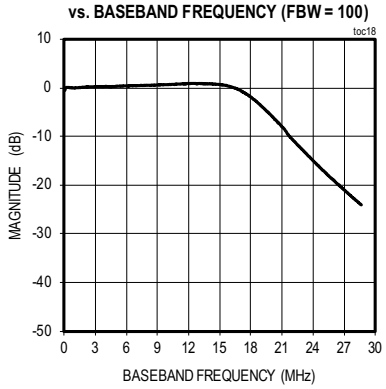
Typical Operating Characteristics (continued)

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. LNA input has specified external matching circuit. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 except for IF filter response plots in which case it is set to GAININ = 000100. For IF filter response plots, MIXPOLE = 1. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

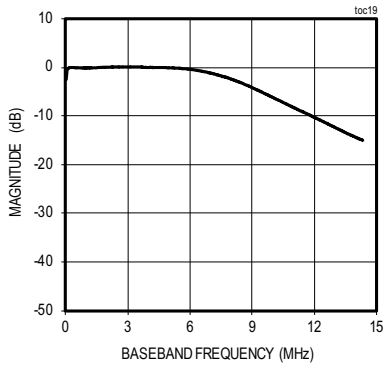
3RD-ORDER LOW-PASS FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 100)



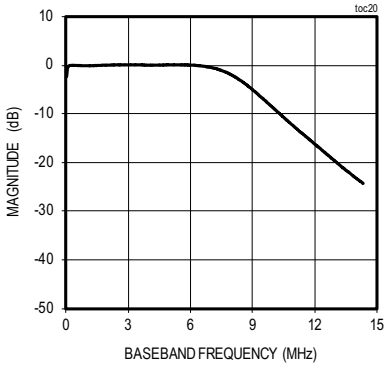
5TH-ORDER LOW-PASS FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 100)



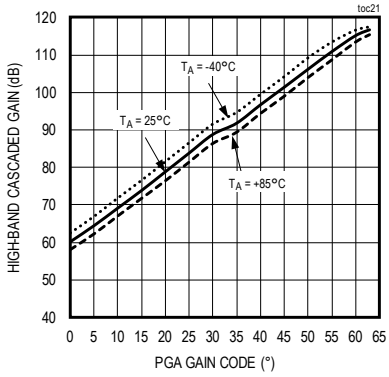
3RD-ORDER LOW-PASS FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 111)



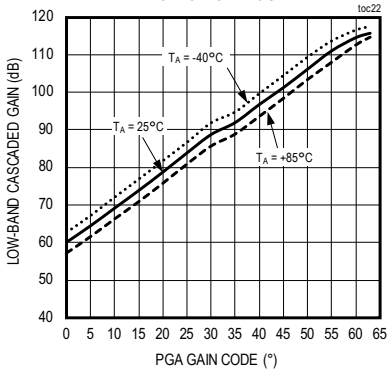
5TH-ORDER LOW-PASS FILTER RESPONSE vs. BASEBAND FREQUENCY (FBW = 111)



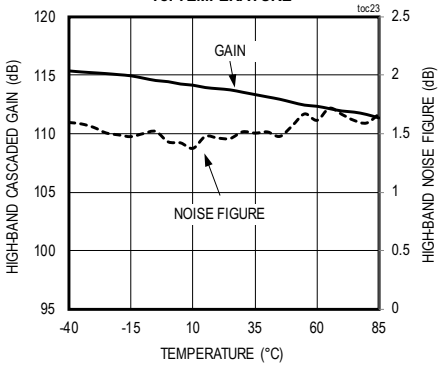
HIGH-BAND CASCADED GAIN vs. PGA GAIN CODE



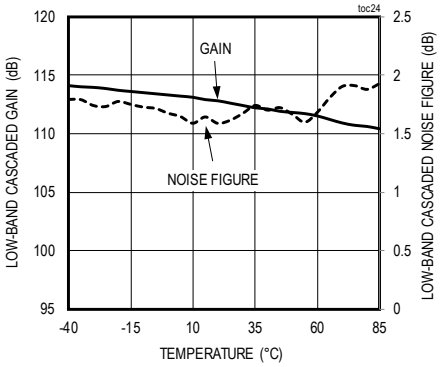
LOW-BAND CASCADED GAIN vs. PGA GAIN CODE



HIGH-BAND CASCADED GAIN AND NOISE FIGURE vs. TEMPERATURE



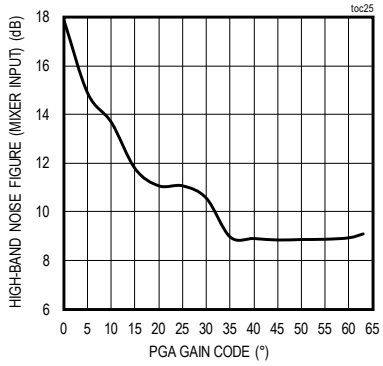
LOW-BAND CASCADED GAIN AND NOISE FIGURE vs. TEMPERATURE



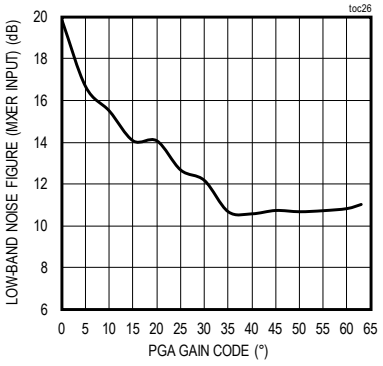
Typical Operating Characteristics (continued)

(MAX2771 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. LNA input has specified external matching circuit. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to GAININ = 111010 except for IF filter response plots in which case it is set to GAININ = 000100. For IF filter response plots, MIXPOLE = 1. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

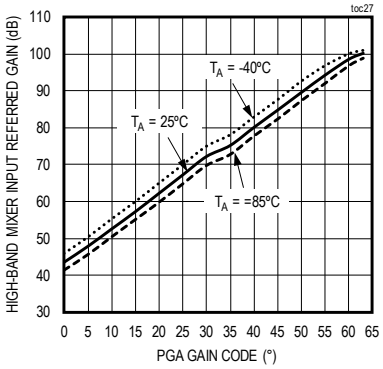
HIGH-BAND NOISE FIGURE (MIXER INPUT) vs. PGA GAIN CODE



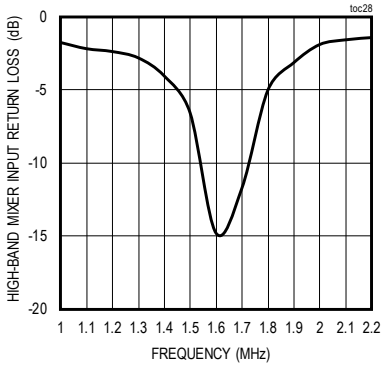
LOW-BAND NOISE FIGURE (MIXER INPUT) vs. PGA GAIN CODE



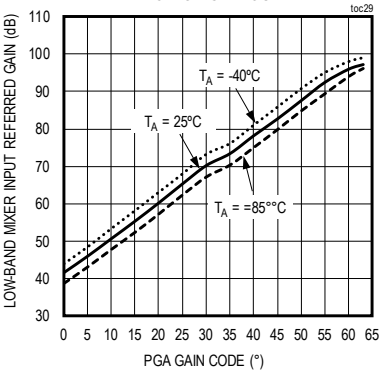
HIGH-BAND MIXER INPUT REFERRED GAIN vs. PGA GAIN CODE



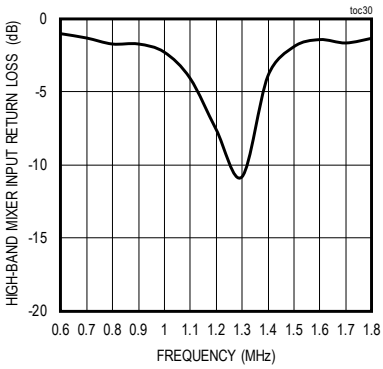
HIGH-BAND MIXER INPUT RETURN LOSS vs. FREQUENCY



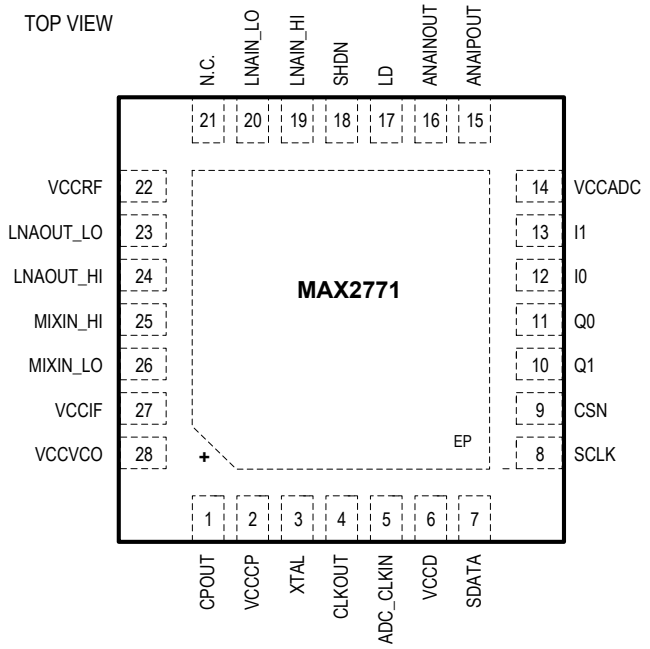
LOW-BAND MIXER INPUT REFERRED GAIN vs. PGA GAIN CODE



LOW-BAND MIXER INPUT RETURN LOSS vs. FREQUENCY



Pin Configuration



*CONNECTED EXPOSED PAD TO GROUND

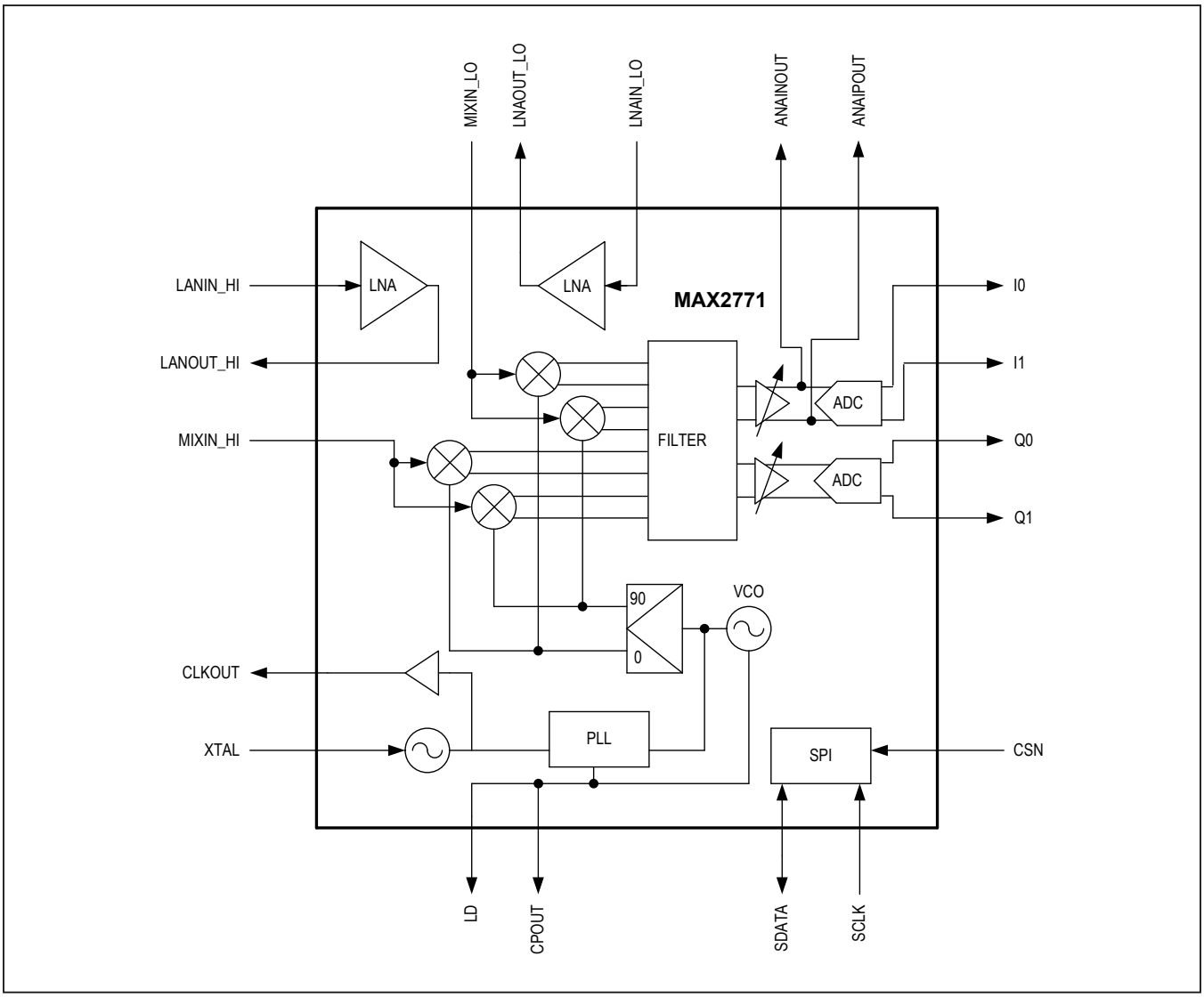
Pin Description

PIN	NAME	FUNCTION	TYPE
1	CPOUT	Charge-Pump Output. Connect a PLL loop filter as a shunt C and a shunt combination of series R and C (see *Typical Application Circuit*).	Analog output
2	VCCCP	PLL Charge-Pump Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.	Power
3	XTAL	XTAL or Reference Oscillator Input. Connect to XTAL or a DC-blocking capacitor if a TCXO is used.	Analog input
4	CLKOUT	Reference Clock Output.	Digital output
5	ADC_CLKIN	ADC Clock Input. Optionally, the ADCs can be clocked from the clock input on this pin. Refer to *ADC Clock Alignment* section for details.	Digital input
6	VCCD	Digital Circuitry Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.	Power
7	SDATA	Data Signal of 3-Wire Serial Interface.	Digital Input/ Output
8	SCLK	Clock Input of 3-Wire Serial Interface. Serial data is clocked in on the rising-edge of the SCLK and output on the falling-edge of SCLK.	Digital Input
9	CSN	Chip-Select Input of 3-Wire Serial Interface. Set CSN low to select device. Set CS high when the SPI transaction is completed.	Digital Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
10	Q1	Q-Channel Voltage Outputs. Bits 0 and 1 of the Q-channel ADC output or analog differential voltage output.	Digital or analog output
11	Q0	Q-Channel Voltage Outputs. Bits 0 and 1 of the Q-channel ADC output or analog differential voltage output.	Digital or analog output
12	I0	I-Channel Voltage Outputs. Bits 0 and 1 of the I-channel ADC output or analog differential voltage output.	Digital or analog output
13	I1	I-Channel Voltage Outputs. Bits 0 and 1 of the I-channel ADC output or analog differential voltage output.	Digital or analog output
14	VCCADC	ADC Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.	Power
15	ANAIPOUT	The Analog I+ Channel is Output On This Pin. This is used for the continuous spectrum monitoring function if the ANAIMON bit is set to 1. If continuous spectrum monitoring feature is not required, leave unconnected.	Analog output
16	ANAINOUT	The Analog I- Channel is Output On This Pin. This is used for the continuous spectrum monitoring function if the ANAIMON bit is set to 1. If continuous spectrum monitoring feature is not required, leave unconnected.	Analog output
17	LD	Lock-Detector CMOS Logic Output. A logic-high indicates the PLL is locked.	Digital output
18	SHDN	Operation Control Logic Input. A logic-low shuts off the entire device.	Digital input
19	LNAIN_HI	High-Band LNA Input Port. Requires external matching circuit of 5.6nH series inductor and 1.7pF shunt capacitor.	Analog input
20	LNAIN_LO	Low-Band LNA Input Port. Requires external matching circuit of 8.4nH series inductor and 1.1pF shunt capacitor.	Analog input
21	NC	No Connection. Leave this pin unconnected.	
22	VCCRF	RF Section Supply Voltage. Bypass to ground with 100nF and 100pF capacitors in parallel as close as possible to the pin.	Power
23	LNAOUT_LO	Low-Band LNA Output. The LNA output is internally matched to 50Ω for L2/L5 band.	Analog output
24	LNAOUT_HI	High-Band LNA Output. The LNA output is internally matched to 50Ω for L1 band.	Analog output
25	MIXIN_HI	High-Band Mixer Input. The mixer input is internally matched to 50Ω for L1 band.	Analog input
26	MIXIN_LO	Low-Band Mixer Input. The mixer input is internally matched to 50Ω for L2/L5 band.	Analog input
27	VCCIF	IF Section Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.	Power
28	VCCVCO	VCO Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.	Power

Functional Diagrams



Detailed Description

Default Register Setting

The registers will contain the reset values specified in the *Registers* section of the data sheet upon power-up. It is necessary for certain bit fields in particular registers to be programmed with fixed values that are different from the power-on reset values. These register bit fields and the required values are given in Table 1. These values must be programmed whenever the IC is power-cycled. Note that these bits are described as “Reserved" in the datasheet. Nevertheless, for these reserved bits alone, the values indicated must be programmed.

Table 2 includes the default register bit values with the above specified bits programmed, as in Table 1.

Table 1. Required Register Bit Field Values

REGISTER ADDRESS	BIT RANGE	BINARY VALUE
0x0	29:22	11111010
0x9	24:22	011

Table 2. Default Register Setting

REGISTER NAME	ADDRESS	DEFAULT
Configuration 1	0x0	0xBEA41603
Configuration 2	0x1	0x20550288
Configuration 3	0x2	0x0EAFA1DC
PLL Configuration	0x3	0x698C0008
PLL Integer Division Ratio	0x4	0x00C00080
PLL Fractional Division Ratio	0x5	0x08000070
DSP Interface	0x6	0x08000000
Clock Configuration 1	0x7	0x010061B2
Test Mode 1	0x8	0x01E0F401
Test Mode 2	0x9	0x00C00002
Clock Configuration 2	0xA	0x010061B0

Low-Noise Amplifier (LNA)

The MAX2771 integrates two low-noise amplifiers, one for the L1 band (high band) and the other for the L2/L5 band (low band). Both inputs require AC coupling capactors. Bits LNAMODE in the Configuration 1 register control the modes of the two LNAs. See Table 3. The high-band LNA input impedance is matched to 50Ω at a frequency of 1575MHz, providing the specified high-band external matching circuit is used. The low-band LNA input impedance is matched to 50Ω at a frequency of 1227MHz, providing the specified low-band external matching circuit is used.

The output of each LNA is brought out to a separate pin. The output impedance of the high-band LNA is matched to 50Ω at frequency of 1575MHz, and the low-band LNA input impedance is matched to 50Ω at a frequency of 1227MHz.

Mixer

The MAX2771 includes a quadrature mixer to output low-IF, or zero-IF, I and Q signals. There are two inputs to the mixer; one for high-band and the other for low-band. The high-band mixer input impedance is matched to 50Ω at a frequency of 1575MHz, while the low-band mixer input impedance is matched to 50Ω at a frequency of 1227MHz. The quadrature mixer requires a low-side LO injection. The output of the LNA and the input of the mixer are brought off-chip to facilitate the use of a SAW filter. On the MAX2771, the RF signal has been made accessible between the first LNA stage output and mixer input. If filtering is not desired, these pins can be connected through a coupling capacitor. However, filtering introduced at this point has minimal effect on the excellent sensitivity of the receiver. For example, for typical device parameters, a SAW filter with 1dB insertion loss would degrade cascaded NF (and therefore receiver sensitivity) by only about 0.15dB. While no external filtering is required for

Table 3. LNA Selection

LNA MODE (CONFIGURATION 1 REGISTER)	MODE
00	LNA_HI is active
01	LNA_LO is active
10	Both LNA_HI and LNA_LO are off
11	RESERVED

stand-alone applications, coexistence with cellular or WiFi transmissions in close proximity may require additional filtering to prevent compressing the receiver front-end. The mixer is configured for the desired band by the MIXERMODE[1:0] bits. Refer to Table 4.

Synthesizer

The MAX2771 integrates a 20-bit, sigma-delta, fractional-N synthesizer allowing the device to tune to a required LO frequency with an accuracy of approximately ±30Hz (when f_{XTAL} ≤ 32MHz). The synthesizer includes a 10-bit reference divider with a divisor range programmable from 1 to 1023, a 15-bit integer portion main divider with a divisor range programmable from 36 to 32767, and also a 20-bit fractional portion main divider. The reference divider is programmable through the RDIV bits in the PLL Integer Division Ratio register, and can accommodate reference frequencies from 8MHz to 44MHz. The reference divider needs to be configured so the Phase Frequency Detector comparison frequency falls between 0.05MHz and 32MHz. In Integer-N mode, if the integer division ratio is divisible by 32, setting the PWRSAV bit of the PLL Configuration Register to 1 will reduce the power consumed by the PLL.

The PLL loop filter is the only external block of the synthesizer. A typical PLL filter is the classic C-R-C network at the charge-pump output. For example, see the *Typical Application Circuit* for the recommended loop filter component values for f_{COMP} = 1.023MHz and loop bandwidth = 56KHz, with charge pump current of 0.5mA and L1 band VCO. To calculate the loop filter component values for different LO frequencies, please refer to the Design Resources section of the MAX2771 product page on the Maxim Integrated website. The desired integer and fractional divider ratios can be calculated by dividing the LO frequency (f_{LO}) by f_{COMP}. f_{COMP} can be calculated by dividing the TCXO frequency, f_{TCXO}, by the PLL reference division ratio, RDIV. For example, let the TCXO frequency be 20MHz, R_{DIV} be 1, and the nominal LO frequency be 1575.42MHz. The following method can be used when calculating divider ratios supporting various reference and comparison frequencies:

$$f_{COMP} = \frac{f_{TCXO}}{RDIV} = \frac{20MHz}{1} = 20MHz$$

$$LO_Frequency_Divider = \frac{f_{LO}}{f_{COMP}} = \frac{1575.42MHz}{20MHz} = 78.771$$

Integer Divider = 78(d) = 000 0000 0100 1110 (binary)

Fractional Divider = 0.771 x 2^{20} = 808452 (decimal) = 1100 0101 0110 0000 0100

In the fractional mode, the synthesizer should not be operated with integer division ratios greater than 251.

There are two LO tuning bands provided. These are referred to as the L1 band and L2/L5 band respectively. The L1 band is designed for L1 and Commercial Mobile Satellite Services (CMSS) such as Inmarsat used for SBAS. The L2/L5 band is for L2 and L5 bands. The selection of a band is done by programming the LOBAND bit in the PLL Configuration register. For example, if the desired LO frequency is 1227.6MHz, since this falls into the L2/L5 band, set LOBAND = 1. Assuming the same comparison TCXO frequencies as the previous example, the PLL divider ratio would be set to 1227.6/20 = 61.38.

Integer Divider = 61(d) = 000 0000 0011 1101 (binary)

Fractional Divider = 0.38 x 2^{20} = 398459 (decimal) = 0110 0001 0100 0111 1011

The LD output provides an indication of the PLL lock state. Note that the lock detector requires a reference clock in order to operate.

IF Filter

The IF filter of the receiver can be programmed to be a low pass filter or a complex bandpass filter by setting the bit FCENX bit in the Configuration 1 register to either 0 for low pass filter mode or 1 for bandpass filter mode. See Table 5.

Table 4. Mixer Selection

MIXERMODE (CONFIGURATION 1 REGISTER)	MODE
00	High-band mixer enabled
01	Low-band mixer enabled
10	Both mixers disabled
11	RESERVED

Table 5. IF Filter Mode Selection

FCENX (CONFIGURATION 1 REGISTER)	FILTER MODE
0	Low Pass
1	Bandpass

Also, the IF filter can be configured either as a 3rd-order Butterworth filter for reduced group delay or a 5th-order Butterworth filter for steeper out-of-band rejection by setting the bit F3OR5 either 1 or 0, respectively, in the Configuration 1 register. See Table 6.

The two-sided 3dB corner bandwidth can be selected to be 2.5MHz, 4.2MHz, 8.7MHz, 16.4MHz, 23.4MHz, or 36MHz by programming the FBW bits in the Configuration 1 register. See Table 7. When the FCENX bit in the Configuration 1 register is set to 1, the low-pass filter becomes a complex bandpass filter and the center frequency can be programmed with the FCEN bits in the Configuration 1 register. The IF center frequency is adjustable in 127 steps with the 7-bit FCEN value. Refer to the *Applications* section for information on how to configure the desired IF filter center frequency. If the filter is configured as a low-pass filter, the FCEN bits are ignored and the center frequency of the filter is at 0Hz.

The narrow-band filter settings are designed to pass the first null-to-first null main lobe of narrowband signals such as GPS L1 (2.046MHz) or Beidou B1 (4.092MHz). The 8.7MHz setting is for the GLONASS L1 band. The 16.4MHz setting is for signals having an intermediate bandwidth greater than the narrow band signals, but not as wide as the 20.46MHz wide signals; for example, Galileo E1 (14.3MHz) or Galileo E6 (10.23MHz). The 23.4MHz setting is for the wide-band signals typically having main lobe bandwidth of 20.46MHz. For example, GPS L1 P(Y), modernized GLONASS L3OC, or BeiDou B2. Finally, the 36MHz setting is designed to allow simultaneous reception of two constellations, specifically GPS and GLONASS in either the L1 or L2 bands. Simultaneous reception of GPS L1 and GLONASS L1 provides a greater selection of visible satellites, which in turn allows faster time to fix and a more accurate navigation solution.

Table 6. IF Filter Order Selection

F3OR5 (CONFIGURATION 1 REGISTER)	IF FILTER ORDER
0	5th order Butterworth
1	3rd order Butterworth

Programmable Gain Amplifier (PGA)

The MAX2771 integrates a baseband programmable gain amplifier that provides typically 59dB of gain control range. The PGA gain can either be controlled autonomously by the MAX2771 using the AGC function, or be directly controlled by the host through programming of the GAININ bits in the Configuration 3 register. The AGCMODE bits in the Configuration 2 register are used to select the control mode for the PGA gain. The gain can be adjusted with approximately 1 dB resolution.

Automatic Gain Control (AGC)

The MAX2771 provides a control loop that automatically programs the PGA gain to provide the ADC with an input power that optimally fills the converter and establishes a desired magnitude bit density at its output. The AGC algorithm operates by counting the number of magnitude bits over 512 ADC clock cycles and comparing the magnitude bit count to the reference value provided through a control word (GAINREF) in the Configuration 2 register. The desired magnitude bit density is expressed as a value of GAINREF in a decimal format divided by the counter length of 512. For example, to achieve the magnitude bit density of 33%, which is optimal for a 2-bit converter, program GAINREF to 170, since 170/512 = 33%. See Table 8.

Table 7. IF Filter Bandwidth Selection

FBW (CONFIGURATION 1 REGISTER)	BANDWIDTH (DOUBLE-SIDED)
000	2.5MHz
010	4.2MHz
001	8.7MHz
011 (Low-pass mode only)	23.4MHz
111 (Low-pass mode only)	16.4MHz
100 (Low-pass mode only)	36.0MHz
All other settings	RESERVED

Table 8. Gain Reference Settings

GAINREF (CONFIGURATION 2 REGISTER)	MAGNITUDE BIT DENSITY REFERENCE
11101010	234
1010100	84
100111010	314

ADC

The MAX2771 features an on-chip ADC to digitize the down-converted GNSS signal. The ADC supports the digital output in three different formats: unsigned binary, sign and magnitude, or two's complement format by setting the FORMAT bits in Configuration 2 register. Refer to Table 9. The sampled output is provided in a 2-bit format (1-bit magnitude and 1-bit sign) by default, and also can be configured as 1-bit or 2-bit in both I and Q channels, or 1-bit, 2-bit, or 3-bit in the I channel only. If only the I channel is used, the Q channel can be disabled with the IQEN bits in the Configuration 2 register. See Table 10. MSB bits are output on the I1 or Q1 pins and LSB bits are output on the I0 or Q0 pins, for I or Q channel, respectively. In the case of 3-bit output data format, the MSB is output on I1, the second bit is on I0, and the LSB is on Q1. The Q ADC must be enabled in 3-bit output data mode by setting the IQEN bit to 1. The number of bits of the ADC can be configured through the BITS field in the Configuration 2 register. See Table 11. Figure 1 illustrates the ADC quantization levels for 2-bit and 3-bit cases and also describes the sign/magnitude data mapping. The variable T = 1 designates the location of the magnitude threshold for the 2-bit case. Also refer to Table 12. The maximum ADC sampling rate is 44MHz.

Table 9. ADC Output Data Format Settings

FORMAT (CONFIGURATION 2 REGISTER)	ADC OUTPUT DATA FORMAT
00	Unsigned Binary
01	Sign and Magnitude
1X	Two's Complement Binary

Table 10. IQ Channels Enable Settings

IQEN (CONFIGURATION 2 REGISTER)	ENABLED CHANNEL
0	I channel only
1	Both I and Q channels

Table 11. ADC Output Bits Setting

BITS (CONFIGURATION 2 REGISTER)	NUMBER OF BITS IN THE ADC
000	1 bit
010	2 bits
100	3 bits

Table 12. Output Data Format

INTEGER VALUE	SIGN/MAGNITUDE			UNSIGNED BINARY			TWO'S COMPLEMENT BINARY		
	1b	2b	3b	1b	2b	3b	1b	2b	3b
7	0	01	011	1	11	111	0	01	011
5	0	01	010	1	11	110	0	01	010
3	0	00	001	1	10	101	0	00	001
1	0	00	000	1	10	110	0	00	000
-1	1	10	100	0	01	011	1	11	111
-3	1	10	101	0	01	010	1	11	110
-5	1	11	110	0	00	001	1	10	101
-7	1	11	111	0	00	000	1	10	100

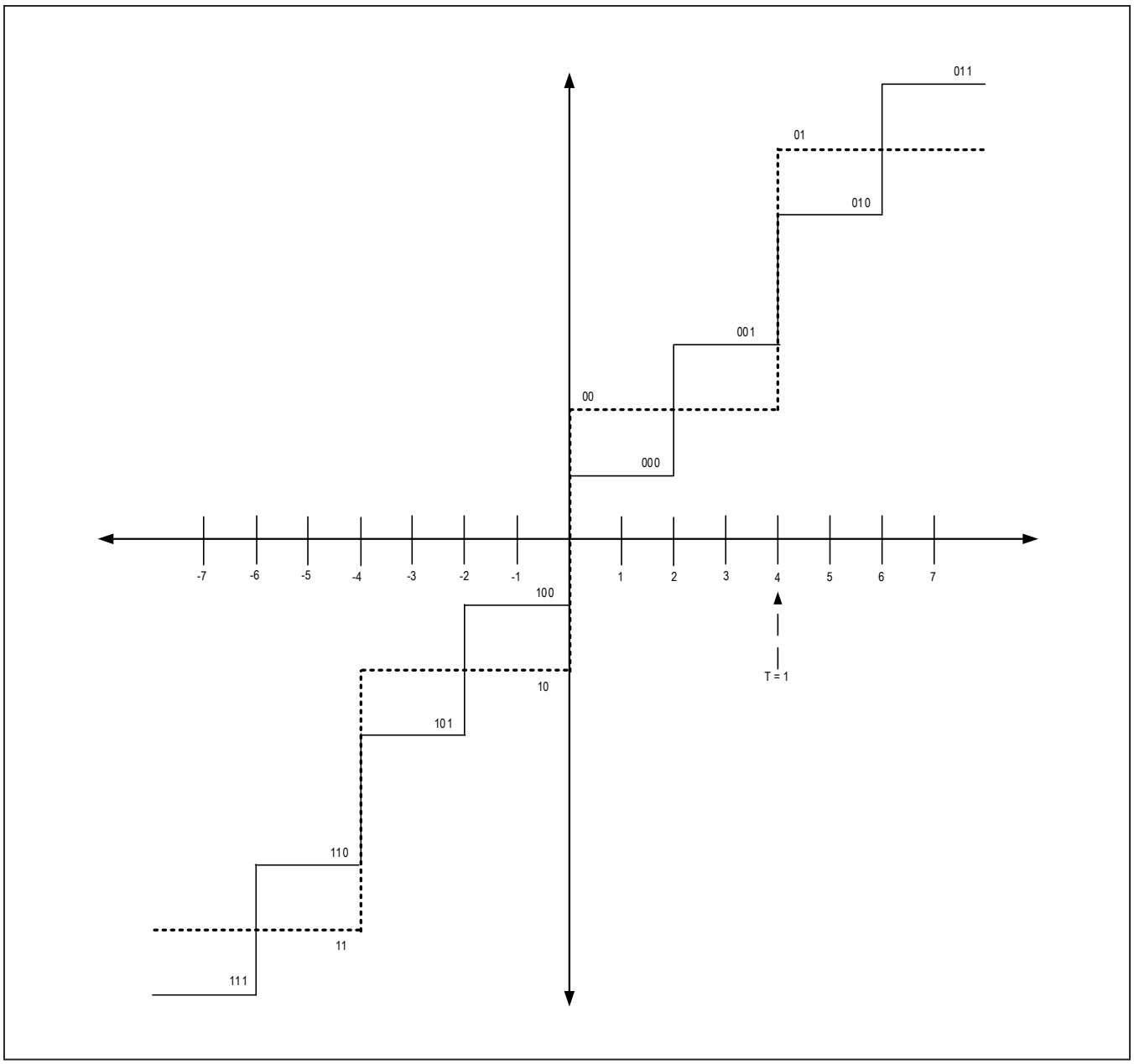


Figure 1. ADC Quantization Levels for 2 and 3-Bit Cases

ADC Fractional Clock Divider

A 12-bit fractional clock divider is located in the clock path prior to the ADC and can be used to generate an ADC clock that is a fraction of the reference input clock. In fractional divider mode, the instantaneous division ratio alternates between integer division ratios to achieve the required fraction. For example, if the fractional output clock is 4.5 times lower frequency than the input clock, an average division ratio of 4.5 is achieved through an equal series of alternating divide-by-4 and divide-by-5 periods. The fractional division ratio is given by:

$$f_{OUT}/f_{IN} = LCOUNT/(4096 - MCOUNT + LCOUNT)$$

where LCOUNT and MCOUNT are the 12-bit counter values in the Clock Configuration 2 register. The fractional division ratio cannot exceed 0.5. This divider can be enabled or bypassed by using the FCLKIN bit in the Clock Configuration 1 register. Also the sampling clock, ADCCLK, can be taken either before or after the Reference Clock Divider/Multiplier depending on the ADCCLK bit setting. Refer to Table 13. Note that REFCLK in this table is possibly the output of the refclk fractional divider.

Moreover, it is possible to take the ADC clock from outside the IC. If the EXTADCCLK bit in the Clock Configuration 1 register is 1, the ADC clock will be taken from the ADC_CLKIN pin instead of using the internally generated clock. This allows simple synchronization of multiple MAX2771 ICs to a common ADC sampling clock.

ADC Clock Alignment

In the case where multiple MAX2771 devices are used in a system, and the ADCs are being clocked at the same rate, which is some fraction of the reference clock frequency, the ADC outputs of the devices will not necessarily be aligned in time. A baseband that is processing the outputs of multiple devices may need to include additional logic to align the ADC samples from each device.

To allow simple synchronization of the ADCs of each device, the ability to clock the ADCs from an externally applied clock is provided. If the EXTADCCLK bit in the Clock Configuration 1 register is 1, the ADC clock will be taken from the ADC_CLKIN pin instead of using the internally generated clock. In a multiple MAX2771 scenario, all devices are assumed to be running off the same TCXO clock. One device would be designated as the clock source and configured to output its ADC clock on its CLKOUT pin. This clock signal can then be buffered and distributed through an external clock tree. The buffered clocks are then input on the ADC_CLKIN pins of all MAX2771 devices (including the clock source), and all devices are configured to use this external clock as their ADC clock. Alternatively, the source of the clock may not necessarily be a MAX2771 but could be some clock source elsewhere in the system.

DSP Interface

GNSS data is output from the ADC as the four logic signals (bit0, bit1, bit2, and bit3) that represent sign/magnitude, unsigned binary, or two's complement binary data in the I (bit0 and bit1) and Q (bit2 and bit3) channels. The resolution of the ADC can be set up to 3 bits per channel. For example, the 2-bit I and Q data in sign/magnitude format is mapped as follows: bit0 = ISIGN, bit1 = IMAG, bit2 = QSIGN, and bit3 = QMAG. The data can be serialized in 16-bit segments of bit0, followed by bit1, bit2, and bit3. The number of bits to be serialized is controlled by the bits STRMBITS in the Configuration 3 register. This selects between bit0; bit0 and bit1; bit0 and bit2; and bit0, bit1, bit2, and bit3 cases. If only bit0 is serialized, the data stream consists of bit0 data only. If a serialization of bit0 and bit1 (or bit2) is selected, the stream data pattern consists of 16 bits of bit0 data, followed by 16 bits of bit1 (or bit2) data. This, in turn, is followed by 16 bits of bit0 data, and so on. In this case, the serial clock must be at least twice as fast as the ADC clock. If a 4-bit serialization of bit0, bit1, bit2, and bit3 is chosen, the serial clock must be at least four times faster than the ADC clock.

Table 13. Frequency of ADC Sampling Clock vs. Reference Clock

FCLKIN (FRACTIONAL CLOCK DIVISION RATIO REGISTER)	ADCCLK (FRACTIONAL CLOCK DIVISION RATIO REGISTER)	SAMPLING CLOCK FREQUENCY
0	0	/2,/4,x2,x4 REFCLK
0	1	REFCLK
1	0	/2,/4,x2,x4 REFCLK x Fractional_Ratio
1	1	REFCLK * Fractional_Ratio

The ADC data is loaded, in parallel, into four holding registers that correspond to four ADC outputs. Holding registers are 16 bits long and are clocked by the ADC clock. At the end of the 16-bit ADC cycle, the data is transferred into four shift registers and shifted serially to the output during the next 16-bit ADC cycle. Shift registers are clocked by a serial clock that must be chosen fast enough so that all data is shifted out before the next set of data is loaded from the ADC. An all-zero pattern follows the data after all valid ADC data are streamed to the output. A DATASYNC signal is used to signal the beginning of each valid 16-bit data slice. In addition, there is a TIME_SYNC signal that is output every 128 to 16,384 cycles of the ADC clock.

Given that the serial clock has to run multiple times faster than the ADC clock, the use of the DSP interface is limited to narrowband signals that don't require a high ADC sampling clock frequency.

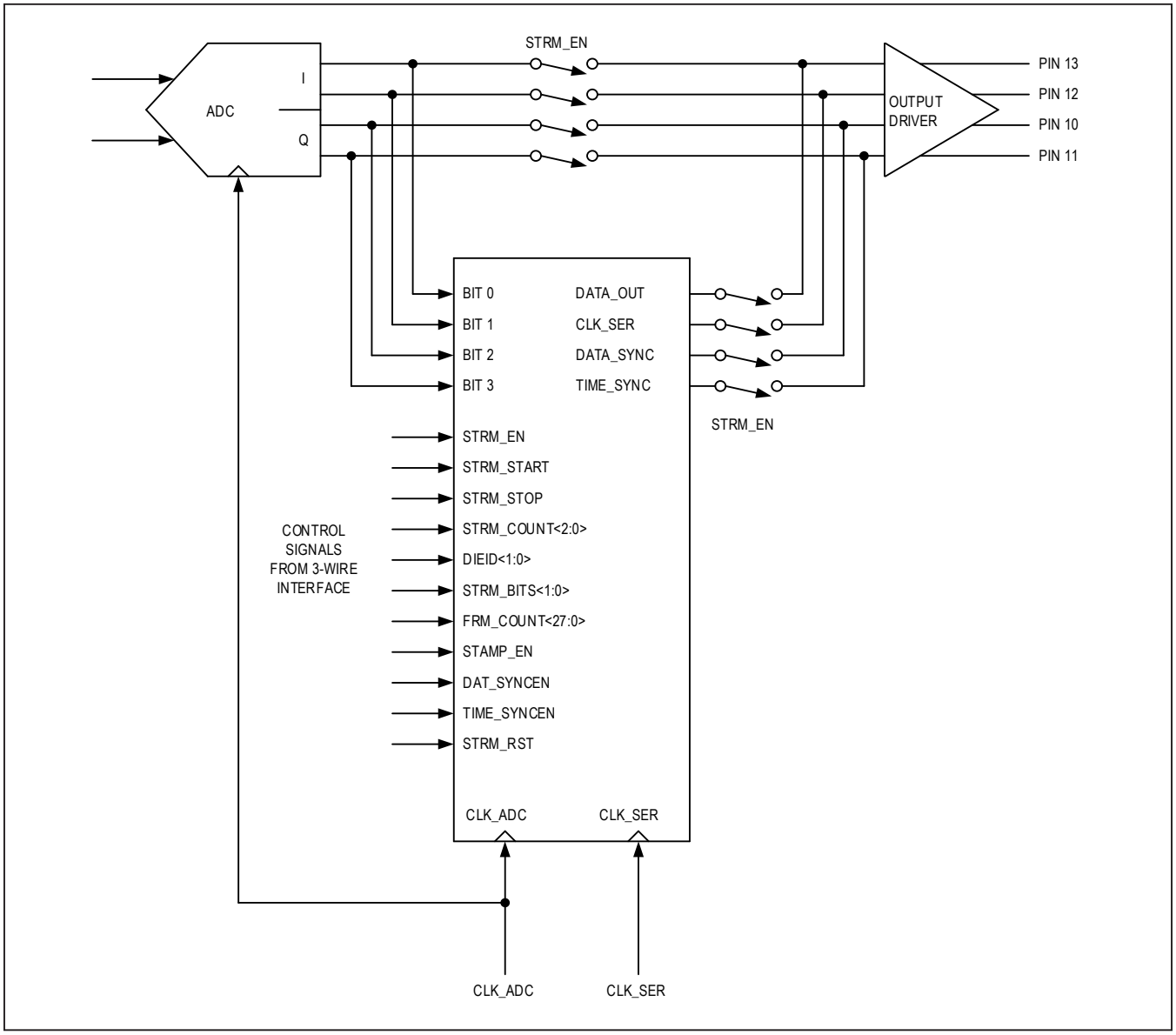


Figure 2. DSP Interface Top Level Connectivity and Control Signals

Reference Clock

The crystal clock input on pin 3 is used to generate internal clocks and a reference clock that is output to the baseband. The block diagram illustrating the clock distribution is shown in Figure 3. There is a 12-bit fractional pre-divider that optionally allows division of the XTAL clock by some fractional amount. In the fractional divider mode, the instantaneous division ratio alternates between integer division ratios to achieve the required fraction. For example, if the fractional output clock is 4.5 times lower frequency than the input clock, an average division ratio of 4.5 is achieved through an equal series of alternating divide-by-4 and divide-by-5 periods. The fractional division ratio is given by:

$$f_{OUT}/f_{IN} = LCOUNT/(4096 - MCOUNT + LCOUNT)$$

where LCOUNT and MCOUNT are the 12-bit counter values in the Clock Configuration 1 register. The fractional division ratio cannot exceed 0.5. This divider can be enabled or bypassed by setting the PREFRACDIV_SEL bit in the Clock Configuration 2 register to either 0 or 1.

The reference clock can then be optionally divided by either two or four, or multiplied by two or four. This is determined by the REFCLK bits in the PLL Configuration Register. Refer to Table 14. This table ignores the fractional ratio. The maximum frequency of the pre-divided reference clock is 22MHz if the x2 option is selected, and 11MHz if the x4 option is selected. The ADC sampling clock can then be generated by a second fractional divider. This is described in the section on the ADC. The CLKOUT signal to the baseband can be selected to either be the output of the integer divider/multiplier block or the ADC clock. This selection is done through the CLKOUT_SEL bit in the Clock Configuration 2 register.

The ADC clock can either be selected to be the internally generated clock, or taken from outside the IC. The EXTADCLK register bit selects whether the ADCs are clocked from the internally generated clock, or use the clock provided on the ADC_CLKIN pin. This feature allows multiple MAX2771 devices connected to a common baseband IC to have synchronized ADC outputs.

The maximum clock frequency for any of these clocks is 44MHz.

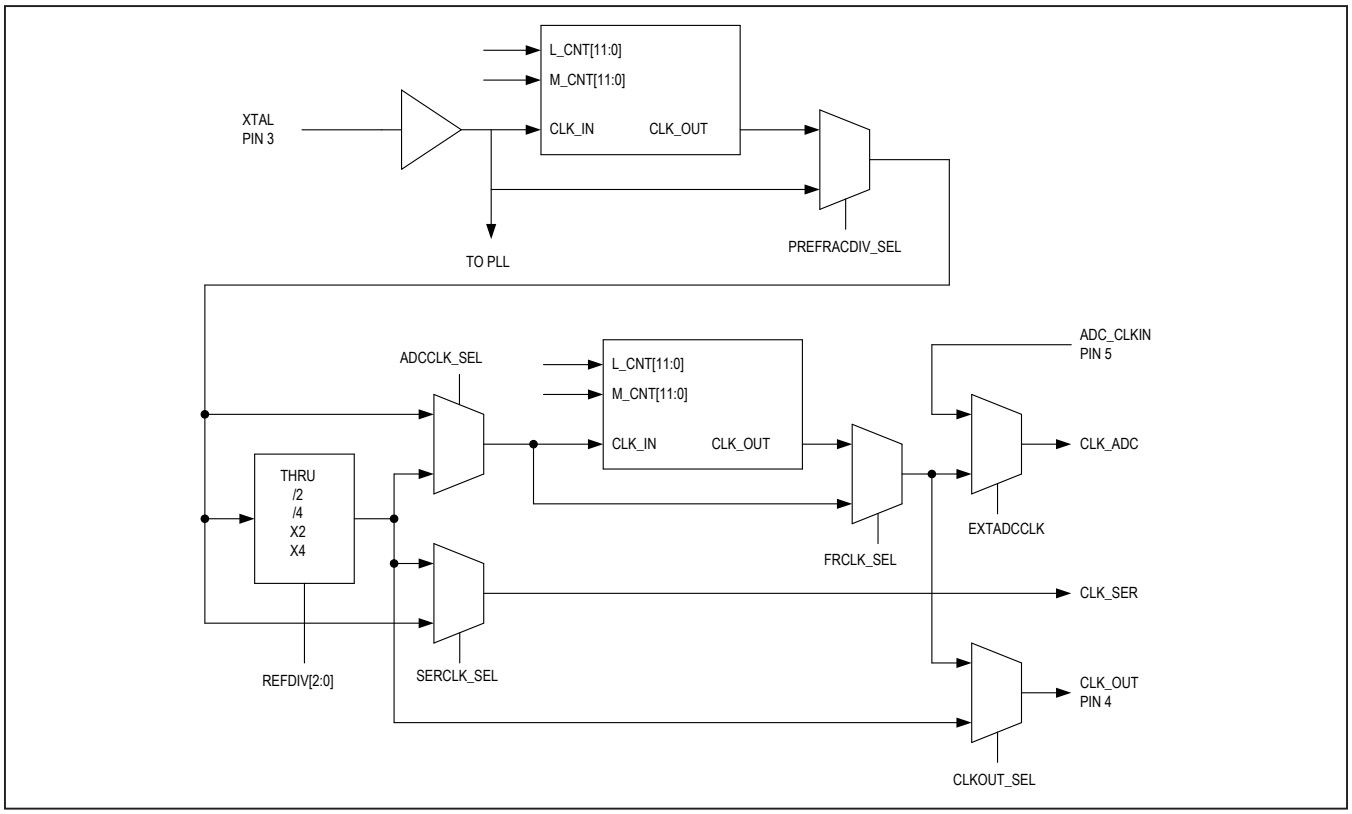


Figure 3. Clock Distribution

Table 14. Reference Divider Settings

REFDIV (PLL CONFIGURATION REGISTER)	CLOCK OUTPUT
000	XTAL frequency x2
001	XTAL frequency ÷4
010	XTAL frequency ÷2
011	XTAL frequency
100	XTAL frequency x4

Serial Interface

A serial interface is used to program the MAX2771 for configuring the different operating modes. The serial interface is controlled by three signals: SCLK (serial clock), CSN (chip select), and SDATA (serial data). The interface is based on the industry-standard Serial Peripheral Interface (SPI). The MAX2771 is a SPI slave and the device responsible for programming the MAX2771, such as a microprocessor or baseband controller, is the SPI master. The SPI master will be referred to henceforth as the “host”. The host is responsible for driving SCLK, CSN, and SDATA. The MAX2771 only drives SDATA at certain times during the transaction so as to avoid bus contention with the master.

The transfer of a set of data between host and MAX2771 is referred to as a “SPI transaction”. An SPI transaction consists of 48 SCLK pulses. The base value of SCLK is low. Data on SDATA is output on the falling edge of SCLK and is sampled on the rising edge of SCLK by both host and the MAX2771.

The SDATA line is normally tri-stated by both the host and the MAX2771. It can only be driven by the MAX2771 during the latter part of a Read SPI transaction provided that CSN = 0. SDATA is driven by the host during the entire SPI transaction in the case of Write transactions, and only during the first part of Read transactions.

The first 12 bits transferred from host to the MAX2771 during an SPI transaction contain the address of the register to be accessed. The first 8 bits are always zero, while the last four bits are the address of the register. The 13th bit transferred from master to MAX2771 is the R/W bit. If R/W = 1, the transaction is a read and the MAX2771 will drive SDATA in the latter part of the transaction. If R/W = 0, the transaction is a write, and the host will continue to drive SDATA for the remainder of the transaction. The 14th through 16th bits are turnaround bits that are denoted T_A. The purpose of these bits is to allow time for the bus to change direction in the case of a read and so avoid any possible contention for the bus. In the case of a read transaction, the host releases SDATA during this interval, and the MAX2771 does not yet start driving SDATA. In the case of a write transaction, the host can continue to drive SDATA during this interval. The value of the bits is irrelevant (don’t care). The remaining bits of the transaction are the data bits. The number of data bits will always be a 32 since all the registers in the MAX2771 are 32-bits wide.

Figure 4 shows a register read transaction. In this example, a 32 bit register is read by the host. The host first asserts CSN, begins driving SDATA with the register address preceded by 8 zeros and starts toggling SCLK. The MAX2771 samples the bits on SDATA on the rising edge of SCLK. After the address is output, the host outputs a R/W bit having value of 1 indicating this a read transaction. The next three bits are the TA bits during which the host releases the SDATA line. In this figure, SDATA is shown as tri-stated during this bit interval to emphasize that nothing is actively driving it. The MAX2771 can be configured to resistively pull up SDATA, pull it down, or apply a bus-hold during periods when it is not driving the bus. The MAX2771 then starts driving SDATA and outputting the 32 bits of the addressed register starting from the most significant bit. After the last bit has been output, the MAX2771 tri-states SDATA, and the host subsequently brings CSN high completing the transaction.

Figure 5 shows a register write transaction. In this example, a 32-bit register is written by the host. The host first asserts CSN, begins driving SDATA with the register address preceded by 8 zeros and starts toggling SCLK. The MAX2771 samples the bits on SDATA on the rising edge of SCLK. After the address is output, the host outputs a R/W bit having value of 0 indicating this a write transaction. The next bits are the TA bits. Since this is a write, the host may choose to continue driving SDATA during this interval. The next 32 SCLKs, the host outputs the 32-bit data to be written to the addressed register starting from the most significant bit. After the last bit has been output, the host tri-states SDATA, and subsequently brings CSN high completing the transaction.

If the host does not assert CSN, the MAX2771 will ignore any activity on SCLK or SDATA. This allows multiple MAX2771 devices to be connected to the SPI and controlled by one host. Only the MAX2771 that has its CSN input asserted will react to the host.

Figure 6 illustrates the timing relationships between the three signals of the three-wire interface. Refer to Table 15.

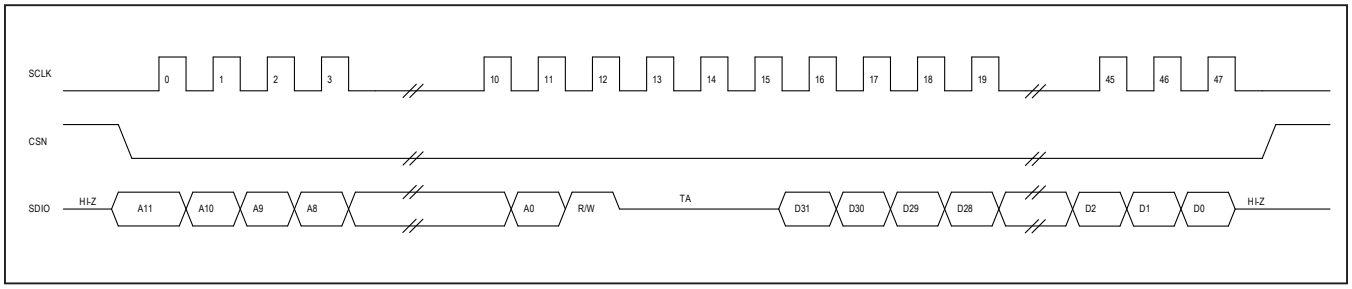


Figure 4. Register Read Functional Timing

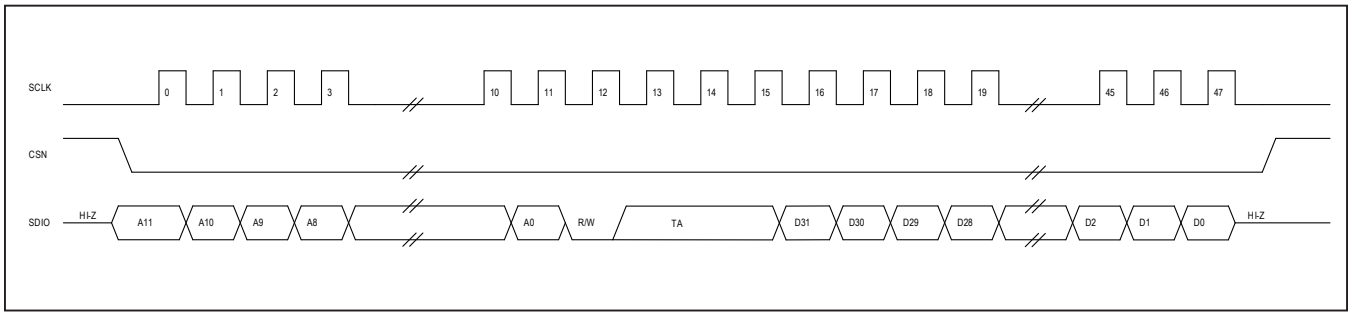


Figure 5. Register Write Functional Timing

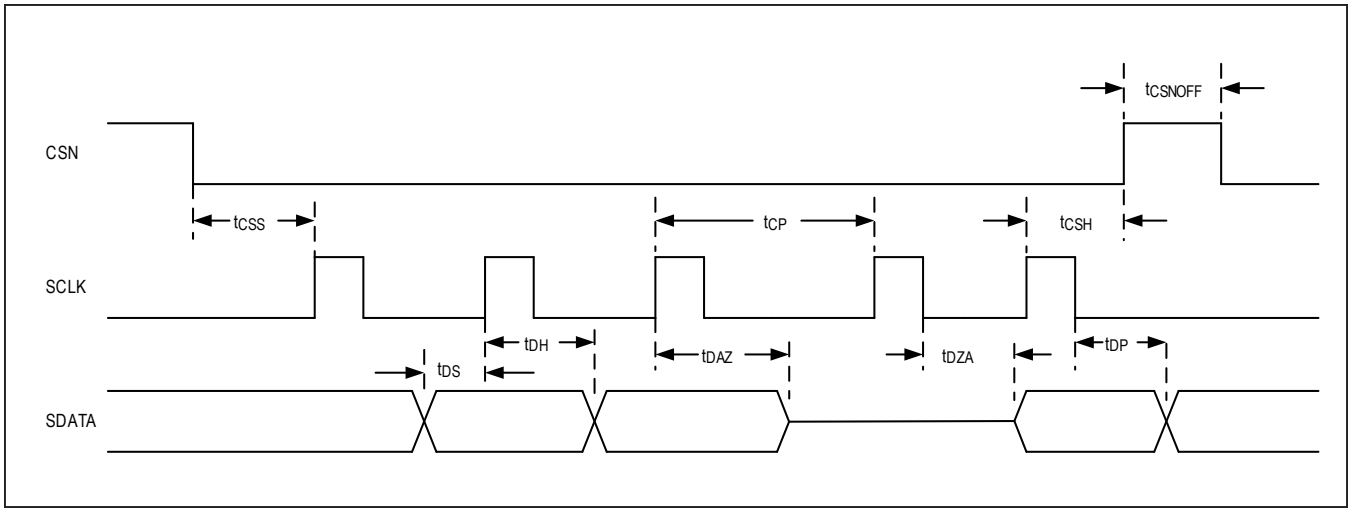


Figure 6. Three-Wire Interface Timing Diagram

Table 15. Serial Interface Timing Requirements

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{CSS}	Falling edge of CSN to rising edge of the first SCLK pulse	10		ns
t_{DS}	Data in to SCLK setup time	10		ns
t_{DH}	Data in to SCLK hold time	10		ns
t_{CP}	SCLK period	250		ns
t_{DAZ}	SCLK falling edge to SDATA tri-stated		25	ns
t_{DZA}	SCLK falling edge to SDATA active		25	ns
t_{CSH}	Last SCLK rising edge to rising edge of CSN	10		ns
t_{DP}	SCLK falling edge to data out propagation delay		25	ns
t_{CSNOFF}	CSN rising edge to next SPI transaction CSN falling edge	100		ns

Register Map

ADDRESS	NAME	MSB							LSB
REGISTER_BLOCK									
0x00	Configuration 1[31:24]	CHIPEN	IDLE	RESERVED[3:0]				RESERVED[3:2]	
	Configuration 1[23:16]	RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]		MIX POLE	LNA MODE [1]
	Configuration 1[15:8]	LNA MODE [0]	MIXERMODE[1:0]		FCEN[6:2]				
	Configuration 1[7:0]	FCEN[1:0]		FBW[2:0]			F3OR5	FCENX	FGAIN
0x01	Configuration 2[31:24]	RE SERVED	RESERVED[1:0]		ANA IMON	IQEN	GAINREF[11:9]		
	Configuration 2[23:16]	GAINREF[8:1]							
	Configuration 2[15:8]	GAIN REF[0]	SPI_SDIO_CON-FIG[1:0]		AGCMODE[1:0]		FORMAT[1:0]		BITS[2]
	Configuration 2[7:0]	BITS[1:0]		DRVCFG[1:0]		RE SERVED	RE SERVED	DIEID[1:0]	
0x02	Configuration 3[31:24]	RESERVED[3:0]				GAININ[5:2]			
	Configuration 3[23:16]	GAININ[1:0]		RE SERVED	HILOAD-EN	RE SERVED	RE SERVED	RE SERVED	RE SERVED
	Configuration 3[15:8]	FHIPEN	RE SERVED	PGAIEN	PGA QEN	STR MEN	STRM START	STRM STOP	RE SERVED [2]
	Configuration 3[7:0]	RESERVED[1:0]		STRMBITS[1:0]		STAM PEN	TIME SYN CEN	DATA SYN CEN	STR MRST
0x03	PLL Configuration[31:24]	REFDIV[2:0]			LOBAND	RE SERVED	RE SERVED	RE SERVED	REF OUTEN
	PLL Configuration[23:16]	RE SERVED	RESERVED[1:0]		IXTAL[1:0]		RESERVED[4:2]		
	PLL Configuration[15:8]	RESERVED[1:0]		RE-SERVED	RESERVED[2:0]			ICP	RE SERVED
	PLL Configuration[7:0]	RE SERVED	RESERVED[2:0]			INT_PLL	PWR SAV	RE SERVED	RE SERVED

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0x04	PLL Integer Division Ratio [31:24]	RESERVED[3:0]				NDIV[14:11]			
	PLL Integer Division Ratio [23:16]	NDIV[10:3]							
	PLL Integer Division Ratio [15:8]	NDIV[2:0]			RDIV[9:5]				
	PLL Integer Division Ratio [7:0]	RDIV[4:0]				RESERVED[2:0]			
0x05	PLL Fractional Division Ratio [31:24]	RESERVED[3:0]				FDIV[19:16]			
	PLL Fractional Division Ratio [23:16]	FDIV[15:8]							
	PLL Fractional Division Ratio [15:8]	FDIV[7:0]							
	PLL Fractional Division Ratio [7:0]	RESERVED[3:0]				RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED
0x06	RESERVED [31:24]	RESERVED[3:0]				RESERVED[27:24]			
	RESERVED [23:16]	RESERVED[23:16]							
	RESERVED [15:8]	RESERVED[15:8]							
	RESERVED [7:0]	RESERVED[7:0]							
0x07	Clock Configuration 1[31:24]	RESERVED[2:0]			EXTA DCCLK	REFCLK_L_CNT[11:8]			
	Clock Configuration 1 [23:16]	REFCLK_L_CNT[7:0]							
	Clock Configuration 1 [15:8]	REFCLK_M_CNT[11:4]							
	Clock Configuration 1 [7:0]	REFCLK_M_CNT[3:0]				FCLKIN	ADCCLK	RE SERVED	MODE
0x08	Test Mode 1[31:24]	RE SERVED	RE SERVED	RESERVED[1:0]		RESERVED[3:0]			
	Test Mode 1[23:16]	RESERVED[3:0]				RESERVED[3:0]			
	Test Mode 1[15:8]	RESERVED[3:0]				RE SERVED	RESERVED[4:2]		
	Test Mode 1[7:0]	RESERVED[1:0]		RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	RE SERVED

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0x09	Test Mode 2[31:24]	RE SERVED	RE SERVED	RD_ CALC	RESERVED[3:0]				RE SERVED [2]
	Test Mode 2[23:16]	RESERVED[1:0]		RE SERVED	RE SERVED	RESERVED[1:0]		RE SERVED	RE SERVED
	Test Mode 2[15:8]	RE SERVED	RE SERVED	RE SERVED	RESERVED[4:0]				
	Test Mode 2[7:0]	RESERVED[4:0]					RE-SERVED	RE-SERVED	RE-SERVED
0x0A	Clock Configuration 2 [31:24]	RESERVED[2:0]			RE SERVED	ADCCLK_L_CNT[11:8]			
	Clock Configuration 2 [23:16]	ADCCLK_L_CNT[7:0]							
	Clock Configuration 2 [15:8]	ADCCLK_M_CNT[11:4]							
	Clock Configuration 2 [7:0]	ADCCLK_M_CNT[3:0]				PRE FRAC DIV_SEL	CLK-OUT_ SEL	RESERVED[1:0]	

Register Details

Configuration 1 (0x0)

Configures RF and IF sections

BIT	31	30	29	28	27	26	25	24
Field	CHIPEN	IDLE	RESERVED[3:0]				RESERVED[3:2]	
Reset	0x1	0x0	0x8				0x8	
Access Type	Write, Read	Write, Read	Write, Read				Write, Read	

BIT	23	22	21	20	19	18	17	16
Field	RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]		MIXPOLE	LNA MODE[1]
Reset	0x8		0x2		0x1		0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	LNA MODE[0]	MIXERMODE[1:0]		FCEN[6:2]				
Reset	0x0	0x0		0x58				
Access Type	Write, Read	Write, Read		Write, Read				

BIT	7	6	5	4	3	2	1	0
Field	FCEN[1:0]		FBW[2:0]			F3OR5	FCENX	FGAIN
Reset	0x58		0x0			0x0	0x1	0x1
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHIPEN	31	Chip enable. Set to 1 to enable the chip and 0 to disable the chip except for the serial bus.	0x0: Disable chip 0x1: Enable chip
IDLE	30	Idle enable	0x0: Operating mode 0x1: Idle mode
RESERVED	29:26	Reserved: Write 1111 to this bitfield.	RESERVED
RESERVED	25:22	Reserved: Write 1010 to this bitfield.	RESERVED
RESERVED	21:20	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	19:18	Reserved: DO NOT CHANGE VALUE	RESERVED
MIXPOLE	17	Mixer pole selection. Set to 1 to put the passive filter pole at mixer output at 36MHz or set to 0 to put the pole at 13MHz.	0x0: Mixer pole at 13MHz 0x1: Mixer pole at 36MHz

Configuration 1 (0x0) (continued)

BITFIELD	BITS	DESCRIPTION	DECODE
LNAMODE	16:15	LNA mode selection	0x0: High band LNA is active 0x1: Low band LNA is active 0x2: Both LNAs disabled 0x3: RESERVED
MIXERMODE	14:13	Mixer mode selection	0x0: High band mixer enabled 0x1: Low band mixer enabled 0x2: Both mixers disabled 0x3: RESERVED
FCEN	12:6	IF filter center frequency setting. Refer to *Applications* section for details on usage.	
FBW	5:3	IF filter bandwidth selection.	0x0: 2.5 MHz 0x1: 8.7 MHz 0x2: 4.2 MHz 0x3: 23.4 MHz (lowpass mode only) 0x4: 36.0 MHz (lowpass mode only) 0x5: RESERVED 0x6: RESERVED 0x7: 16.4 MHz (lowpass mode only)
F3OR5	2	Filter order selection	0x0: 5th order filter 0x1: 3rd order filter
FCENX	1	Polyphase filter selection	0x0: Lowpass filter 0x1: Complex bandpass filter
FGAIN	0	IF filter gain setting	0x0: Filter gain reduced 6dB 0x1: Normal filter gain

Configuration 2 (0x1)

Configures AGC and output sections

BIT	31	30	29	28	27	26	25	24
Field	RESERVED	RESERVED[1:0]		ANAIMON	IQEN	GAINREF[11:9]		
Reset	0x0	0x1		0x0	0x0	170		
Access Type	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read		

BIT	23	22	21	20	19	18	17	16
Field	GAINREF[8:1]							
Reset	170							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	GAINREF[0]	SPI_SDIO_CONFIG[1:0]		AGCMODE[1:0]		FORMAT[1:0]		BITS[2]
Reset	170	0x0		0x0		0x1		0x2
Access Type	Write, Read	Write, Read		Write, Read		Write, Read		Write, Read

BIT	7	6	5	4	3	2	1	0
Field	BITS[1:0]		DRVCFG[1:0]		RESERVED	RESERVED	DIEID[1:0]	
Reset	0x2		0x0		0x1	0x0	0x0	
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	30:29	Reserved: DO NOT CHANGE VALUE	RESERVED
ANAIMON	28	Enables continuous spectrum monitoring by routing analog I outputs to pins	0x0: Monitoring disabled 0x1: Monitoring enabled
IQEN	27	I and Q channels enable	0x0: I channel only enabled 0x1: Both I and Q channels enabled
GAINREF	26:15	AGC gain reference value expressed by the number of MSB counts (magnitude bit density)	
SPI_SDIO_CONFIG	14:13	SPI SDIO pin configuration when tri-stated	0x0: Nothing applied 0x1: Pull-down resistor applied 0x2: Pull-up resistor applied 0x3: Bus-hold applied

Configuration 2 (0x1) (continued)

BITFIELD	BITS	DESCRIPTION	DECODE
AGCMODE	12:11	AGC mode control	0x0: Independent I and Q 0x1: Reserved 0x2: Gain set by programming of GAININ bits 0x3: Reserved
FORMAT	10:9	Output data format	0x0: Unsigned binary 0x1: Sign and magnitude 0x2: Two's complement binary 0x3: Two's complement binary
BITS	8:6	Number of bits in the ADC	0x0: 1 bit 0x1: Reserved 0x2: 2 bits 0x3: Reserved 0x4: 3 bits 0x5: Reserved 0x6: Reserved 0x7: Reserved
DRVCFG	5:4	output driver configuration	0x0: CMOS logic 0x1: Reserved 0x2: Analog outputs (ADC bypass mode) 0x3: Analog outputs (ADC bypass mode)
RESERVED	3	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	2	Reserved: DO NOT CHANGE VALUE	RESERVED
DIEID	1:0	Identifies version of IC	

Configuration 3 (0x2)

Configures support and test functions for IF filter and AGC

BIT	31	30	29	28	27	26	25	24
Field	RESERVED[3:0]				GAININ[5:2]			
Reset	0x0				0x3A			
Access Type	Write, Read				Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	GAININ[1:0]		RESERVED	HILOADEN	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0x3A		0x1	0x0	0x1	0x1	0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	FHIPEN	RESERVED	PGAIEN	PGAQEN	STRMEN	STRM START	STRMSTOP	RE SERVED[2]
Reset	0x1	0x0	0x1	0x0	0x0	0x0	0x0	0x7
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		STRMBITS[1:0]		STAMPEN	TIME SYNCEN	DATA SYNCEN	STRMRST
Reset	0x7		0x1		0x1	0x1	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31:28	Reserved: DO NOT CHANGE VALUE	RESERVED
GAININ	27:22	PGA gain value programming in steps of approximately 1dB per LSB.	
RESERVED	21	Reserved: DO NOT CHANGE VALUE	RESERVED
HILOADEN	20	Enable output driver to drive high loads	0x0: Disable high load 0x1: Enable high load
RESERVED	19	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	18	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	17	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	16	Reserved: DO NOT CHANGE VALUE	RESERVED
FHIPEN	15	Enable of highpass coupling between filter and PGA.	0x0: Disable coupling 0x1: Enable coupling
RESERVED	14	Reserved: DO NOT CHANGE VALUE	RESERVED

Configuration 3 (0x2) (continued)

BITFIELD	BITS	DESCRIPTION	DECODE
PGAIEN	13	I-channel PGA enable	0x0: Disable I channel PGA 0x1: Enable I channel PGA
PGAQEN	12	Q-channel PGA enable	0x0: Disable Q channel PGA 0x1: Enable Q channel PGA
STRMEN	11	Enable DSP interface for serial streaming of data. Configures the IC such that the DSP interface is inserted in the signal path.	0x0: Disable DSP interface 0x1: Enable DSP interface
STRMSTART	10	The rising edge of this bit enables data streaming to the output. It also enables clock, data sync, and frame sync outputs.	
STRMSTOP	9	The rising edge of this bit disables data streaming to the output. It also disables clock, data sync, and frame sync outputs.	
RESERVED	8:6	Reserved: DO NOT CHANGE VALUE	RESERVED
STRMBITS	5:4	Number of bits streamed	0x0: Reserved 0x1: I MSB, I LSB 0x2: Reserved 0x3: I MSB, I LSB, Q MSB, Q LSB
STAMPEN	3	Enables the insertion of the frame number at the beginning of each frame. If disabled, only the ADC data is streamed to the output.	0x0: Disable frame number insertion 0x1: Enable frame number insertion
TIME SYNCEN	2	Enables the output of the time sync pulses at all times when streaming is enabled by the STRMEN command. Otherwise, the time sync pulses are available only when data streaming is active at the output; for example, in the time intervals bound by the STRM-START and STRMSTOP commands.	
DATA SYNCEN	1	Enables the sync pulses at the DATASYNC output. Each pulse is coincident with the beginning of the 16-bit data word that corresponds to a given output bit.	
STRMRST	0	This command resets all the counters irrespective of the timing within the stream cycle.	

PLL Configuration (0x3)

PLL, VCO and CLK configuration

BIT	31	30	29	28	27	26	25	24
Field	REFDIV[2:0]			LOBAND	RESERVED	RESERVED	RESERVED	REFOUTEN
Reset	0x3			0x0	0x1	0x0	0x0	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	23	22	21	20	19	18	17	16
Field	RESERVED	RESERVED[1:0]		IXTAL[1:0]		RESERVED[4:2]		
Reset	0x1	0x0		0x1		0x10		
Access Type	Write, Read	Write, Read		Write, Read		Write, Read		

BIT	15	14	13	12	11	10	9	8
Field	RESERVED[1:0]		RESERVED	RESERVED[2:0]			ICP	RESERVED
Reset	0x10		0x0	0x0			0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read			Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED[2:0]			INT_PLL	PWRSAV	RESERVED	RESERVED
Reset	0x0	0x0			0x1	0x0	0x0	0x0
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REFDIV	31:29	Clock output divider ratio	0x0: XTAL frequency x2 0x1: XTAL frequency /4 0x2: XTAL frequency /2 0x3: XTAL frequency 0x4: XTAL frequency x4 0x5: Reserved 0x6: Reserved 0x7: Reserved
LOBAND	28	Local Oscillator band selection	0x0: L1 band 0x1: L2/L5 band
RESERVED	27	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	26	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	25	Reserved: DO NOT CHANGE VALUE	RESERVED
REFOUTEN	24	Output clock buffer enable	0x0: Disable clock buffer 0x1: Enable clock buffer

PLL Configuration (0x3) (continued)

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	23	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	22:21	Reserved: DO NOT CHANGE VALUE	RESERVED
IXTAL	20:19	Current programming for XTAL oscillator/buffer	0x0: Reserved 0x1: Normal current 0x2: Reserved 0x3: High current
RESERVED	18:14	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	13	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	12:10	Reserved: DO NOT CHANGE VALUE	RESERVED
ICP	9	Charge pump current selection	0x0: 0.5 mA 0x1: 1 mA
RESERVED	8	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	7	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	6:4	Reserved: DO NOT CHANGE VALUE	RESERVED
INT_PLL	3	PLL mode control. Selects either integer-N or fractional-N PLL mode.	0x0: Fractional-N PLL 0x1: Integer-N PLL
PWRSAV	2	Enable PLL power-save mode	0x0: Disable PLL power-save mode 0x1: Enable PLL power-save mode
RESERVED	1	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	0	Reserved: DO NOT CHANGE VALUE	RESERVED

PLL Integer Division Ratio (0x4)

PLL main and reference division ratios, other controls

BIT	31	30	29	28	27	26	25	24
Field	RESERVED[3:0]				NDIV[14:11]			
Reset	0x0				1536			
Access Type	Write, Read				Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	NDIV[10:3]							
Reset	1536							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	NDIV[2:0]			RDIV[9:5]				
Reset	1536			16				
Access Type	Write, Read			Write, Read				

BIT	7	6	5	4	3	2	1	0
Field	RDIV[4:0]					RESERVED[2:0]		
Reset	16					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31:28	Reserved: DO NOT CHANGE VALUE	RESERVED
NDIV	27:13	PLL integer division ratio	
RDIV	12:3	PLL reference division ratio	
RESERVED	2:0	Reserved: DO NOT CHANGE VALUE	RESERVED

PLL Fractional Division Ratio (0x5)

PLL fractional division ratio, other controls

BIT	31	30	29	28	27	26	25	24
Field	RESERVED[3:0]				FDIV[19:16]			
Reset	0x0				0x80000			
Access Type	Write, Read, Dual				Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	FDIV[15:8]							
Reset	0x80000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	FDIV[7:0]							
Reset	0x80000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[3:0]				RESERVED	RESERVED	RESERVED	RESERVED
Reset	0x7				0x0	0x0	0x0	0x0
Access Type	Write, Read, Dual				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31:28	Reserved: DO NOT CHANGE VALUE	RESERVED
FDIV	27:8	PLL fractional division ratio	
RESERVED	7:4	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	3	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	2	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	1	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	0	Reserved: DO NOT CHANGE VALUE	RESERVED

RESERVED (0x6)

Reserved

BIT	31	30	29	28	27	26	25	24
Field	RESERVED[3:0]				RESERVED[27:24]			
Reset	0x0				0x8000000			
Access Type	Write, Read, Dual				Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	RESERVED[23:16]							
Reset	0x8000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	RESERVED[15:8]							
Reset	0x8000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[7:0]							
Reset	0x8000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31:28	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	27:0	Reserved: DO NOT CHANGE VALUE	RESERVED

Clock Configuration 1 (0x7)

Clock Configuration

BIT	31	30	29	28	27	26	25	24
Field	RESERVED[2:0]			EXTADC CLK	REFCLK_L_CNT[11:8]			
Reset	0x0			0x0	256			
Access Type	Write, Read			Write, Read	Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	REFCLK_L_CNT[7:0]							
Reset	256							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	REFCLK_M_CNT[11:4]							
Reset	1563							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	REFCLK_M_CNT[3:0]				FCLKIN	ADCCLK	RESERVED	MODE
Reset	1563				0x0	0x0	0x1	0x0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31:29	Reserved: DO NOT CHANGE VALUE	RESERVED
EXTADCCLK	28	Selects either internally generated or externally applied clock as ADC sampling clock	0x0: Use internally generated clock 0x1: Use clock provided on ADC_CLKIN pin
REFCLK_L_CNT	27:16	Sets the value for the L counter	
REFCLK_M_CNT	15:4	Sets the value for the M counter	
FCLKIN	3	Fractional clock divider selection	0x0: Bypass ADC clock divider 0x1: Take ADC clock from fractional divider
ADCCLK	2	ADC clock selection	0x0: Use output of reference clock divider/multiplier 0x1: Bypass reference clock divider/multiplier
RESERVED	1	Reserved: DO NOT CHANGE VALUE	RESERVED
MODE	0	DSP interface mode selection	

Test Mode 1 (0x8)

RESERVED

BIT	31	30	29	28	27	26	25	24
Field	RESERVED	RESERVED	RESERVED[1:0]		RESERVED[3:0]			
Reset	0x0	0x0	0x0		0x1			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	RESERVED[3:0]				RESERVED[3:0]			
Reset	0xE				0x0			
Access Type	Write, Read				Write, Read			

BIT	15	14	13	12	11	10	9	8
Field	RESERVED[3:0]				RESERVED	RESERVED[4:2]		
Reset	0xF				0x0	0x10		
Access Type	Write, Read				Write, Read	Write, Read, Dual		

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0x10		0x0	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read, Dual		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	30	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	29:28	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	27:24	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	23:20	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	19:16	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	15:12	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	11	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	10:6	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	5	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	4	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	3	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	2	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	1	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	0	Reserved: DO NOT CHANGE VALUE	RESERVED

Test Mode 2 (0x9)

RESERVED

BIT	31	30	29	28	27	26	25	24
Field	RESERVED	RESERVED	RD_CALC	RESERVED[3:0]				RE SERVED[2]
Reset	0x0	0x0	0x0	0x0				0x0
Access Type	Write Only	Write, Read	Write, Read	Write, Read				Write, Read

BIT	23	22	21	20	19	18	17	16
Field	RESERVED[1:0]		RESERVED	RESERVED	RESERVED[1:0]		RESERVED	RESERVED
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	RESERVED	RESERVED	RESERVED	RESERVED[4:0]				
Reset	0x0	0x0	0x0	0x00				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read, Dual				

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					RESERVED	RESERVED	RESERVED
Reset	0x00					0x0	0x1	0x0
Access Type	Write, Read, Dual					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	30	Reserved: DO NOT CHANGE VALUE	RESERVED
RD_CALC	29	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	28:25	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	24:22	Reserved: Write 011 to this bitfield.	RESERVED
RESERVED	21	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	20	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	19:18	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	17	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	16	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	15	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	14	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	13	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	12:8	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	7:3	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	2	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	1	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	0	Reserved: DO NOT CHANGE VALUE	RESERVED

Clock Configuration 2 (0xA)

Clock Configuration

BIT	31	30	29	28	27	26	25	24
Field	RESERVED[2:0]			RESERVED	ADCCLK_L_CNT[11:8]			
Reset	0x0			0x0	256			
Access Type	Write, Read			Write, Read	Write, Read			

BIT	23	22	21	20	19	18	17	16
Field	ADCCLK_L_CNT[7:0]							
Reset	256							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	ADCCLK_M_CNT[11:4]							
Reset	1563							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	ADCCLK_M_CNT[3:0]				PRE FRACDIV_ SEL	CLKOUT_ SEL	RESERVED[1:0]	
Reset	1563				0x0	0x0	0x0	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	31:29	Reserved: DO NOT CHANGE VALUE	RESERVED
RESERVED	28	Reserved: DO NOT CHANGE VALUE	RESERVED
ADCCLK_ L_CNT	27:16	Sets the value for the L counter	
ADCCLK_ M_CNT	15:4	Sets the value for the M counter	
PRE FRACDIV_ SEL	3	Fractional clock divider selection	0x0: Bypass fractional clock divider 0x1: Enable fractional divider
CLKOUT_ SEL	2	CLKOUT selection	0x0: Integer divider/multiplier output 0x1: ADC clock
RESERVED	1:0	Reserved: DO NOT CHANGE VALUE	RESERVED

Applications Information

IF Filter Center Frequency Configuration

The FCEN bits in the Configuration 1 register are used to set the center frequency of the IF filter when it is configured as a bandpass filter. The following equations are used to calculate the required setting of FCEN to obtain the target center frequency. The center frequency should not be set higher than 9MHz for any filter bandwidth.

For FBW = 000 corresponding to a 2.5MHz filter bandwidth, the center frequency is calculated using the following equation:

$$F_{CENTER} = \left(\frac{128 - FCEN}{2}\right) \times 0.195MHz$$

For FBW = 010 corresponding to a 4.2MHz filter bandwidth, the center frequency is calculated using the following equation:

$$F_{CENTER} = \left(\frac{128 - FCEN}{2}\right) \times 0.355MHz$$

For FBW = 001 corresponding to a 8.7MHz filter bandwidth, the center frequency is calculated using the following equation:

$$F_{CENTER} = \left(\frac{128 - FCEN}{2}\right) \times 0.66MHz$$

Here are some examples: If FBW = 000, and FCEN[6:0] = 1011000, then the 2.5MHz wide filter will be centered at approximately [(128 – 88)/2](0.195) MHz = 3.9MHz.

If FBW = 001, and FCEN = 1101001, then the 8.7MHz wide filter will be centered at approximately

[(128 – 105)/2](0.66) MHz = 7.6MHz.

The calculations give approximate center frequencies. The center frequency needs to be tuned empirically.

Operation for Wideband Signals

Some signals used for precision GNSS or modernized GNSS have wide bandwidths. For example, the GPS L1 P(Y) signal has a main lobe (first null spacing) of 20.46 MHz, and the Galileo E6 signal is 10.23 MHz wide. For such wideband signals, the use of the wideband lowpass filter is recommended so as to fit the entire main lobe of the signal within the passband of the filter and by doing so, avoid reducing the SNR.

First, the LO frequency has to be tuned to the center of the wanted signal so as to down-convert the signal to DC. For the case of the GPS L1 P(Y) signal, the required LO frequency is 1575.42MHz. As an example, assume the TXCO frequency is 16.368 MHz. Assume the PLL reference division ratio (RDIV) = 16 giving a comparision frequency of 1.023 MHz. This allows use of the Integer-N PLL. Set the INT_PLL bit in the PLL Configuration register to 1. The PLL integer division ratio (NDIV) needs to be set to 1575.42/1.023 = 1540.

The IF filter is configured as a low pass 5th-order Butterworth 23.4MHz filter. Configure FBW = 011, F3OR5 = 0, and FCENX = 0. The FCEN bits can be left untouched since they are ignored for the lowpass filter case. Set the filter pole at the mixer output to 36MHz by setting MIXPOLE = 1. The ADC sampling rate should be set to a few MHz beyond the double-sided passband of the IF filter which is 23.4MHz in this case. This is to avoid degradation due to aliasing of noise. The offset frequency (from the 3dB corner frequency) at which the attenuation is 20dB is 18.5MHz. Hence, an ADC sampling rate of at least two times this, or 37MHz, is required. With a 16.368MHz TCXO clock, it is not possible, given the limitations on fractional division ratio and maximum frequency of the clock multiplier, to generate a 37MHz clock internally. The ADC clock is, therefore, provided from an external source on the ADC_CLKIN pin and the EXTADCLK register bit set to use the externally applied ADC clock.

As a second example, assume reception of the Galileo E5a signal is desired. This has a bandwidth of 20.46MHz and is centered at a frequency of 1176.45MHz. Since this frequency is in the L2/L5 band, the LOBAND bit in the PLL Configuration register must be set to 1. Assuming the same TXCO and reference division ratios as in the prior example, this means the integer division ratio must be 1150. Again, since the center frequency is an integer multiple of 1.023MHz, the PLL can be operated as an Integer-N PLL. (The use of a 1.023MHz comparison frequency is convenient since most GNSS carrier frequencies will be integer multiples of 1.023MHz.) Since this is also a 20.46MHz wide signal, the IF filter settings and ADC clock configuration are the same as the prior example.

For a final example, consider reception of the Galileo E1 signal. This is 14.3MHz wide and centered at the frequency of 1575.42MHz. Assuming the same conditions as the prior examples, the synthesizer will be programmed identically to the first example. The IF filter will be programmed identically to the first example except for the bandwidth. The 16.4MHz wide filter setting should be used instead (FBW = 111). An ADC sampling rate of at least 26MHz is required. In this case, it is decided to simply multiply the TXCO clock by 2 giving an ADC clock frequency of 32.7MHz.

Determining AGC Gain Setpoint

When the MAX2771 PGA gain is determined by the AGC, the user may wish to know what the actual gain value determined by the AGC is. This is not directly readable through a SPI register. However, it can be determined indirectly through the following method. Bypass the on-chip ADCs, and measure the noise power or noise power density at the analog monitoring output. Say it is -68.5dBm/Hz for example. Then switch the AGC to fixed mode where the PGA gain is determined by the value programmed into the register. Remeasure the noise power density. Say it is -63.3dBm/Hz. Then take the difference between these two readings, rounding off to the nearest dB, and compare to the 58dB setting of the PGA. In this example, the delta between the two readings (rounded off) is 5dB, so we know the set point must be 58 – 5 = 53dB.

PCB Layout Considerations

The MAX2771 EV kit can be used as a starting point for layout. For best performance, take into consideration grounding and routing of RF, baseband, and power supply lines. Make connections from vias to the ground plane as short as possible. On the high impedance ports, keep traces short to minimize shunt capacitance. EV kit Gerber files are available on the MAX2771 product page of the Maxim Integrated website.

Power-Supply Layout

To minimize coupling between different sections of the IC, a star power-supply routing configuration with a large decoupling capacitor at a central VCC_ node is recommended. The VCC_ traces branch out from this node, each going to a separate VCC_ node in the circuit. Place a bypass capacitor as close as possible to each supply pin. This arrangement provides local decoupling at each VCC_ pin. Use at least one via per bypass capacitor for a low inductance ground connection. Do not share the capacitor ground vias with any other branch. Refer to the application note General Layout Guidelines for RF and Mixed-Signal PCBs, available on the MAX2771 product page for more information.

Typical Application Circuit

Circuit 1

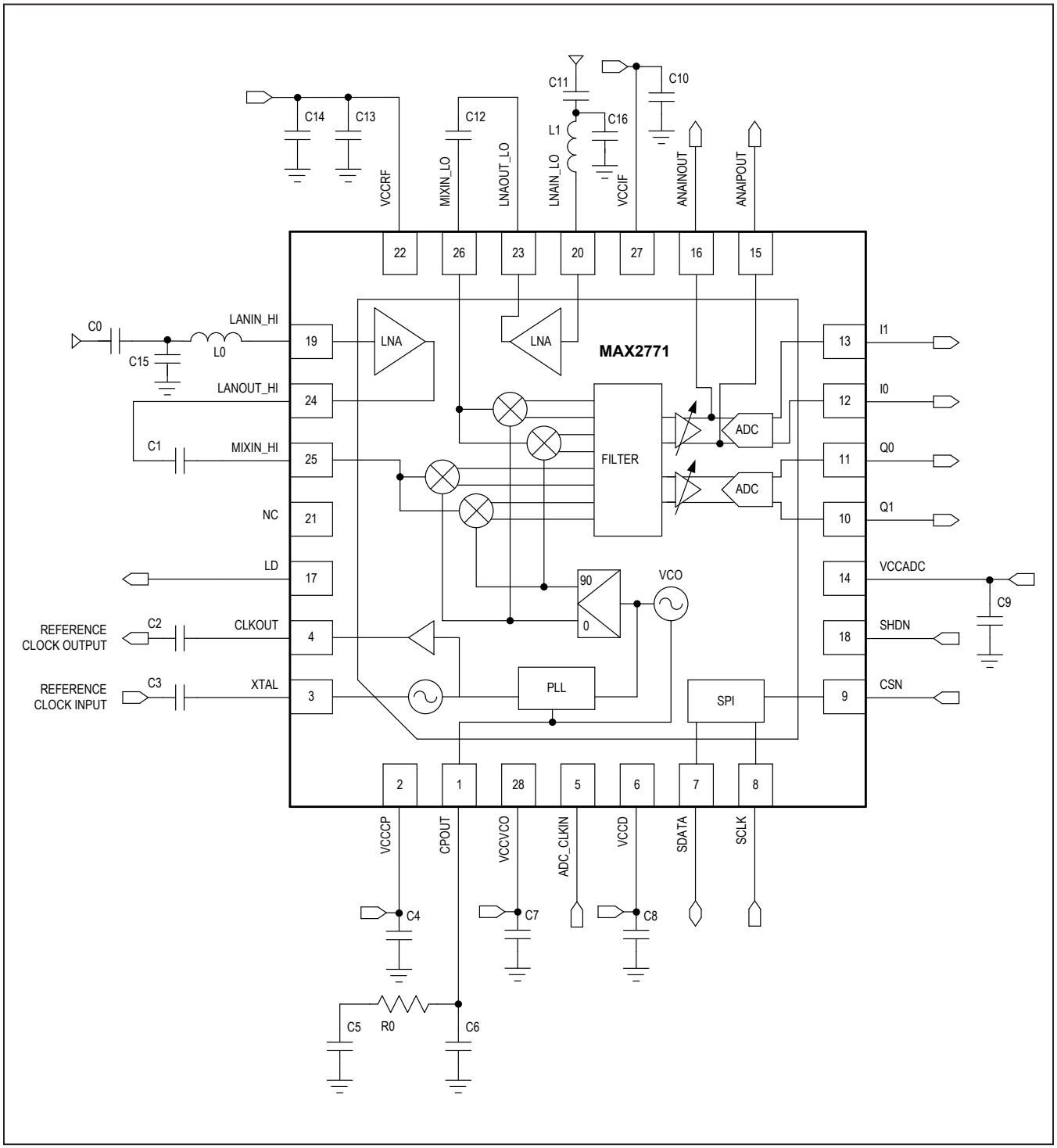


Table 16. External Component List

DESIGNATION	QUANTITY	DESCRIPTION
C0, C11	2	0.47nF AC-coupling capacitors
C5	1	0.75nF PLL loop filter capacitor
C6	1	15pF PLL loop filter capacitor
C4, C7, C8, C9, C10, C13	6	0.1µF supply voltage bypass capacitor
C2, C3	2	10nF AC-coupling capacitor
C1, C12	2	0.47nF AC-coupling capacitor
C14	1	0.1nF supply voltage bypass capacitor
R0	1	15kΩ PLL loop filter resistor
L0	1	5.6 nH RF matching inductor for high-band LNA inputs
L1	1	8.4 nH RF matching inductor for low-band LNA input
C15	1	1.7 pF RF matching capacitor for high-band LNA input
C16	1	1.1 pF RF matching capacitor for low-band LNA input

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX2771ETI+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/18	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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