MAX20751

Multiphase Master with PMBus Interface and Internal Buck Converter

General Description

The MAX20751 PMBus™-compliant multiphase master IC, with extensive status and parameter monitoring, is capable of driving up to four smart-slave integrated power devices.

Utilizing Maxim's smart-slave ICs, the device provides a high-density and flexible solution that can be tailored to a range of power loads used in communication equipment. Proprietary-coupled inductors, recommended to reduce the effective inductor value without excessive ripple current, results in improved transient response and reduction in the number of output capacitors required.

The device incorporates current reporting, temperature monitoring, fault detection, and PMBus support. Overcurrent and overtemperature faults are detected by the individual smart slaves and faults communicated through the master IC. The highest junction temperature is reported, both before and after smart-slave regulation.

The device features an integrated switching regulator that can optionally be used to supply the V_{DD} rail for the master controller and smart-slave devices to reduce the power-rail requirements and simplify the regulator design.

Applications

- Communication, Networking, Servers, and Storage Equipment
  - ASICs
  - Microprocessor Chipsets
  - Memory V_{DDQ}
  - Other High-Current Digital ICs

***Ordering Information* appears at end of data sheet.**

PMBus is a trademark of SMIF, Inc.

Benefits and Features

- Increased Power Density with Fewer External Components Needed
  - Scalable, Multiphase Solution
  - Compatibility with Coupled Inductors Enables Fast Transient Response and Reduced C_{OUT}
  - Integrated Internal Switching Regulator to Power Smart Slaves
- Optimized Component Performance and Efficiency with Reduced Design-In Time
  - PMBus-Compliant Interface for Telemetry and Power Management
  - Field-Programmable Memory to Allow Storage of Desired Configuration Parameters
  - Fault Logging
- Comprehensive System and IC Self-Protection Features Promote Increased Power-Supply Reliability
  - Overcurrent and Overtemperature
  - Boost Voltage UVLO
  - VX Short to Ground or V_{DDH} Detection
  - Phase-Current Steering for Thermal Balancing
- 36-Pin (6mm x 6mm) QFN Package

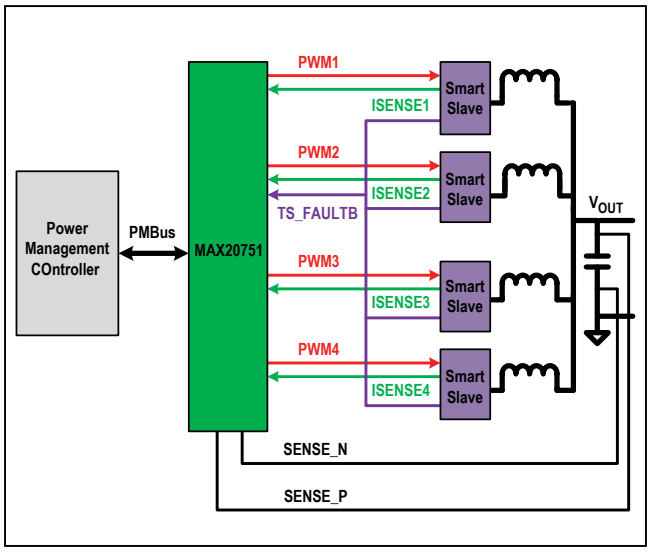


Figure 1. Basic Application Circuit

maxim integrated™

Absolute Maximum Ratings

V_{DD33} Supply Voltage.....-0.3V to +4V
VIN_UV, VR_ON and PWRGD Pins.....-0.3V to +4V
V_{DD} Supply Voltage .....-0.3V to +2.5V
PVX to PGND.....-0.6V to V_{DD33} + 0.6V
PMBus Pins (PMD, PMC, ALERTB).....-0.3V to +6V
SENSE_N.....-0.3V to V_{DD} +0.3V
SENSE_P.....-0.3V to +4V
R_REF, MRAMP, R_SELx, PWMx, TS_FAULTB, ISENSEx, A1_OUT, A2_x, A2B_OUT, A3_x.....-0.3 to V_{DD} + 0.3V
Junction Temperature (T_J).....+150°C
Storage Temperature Range.....-65°C to +150°C
Peak Reflow Temperature.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ratings

V_{DD33} Supply Voltage.....+2.97V to +3.63V
V_{DD} Supply Voltage .....+1.71V to +1.98V
VIN_UV, VR_ON and PWRGD .....-0.1V to +3.6V
PMBus Pins (PMD, PMC, ALERTB) .....-0.1V to +5.5V
SENSE_N.....-0.1V to +0.2V
SENSE_P .....-0.1V to +2.5V
Junction Temperature Range (T_J).....-40°C to +125°C

Package Thermal Characteristics

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}).....1.7°C/W

This product is completely Halogen-free and Pb-free, employing SnAgCu solder balls. The product is RoHS compliant with an -e1 termination finish and is compatible with both SnPb and Pb-free soldering operations. The product is MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.

Electrical Characteristics

(V_{DD} = 1.71V to 1.98V, V_{DD33} = 3.3V ±10%, **T_J = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES AND CURRENTS						
Supply Voltage Range	V_{DD}	If external V_{DD} supply is used	1.71	1.86	1.98	V
Supply Current	I_{DD}	PWM not switching (Note 2)	14	17	20	mA
3.3V Supply Voltage Range	V_{DD33}		2.97	3.30	3.63	V
3.3V Supply Current	I_{DD33}	No load, internal integrated switcher disabled, PMBus idle (Note 2)		24	130	µA
V_{DD} UVLO (UNDERVOLTAGE LOCKOUT)						
Supply Voltage Undervoltage-Lockout Rising Threshold	$V_{DD_UVLO_RIS}$	(Note 2)		1.62	1.66	V
Supply Voltage Undervoltage-Lockout Falling Threshold	$V_{DD_UVLO_FAL}$	(Note 2)	1.58	1.60		V
V_{DD33} UVLO						
3.3V Supply Voltage Undervoltage-Lockout Rising Threshold	$V_{DD33_UV_RIS}$	(Note 2)		2.90	2.95	V
3.3V Supply Voltage Undervoltage-Lockout Falling Threshold	$V_{DD33_UV_FAL}$	(Note 2)	2.80	2.85		V

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 1.98V, V_{DD33} = 3.3V ±10%, T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN UVLO (USING VIN_UV PIN)						
VIN_UV Rising Threshold	VIN_UV_{RIS}	(Note 2)		0.380	0.390	V
VIN_UV Falling Threshold	VIN_UV_{FAL}	(Note 2)	0.318	0.328		V
Delay from VIN_UV UVLO to System Shutdown	$t_{dVIN_UV_UVLO}$		125		275	ns
INTEGRATED INTERNAL SWITCHER						
Output Valley Voltage	V_{OUT_IIS}			1.86		V
Current Driving Capability	I_{OUT_IIS}	Tested at L = 2.2µH, t_{ON} = 1.30µs	300			mA
Switcher Peak Inductor Current	I_{LPK_IIS}				1.5	A
High-Side Switch On-Time	t_{ON_IIS}	Default 1.30µs (Notes 1, 2)	0.52	0.65	0.78	µs
			1.04	1.30	1.56	
			1.52	1.90	3.28	
			2.20	2.75	3.30	
V_{NOM} (NOMINAL OUTPUT VOLTAGE AFTER STARTUP, WITHOUT DROOP)						
Output Voltage Range	V_{NOM}	Programmable through R_SEL or PMBus, direct feedback of V_{OUT} to SENSE_P (Notes 1, 2)	0.500		1.520	V
Resolution		(Note 2)		5		mV
DC Accuracy		1V ≤ V_{NOM} ≤ 1.52V (Note 2)	-0.5		+0.5	%
		0.5V ≤ V_{NOM} < 1V (Note 2)	-5		+5	mV
VID Set Point (V_{OUT} Fine-Adjustment Voltage)	$V_{OUT_FINE_ADJ}$	Programmable with PMBus, default is 0.00mV. (Notes 1, 2)	3.25	3.75	4.25	mV
			2.00	2.50	3.00	
			0.75	1.25	1.75	
			-0.50	0.00	+0.50	
			-1.75	-1.25	-0.75	
			-3.00	-2.50	-2.00	
			-4.25	-3.75	-3.25	
			-5.50	-5.00	-4.50	
SWITCHING FREQUENCY						
Nominal Switching Frequency Range	f_{SW}	Programmable through R_SEL or PMBus (Note 1)	300		800	kHz
Switching Frequency Tolerance	f_{SW_TOL}	(Note 2)	-10		+10	%
OUTPUT-VOLTAGE STARTUP SLEW RATES						
Output-Voltage Slew Rate After Initial Jump from 0V	S_{VOUT}	Programmable through R_SEL or PMBus (Note 1)		0.5		mV/µs
				1.25		
				2.5		
				5		

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 1.98V, V_{DD33} = 3.3V ±10%, T_J = +25°C, unless otherwise noted.).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
R_REF						
Reference Voltage for R_REF	V_{R_REF}	(Note 2)	0.79	0.80	0.81	V
AMPLIFIER A1						
A1 Amplifier Closed-Loop Differential Gain	A_{1DM}	(Note 2)	2.17	2.19	2.23	V/V
Error-Amplifier Closed-Loop BW	CLBW		7		15	MHz
Positive Sense Line Current	I_{SENSE_P}	VSENSE_N grounded (Note 2)			90	µA
Negative Sense Line Current	I_{SENSE_N}	VSENSE_P grounded (Note 2)	-90			µA
AMPLIFIER A2						
Amplifier Closed-Loop Gain of A2 with feedback capacitor C2 shorted	A_{V2}	Set through external R (Note 1)	1		4	V/V
A2 Amplifier Open-Loop Gain	A_{OL2}		60			dB
Closed-Loop Bandwidth	CLBW_A2	Gain = 2	10			MHz
AMPLIFIER A2B						
A2B Amplifier Closed-Loop Gain	A_{DM}			1		V/V
Closed-Loop Bandwidth	CLBW_A2B		11			MHz
AMPLIFIER A3						
A3 Amplifier Open-Loop Gain	A_{OL3}		60			dB
Closed-Loop Bandwidth	CLBW_A3	Gain = 2	10			MHz
MODULATOR RAMP RATE						
Ramp-Rate Programming Range	M_{RAMP}	Program through R at MRAMP pin (Note 1)	0.4		2	V/µs
OVERCURRENT PROTECTION (OCP)						
Positive Current Limit (Sustaining), Programmed Through R_{DES}	P_{OCP}	Voltage across R_{DES} referred to VCM, 4-phase system (Notes 1, 2)	-0.658	-0.598	-0.538	V
Negative Current Limit (Sustaining)	N_{OCP}	Voltage across R_{DES} referred to VCM, 4-phase system (Note 2)	0.157	0.183	0.209	V
Positive Current-Limit Tolerance	I_{LIM_TOL}	Not including the external resistor tolerance (1%) (Note 2)	-10		+10	%
OVERVOLTAGE PROTECTION (OVP)						
Tracking OVP Threshold Voltage Above V_{NOM} (Rising)	V_TRA_OVP	(Note 2)		205	217	mV
Tracking OVP Threshold Voltage (Falling)		(Note 2)	187	199		
Tracking OVP Blanking Time from the End of an I_{DAC} Transition	t_BL_OVP			90		µs

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 1.98V, V_{DD33} = 3.3V ±10%, T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Umbrella OVP Threshold Voltage (Rising)	$V_{_UMB_OVP}$	(Note 2)		2.52	2.59	V
Umbrella OVP Threshold Voltage (Falling)		(Note 2)	2.38	2.45		V
Delay Time to Respond to OVP	t_{d_OVP}			1		µs
VR_ON (ENABLE) PIN						
VR_ON_{IH}	VR_ON	(Note 2)	0.9			V
VR_ON_{IL}		(Note 2)			0.2	V
VR_ON Deglitch Filter Time	t_{FLT_VRON}			2		µs
PWRGD (Note 3)						
PWRGD Assert Threshold (Rising)	V_{THR_PG}	Referenced to V_{NOM} (Note 2)		-225	-216	mV
PWRGD Deassert Threshold (Falling)		Referenced to V_{NOM} (Note 2)	-234	-227		mV
PWRGD Deassert Threshold Deglitch Filter Time					8	µs
PWRGD High-Deglitch Filter Time	t_{d_PG}	PWRGD remains deasserted until 90µs after the end of the startup I_{DAC} transition		90		µs
Output Low Voltage	V_{PG_OL}	I_{OL} = -4mA (Note 2)			0.3	V
ORTHOGONAL CURRENT REBALANCING (OCR)						
Gain	OCR	Programmable through PMBus (Note 1)		0		
				1.8		
				3.5		
				4.4		
PMBus (PMC, PMD, ALERTB PINS)						
Input High Voltage (PMC, PMD)	V_{IH}	(Note 2)	1.5		V_{PM}	V
Input Low Voltage (PMC, PMD)	V_{IL}	(Note 2)	-0.1		+0.8	V
Output Low Voltage (PMD, ALERTB)	V_{OL}	I_{OL} = -4mA (Note 2)			0.4	V
PMBus Resistor Pullup Voltage (PMC, PMD, ALERTB)	V_{PM}		1.71		5.5	V
PMBus Clock Frequency	f_{PMC}			100	400	kHz
NONVOLATILE MEMORY PROGRAMMING						
Temperature Range for Programming Data into Nonvolatile Memory	$TEMP_{NVM_PROG}$	Applies only to STORE_USER_ALL PMBus command	-40		+85	°C

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 1.98V, V_{DD33} = 3.3V ±10%, T_J = +25°C, unless otherwise noted.).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMBus MONITORING AND TELEMETRY						
Range of Reported Output Current as a Percentage of Positive Output Current-Limit IPLIM	$IOUT_{REPORT}$	1, 2, or 3 slaves	-30		+100	%
		4 slaves	-30		+88	
Error of Reported Output Current		4-phase system at 100A, 1.0V, not including R_{DES} tolerance (Note 2)	-6		+6	
Resolution of Reported Output Current				0.5		A
Update Rate of Reported Output Current				512		µs
Overcurrent Warning Response Time Delay After Update				1		ms
Range of Reported Highest Slave Temperature	$TEMP_{REPORT}$		-40		+127	°C
Error of Reported Highest Slave Temperature		4-phase system at 70A, 1.0V (Note 2)	-6		+6	°C
Resolution of Reported Slave Temperature				1		°C
Update Rate of Reported Slave Temperature				3		ms
Temperature Warning or Fault-Response Time Delay After Update				1		ms
Scaled Voltage Range of Input Voltage at VIN_UV Pin	VIN_{SCALE}		0.317		1.383	V
Range of Reported Input Voltage	VIN_{REPORT}	140/2048 for VIN_UV/VIN voltage ratio, no offset added	4.625		20.25	V
Error of Reported Input Voltage		Not including tolerance of resistor voltage-divider (Note 2)	-2		+2	%
Resolution of Reported Input Voltage				31.25		mV
Update Rate of Reported Input Voltage				3		ms
Input-Voltage Warning or Fault-Response Time Delay After Update				1		ms

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 1.98V, V_{DD33} = 3.3V ±10%, T_J = +25°C, unless otherwise noted.)

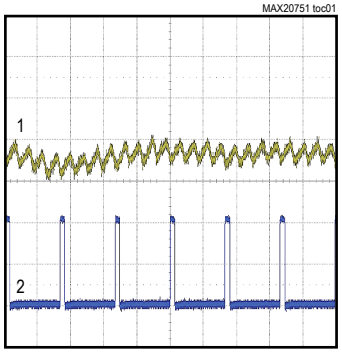
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Range of Reported Output Voltage	$VOUT_{REPORT}$		0.500		1.520	V
Error of Reported Output Voltage		1.000V ≤ V_{OUT} ≤ 1.520V (Note 2)	-1		+1	%
		0.500V ≤ V_{OUT} < 1.000V (Note 2)	-10		+10	mV
Resolution of Reported Output Voltage				5		mV
Update Rate of Reported Output Voltage				3		ms
Output Voltage Warning or Fault-Response Time Delay After Update				1		ms
Range of Reported Output Power as a Percentage of (V_{OUT}) x (IPLIM)	$POUT_{REPORT}$	1, 2, or 3 slaves	0		100	%
		4 slaves	0		88	
Error of Reported Output Power		4-phase system at 100A, 1.0V, not including R_{DES} tolerance (Note 2)	-7		+7	%
Resolution of Reported Output Power				2		W
Update Rate of Reported Output Power				3		ms

Note 1: Parameters are programmable.
Note 2: Specifications apply over the TJ = -40°C to +105°C temperature range.
Note 3: PWRGD output signal is different from the PMBus POWER_GOOD signal.

Typical Operating Characteristics

(V_{IN} = 12V, V_{OUT} = 1.00V, f_{SW} = 300kHz, Four Phases, C_{OUT} = 32 x 47µF Multilayer Ceramic Capacitors, L_{OUT} = 100nH/Phase Two Winding-Coupled Inductor for Each Pair of Phases.)

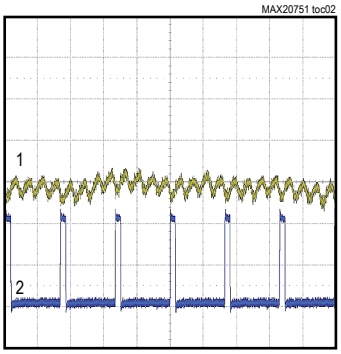
OUTPUT-VOLTAGE RIPPLE - NO LOAD



Time/div: 2µs

CONDITIONS: TRIGGER ON PWM2, POSITIVE-GOING EDGE
1. V_{OUT}: 5mV/div, 20MHz BANDWIDTH
2. PWM2: 1.00V/div, 20MHz BANDWIDTH

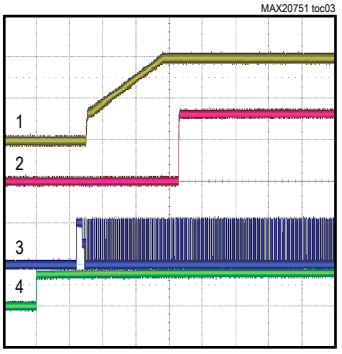
OUTPUT-VOLTAGE RIPPLE - 120A LOAD



Time/div: 2µs

CONDITIONS: TRIGGER ON PWM2, POSITIVE-GOING EDGE
1. V_{OUT}: 5mV/div, 20MHz BANDWIDTH
2. PWM2: 1.00V/div, 20MHz BANDWIDTH

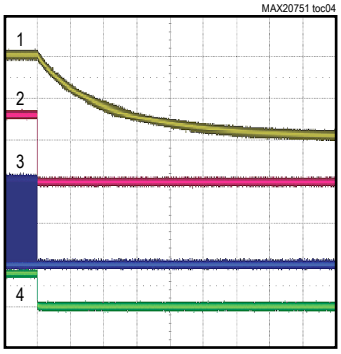
TURN-ON WAVEFORMS - NO LOAD



Time/div: 200µs

CONDITIONS: TRIGGER ON VR_ON, POSITIVE-GOING EDGE
1. V_{OUT}: 500mV/div, 20MHz BANDWIDTH
2. PWRGD: 2.00V/div, 20MHz BANDWIDTH
3. PWM2: 2.00V/div, 20MHz BANDWIDTH
4. VR_ON: 2.00V/div, 20MHz BANDWIDTH

TURN-OFF WAVEFORMS - NO LOAD



Time/div: 20ms

CONDITIONS: TRIGGER ON VR_ON, NEGATIVE-GOING EDGE
1. V_{OUT}: 500mV/div, 20MHz BANDWIDTH
2. PWRGD: 2.00V/div, 20MHz BANDWIDTH
3. PWM2: 1.00V/div, 20MHz BANDWIDTH
4. VR_ON: 2.00V/div, 20MHz BANDWIDTH

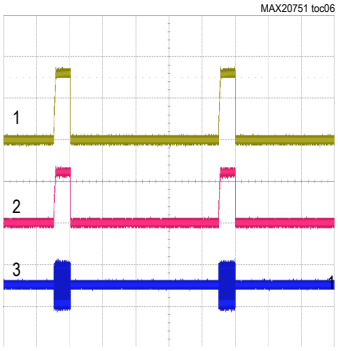
OUTPUT-VOLTAGE LOAD TRANSIENT RESPONSE (60A-90A)



Time/div: 20µs

CONDITIONS: TRIGGER ON V_{OUT}, POSITIVE-GOING EDGE
1. V_{OUT}: 50mV/div, 20MHz BANDWIDTH

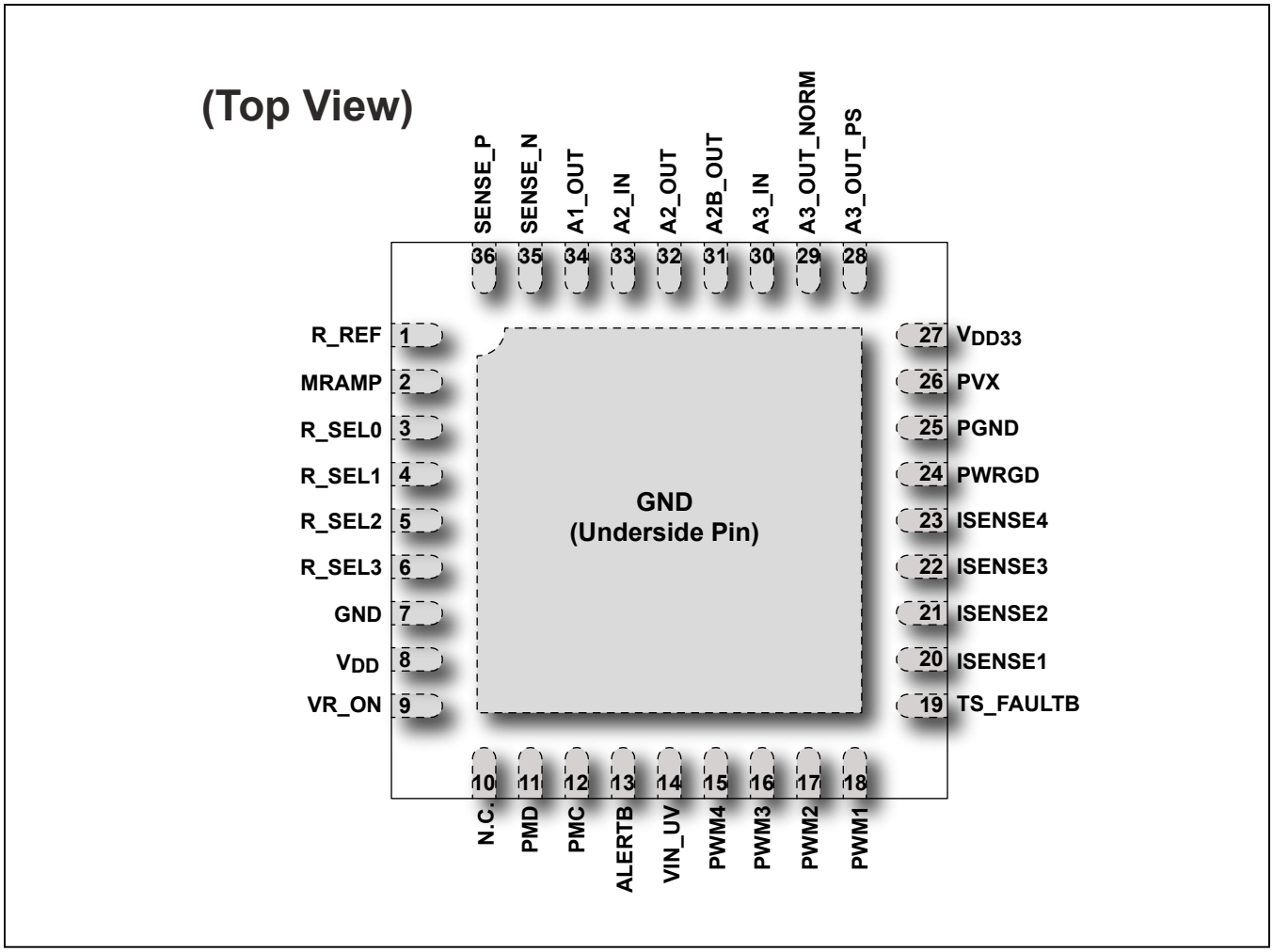
OUTPUT VOLTAGE IN HICCUP-MODE OVERCURRENT PROTECTION



Time/div: 10ms

CONDITIONS: TRIGGER ON V_{OUT}, NEGATIVE-GOING EDGE
1. V_{OUT}: 500mV/div, 20MHz BANDWIDTH
2. I_{OUT}: 133.3A/div, 20MHz BANDWIDTH
3. PWM2: 2.00V/div, 20MHz BANDWIDTH

Pin Configuration



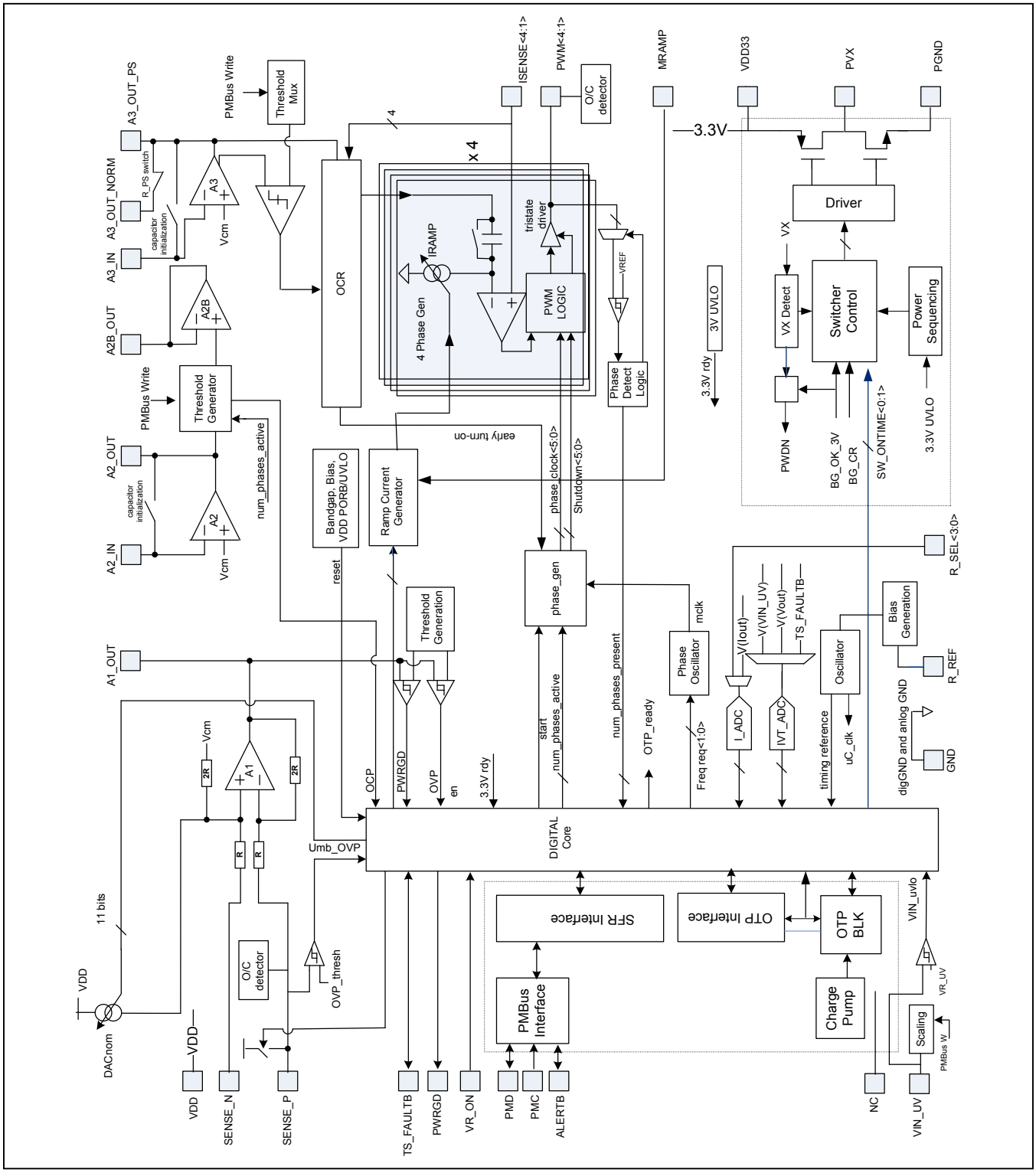
Pin Description

PIN	NAME	FUNCTION
1	R_REF	Connect the 20kΩ reference resistor R_REF from this pin to ground. The resistor should have ±0.5% tolerance or lower, with a temperature coefficient of ±25ppm/°C or lower.
2	MRAMP	Connect this node to ground through a resistor to program the PWM regulator modulator ramp rate.
3–6	R_SEL0–R_SEL3	Programming Input. Connect these nodes to ground through a configuration resistor with ±1% tolerance or lower and a temperature coefficient of ±100ppm/°C or lower.
7	GND	Ground
8	V_{DD}	V_{DD} Supply Voltage Connection
9	VR_ON	Input for Regulator to Enable Regulation
10	N.C.	No Connection. This node should not be connected to any other devices or components. It is connected internally.

Pin Description (continued)

PIN	NAME	FUNCTION
11	PMD	PMBus Data I/O
12	PMC	PMBus Clock
13	ALERTB	Open-Drain, Active-Low PMBus Alert Output
14	VIN_UV	Scaled Version of Slave V_{DDH} Voltage. A resistor-divider on this input is used to program the input undervoltage lockout (UVLO) threshold for the slave V_{DDH} supply.
15–18	PWM4–PWM1	Pulse-Width-Modulation Phase-Control Outputs for the Regulator. Connect these nodes to the input pins of the slave devices selected for the application. Connect pins for phases not populated to ground. Do not leave any PWM pin unconnected.
19	TS_FAULTB	Temperature Sensor and Slave Fault Flag. Connect this node to the TSENSE outputs of the slave ICs. This node is an analog representation of the junction temperature for the hottest slave of the regulator during normal operation and is also used by the slave devices to report faults (a fault condition is asserted low).
20–23	ISENSE1–ISENSE4	Phase Current-Sense Inputs. Connect these nodes to the ISENSE outputs of the slave devices. Ground the pin if not in use (the corresponding RPH resistor should not be connected to ISENSE when ISENSE is connected to ground) to minimize noise into the device.
24	PWRGD	Power-Good Output for the Regulator. This node indicates whether the output voltage is within regulation. This open-drain output should be pulled high externally with a resistor of approximately 10kΩ.
25	PGND	Power Ground. Connect this node to power ground.
26	PVX	Internal Switcher Switching Node. This node should be connected to an inductor for correct operation.
27	V_{DD33}	3.3V Supply for the IC and Internal Switcher
28	A3_OUT_PS	Phase-Shedding Feature (disabled in the MAX20751). This pin must be connected to A3_OUT_NORM with a short trace or a 0Ω resistor.
29	A3_OUT_NORM	Phase Current-Loop Amplifier Output for the Regulator. Must be connected to A3_OUT_PS with a short trace or a 0Ω resistor.
30	A3_IN	Phase Current-Loop Amplifier Negative Input
31	A2B_OUT	This node has the same value as A2_OUT during normal operation, but has programmable positive and negative voltage clamps that limit the maximum positive and negative output current.
32	A2_OUT	Voltage-Loop Amplifier Output
33	A2_IN	Voltage-Loop Amplifier Negative Input
34	A1_OUT	Differential Error-Amplifier Output
35	SENSE_N	Negative Remote-Voltage Sense
36	SENSE_P	Positive Remote-Voltage Sense

Block Diagram



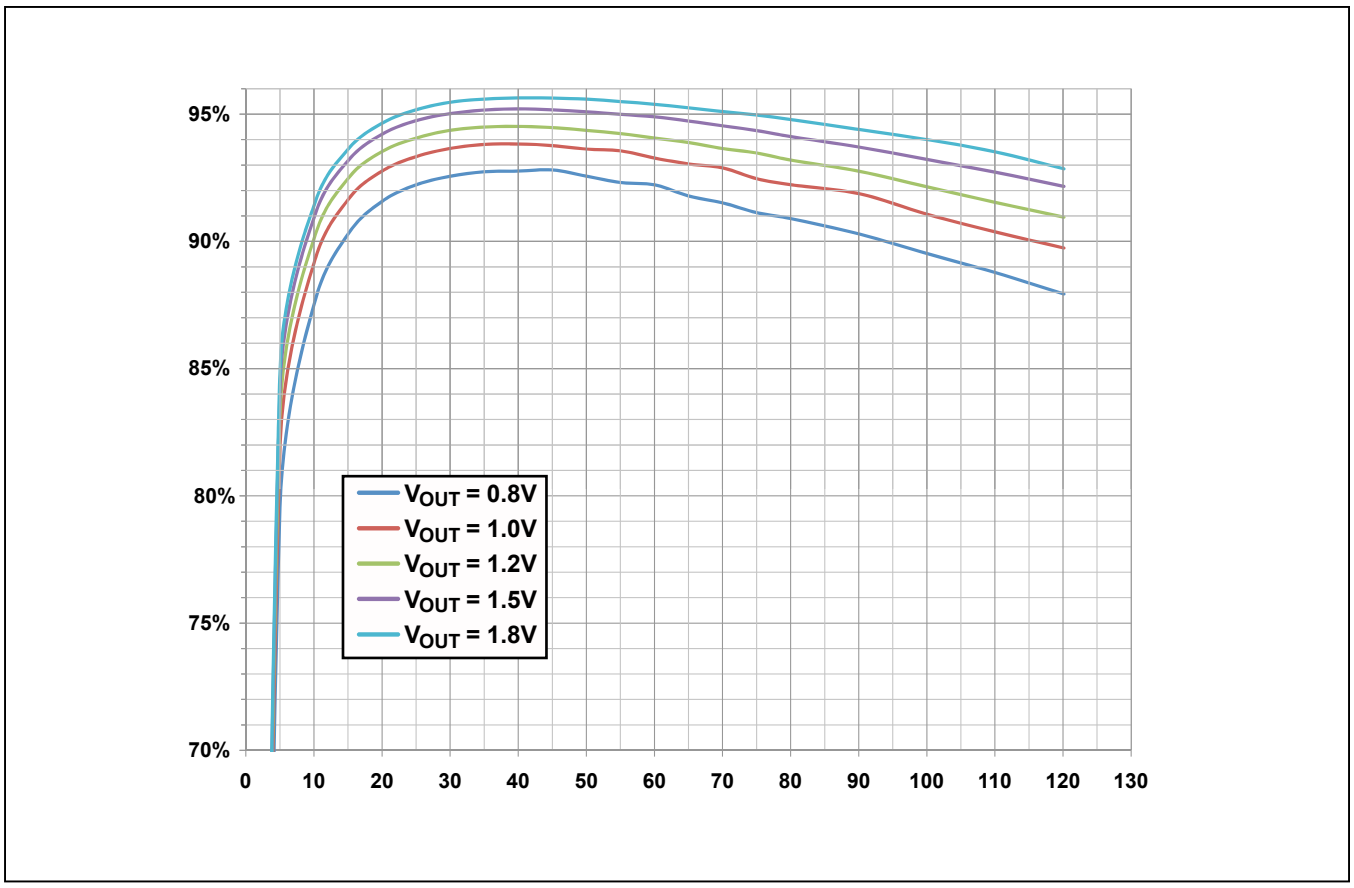


Figure 2. System Efficiency: 4-Phase,100nH/Phase-Coupled Inductors, 350kHz Switching Frequency (V_{IN} = 12V)

Theory of Operation

The MAX20751 master IC provides a high-frequency, highly integrated compact solution for high-performance, low-voltage power conversion (with PMBus interface). The basic system architecture consists of a single-rail master controller and up to four smart-slave devices. These ICs, along with a small number of external components, provide a complete solution for single-rail voltage regulation.

The master IC contains a pulse-width-modulation (PWM) control circuit, PMBus interface, and multiphase control circuits for low-loss operation over a wide range of load currents. The applicable smart-slave ICs utilize the full benefits of a synchronous rectification topology. Both the top and bottom power FETs are integrated on-chip, with no external power components (MOSFETs or Schottky diodes) required. Each smart-slave device contains temperature and current monitoring. PWM signals are generated in the master IC and sent to the slaves. Current-sense and temperature feedback signals are generated in the slaves and sent to the master.

The smart-slave ICs have integrated lossless current-sense technology. This current-sense technology provides accurate current information that is not affected by temperature, process variation, or tolerances of passive elements such as the output inductor, resistors and capacitors, and NTCs used in other systems to extract current information. With this approach, a current-sense signal is fed back to the master as a current instead of a voltage, as is the case with DCR and other forms of current sensing. This allows very robust system feedback of current, with better noise immunity than other methods. The current information can be used to control the load line precisely and in the calculation of real output-power measurements. Highly precise current information removes the challenges of meeting load-line specifications, especially at light load, an area known to challenge DCR current sensing due to the low signal levels and tolerances involved.

The output voltage, output-voltage turn-on slew rate, PMBus address, and PMBus output-current gain are hardware programmable using configuration resistors, as discussed in the *Configuration* section.

An internal integrated switching regulator allows creation of the V_{DD} supply from the V_{DD33} supply, with the addition of an LC filter.

Control Architecture

Figure 3 shows the internal amplifier stages of the master and how phase-current information is used to generate the phase-control signals, as well as provide accurate current reporting. The master IC contains multiple amplifier stages and one duty-cycle modulator for each phase, to allow independent control of the high-side MOSFET on-time according to each individual phase current.

The first amplifier stage (A1) in Figure 3 is a differential amplifier, the output being the error between the DAC reference voltage and the differential voltage-sense lines multiplied by a factor of 2.19. This stage enables true remote voltage sensing, and its differential structure provides high common-mode rejection ratio to protect from any noise present at the processor ground. The second amplifier stage (A2) provides voltage-loop compensation, with its DC gain used to set the load line of the voltage regulator. The A2 amplifier is followed by a clamping circuit and buffer amplifier (A2B) to provide overcurrent protection (OCP). The output of amplifier A2B is converted to a current through the resistor (R_{DES}) and represents the desired total system current (I_{DES}), which sets the target for the current loop. The third amplifier (A3) acts as a current-error amplifier, as it receives the current command (through R_{DES}) and each individual sensed current from the smart-slave ICs (through resistors R_{PH1}, R_{PH2}, and R_{PH3}, as shown in Figure 3. This stage has an integrator connection. The very large DC gain of the A3 stage guarantees that the total load current equals the current command (I_{DES}) in steady state. As a result, the load line of the voltage regulator is set by the gain of the voltage-loop amplifier (A2). Zero load line can be achieved by configuring the amplifier as an integrator by placing capacitor C2 in series with R2, as shown in Figure 3.

The system also offers programmable modulator ramp-rate stability and noise immunity, set by connecting a resistor between the MRAMP pin and ground. This ramp determines the duty-cycle modulator gain and is used to tune the current-loop compensation.

Loop compensation is implemented by adding series or parallel RC networks across the voltage-loop and current-loop amplifiers (A2 and A3), respectively. For the voltage loop, lead compensation can be added by using a series RC network across the R1 resistor, as shown in Figure 3 (RLD_A2 and CLD_A2). Lag compensation can be added by adding a series RC network across the R2-C2 network resistor.

Compensation for the current loop is achieved by placing a series RC network across the current-loop amplifier feedback (R_{INT}-C_{INT}, in Figure 3). This network provides extremely high gain at low frequency, which guarantees tight current regulation (i.e., the output current is very close to the current command).

Integrated 1.8V Switching Regulator

The MAX20751 master IC features an integrated switching regulator that provides the bias current to the master controller and to the smart-slave ICs (both core analog/digital circuits and gate drive).

This regulator enables efficient power conversion from the 3.3V supply at both light load and heavy load using a pulse-frequency-modulation (PFM) mode of operation. The external LC filter for this regulator is extremely small and inexpensive, as it only requires a chip inductor and small case-size ceramic capacitors. The control scheme adopted here is voltage mode constant on-time with the inductor always operated in the discontinuous-conduction mode (DCM) of operation, providing an inherent current-limiting protection as well as soft-start capability. Details of the integrated regulator can be seen in the *Block Diagram*. The PGND pin should connect to the GND pins through a single wide trace or via.

In order to achieve simple average-output current-limiting protection, this converter is forced to stay in DCM mode by only allowing high-side turn-on when the current reaches zero. The peak current in the inductor is given in Equation 1.

Equation 1:

$$I_P = \frac{V_{DD33} - V_{DD}}{L_{PVX}} t_{ON}$$

where:

L_{PVX} is the switcher inductor

The maximum average current is given by Equation 2.

Equation 2:

$$I_{MAX_AVE} = \frac{V_{DD33} - V_{DD}}{2L_{PVX}} t_{ON}$$

If load current is higher than IMAX_AVE, the V_{DD} voltage drops. If V_{DD} drops below the falling UVLO threshold, the device resets.

The on-time (t_{ON}) is programmable using the PMBus. Table 1 shows the programmable on-times. Before V_{DD} has risen above the rising undervoltage-lockout (UVLO) threshold, the lowest on-time of 0.64µs is used. When V_{DD} has risen above both the rising and falling UVLO thresholds, the switcher uses the programmed on-time. The default value is 1.30µs.

The switcher becomes active when V_{DD33} voltage has risen above its rising UVLO threshold.

The inductor (L_{PVX}) must be able to support the maximum peak current without saturating significantly, since the inductor impedance is what provides the current limit. The maximum peak current occurs at startup from zero output voltage.

The output-voltage peak-to-peak ripple depends on the capacitor (C_{VDD}). The worst-case ripple occurs at light load and is given in Equation 3.

Equation 3:

$$\Delta V_{P-P} = \frac{I_P}{2C_{VDD}} \times \frac{V_{DD33}}{V_{DD}} t_{ON}$$

where:

ΔV_{P-P} should be 30mV or less

Table 1. On-Time Selection Table

ON-TIME (µs)	0.64	1.30 (Default)	1.91	2.76

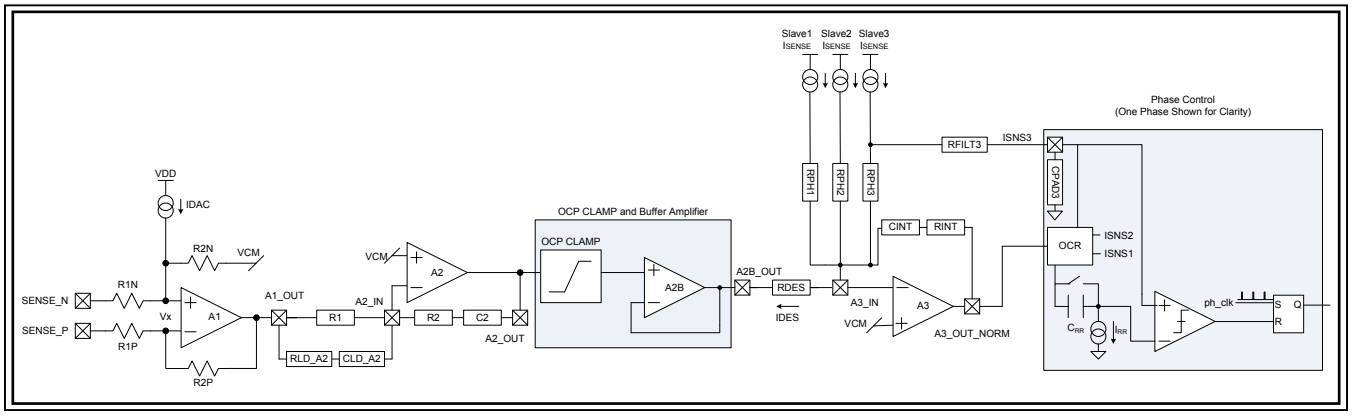


Figure 3. Control Architecture

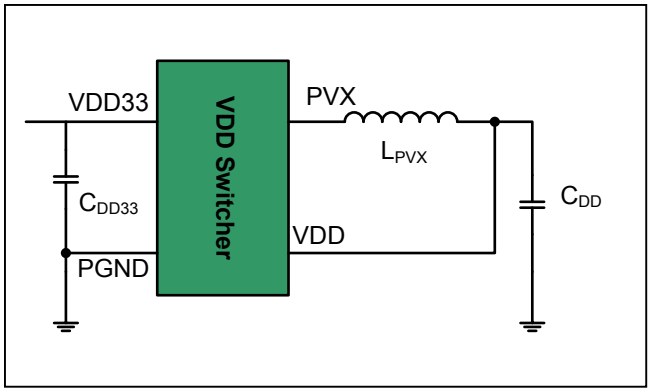


Figure 4. Integrated Switcher Circuit

The control method regulates the valley voltage. The peak voltage is the valley voltage plus the peak-to-peak ripple voltage.

The current from the V_{DD33} supply occurs in pulses of charge given by Equation 4.

Equation 4:

$$Q_{VDD33} = \frac{I_P}{2} t_{ON}$$

where:

I_P is the peak current

Capacitor C_{DD33} at the V_{DD33} pin should be chosen to supply the peak current and charge without too much voltage change. A ceramic capacitor of at least 10µF is recommended.

To estimate the V_{DD33} current using the integrated switching regulator, assume a minimum efficiency of 80% for the integrated switching regulator. For example, if the maximum total master and slave IC current from V_{DD} is 175mA, V_{DD} = 1.9V, and V_{DD33} = 3.3V, then the V_{DD33} current for the integrated switching regulator is (175mA x 1.9V)/(3.3V x 0.80) = 126mA.

To estimate the total V_{DD33} current, also include the PMBus resistor pulldown current if operated from V_{DD33}. For example, if 2.15kΩ pulldown resistors are used from the PMC, PMD, and ALERTB pins to V_{DD33}, then the maximum PMBus current is 3 x 3.3V/2.15kΩ = 4.6mA. Therefore, the total V_{DD33} current for the integrated switching regulator and PMBus is, approximately, 131mA.

The integrated switching regulator can be disabled by removing LPVX and connecting a 10Ω resistor from PVX to V_{DD33}. An external supply is then applied to V_{DD}.

Startup and Shutdown Operation

When VDD and VDD33 are above their rising UVLO thresholds, the device is enabled and goes through an initialization and phase-detection procedure. Configuration resistors are read and external resistors checked for valid values. Any faults will prevent the output voltage from turning on.

The PMBus communication and telemetry are then enabled. The VIN_UV voltage must be above its rising UVLO threshold for the output voltage to turn on.

If the output voltage is programmed to below 0.25V through the PMBus VOUT_COMMAND, the output is disabled. Programming the output voltage to any other allowable voltage using the PMBus VOUT_COMMAND allows the output voltage to turn on.

Depending on how the voltage-regulation enable is configured, a VR_en signal from VR_ON and/or the PMBus OPERATION command may also be required for the output voltage to turn on. The default configuration for the VR_en signal is the VR_ON signal at the high logic level, with no PMBus command needed.

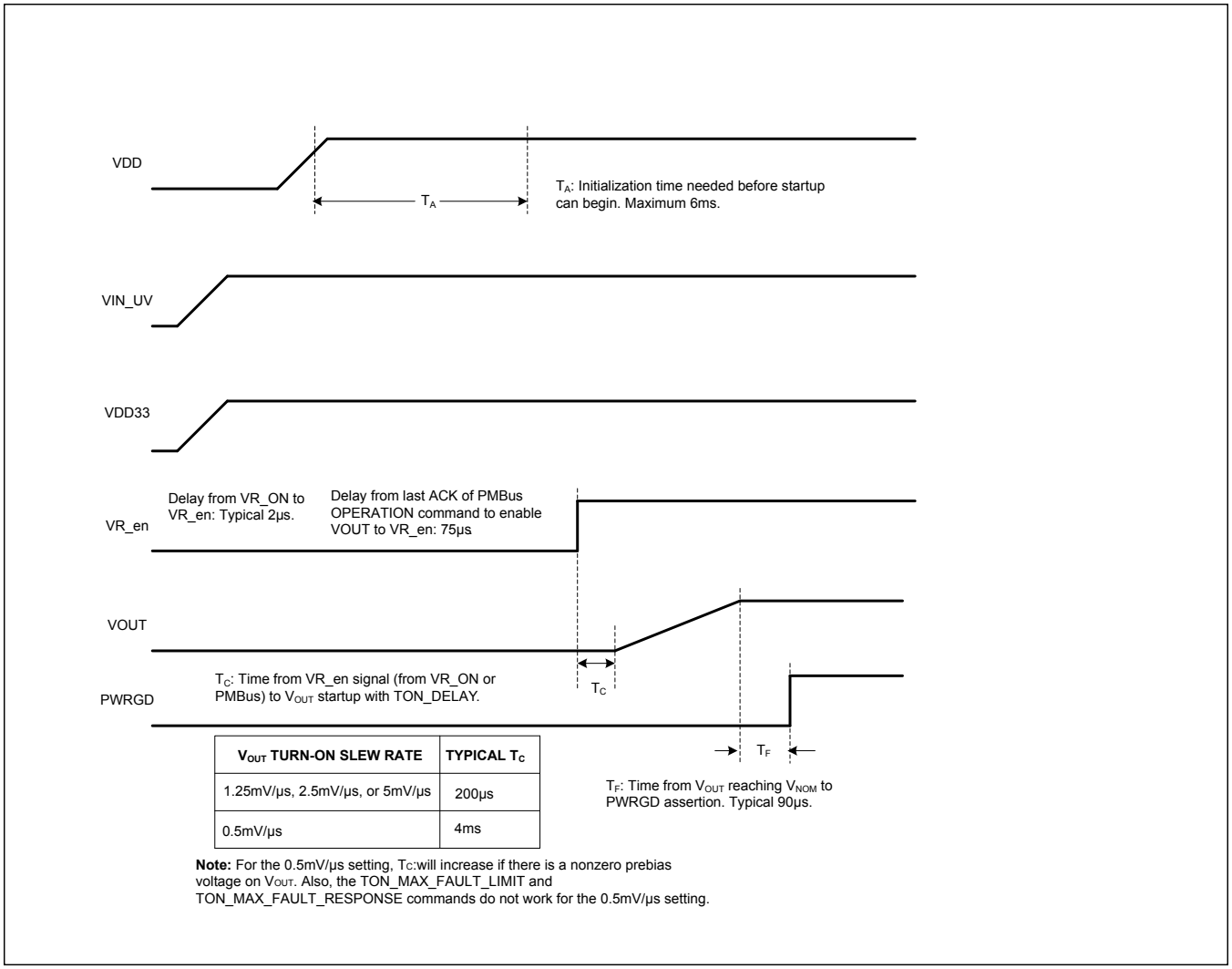
When the VIN_UV voltage is above its rising UVLO threshold and the proper VR_en signal, if required, has occurred, the output voltage turns on after the PMBus programmable TON_DELAY time. The default TON_DELAY time is 0ms.

After the output voltage has reached its nominal value, the PWRGD signal is asserted.

The startup sequence caused by VR_ON going high is shown in Figure 5.

When shutdown occurs, the master IC causes the VX nodes of the slaves to stop switching, which then causes the output voltage to turn off. The PWRGD signal is deasserted and is actively pulled low.

Depending on how the voltage-regulation enable is configured, the output voltage can be turned off using the VR_en signal from VR_ON and/or the PMBus OPERATION command. Depending on the PMBus configuration, the output turns off immediately or with sequencing. When the output turns off with sequencing, there is a delay time determined by the PMBus programmable TOFF_DELAY command and then V_{OUT} ramps down with a turn-off slew rate that is the same as the turn-on slew rate for turn-on slew rates of 1.25mV/µs, 2.5mV/µs, and 5mv/µs. For turn-on slew rate 0.5mV/µs, if sequencing is used, the delay time is followed by an immediate turn-off (no slew rate-controlled V_{OUT} ramp-down). The default TOFF_DELAY time is 0ms. Note that when V_{OUT} ramps down, energy



V_{OUT} TURN-ON SLEW RATE	TYPICAL T_C
1.25mV/µs, 2.5mV/µs, or 5mV/µs	200µs
0.5mV/µs	4ms

Note: For the 0.5mV/µs setting, T_C:will increase if there is a nonzero prebias voltage on V_{OUT}. Also, the TON_MAX_FAULT_LIMIT and TON_MAX_FAULT_RESPONSE commands do not work for the 0.5mV/µs setting.

Figure 5. Startup Sequence

may be delivered from V_{OUT} to V_{IN}. The V_{IN} capacitors should be sized to absorb this energy to prevent a large increase in the V_{IN} voltage.

The output voltage can be turned off by programming the output voltage below 0.25V using the PMBus VOUT_COMMAND. The turn-off in this case is also determined by the PMBus configuration.

If the V_{DD} or V_{DD33} supplies go below their falling UVLO thresholds, the output voltage is turned off and the system is reset.

The output voltage can be turned off by the VIN_UV voltage going below the VIN_UV falling UVLO threshold. This is logged as a hardware fault.

The VIN_UV UVLO thresholds should be higher than the corresponding smart-slave IC's V_{DDH} UVLO thresholds to prevent a slave fault from occurring, which could potentially prevent the output voltage from turning back on. If this occurs, the system may need to be reset by bringing the V_{DD} or V_{DD33} supplies below their falling UVLO thresholds.

The shutdown sequence caused by VR_ON going low is shown in Figure 6.

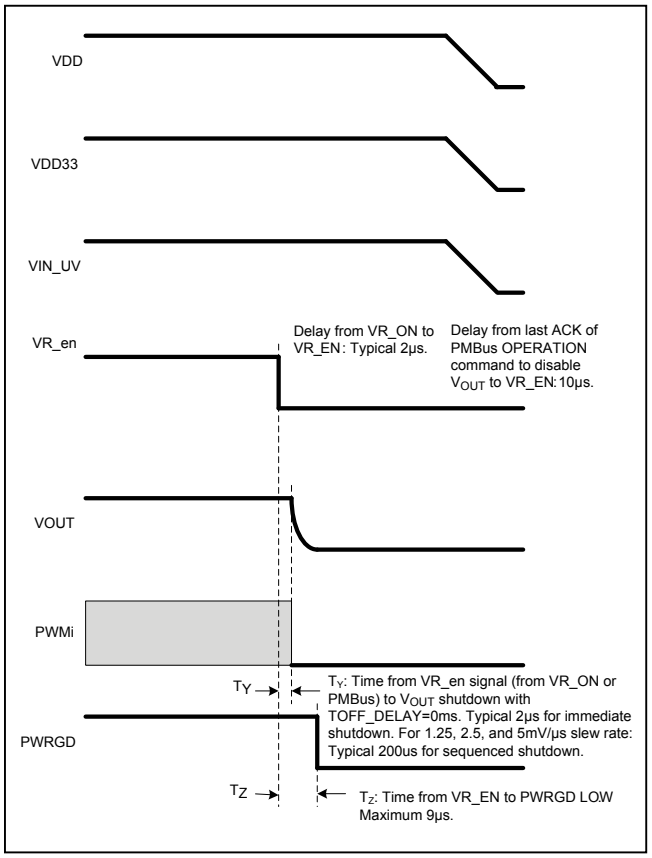


Figure 6. Shutdown Sequence

Droop and Load-Line Regulation

If the A2 amplifier series R2-C2 network is replaced by resistor R2 only, the MAX20751 provides accurate output load line over the entire range of output currents. The load line is set by the combination of the R1, R2, and R_{DES} resistors.

Switching Frequency and Output-Voltage Turn-On Slew Rate

The switching frequency and output voltage turn-on slew rate are programmable using configuration resistors. See the *Configuration* section. They are also programmable using the PMBus.

Orthogonal Current Rebalancing (OCR)

Phase-current imbalance can occur due to high-frequency loading transients. The purpose of the OCR circuit is to reduce phase-current imbalance.

This is accomplished by modifying the output of the A3 amplifier for each individual phase (k). Instead of the A3 amplifier output voltage being fed directly to the PWM comparator of a phase, a control voltage (V_{Ck}) is used. The equation for V_{Ck} is given in Equation 5.

Equation 5:

$$V_{Ck} = V_{O3} - G_{OCR}\left(V_{RPHk} - \frac{1}{N}\sum_{i=1}^{N} V_{RPHi}\right)$$

where:

V_{RPHk} = Voltage on resistor RPHk (a voltage proportional to the current in phase k)

V_{O3} = A3_OUT_NORM voltage

N = Total number of phases

G_{OCR} = Gain of the OCR circuit

V_{Ck} = Voltage fed to the phase k PWM comparator instead of the A3 amplifier output voltage

The difference between the current of a phase k from the average current (with some gain G_{OCR}) is subtracted from V_{O3} to determine the control voltage (V_{Ck}). If the current in any phase is greater than the average of all the phases, then the corresponding V_{Ck} voltage will be less than V_{O3} and the subsequent PWM pulse for that phase shorter, thus preventing further phase-current imbalance.

The default gain (G_{OCR}) is 1.8.

Input Voltage Undervoltage Lockout (UVLO) Using the VIN_UV Pin

The VIN_UV pin on the master IC is connected to the middle point of a voltage-divider from the slave V_{DDH} (power input rail) to ground. This pin provides an externally programmable input supply UVLO and sensing for the PMBus V_{IN} telemetry.

The UVLO function is provided by comparing the VIN_UV voltage to internal references with a comparator. When the V_{IN_UVLO} voltage exceeds the rising threshold, the system is allowed to operate and the falling reference voltage is then used as a disable point for built-in hysteresis. See the *Electrical Characteristics* table for more details.

Figure 7 shows the VIN_UV circuit. Resistors R_{IN} and R_{GND} form a voltage-divider that scales the V_{IN} voltage to the VIN_UV pin. The scale factor (VIN_RATIO) is given by Equation 6. VIN_RATIO is programmable using the PMBus. The default value is (140/2048) = 0.06836.

Equation 6:

$$VIN_RATIO = \frac{R_{GND}}{R_{GND} + R_{IN}}$$

$R_{GND}||R_{IN}$ should be approximately 2kΩ with capacitor C_{IN_UV} = 100pF. It is suggested to use 1% tolerance resistors with the values R_{GND} = 2.15kΩ and R_{IN} = 29.4kΩ. The value for VIN_RATIO should be less than or equal to 140/2048.

Phase Population Order

Depending on the total number of phases in the system, specific phase positions must be populated, while the others must be deactivated by connecting a 0Ω resistor between the MAX20751's phase-control pins (PWMk) of the inactive phases and ground (Table 2).

The phase number is defined by the PWMx pin name (e.g., phase 2 is driven by PWM2).

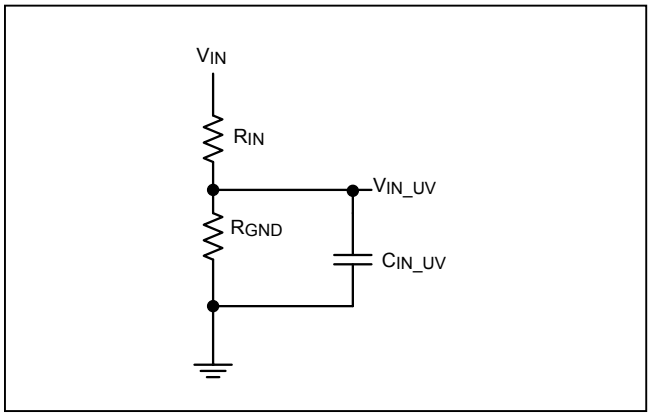


Figure 7. VIN_UV Pin Voltage-Divider Circuit

Table 2. Phase Population Positions

NUMBER OF POPULATED PHASES	POSITIONS TO BE POPULATED (BY FIRING SEQUENCE)
1	2
2	2, 1
3	2, 1, 3
4	2, 4, 1, 3

For example, for 2-phase operation, only phases 2 and 1 are used; therefore, pins PWM4 and PWM3 should each be connected to GND with 0Ω resistors.

For 3-phase operation, PWM4 should be connected to GND with a 0Ω resistor. For single-phase operation PWM4, PWM3, and PWM1 should each be connected to GND with 0Ω resistors.

If the wrong PWMk pins are connected to GND with 0Ω resistors, a configuration fault occurs in the fault-checking procedure (occurring prior to V_{OUT} startup) and operation is halted.

Protection And Monitoring

The master IC includes multiple protection circuits to protect the regulator and load, and to monitor the output voltage, as described in the following sections.

Fault Detection when V_{DD} and V_{DD33} are Initially Applied

When V_{DD} and V_{DD33} are initially applied and at their proper levels, the master IC checks the following resistor values and connections and if detected as being outside the correct range or open, an error is flagged and the regulator will not start regulation:

- R_{MRAMP}
- R_{REF}
- SENSE_P Open

PWRGD (Power-Good) Pin

The PWRGD output (different from the PMBus POWER_GOOD signal) is an active-high, open-drain output used to show that the output is settled at its commanded voltage. The output goes high after a fixed delay, after the end of the output-voltage startup transition, assuming the output voltage is above the PWRGD threshold. It is deasserted when any of the following occurs:

- The output voltage drops below the threshold, relative to the nominal voltage, for any reason.
- An OVP fault is detected.
- An OCP fault is detected when the mode is set to hiccup mode and the regulator shuts down the output voltage during the shutdown part of the hiccup cycle. In constant current-limit mode, the PWRGD signal is based on the PWRGD voltage threshold only.
- The output is disabled.

Overcurrent Protection (OCP)

System OCP is based on a fixed voltage threshold for the voltage across the R_{DES} resistor. The overcurrent threshold is therefore set by selecting an appropriate value of R_{DES} for the design. The voltage threshold is scaled internally, depending on the number of active phases (i.e., the voltage threshold is a fixed per-phase value).

The OCP trips when the peak voltage over RDES reaches the inception value and remains tripped down to the nominal/sustaining value (i.e., the values shown are the sustaining currents and not the inception point, which is 5% higher). Negative (sinking) OCP is automatically set to 30% of the positive value.

The OCP is based on the instantaneous voltage over RDES, and a small ripple voltage reflecting the output-voltage ripple may be present. If the instantaneous commanded current (output of amplifier A2) reaches the inception voltage, the commanded current is immediately clamped to the sustaining value. If the commanded current drops below the sustaining value, it must once again reach the inception point before clamping commences.

An overcurrent fault is logged in the fault log if clamping continues for 5ms, to ensure that only periods of continuous overloads are recorded as faults.

Table 3. Master Faults

MAX20751 PROTECTION	MAX20751 OUTPUT SIGNAL(S) SHOWING FAULT	SYSTEM SHUTDOWN	SYSTEM LATCHED OFF?	LOGGED IN FAULT LOG?
Resistor Out-of-Range Detected at Startup	PWRGD low	System does not start	Yes	Yes
OCP: Hiccup or CCM	PWRGD low (if output drops below threshold)	No	No	Yes (after 5ms)
Fixed (Umbrella) or Tracking OVP	PWRGD low	Yes	Yes	Yes
VIN_UV UVLO	PWRGD low (if output drops below threshold)	Yes	No	Yes
Output Undervoltage	PWRGD low	No	No	No
V_{DD} UVLO	PWRGD low	Yes	No (system in reset)	No
V_{DD33} UVLO	PWRGD low	Yes	No (system in reset)	No

Table 4. Effects of Slave Faults

SLAVE FAULT	MAX20751 OUTPUT SIGNAL SHOWING FAULT	SYSTEM SHUTDOWN	SYSTEM LATCHED OFF*	LOGGED IN FAULT LOG
Slave Cycle-by-Cycle OCP (Sinking or Sourcing Current)	None	No	No	Yes
Slave Sourcing OCP Current Shutdown	PWRGD low	Yes	Yes (through slave)	Yes
Slave OTP Shutdown (Sent to Master through Slave TS_FAULTB Low)	PWRGD low	Yes	Yes (through slave)	Yes
Slave Boost UVLO (Undervoltage Lockout on Boost Supply)	PWRGD low	Yes	No	Yes
Slave VX Short-to-Ground or V_{DDH}	PWRGD low	Yes	Yes (through slave)	Yes

***Note:** "Yes (through slave)" refers to the fact that the slave latches in this condition and therefore the system latches. Once the slave fault is cleared by cycling its power, the system can restart. This table shows the effect on the system.*

Three modes of operation are provided for positive (sourcing) OCP: shutdown, constant current, and hiccup (default); negative OCP is always constant current. The mode can be changed using PMBus commands. If hiccup OCP mode is selected, when the OCP is exceeded, the system will deliver the maximum programmed sustaining current for 5ms before shutting down and waiting 45ms before restarting. This cycling continues until the commanded current falls below the programmed value. Should constant-current mode be selected, the system tries to regulate at the OCP sustaining current until the commanded current falls below the sustaining value. The upper threshold of current delivery is the OCP inception point and, once this level is reached, the system folds back to the sustaining level (the programmed value) to deliver constant current indefinitely. The shutdown mode is similar to the constant-current mode but shuts down VOUT after 5ms. The VOUT voltage can be enabled again by using the VR_ON signal and/or the OPERATION PMBus command.

Overvoltage Protection (OVP)

Two separate OVP circuits are included, one based on the programmed nominal output voltage, the other on an "umbrella" fixed value. If either is tripped, an OVP fault is recorded, PWRGD is deasserted, and the system stops regulating. OVP faults can only be cleared by toggling the V_{DD} or V_{DD33} supply rail.

Undervoltage Lockout

The master IC includes three UVLO circuits, V_{DD} rail, V_{DD33} rail and V_{DDH} (i.e., V_{IN}). V_{IN} is monitored through an external resistor-divider to bring the voltage down to within the operating range of the VIN_UV pin. If a V_{IN} UVLO is detected, the system stops regulating and indicates an input-voltage fault. Once the input voltage rises above the rising threshold, the IC reinitiates and follows the same startup procedure as if enabled by VR_ON.

Configuration

Determining the Optimum Number of Phases, I_{OUTMAX}, and Overcurrent Protection

The typical starting point for a voltage-regulator design is to choose a value of maximum output current (I_{OUTMAX}). The value of I_{OUTMAX} is determined by the MAX20751 system overcurrent-protection (OCP) setting and is set to 85% of this setting. Therefore, a target minimum system OCP rating can easily be determined based on I_{OUTMAX}. Once this value is known, the area available, smart-slave part numbers to be used, and the desired performance

Table 5. Selection of R_{DES} for Overcurrent Limit and Maximum Output Current I_{OUTMAX} = 0.85 I_{OCP}

1-PHASE OCP (A)	2-PHASE OCP (A)	3-PHASE OCP (A)	4-PHASE OCP (A)	R_{DES} (Ω)
25	50	75	100	604
27.3	54.7	82	109.3	549
29.7	59.3	89	118.6	511
32	64	96	128	464
34.3	68.6	103	137.3	432
36.7	73.3	110	146.6	412
39	78	116.9	155.9	383
41.3	82.6	123.9	165.2	365
43.6	87.3	130.9	174.6	340
46	91.9	137.9	183.9	324
48.3	96.6	144.9	193.2	309
50.6	101.3	151.9	202.5	294
53	105.9	158.9	211.8	280
55.3	110.6	165.9	221.2	274
57.6	115.2	172.9	230.5	261
60	119.9	179.9	239.8	249

versus cost should all be considered, with the number of phases and smart-slave devices determined. Efficiency curves and ratings shown on the respective smart-slave data sheets can be used for this purpose. If any phases aren't used, their corresponding PWMx pins should be connected to GND with 0Ω resistors, as discussed in the *Phase Population Order* section.

Selecting R_{DES}

With the number of phases and part numbers known, R_{DES} should be selected to give the correct overcurrent-protection (OCP) value. The OCP value is set by R_{DES}, in that the master IC uses a fixed value of 150mV per phase. Since R_{DES} is also used by

Table 6. Using R_SEL3 to Set the V_{OUT} Slew Rate and Switching Frequency

V_{OUT} SLEW RATE (V/ms)	f_{SW} (kHz)	R_SEL3 (Ω)
1.25	300	0
	350	17.8
	400	33.2
	450	48.7
	500	64.9
	600	80.6
	700	95.3
	800	115
2.5	300	133
	350	154
	400	178
	450	200
	500	226
	600	249
	700	274
	800	301
5	300	332
	350	365
	400	402
	450	432
	500	464
	600	499
	700	536
	800	576
0.5	300	619
	350	665
	400	715
	450	768
	500	825
	600	887
	700	953
	800	1020

the PMBus telemetry circuitry to measure the output current (I_{OUT}), the value of R_{DES} must be selected from Table 5 of standard 1% resistors.

For example, if an I_{OUTMAX} of 170A is required, I_{OCP} must be a minimum of 170/0.85 = 200A. If a 4-phase design has been selected, looking in the 4-Phase OCP column, we see the next highest value for I_{OCP} is 202.5A and requires the use of R_{DES} with a value of 294Ω, which gives a nominal reported I_{OUTMAX} of 0.85 x 202.5 = 172A (I_{OUTMAX} is rounded to an integer value). Care should be taken with tolerance and rounding to ensure that the required I_{OUTMAX} is met.

Using Configuration Resistors to Program the Output-Voltage Slew Rate and Switching Frequency

R_SEL3 is used to set the output-voltage slew rate and switching frequency. Table 6 shows the output-voltage slew rates, switching frequencies, and corresponding values for R_SEL3.

R_SEL3 has 32 possible values, with each value corresponding to a distinct pairing of slew rate and switching frequency.

For example, to choose an output-voltage slew rate of 0.5V/ms and a switching frequency of 350kHz, R_SEL3 = 665Ω.

Using Configuration Resistors to Program the Output Voltage, PMBus Address Lowest 3 Bits, and I_{OUT} Telemetry for the R_{DES} Value Being Used

Table 7 shows the parameter values and corresponding configuration resistor values used to program the output voltage, PMBus address lowest 3 bits (PMAD[3:1]), and PMBus I_{OUT} telemetry circuitry with the R_{DES} value used in the overcurrent-limit circuit.

R_SEL2 and R_SEL1 are the configuration resistors used to set the output voltage. The output voltage is the sum of the two voltages chosen by R_SEL2 and R_SEL1.

R_SEL1 and R_SEL0 are the configuration resistors used to set the lowest 3 bits (PMAD[3:1]) of the entire PMBus address (PMAD[7:1]). The upper 4 bits (PMAD[7:4]) are constant at the value 1110b.

R_SEL0 is the configuration resistor used to program the PMBus I_{OUT} telemetry circuitry with the R_{DES} value being used in the overcurrent-limit circuit.

Table 7. Using R_SEL2, R_SEL1, and R_SEL0 to Set the Output Voltage, Set the Lowest PMBus Address Bits, and Program the I_{OUT} Telemetry with the R_{DES} Value Being Used

V_{OUT} (V)	R_SEL2 (Ω)	PMAD [2:1]	V_{OUT} (V)	R_SEL1 (Ω)	PMAD3	R_{DES} (Ω)	R_SEL0 (Ω)
	0	00	-0.005	0	0	604	0
	17.8		0.000	17.8		549	17.8
	33.2		0.005	33.2		511	33.2
	48.7		0.010	48.7		464	48.7
	64.9		0.015	64.9		432	64.9
	80.6		0.020	80.6		412	80.6
0.490	95.3		0.025	95.3		383	95.3
0.530	115		0.030	115		365	115
0.570	133	01	-0.005	133		340	133
0.610	154		0.000	154		324	154
0.650	178		0.005	178		309	178
0.690	200		0.010	200		294	200
0.730	226		0.015	226		280	226
0.770	249		0.020	249		274	249
0.810	274		0.025	274		261	274
0.850	301		0.030	301		249	301
0.890	332	10	-0.005	332	1	604	332
0.930	365		0.000	365		549	365
0.970	402		0.005	402		511	402
1.010	432		0.010	432		464	432
1.050	464		0.015	464		432	464
1.090	499		0.020	499		412	499
1.130	536		0.025	536		383	536
1.170	576		0.030	576		365	576
1.210	619	11	-0.005	619		340	619
1.250	665		0.000	665		324	665
1.290	715		0.005	715		309	715
1.330	768		0.010	768		294	768
1.370	825		0.015	825		280	825
1.410	887		0.020	887		274	887
1.450	953		0.025	953		261	953
1.490	1020		0.030	1020		249	1020

Note 1: Selecting V_{OUT} below 0.25V disables the output voltage.
Note 2: R_{DES} defines I_{OCP}, I_{OUTMAX}, and the I_{OUT} PMBus telemetry.

Each R_SELx resistor has 32 possible values, with each value corresponding to one or more programmable parameters.

For example, to program 1.000V output voltage, PMAD[3:1] = 011b, and R_{DES} = 294Ω, use:

R_SEL2 = 402Ω (0.970V),

R_SEL1 = 1020Ω (PMAD[2:1] = 11b, 0.030V),

R_SEL0 = 200Ω (PMAD3 = 0b, R_{DES} = 294Ω)

This results in the output voltage = 0.970V + 0.030V = 1.000V, PMAD[3:1] = 011b, and R_{DES} = 294Ω.

The output voltage can also be programmed using the PMBus. Note that the output voltage is disabled if it is set below 0.25V through the PMBus.

Inductor Phase-Current Ripple

For coupled inductors, the inductor peak-to-peak phase-current ripple can be calculated from Equation 7 (which assumes perfect coupling for coupled inductors, and duty cycle ≤ 1/N).

Equation 7:

$$I_{PHPP} = \frac{V_{OUT}}{f_{SW}L}\left(\frac{1}{n_{CW}} - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

I_{PHPP} = Peak-to-peak phase-current ripple in the inductor

f_{SW} = Switching frequency

L = Inductance per phase

n_{CW} = Number of coupled windings

V_{IN} = Input voltage

V_{OUT} = Output voltage

In practice, the coupling will not be perfect, but good coupling can be achieved, with the actual ripple current close to what is calculated by the equation.

The output current ripple is given by Equation 8, assuming duty cycle ≤ 1/N.

Equation 8:

$$I_{PP} = \frac{V_{OUT}}{f_{SW}L}\left(\frac{1}{N} - \frac{V_{OUT}}{V_{IN}}\right)N$$

where:

I_{PP} = Peak-to-peak output-current ripple

L = Inductance per phase

N = Number of phases

Output Capacitance Calculation

One criterion for determining the value of the output capacitance (C_{OUT}) is the maximum allowable output-voltage overshoot (ΔV_{OST}) during unloading transients. For a maximum unloading current step (ΔI) and maximum allowed output-voltage overshoot change (ΔV_{OST}), the required output capacitance is given by Equation 9.

Equation 9:

$$C_{OUT} \geq \frac{(\Delta I)^2 \frac{L}{N}}{2(\Delta V_{OST})V_{OUT}}$$

where:

L = Inductance per phase

N = Number of phases

V_{OUT} = Nominal output voltage

For example, in a case where allowable overshoot is the limiting factor for a 3-phase system with 250nH of inductance per phase, 1.0V output, maximum current step of 50A, and maximum allowable overshoot of 100mV, the minimum C_{OUT} theoretically required is 1042µF. Selecting a higher value gives good design margin against component variation and effective capacitance loss due to voltage bias.

Bleed Resistor

A small bleed resistor of approximately 100Ω should be connected between the output of the regulator and ground to ensure that the output capacitors are discharged shortly after the output is disabled. The resistor should be sized so that when the maximum expected output voltage is applied, the resistor's power dissipation is sufficiently below its rated power dissipation.

Droop and No-Droop Operation

The device provides accurate output-droop resistance over the entire range of output currents. The R_{DROOP} is set by the combination of the R1, R2, and R_{DES} resistors, according to Equation 10.

Equation 10:

$$R_{DROOP} = \frac{R_1 R_{DES}}{R_2 2.19 A_I}$$

where:

A_I = Slave current gain factor

R1 = Having a typical value of 600 to 800. The R2/R1 should be a minimum of 0.45

If $R_2/R_1 < 1$, then R_1 should be between 600Ω and 800Ω, R_2 should be 353Ω, minimum, and the ratio of R2/R1 should be 0.45, minimum.

If $R_2/R_1 > 1$, then R_1 should be between 400Ω and 800Ω. R_2 should be 400Ω, minimum.

No-droop operation can be achieved by adding capacitor C2 in series with R_2 in the A2 stage, according to Equation 11.

Equation 11:

$$C2 \geq \frac{\sqrt{\frac{L}{N}C_{OUT}}}{R_2}$$

Above the frequency (Equation 12), the voltage-regulator impedance approaches R_{DROOP}.

Equation 12:

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

With either the droop or no-droop configuration, above the frequency (Equation 13).

Equation 13:

$$f_{ZINT} = \frac{1}{2\pi\left(R_{INT} + \frac{R_{PH}}{N}\right)C_{INT}}$$

where:

N = Number of phases

The voltage-regulator impedance approaches:

$$R_{DROOP}\left(\frac{R_{INT} + \frac{R_{PH}}{N}}{R_{INT}}\right)$$

up to the voltage-loop bandwidth, unless the lead network is used.

R_{FILT} Selection

The R_{FILT} resistor, together with the capacitance at the ISENSE pin, creates a lowpass filter for the sensed smart-slave phase-current signal. A 3.01kΩ resistor should be used for R_{FILT}.

Selecting the Modulator Ramp Rate

The modulator ramp rate is set using external resistor R_{MRAMP} from the MRAMP pin to GND.

The ramp rate (S_{RAMP}) can be determined from the switching frequency (f_{SW}), steady-state ramp voltage (V_{RAMPD}), and duty cycle ($D = V_{OUT}/V_{IN}$), according to Equation 14.

Equation 14:

$$S_{RAMP} = \frac{V_{RAMPD}}{D} f_{SW}$$

The V_{RAMPD} voltage typically ranges from 100mV to 300mV. Note that V_{RAMPD} changes with D, while S_{RAMP} remains constant.

A smaller S_{RAMP} provides a larger-loop bandwidth for the total inductor current (see the *Loop Bandwidths* section). Once a ramp-rate value has been determined, the value of the resistor can be calculated using Equation 15.

Equation 15:

$$R_{MRAMP} = \frac{23.81}{S_{RAMP}}$$

where:

R_{MRAMP} is in kΩ

S_{RAMP} is in V/µs

Example: If the required ramp rate = 1.0V/µs, then R_{MRAMP} = 23.81kΩ, and the closest 1% value is 23.7kΩ.

R_{INT} Selection

Set R_{INT} according to Equation 16.

Equation 16:

For single phase:

$$R_{INT} < \frac{\left(V_{DD_MIN}\text{-}0.2V\text{-}V_{CM}\right)}{\left(\frac{0.15V}{R_{DES}}N + \frac{I_{PP}}{A_I}\right)}$$

For 2 or more phases:

$$R_{INT} < MIN\left[\frac{\left(V_{DD_MIN}\text{-}0.2V\text{-}V_{CM}\right)}{\left(\frac{0.15V}{R_{DES}}N + \frac{I_{PP}}{A_I}\right)}, 3R_{DES}\right]$$

where:

V_{DD_MIN} = Minimum V_{DD} voltage used in the application

V_{CM} = Compensation circuit common-mode voltage = 0.85V

R_{DES} = Resistor used to set the I_{OCP} value

I_{PP} = Peak-to-peak ripple of the output current

A_I = Save current-gain factor

Note that a larger R_{INT} provides a larger-loop bandwidth for the total inductor current (see the *Loop Bandwidths* section).

R_{PH} Selection

Each of the Maxim slave's current-sense pins is connected to the A3_IN pin of the master IC through its phase resistor (R_{PHk}). The value of each phase resistor determines the amplitude of the phase current-sense signal, which must be below 0.4V at all times, up to and including the overcurrent limit.

To help prevent phase-current imbalance due to load transients, set according to Equation 17.

Equation 17:

$$R_{PH} \geq \frac{R_{INT}}{(G_{OCR} + 1)}$$

where:

G_{OCR} = Gain of the OCR circuit

Current Steering

The phase-current-balancing circuitry works to keep the voltages across the R_{PH} resistors approximately equal. By increasing the R_{PH} resistor from the nominal value on a particular phase, the steady-state current in that phase can be reduced with respect to the other phases. This may be useful in reducing the temperature on the smart-slave device and inductor of that phase, if they tend to get hotter than the corresponding components of the other phases when the phase currents are all equal. Care should be taken so the inductors of the other phases do not saturate because of too much current; with coupled inductors, the relative balance of phase currents is also important.

C_{INT} Value

C_{INT} should be selected to match the time constant of the double pole, which is intrinsic in the buck-converter duty cycle-to-output transfer function given by Equation 19.

Equation 19:

$$C_{INT} \geq \frac{\sqrt{\frac{L}{N} C_{OUT}}}{\left(R_{INT} + \frac{R_{PH}}{N}\right)}$$

Loop Bandwidths

The output-voltage loop bandwidth is given by Equation 20 (if the lead network is not used).

Equation 20:

$$BW_{VL} = \frac{1}{2\pi R_{DROOP} \left(\frac{R_{INT} + \frac{R_{PH}}{N}}{R_{INT}}\right) C_{OUT}}$$

If the lead network is used, the output-voltage loop bandwidth and phase margin can be increased.

The loop bandwidth for the total inductor current is given by Equation 21.

Equation 21:

$$BW_{IL} < \frac{V_{INT} f_{SW}}{S_{RAMP}} \frac{N}{2\pi L} \frac{\left(R_{INT} + \frac{R_{PH}}{N}\right)}{A_I}$$

where:

L = Inductance per phase

A_I = Slave current gain factor

The loop bandwidths should meet the conditions given by Equation 22.

Equation 22:

$$BW_{VL} < BW_{IL} \quad \text{(by at least 50kHz difference)}$$

$$BW_{VL} < \frac{f_{SW}}{4}$$

Note: If $BW_{VL} < BW_{IL}$ + 50kHz cannot be met, additional phase margin can be added with the lead network.

Increasing V_{OUT} Using Resistor Voltage-Divider Feedback

To obtain a V_{OUT} value above the maximum V_{NOM} value, a resistor voltage-divider feedback circuit can be used, as shown in Figure 8. The equations for choosing R_{VO_SP}, R_{SP_GND}, and R_{SN} are as follows:

$$\frac{R_{VO_SP}}{R_{SP_GND}} = \frac{V_{OUT}}{V_{NOM}} - 1$$

$$R_{SN} = \frac{R_{VO_SP} R_{SP_GND}}{R_{VO_SP} + R_{SP_GND}}$$

Choose $R_{SN} \leq 150\Omega$, then:

$$R_{VO_SP} = \frac{V_{OUT}}{V_{NOM}} R_{SN}$$

$$R_{SP_GND} = \frac{R_{VO_SP}}{\left(\frac{V_{OUT}}{V_{NOM}} - 1\right)}$$

where:

V_{NOM} = Nominal output voltage programmed with the R_SEL table or PMBus command.

The size of the resistors should be chosen so that their power dissipation is within their rated value. R_{SN} can be omitted for a slight (usually less than 1%) reduction in accuracy.

The MAX20751 regulates and monitors the voltage from SENSE_P to SENSE_N; therefore, the PWRGD and OVP thresholds, droop resistance, V_{OUT} slew rates, etc., are all scaled by the voltage-divider feedback.

MAX20751 PMBus Interface Overview

Refer to Maxim AN5941: *MAX20751 PMBus Application Note.*

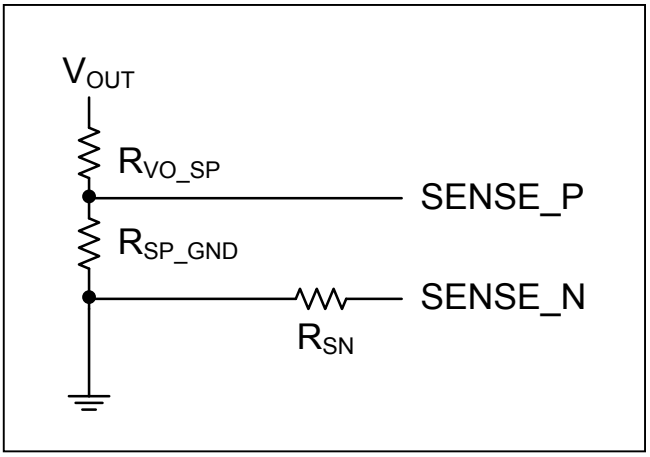


Figure 8. Increasing V_{OUT} Using Resistor Voltage-Divider Feedback

Basic PCB Layout Guidelines

For electrical and thermal reasons, the second layer from the top and bottom should be reserved for contiguous power ground planes. It is recommended to place the MAX20751 master away from the load current path. An analog ground (AGND) copper polygon or plane should be used and the MAX20751 GND pins connected to it. The AGND (or quiet ground) polygon or plane should extend underneath the MAX20751 on one of the inner layers and be connected to the MAX20751 PGND pin at one point through a single wide trace or via. AGND should be used as a shield for the control signals (I_{SENSE}, PWM, SENSE_P/SENSE_N, and TS_FAULTB). The control signals to and from the slaves are ideally the same length for each phase.

SENSE_P/SENSE_N: These output sense lines are important for regulation and should be routed as a differential pair with sufficient AGND plane shielding.

I_{SENSE} Signals: The reconstructed current signals should be kept away from noise sources and shielded with sufficient AGND plane.

PWM Signals: Keep away from noise-sensitive traces and provide sufficient GND plane shielding. See *Master/Slave Placement*.

TS_FAULTB: Provides AGND plane shielding.

V_{DD}/V_{DD33}: Place decoupling capacitors as close as possible to the part and on the same layer.

Compensation: The compensation components should be placed as close as possible to the master and the amplifier inputs/outputs they connect to and away from noisy signals.

R_{REF}/R_SEL/R_{MRAMP}: These components should be placed close to the master and away from noisy signals.

Master/Slave Placement: Position the master IC so the side with all slave-related signals is facing the slaves. This will avoid having noisy lines go under the master and interact with the analog compensation nets (Figure 9).

Internal V_{DD} Switcher

- Place the inductor (A) as close as possible to the PVX (phase output) pin.
- Place a 100nF MLCC very close to the V_{DD} pin to filter high frequencies. A 22µF to 47µF MLCC is required, and should also be placed close to the inductor and the IC.
- 3.3V power supply requires a small 100nF MLCC close to the master's pin, followed by a larger 10µF MLCC.
- Use a PGND plane or polygon underneath the V_{DD} switcher components. Connect the MAX20751 PGND pin to the PGND plane or polygon. The PGND pin should connect to the MAX20751 GND pins through a single wide trace or via. The PGND plane or polygon should also connect to the power ground planes.
- To make filtering capacitors effective, place vias to shorten their path to the PGND pin. The number of vias should be as many as allowed by area to reduce path resistance to PGND.

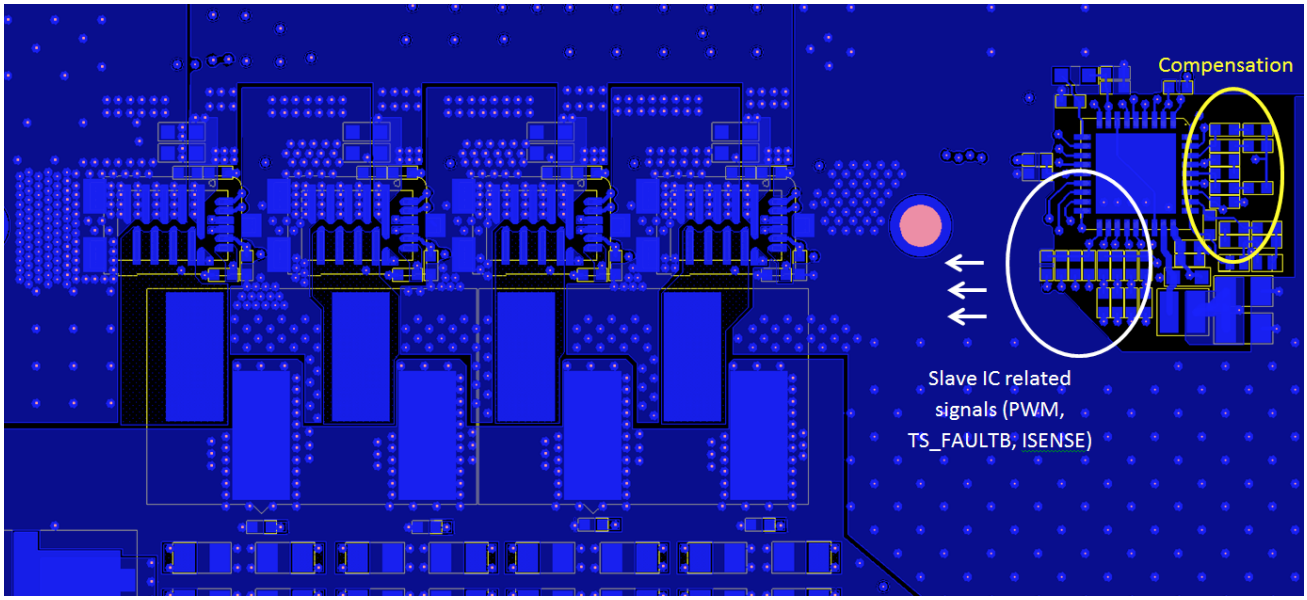


Figure 9. Board and Layout for Slave Signals

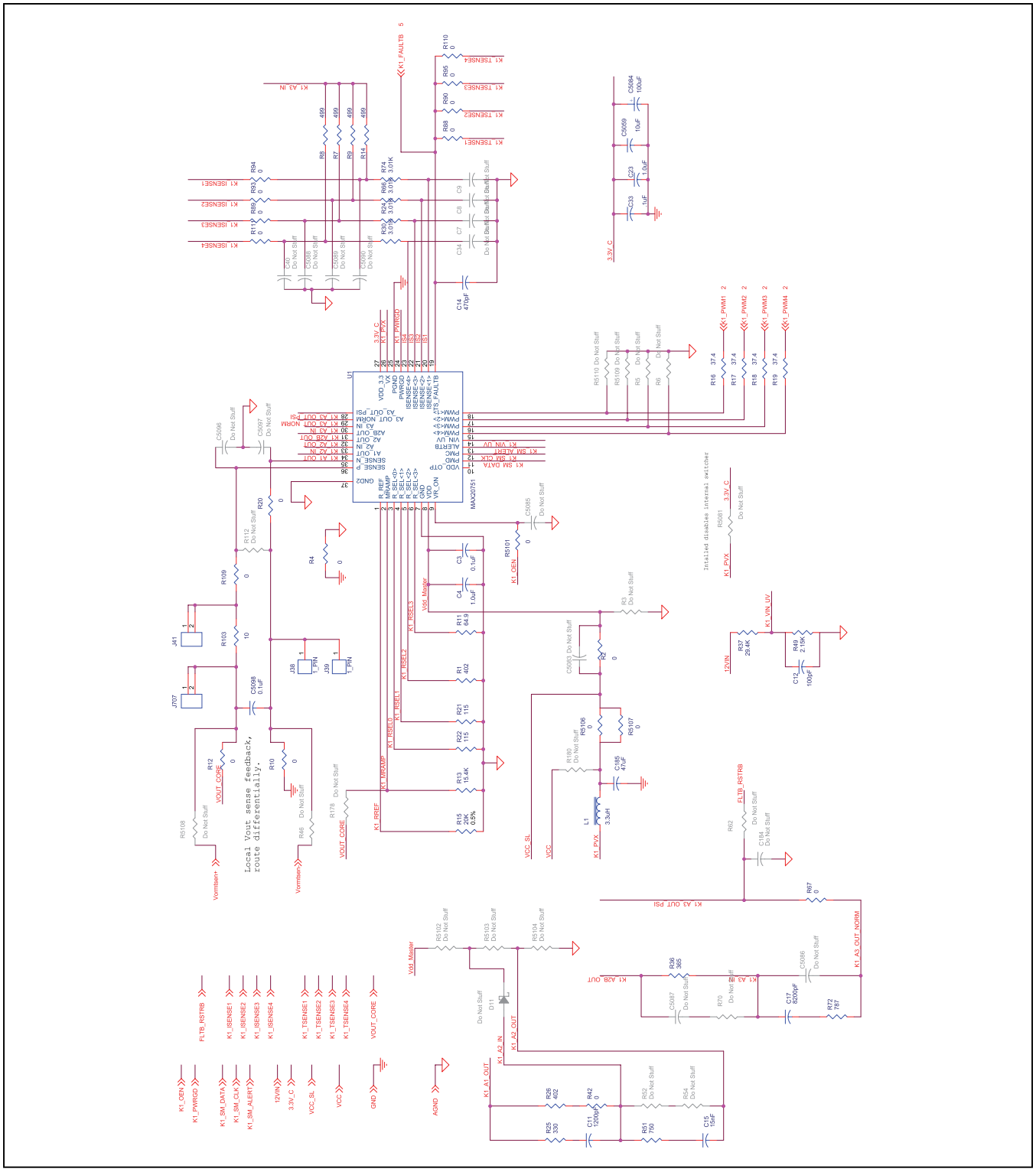


Figure 10. MAX20751 Schematic

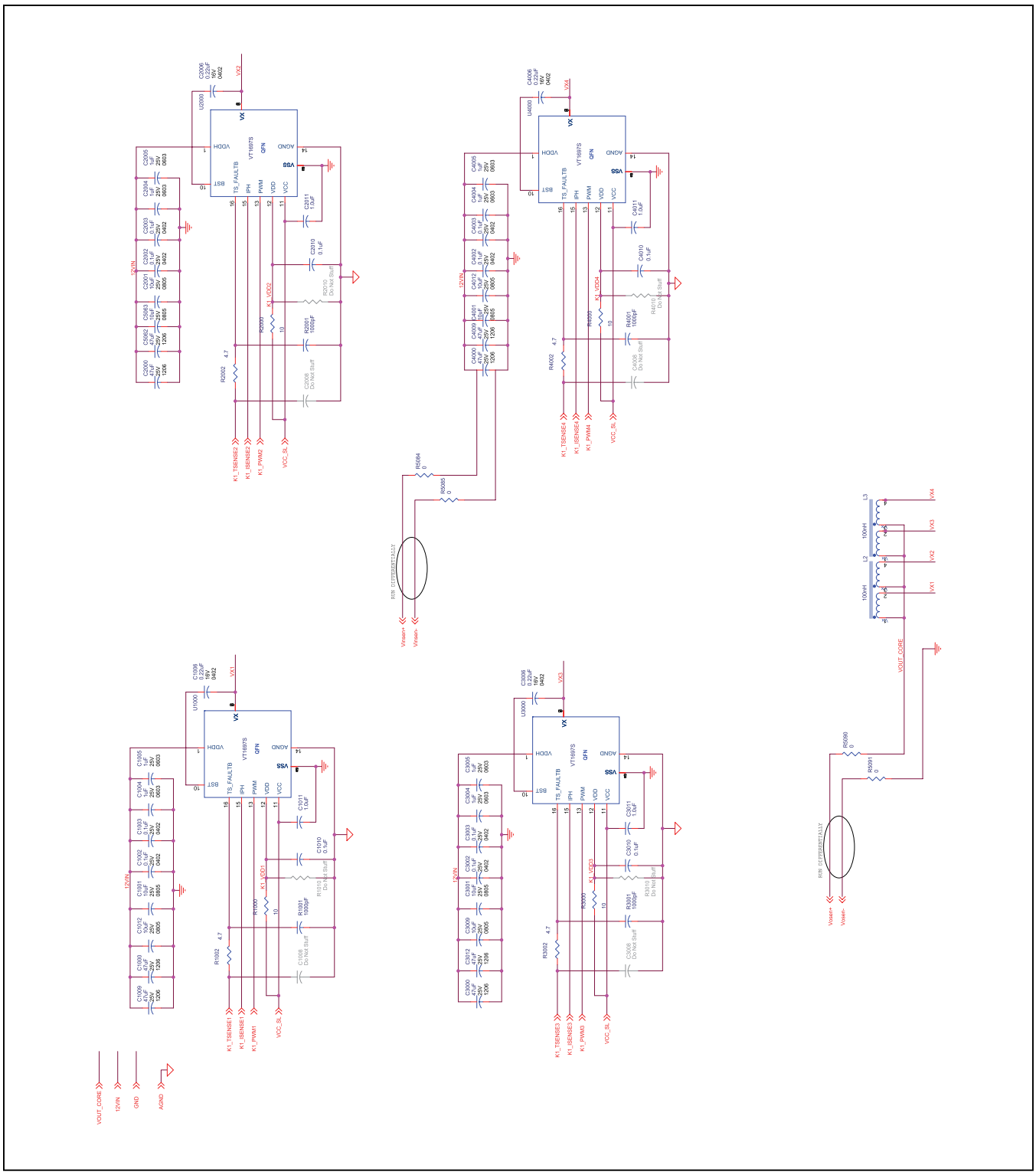


Figure 11. Smart Slave ICs Schematic

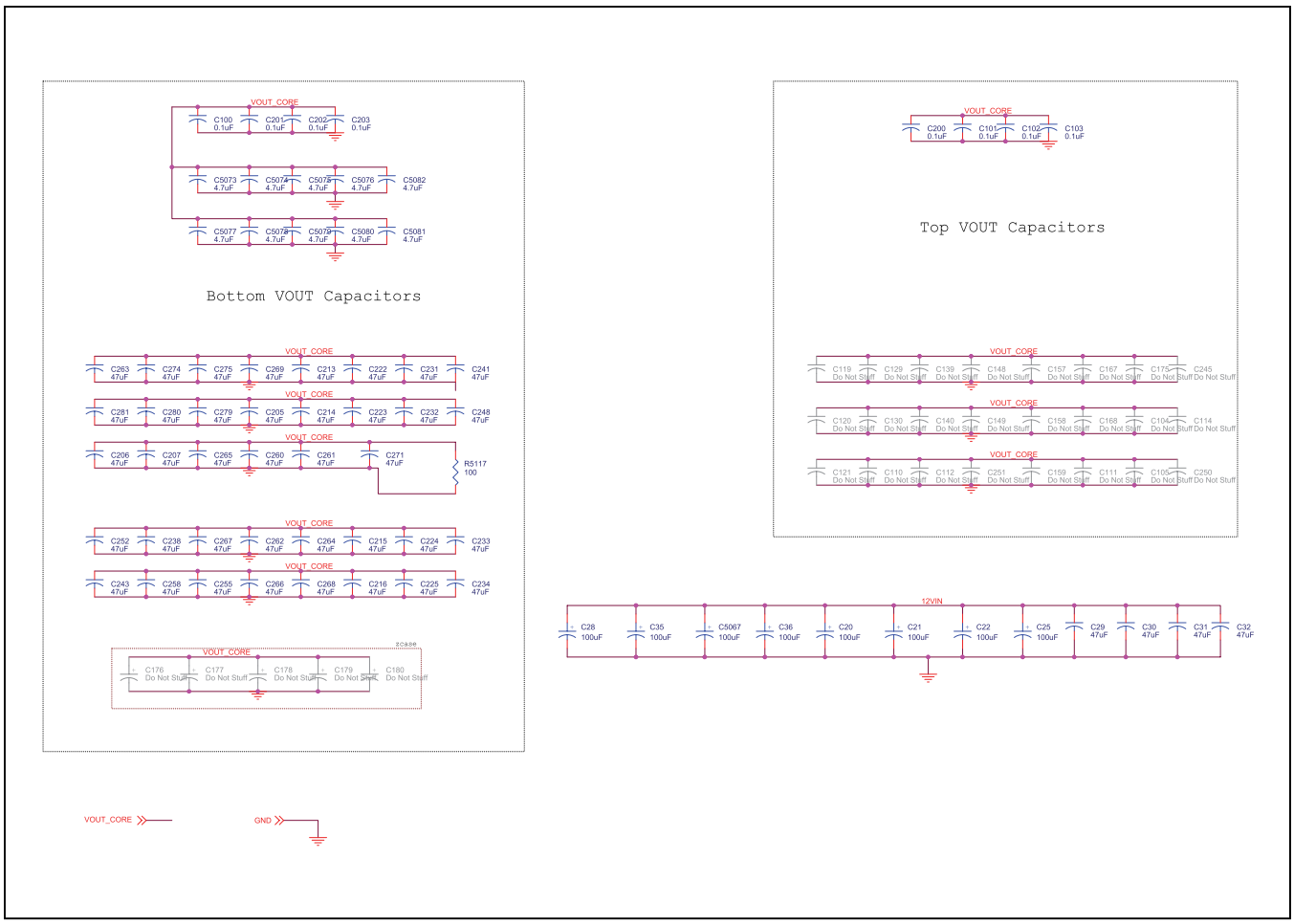


Figure 12. V_{IN} and V_{OUT} Capacitors Schematic

Ordering Information

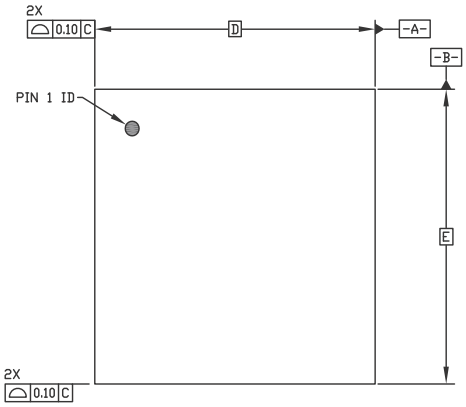
PART	DESCRIPTION	PIN-PACKAGE	TEMP RANGE	PKG. CODE	OUTLINE NO.	LAND PATTERN NO.
MAX20751EKX+	Master	36 QFN (Type C)	-40°C to +125°C	K3666+1	ES AP-3565	—
MAX20751EKX+T	Master	36 QFN (Type C)	-40°C to +125°C	K3666+1	ES AP-3565	—

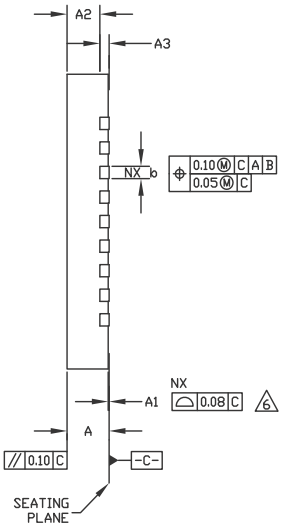
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel (2.5kμ).

Package Information

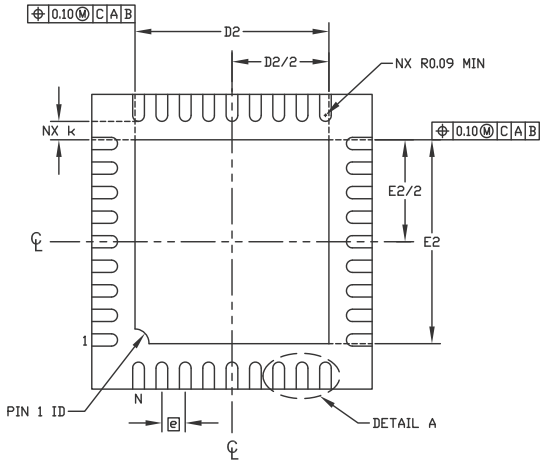
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

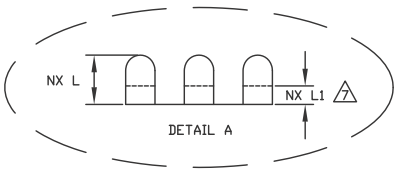
	Title:	Doc No.	Rev.
	Package Outline - 36 Lead QFN [Type C]	ES AP-3565	0
		Page 1 of 3	





BOTTOM VIEW





	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.70	0.80	0.024	0.028	0.031
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	6.00 BSC			0.236 BSC		
D2	4.00	4.15	4.25	0.157	0.163	0.167
E	6.00 BSC			0.236 BSC		
E2	4.00	4.15	4.25	0.157	0.163	0.167
e	0.50 BSC			0.020 BSC		
k	0.20	–	–	0.008	–	–
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0.03	–	0.15	0.001	–	0.006
N	36 PINS			36 PINS		
ND	9 PINS			9 PINS		
NE	9 PINS			9 PINS		

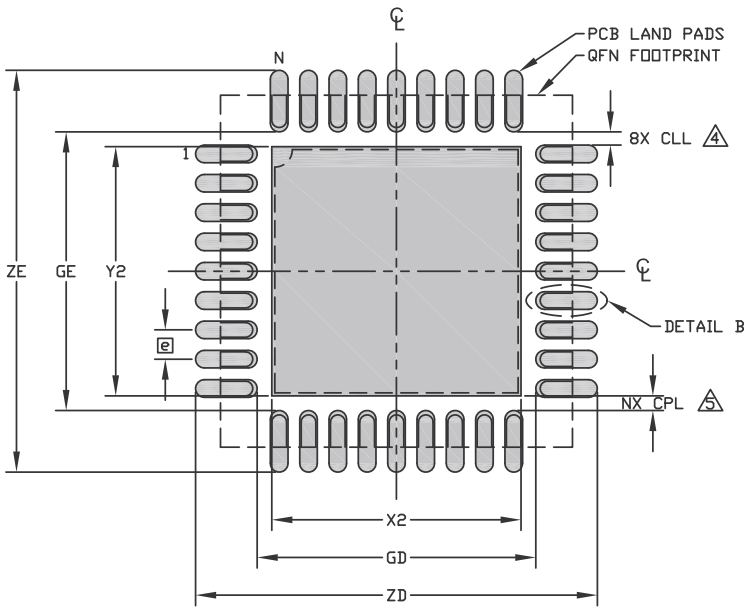
NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. Dimensioning & tolerancing conform to ASME Y14.5-2009.
4. Package is JEDEC MO-220 compliant.
5. N is the total number of terminals, ND and NE are the number of terminals per side.
6. Coplanarity applies to both terminals and heat sink.
7. L1 is the pullback of the terminal metal from the plastic body edge.

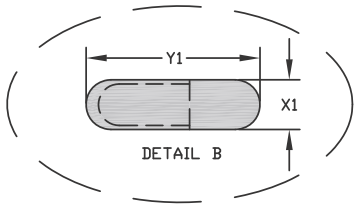
Package Information (continued)

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	Title:	Doc No.	Rev.
	Package Outline - 36 Lead QFN [Type C]	**ES AP-3565**	**0**
		Page 2 of 3	

RECOMMENDED LAND PATTERN
WITH QFN OVERLAY





DIM	MILLIMETERS MIN	NOM	MAX	INCHES MIN	NOM	MAX
CLL		0.23 REF			0.009 REF	
CPL		0.25 REF			0.010 REF	
e		0.50 BSC			0.020 BSC	
GD		4.75 REF			0.187 REF	
GE		4.75 REF			0.187 REF	
N		36 PINS			36 PINS	
X1		0.30 TYP			0.012 TYP	
X2		4.25 REF			0.167 REF	
Y1		1.05 TYP			0.041 TYP	
Y2		4.25 REF			0.167 REF	
ZD		6.85 REF			0.270 REF	
ZE		6.85 REF			0.270 REF	

NOTES:
1. Millimeters is the controlling dimension.
2. Drawing is not to scale.
3. N is the total number of terminals.
4. CLL is the corner pad edge to adjacent inside pad distance.
5. CPL is the central pad to inside edge of lead pad distance.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial Release	—
1	10/14	Replaced Figures 10 and 11	28, 29
2	3/15	Corrected application note number	26

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