19-4420; Rev 1; 6/09

EVALUATION KIT AVAILABLE

Ultrasound VGA Integrated with CW Octal Mixer

MAX2036

General Description

The MAX2036 8-channel variable-gain amplifier (VGA) and programmable octal mixer array is designed for high linearity, high dynamic range, and low-noise performance targeting ultrasound imaging and Doppler applications. Each amplifier features differential inputs and outputs and a total gain range of 50dB (typ). In addition, the VGAs offer very low output-referred noise performance suitable for interfacing with 10-bit ADCs.

The MAX2036 VGA is optimized for less than ±0.5dB absolute gain error to ensure minimal channel-to-channel ultrasound beamforming focus error. The device's differential outputs are designed to directly drive ultrasound ADCs through an external passive anti-aliasing filter. A switchable clamp is also provided at each amplifier's output to limit the output signals, thereby preventing ADC overdrive or saturation.

Dynamic performance of the device is optimized to reduce distortion to support second-harmonic imaging. The device achieves a second-harmonic distortion specification of -62dBc at V_{OUT} = 1.5V_{P-P} and f_{IN} = 5MHz, and an ultrasound-specific* two-tone third-order intermodulation distortion specification of -52dBc at V_{OUT} = 1.5V_{P-P} and f_{IN} = 5MHz.

The MAX2036 also integrates an octal quadrature mixer array and programmable LO phase generators for a complete CW beamforming solution. The LO phase selection for each channel can be programmed using a digital serial interface and a single high-frequency clock or the LOs for each complex mixer pair can be directly driven using separate 4 x LO clocks. The serial interface is designed to allow multiple devices to be easily daisy-chained in order to minimize program interface wiring. The LO phase dividers can be programmed to allow 4, 8, or 16 quadrature phases. The input path of each CW mixer consists of a selectable lowpass filter for optimal CWD noise performance. The outputs of the mixers are summed into I and Q differential current outputs. The mixers and LO generators are designed to have exceptionally low noise performance of -155dBc/Hz at 1kHz offset from a 1.25MHz carrier.

The MAX2036 operates from a +5.0V power supply, consuming only 120mW/channel in VGA mode and 269mW/channel in normal power CW mode. A low-power CW mode is also available and consumes only 226mW/channel. The device is available in a lead-free 100-pin TQFP package (14mm x 14mm) with an exposed pad. Electrical performance is guaranteed over a 0°C to +70°C temperature range.

Applications

Ultrasound Imaging

Sonar

Features

- **8-Channel Configuration**
- **High Integration for Ultrasound Imaging Applications**
- **Pin Compatible with the MAX2035 Ultrasound VGA**

VGA Features

- **Maximum Gain, Gain Range, and Output-Referred Noise Optimized for Interfacing with 10-Bit ADCs**
  - **Maximum Gain of 39.5dB**
  - **Total Gain Range of 50dB**
  - **60nV/√Hz Ultra-Low Output-Referred Noise at 5MHz**
- **±0.5dB Absolute Gain Error**
- **120mW Consumption per Channel**
- **Switchable Output VGA Clamp Eliminating ADC Overdrive**
- **Fully Differential VGA Outputs for Direct ADC Drive**
- **Variable Gain Range Achieves 50dB Dynamic Range**
- **-62dBc HD2 at V_{OUT} = 1.5V_{P-P} and f_{IN} = 5MHz**
- **Two-Tone Ultrasound-Specific* IMD3 of -52dBc at V_{OUT} = 1.5V_{P-P} and f_{IN} = 5MHz**

CWD Mixer Features

- **Low Mixer Noise of -155dBc/Hz at 1kHz Offset from 1.25MHz Carrier**
- **Serial-Programmable LO Phase Generator for 4, 8, 16 LO Quadrature Phase Resolution**
- **Optional Individual Channel 4 x f_{LO} LO Input Drive Capability**
- **269mW Power Consumption per Channel (Normal Power Mode) and 226mW Power Consumption per Channel (Low-Power Mode)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2036CCQ+D	0°C to +70°C	100 TQFP-EP†
MAX2036CCQ+TD	0°C to +70°C	100 TQFP-EP†

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
D = Dry packing.
†EP = Exposed pad.

**See the* Ultrasound-Specific IMD3 Specification in the Applications Information *section.*

Pin Configuration appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Ultrasound VGA Integrated with CW Octal Mixer

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{REF} to GND .....-0.3V to +5.5V
Any Other Pins to GND.....-0.3V to (V_{CC} + 0.3V)
CW Mixer Output Voltage to GND (CW_IOUT+, CW_IOUT-, CW_QOUT+, CW_QOUT-) 13V
VGA Differential Input Voltage (VGIN_+, VGIN_-).....$8.0V_{P-P}$
Analog Gain Control Differential Input Voltage (VG_CTL+, VG_CTL-) .....$8.0V_{P-P}$
CW Mixer Differential Input Voltage (CWIN_+, CWIN_-).....$8.0V_{P-P}$
CW Mixer LVDS LO Differential Input Voltage.....$8.0V_{P-P}$
Continuous Power Dissipation (T_A = +70°C)
100-Pin TQFP (derated 45.5mW/°C above +70°C)..3636.4mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature .....+150°C
θ_{JC} (Note 1) .....+2°C/W
θ_{JA} (Note 1).....+22°C/W
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—VGA MODE

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, V_{CM} = (3/5)V_{REF}, T_A = 0°C to +70°C, V_{GND} = 0V, LOW_PWR = 0, M4_EN = 0, CW_FILTER = 0 or 1, TEST_MODE = 0, PD = 0, CW_VG = 1, CW_M1 = 0, CW_M2 = 0, no RF signals applied, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, CW mixer outputs pulled up to +11V through four separate ±0.1% 115Ω resistors, all CW channels programmed off. Typical values are at V_{CC} = V_{REF} = 5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VGA MODE							
Supply Voltage Range	V_{CC}			4.75	5	5.25	V
V_{CC} External Reference Voltage Range	V_{REF}	(Note 3)		4.75	5	5.25	V
Total Power-Supply Current		Refers to V_{CC} supply current plus V_{REF} current	PD = 0		204	231	mA
			PD =1		27	33	
V_{CC} Supply Current	I_{VCC}				192	216	mA
V_{REF} Current	I_{REF}				12	15	mA
Current Consumption per Amplifier Channel		Refers to V_{CC} supply current			24	27	mA
Differential Analog Control Voltage Range		Minimum gain			+2		V_{P-P}
		Maximum gain			-2		
Differential Analog Control Common-Mode Voltage	V_{CM}			2.85	3	3.15	V
Analog Control Input Source/Sink Current					4.5	5	mA
LOGIC INPUTS							
CMOS Input High Voltage	V_{IH}			2.3			V
CMOS Input Low Voltage	V_{IL}					0.8	V

DC ELECTRICAL CHARACTERISTICS—CM MIXER MODE

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, LOW_PWR = 0, M4_EN = 0, CW_FILTER = 0 or 1, TEST_MODE = 0, PD = 0, CW_VG = 0, CW_M1 = 0, CW_M2 = 0, no RF signals applied, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, CW mixer outputs pulled up to +11V through four separate ±0.1% 115Ω resistors. Typical values are at V_{CC} = V_{REF} = 5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CW MIXER MODE						
Current in Full-Power Mode 5V V_{CC} Supply	I_{CC_FP}	Refers to V_{CC} supply current (all 8 channels)		245	265	mA
Current in Full-Power Mode 11V V_{MIX} Supply	I_{MIX_FP}	Refers to V_{MIX} supply current (all 8 channels)		106	120	mA
Current in Full-Power Mode 5V V_{REF} Supply	I_{REF_FP}	Refers to V_{REF} supply current (all 8 channels)		17	21	mA
Power Dissipation in Full-Power Mode	P_{DISS_FP}	Total power dissipation (all 8 channels including both 5V (V_{CC} and V_{REF}) and 11V mixer pullup supply power dissipation in the device) (Note 4)		2.15	2.41	W
Current in Low-Power Mode 5V V_{CC} Supply	I_{CC_LP}	LOW_PWR = 1; refers to V_{CC} supply current (all 8 channels)		245	265	mA
Current in Low-Power Mode 11V V_{MIX} Supply	I_{MIX_LP}	LOW_PWR = 1; refers to V_{MIX} supply current (all 8 channels)		53	60	mA
Current in Low-Power Mode 5V V_{REF} Supply	I_{REF_LP}	LOW_PWR = 1; refers to V_{REF} supply current (all 8 channels)		17	21	mA
Power Dissipation in Low-Power Mode	P_{DISS_LP}	LOW_PWR = 1; total power dissipation (all 8 channels including both 5V (V_{CC} and V_{REF}) and 11V mixer pullup supply power dissipation in the device) (Note 4)		1.81	2.06	W
Mixer LVDS LO Input Common-Mode Voltage		Modes 1 and 2 (Note 5)		1.25 ±0.2		V
LVDS LO Differential Input Voltage		Modes 1 and 2	200	700		mV_{P-P}
LVDS LO Input Common-Mode Current		Per pin		150	200	µA
LVDS LO Differential Input Resistance		Modes 1 and 2 (Note 6)		30		kΩ
Mixer IF Common-Mode Output Current		Common-mode current in each of the differential mixer outputs (Note 7)		3.25	3.75	mA
DATA Output High Voltage		DOUT voltage when terminated in DIN (daisy chain) (Note 8)	4.5			V
DATA Output Low Voltage		DOUT voltage when terminated in DIN (daisy chain) (Note 8)			0.5	V

Ultrasound VGA Integrated with CW Octal Mixer

AC ELECTRICAL CHARACTERISTICS—VGA MODE

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, V_{CM} = (3/5)V_{REF}, T_A = 0°C to +70°C, V_{GND} = 0V, LOW_PWR = 0, M4_EN = 0, CW_FILTER = 1, TEST_MODE = 0, PD = 0, CW_VG = 1, CW_M1 = 0, CW_M2 = 0, VG_CLAMP_MODE = 1, f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, CW mixer outputs pulled up to +11V through four separate ±0.1% 115Ω resistors, differential mixer inputs are driven from a low-impedance source. Typical values are at V_{CC} = V_{REF} = 5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Mode Select Response Time		CW_VG set from logic 1 to 0 or from 0 to 1 (Note 9)			2		µs
VGA MODE							
Large-Signal Bandwidth	f-3dB	V_{OUT} = 1.5V_{P-P}, 3dB bandwidth, gain = 20dB	Differential output capacitance is 10pF, capacitance to GND at each single-ended output is 60pF, R_L = 1kΩ		17		MHz
			No capacitive load, R_L = 1kΩ		22		
Differential Input Resistance	R_{IN}			170	200	230	Ω
Input Effective Capacitance	C_{IN}	f_{RF} = 10MHz, each input to ground			15		pF
Differential Output Resistance	R_{OUT}				100		Ω
Maximum Gain					39.5		dB
Minimum Gain					-10.5		dB
Gain Range					50		dB
Absolute Gain Error		T_A = +25°C, -2.0V < VG_CTL < -1.8V, V_{REF} = 5V			±0.6		dB
		T_A = +25°C, -1.8V < VG_CTL < +1.2V, V_{REF} = 5V			±0.5		
		T_A = +25°C, +1.2V < VG_CTL < +2.0V, V_{REF} = 5V			±1.2		
VGA Gain Response Time		50dB gain change to within 1dB final value			1		µs
Input-Referred Noise		VG_CTL set for maximum gain, no input signal			2		nV/√Hz
Output-Referred Noise		VG_CTL set for +20dB of gain	No input signal		60		nV/√Hz
			V_{OUT} = 1.5V_{P-P}, 1kHz offset		120		
Second Harmonic	HD2	VG_CLAMP_MODE = 1, VG_CTL set for +20dB of gain, f_{RF} = 5MHz, V_{OUT} = 1.5V_{P-P}		-55	-62		dBc
		VG_CLAMP_MODE = 1, VG_CTL set for +20dB of gain, f_{RF} = 10MHz, V_{OUT} = 1.5V_{P-P}			-62		
Third-Order Intermodulation Distortion	IMD3	VG_CTL set for +20dB of gain, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1.5V_{P-P}, V_{REF} = 5V (Note 3)		-40	-52		dBc
Channel-to-Channel Crosstalk		V_{OUT} = 1V_{P-P} differential, f_{RF} = 10MHz, VG_CTL set for +20dB of gain			-80		dB

AC ELECTRICAL CHARACTERISTICS—CW MIXER MODE (continued)

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, LOW_PWR = 0, M4_EN = 0, CW_FILTER = 1, TEST_MODE = 0, PD = 0, CW_VG = 0, CW_M1 = 0, CW_M2 = 0, VG_CLAMP_MODE = 1, f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, CW mixer outputs pulled up to +11V through four separate ±0.1% 115Ω resistors, differential mixer inputs are driven from a low-impedance source. Typical values are at V_{CC} = V_{REF} = 5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Voltage at Clamp ON		VG_CLAMP_MODE = 0, VG_CTL set for +20dB of gain, 350mV$_{P-P}$ differential input		2.2		V_{P-P} differential
Maximum Output Voltage at Clamp OFF		VG_CLAMP_MODE = 1, VG_CTL set for +20dB of gain, 350mV$_{P-P}$ differential input		3.4		V_{P-P} differential
CW MIXER MODE						
Mixer RF Frequency Range			0.9		7.6	MHz
Mixer LO Frequency Range			1		7.5	MHz
Mixer IF Frequency Range					100	kHz
Maximum Input Voltage Range					1.8	V_{P-P} differential
Differential Input Resistance		CW_FILTER = 0		633		Ω
		CW_FILTER = 1		1440		
Input-Referred Noise Voltage		Mode 3, f_{RF} = f_{LO}/4 = 1.25MHz, measured at a 1kHz offset frequency; clutter tone at 0.9V$_{P-P}$ differential measured at the mixer input		6		nV/√Hz
		Mode 3, RF terminated into 50Ω; f_{LO}/4 = 1.25MHz, measured at 1kHz offset		4.6		
Third-Order Intermodulation Distortion	IMD3	Mode 1, f_{RF1} = 5MHz at 0.9V$_{P-P}$ differential input, Doppler tone f_{RF2} = 5.01MHz at 25dBc from clutter tone, f_{LO}/16 = 5MHz (Note 10)		-50		dBc
Mixer Output Voltage Compliance		(Note 11)	4.75		12.00	V
Channel-to-Channel Phase Matching		Measured under zero beat conditions, f_{RF} = 5MHz, f_{LO}/16 = 5MHz (Note 12)		±3		Degrees
Channel-to-Channel Gain Matching		Measured under zero beat conditions, f_{RF} = 5MHz, f_{LO}/16 = 5MHz (Note 12)		±2		dB
Transconductance (Note 13)		CW_FILTER = 1; f_{RF} = 1.1MHz at 1V$_{P-P}$ differential, f_{LO}/16 = 1MHz		2.8		mS
		CW_FILTER = 0 (low LPF cutoff frequency); f_{RF} = 1.1MHz at 1V$_{P-P}$ differential, f_{LO}/16 = 1MHz		2.8		

Ultrasound VGA Integrated with CW Octal Mixer

AC ELECTRICAL CHARACTERISTICS—CW MIXER MODE (continued)

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, LOW_PWR = 0, M4_EN = 0, CW_FILTER = 1, TEST_MODE = 0, PD = 0, CW_VG = 0, CW_M1 = 0, CW_M2 = 0, VG_CLAMP_MODE = 1, f_{RF} = f_{LO}/16 = 5MHz, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, CW mixer outputs pulled up to +11V through four separate ±0.1% 115Ω resistors, differential mixer inputs are driven from a low-impedance source. Typical values are at V_{CC} = V_{REF} = 5V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL SHIFT REGISTER						
Serial Shift Register Programming Rate					10	MHz
Minimum Data Set-Up Time	t_{DSU}			30		ns
Minimum Data Hold Time	t_{HLD}			2		ns
Minimum Data Clock Time	t_{DCLK}			100		ns
Minimum Data Clock Pulse Width High	$t_{DCLKPWH}$			30		ns
Minimum Data Clock Pulse Width Low	$t_{DCLKPWL}$			30		ns
Minimum Load Line	t_{LD}			30		ns
Minimum Load Line High to Mixer Clock On	t_{MIXCLK}			30		ns
Minimum Data Clock to Load Line High	t_{CLH}			30		ns

Note 2: Specifications at T_A = +25°C and T_A = +70°C are guaranteed by production. Specifications at T_A = 0°C are guaranteed by design and characterization.

Note 3: Noise performance of the device is dependent on the noise contribution from the supply to V_{REF}. Use a low-noise supply for V_{REF}. V_{CC} and V_{REF} can be connected together to share the same supply voltage if the supply for V_{CC} exhibits low noise.

Note 4: Total on-chip power dissipation is calculated as $P_{DISS} = V_{CC} \times I_{CC} + V_{REF} \times I_{REF} + [11V - (I_{MIX}/4) \times 115] \times I_{MIX}$.

Note 5: Note that the LVDS CWD LO clocks are DC-coupled. This is to ensure immediate synchronization when the clock is first turned on. An AC-coupled LO is problematic in that the RC time constant associated with the coupling capacitors and the input impedance of the pin causes there to be a period of time (related to the RC time constant) when the DC level on the chip side of the capacitor is outside the acceptable common-mode range and the LO swing does not exceed both the logic thresholds required for proper operation. This problem associated with AC-coupling would cause an inability to ensure synchronization among beamforming channels. The LVDS signal is terminated differentially with an external 100Ω resistor on the board.

Note 6: External 100Ω resistor terminates the LVDS differential signal path.

Note 7: The mixer common-mode current (3.25mA/channel) is specified as the common-mode current in each of the differential mixer outputs (CW_QOUT+, CW_QOUT-, CW_IOUT+, CW_IOUT-).

Note 8: Specification guaranteed only for DOUT driving DIN of the next device in a daisy-chain fashion.

Note 9: This response time does not include the CW output highpass filter. When switching to VGA mode, the CW outputs stop drawing current and the output voltage goes to the rail. If a highpass filter is used, the recovery time can be excessive and a switching network is recommended as shown in the *Applications Information* section.

Note 10: See the *Ultrasound-Specific IMD3 Specification* in the *Applications Information* section.

Note 11: Mixer output-voltage compliance is the range of acceptable voltages allowed on the CW mixer outputs.

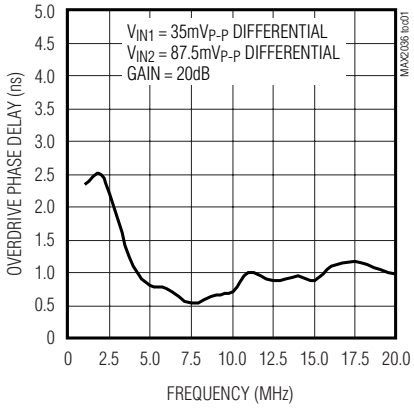
Note 12: Channel-to-channel gain-and-phase matching measured on 30 pieces during engineering characterization at room temperature. Each mixer is used as a phase detector and produces a DC voltage in the IQ plane. The phase is given by the angle of the vector drawn on that plane. Multiple channels from multiple parts are compared to each other to produce the phase variation.

Note 13: Transconductance is defined as the quadrature summing of the CW differential output current at baseband divided by the mixer's input voltage.

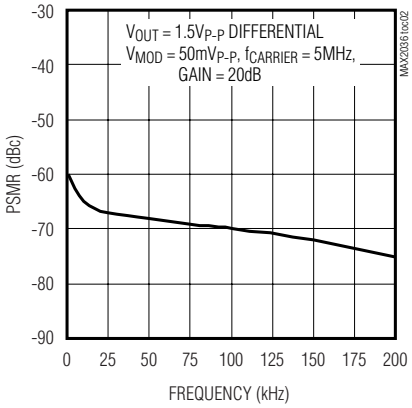
Typical Operating Characteristics

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, V_{GND} = 0V, PD = 0, VG_CLAMP_MODE = 1, f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, T_A = 0°C to +70°C. Typical values are at V_{CC} = V_{REF} = 5V, V_{CM} = 3.0V, T_A = +25°C, unless otherwise noted.)

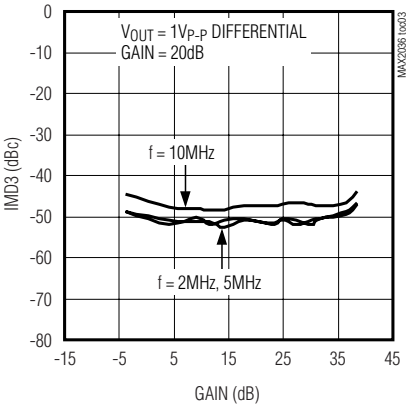
OVERDRIVE PHASE DELAY vs. FREQUENCY



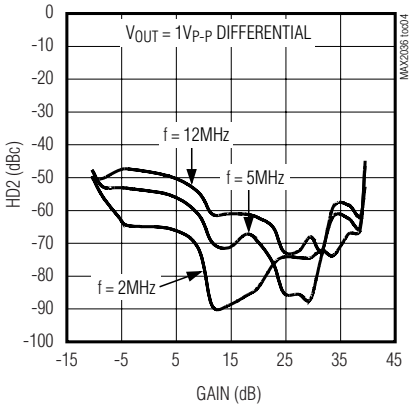
POWER-SUPPLY MODULATION RATIO



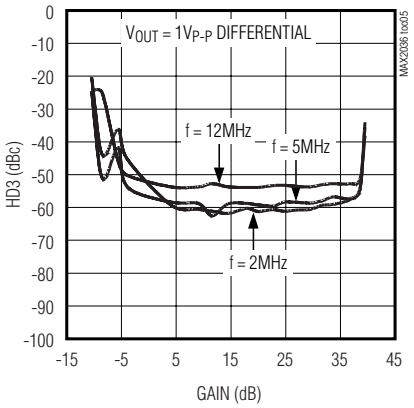
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. GAIN



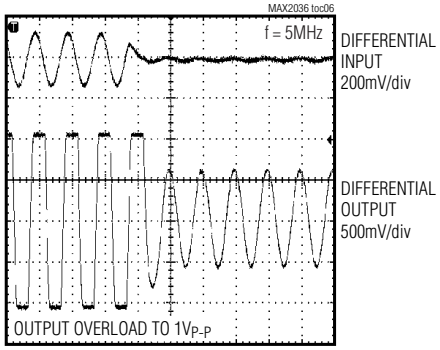
SECOND-HARMONIC DISTORTION vs. GAIN



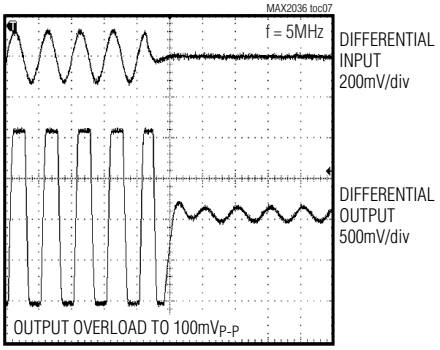
THIRD-HARMONIC DISTORTION vs. GAIN



OVERLOAD RECOVERY TIME



OVERLOAD RECOVERY TIME

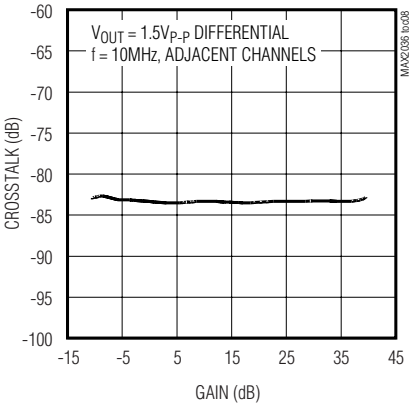


Ultrasound VGA Integrated with CW Octal Mixer

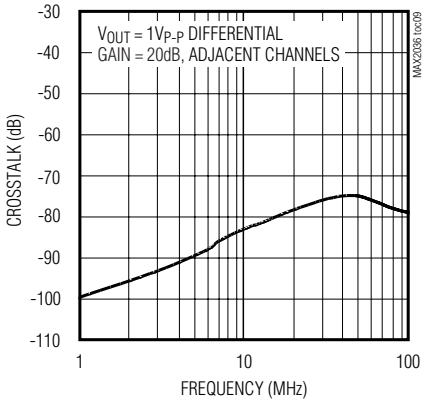
Typical Operating Characteristics (continued)

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, V_{GND} = 0V, PD = 0, VG_CLAMP_MODE = 1, f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, T_A = 0°C to +70°C. Typical values are at V_{CC} = V_{REF} = 5V, V_{CM} = 3.0V, T_A = +25°C, unless otherwise noted.)

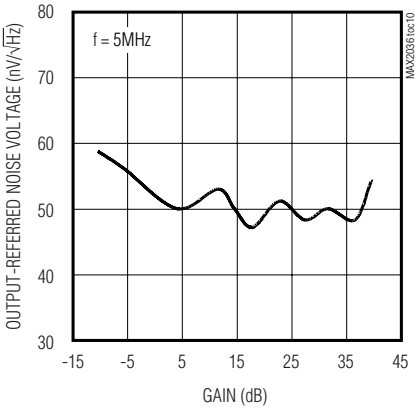
CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN



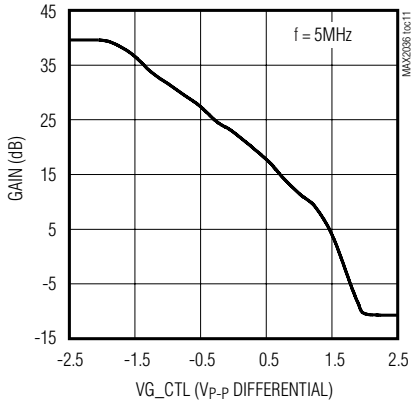
CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



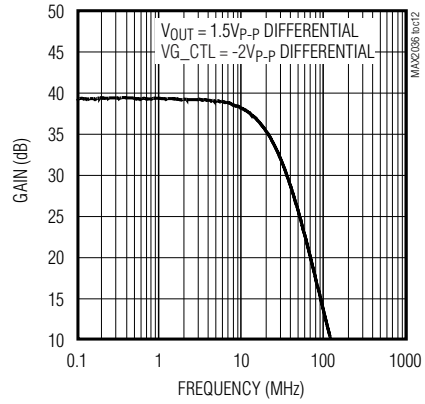
OUTPUT-REFERRED NOISE VOLTAGE vs. GAIN



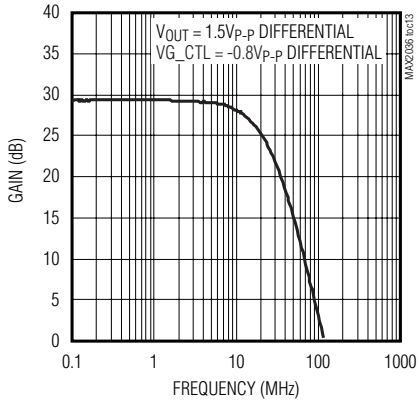
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE (VG_CTL)



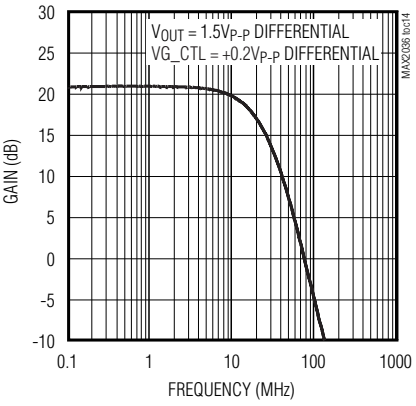
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



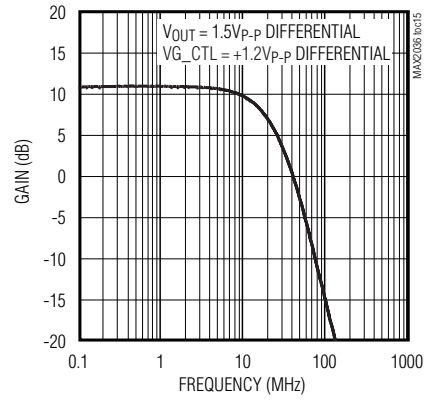
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



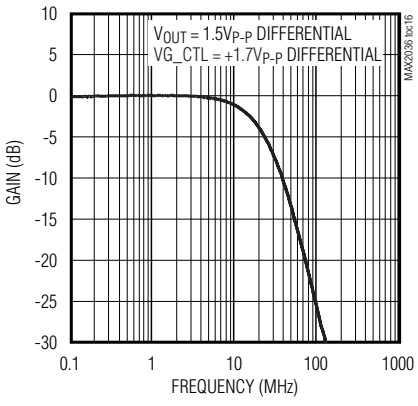
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



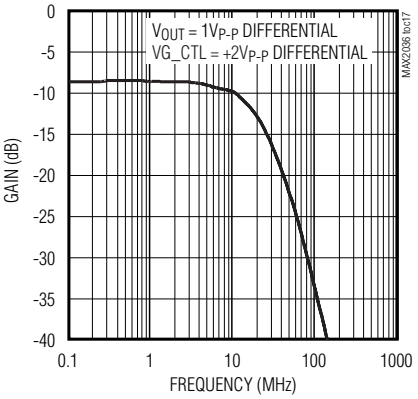
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



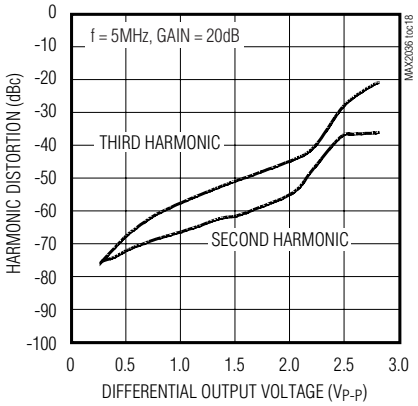
Typical Operating Characteristics (continued)

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, V_{GND} = 0V, PD = 0, VG_CLAMP_MODE = 1, f_{RF} = 5MHz, capacitance to GND at each of the VGA differential outputs is 60pF, differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ, T_A = 0°C to +70°C. Typical values are at V_{CC} = V_{REF} = 5V, V_{CM} = 3.0V, T_A = +25°C, unless otherwise noted.)

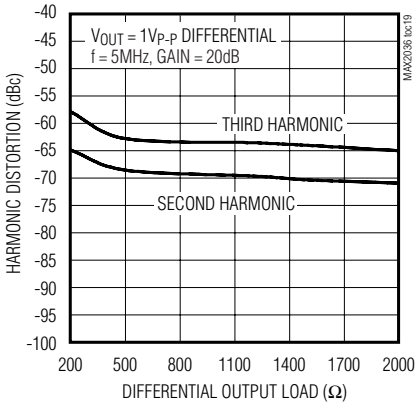
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY



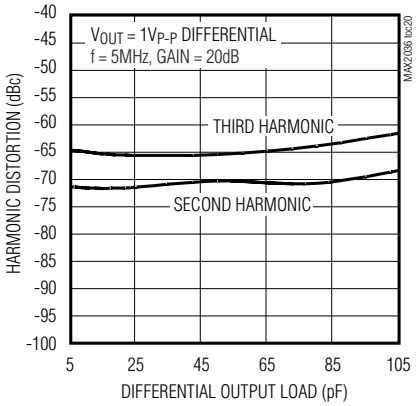
HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT VOLTAGE



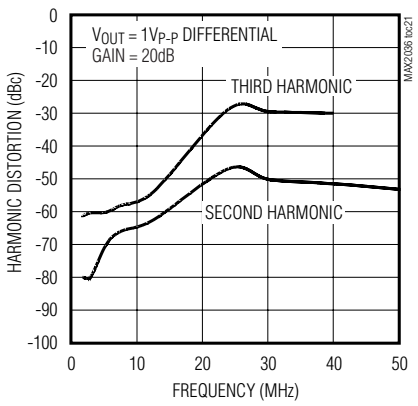
HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT LOAD RESISTANCE



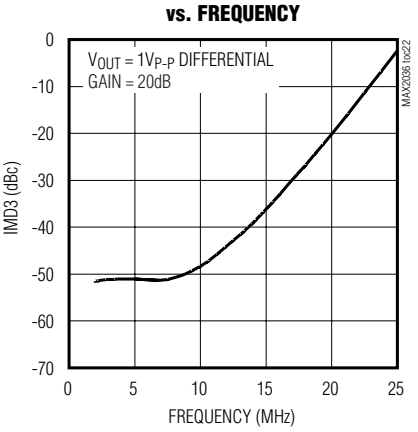
HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT LOAD CAPACITANCE



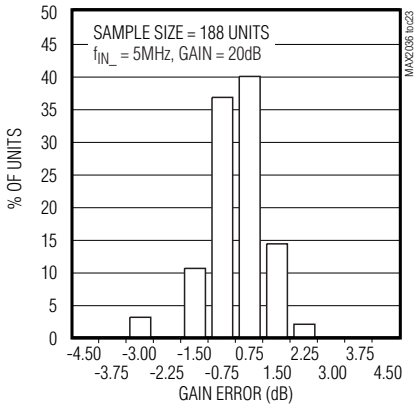
HARMONIC DISTORTION vs. FREQUENCY



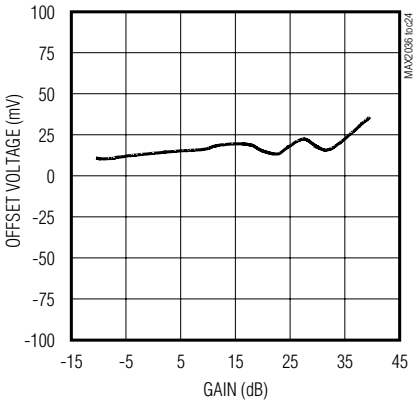
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. FREQUENCY



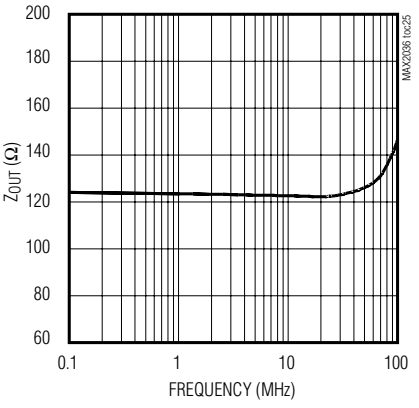
GAIN ERROR HISTOGRAM



OUTPUT COMMON-MODE OFFSET VOLTAGE vs. GAIN



DIFFERENTIAL OUTPUT IMPEDANCE MAGNITUDE vs. FREQUENCY

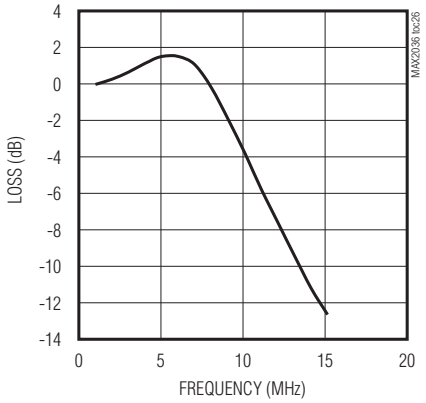


Ultrasound VGA Integrated with CW Octal Mixer

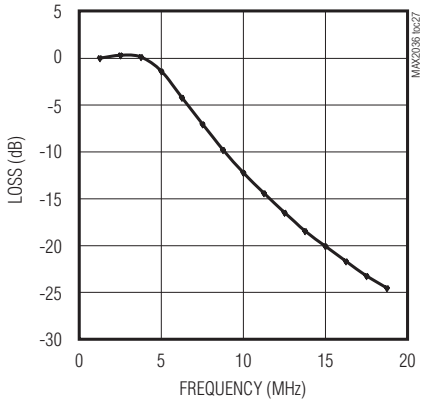
Typical Operating Characteristics (continued)

(Figure 7, V_{CC} = V_{REF} = 4.75V to 5.25V, V_{GND} = 0V, LOW_PWR = 0, M4_EN = 0, CW_FILTER = 1, TEST_MODE = 0, PD = 0, CW_VG = 0, CW_M1 = 0, CW_M2 = 0, CW mixer outputs pulled up to +11V through four separate ±0.1% 115Ω resistors, differential mixer inputs are driven from a low impedance source.)

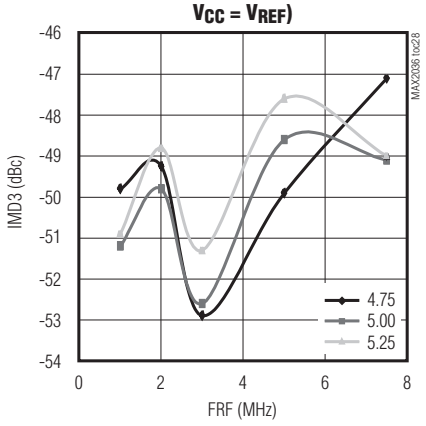
CW FILTER RESPONSE (CW_FILTER = 1)



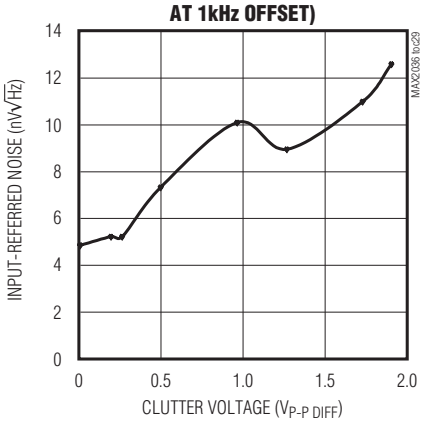
CW FILTER RESPONSE (CW_FILTER = 0)



CW IMD3 vs. FREQUENCY (MODE 1, V_{RF} = 900mV_{P-P} DIFFERENTIAL V_{CC} = V_{REF})



INPUT-REFERRED NOISE vs. CLUTTER VOLTAGE (MODE 4, F_CLUTTER = 1.25MHz AT 1kHz OFFSET)



Pin Description

PIN	NAME	FUNCTION
1	CWIN2-	CW Mixer Channel 2 Inverting Differential Input
2	CWIN2+	CW Mixer Channel 2 Noninverting Differential Input
3	VGIN3-	VGA Channel 3 Inverting Differential Input
4	VGIN3+	VGA Channel 3 Noninverting Differential Input
5, 10, 19, 24, 29, 34, 58, 79, 81, 96	GND	Ground
6	CWIN3-	CW Mixer Channel 3 Inverting Differential Input
7	CWIN3+	CW Mixer Channel 3 Noninverting Differential Input
8	VGIN4-	VGA Channel 4 Inverting Differential Input
9	VGIN4+	VGA Channel 4 Noninverting Differential Input
11	CWIN4-	CW Mixer Channel 4 Inverting Differential Input
12	CWIN4+	CW Mixer Channel 4 Noninverting Differential Input
13	EXT_C1	External Compensation. Connect a 4.7µF capacitor to ground as close as possible to the pin to bypass the internal biasing circuitry.
14	EXT_C2	External Compensation. Connect a 4.7µF capacitor to ground as close as possible to the pin to bypass the internal biasing circuitry.
15	EXT_C3	External Compensation. Connect a 4.7µF capacitor to ground as close as possible to the pin to bypass the internal biasing circuitry.
16, 42, 46, 54, 72, 82, 87	V_{CC}	5V Power Supply. Connect to an external +5V power supply. Bypass each V_{CC} supply to ground with 0.1µF capacitors as close as possible to the pins.
17	VGIN5-	VGA Channel 5 Inverting Differential Input
18	VGIN5+	VGA Channel 5 Noninverting Differential Input
20	CWIN5-	CW Mixer Channel 5 Inverting Differential Input
21	CWIN5+	CW Mixer Channel 5 Noninverting Differential Input
22	VGIN6-	VGA Channel 6 Inverting Differential Input
23	VGIN6+	VGA Channel 6 Noninverting Differential Input
25	CWIN6-	CW Mixer Channel 6 Inverting Differential Input
26	CWIN6+	CW Mixer Channel 6 Noninverting Differential Input
27	VGIN7-	VGA Channel 7 Inverting Differential Input
28	VGIN7+	VGA Channel 7 Noninverting Differential Input
30	CWIN7-	CW Mixer Channel 7 Inverting Differential Input
31	CWIN7+	CW Mixer Channel 7 Noninverting Differential Input
32	VGIN8-	VGA Channel 8 Inverting Differential Input
33	VGIN8+	VGA Channel 8 Noninverting Differential Input
35	CWIN8-	CW Mixer Channel 8 Inverting Differential Input
36	CWIN8+	CW Mixer Channel 8 Noninverting Differential Input
37, 93	V_{REF}	5V Reference Supply. Connect to a low-noise power supply. Bypass to GND with a 0.1µF capacitor as close as possible to the pins. Note that noise performance of the device is dependent on the noise contribution from the supply to V_{REF}. Use a low-noise supply for V_{REF}. V_{CC} and V_{REF} can be connected together to share the same supply voltage if the supply for V_{CC} exhibits low noise.

Ultrasound VGA Integrated with CW Octal Mixer

Pin Description (continued)

PIN	NAME	FUNCTION
38	EXT_RES	External Resistor. Connect a 0.1% 7.5kΩ resistor to ground as close as possible to the pin to set the bias for the internal biasing circuitry.
39	CW_VG	CW Mixer VGA Enable. Selects for VGA or CW mixer operation. Set CW_VG to a logic-high to enable the VGAs while the CW mixers are powered down. Set CW_VG to a logic-low to enable the CW mixers while the VGAs are powered down.
40	PD	Power-Down Switch. Drive PD high to set the device in power-down mode. Drive PD low for normal operation.
41	CW_FILTER	CW Filter Mode Corner Frequency Select. Selects in corner frequency of the internal lowpass filter for the CW path. Set CW_FILTER to a logic-high for a corner frequency of 9.5MHz. Set CW_FILTER to a logic-low for a corner frequency of 4.5MHz.
43	M4_EN	Mode 4 Enable. Set M4_EN to a logic-high to override the serial port and activate all 8 channels of the CW path.
44	LOW_PWR	Low-Power Enable. Set high to enable low-power CW mixer mode for the device.
45	DOUT	Serial Port Data Output. Data output for ease of daisy-chaining CW channels for analog beam-forming programming.
47	N.C.	No Connect. Leave this pin unconnected (this pin is the TEST_MODE pin called out in the MAX2036 EV kit data sheet).
48	LO8	CW LO Input for Channel 8. LO clock input for modes 3 and 4.
49	VGOUT8+	VGA Channel 8 Noninverting Differential Output
50	VGOUT8-	VGA Channel 8 Inverting Differential Output
51	LO7	CW LO Input for Channel 7. LO clock input for modes 3 and 4.
52	VGOUT7+	VGA Channel 7 Noninverting Differential Output
53	VGOUT7-	VGA Channel 7 Inverting Differential Output
55	LO6	CW LO Input for Channel 6. LO clock input for modes 3 and 4.
56	VGOUT6+	VGA Channel 6 Noninverting Differential Output
57	VGOUT6-	VGA Channel 6 Inverting Differential Output
59	LO5	CW LO Input for Channel 5. LO clock input for modes 3 and 4.
60	VGOUT5+	VGA Channel 5 Noninverting Differential Output
61	VGOUT5-	VGA Channel 5 Inverting Differential Output
62	VG_CTL-	VGA Analog Gain Control Differential Input. Set the differential to -2V for maximum gain (+39.5dB) and +2V for minimum gain (-10.5dB).
63	VG_CTL+	
64	LO_LVDS-	CW LVDS LO Inverting Differential Input. LO clock inverting input for modes 1 and 2.
65	LO_LVDS+	CW LVDS LO Noninverting Differential Input. LO clock noninverting input for modes 1 and 2.
66	LO4	CW LO Input for Channel 4. LO clock input for modes 3 and 4.
67	VGOUT4+	VGA Channel 4 Noninverting Differential Output
68	VGOUT4-	VGA Channel 4 Inverting Differential Output
69	LO3	CW LO Input for Channel 3. LO clock input for modes 3 and 4.
70	VGOUT3+	VGA Channel 3 Noninverting Differential Output
71	VGOUT3-	VGA Channel 3 Inverting Differential Output
73	LO2	CW LO Input for Channel 2. LO clock input for modes 3 and 4.
74	VGOUT2+	VGA Channel 2 Noninverting Differential Output

Pin Description (continued)

PIN	NAME	FUNCTION
75	VGOUT2-	VGA Channel 2 Inverting Differential Output
76	LO1	CW LO Input for Channel 1. LO clock input for modes 3 and 4.
77	VGOUT1+	VGA Channel 1 Noninverting Differential Output
78	VGOUT1-	VGA Channel 1 Inverting Differential Output
80	DIN	Serial Port Data Input. Data input to program the serial shift registers.
83	CLK	Serial Port Data Clock. Clock input for programming the serial shift registers.
84	CW_M1	CW Mode Select Input 1. Input for programming beamforming mode 1, 2, 3, or 4. See Table 1 for mode programming details.
85	CW_M2	CW Mode Select Input 2. Input for programming beamforming mode 1, 2, 3, or 4. See Table 1 for mode programming details.
86	VG_CLAMP_MODE	VGA Clamp Mode Enable. Drive VG_CLAMP_MODE low to enable VGA clamp mode. VGA output is clamped at typically $2.2V_{P-P}$ differential. Drive VG_CLAMP_MODE high to disable VGA clamp mode.
88	LOAD	Serial Port Load. Loads the data from the serial shift registers into the I/Q phase dividers. Pull LOAD bus from high to low, and from low to high for programming the I/Q phase dividers.
89	CW_QOUT+	CW Mixer Noninverting Differential Quadrature Output. CW mixer output for 8 quadrature mixers combined.
90	CW_QOUT-	CW Mixer Inverting Differential Quadrature Output. CW mixer output for 8 quadrature mixers combined.
91	CW_IOUT-	CW Mixer Inverting Differential In-Phase Output. CW mixer output for 8 in-phase mixers combined.
92	CW_IOUT+	CW Mixer Noninverting Differential In-Phase Output. CW mixer output for 8 in-phase mixers combined.
94	VGIN1-	VGA Channel 1 Inverting Differential Input
95	VGIN1+	VGA Channel 1 Noninverting Differential Input
97	CWIN1-	CW Mixer Channel 1 Inverting Differential Input
98	CWIN1+	CW Mixer Channel 1 Noninverting Differential Input
99	VGIN2-	VGA Channel 2 Inverting Differential Input
100	VGIN2+	VGA Channel 2 Noninverting Differential Input
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large PCB ground plane to maximize thermal performance.

Ultrasound VGA Integrated with CW Octal Mixer

Detailed Description

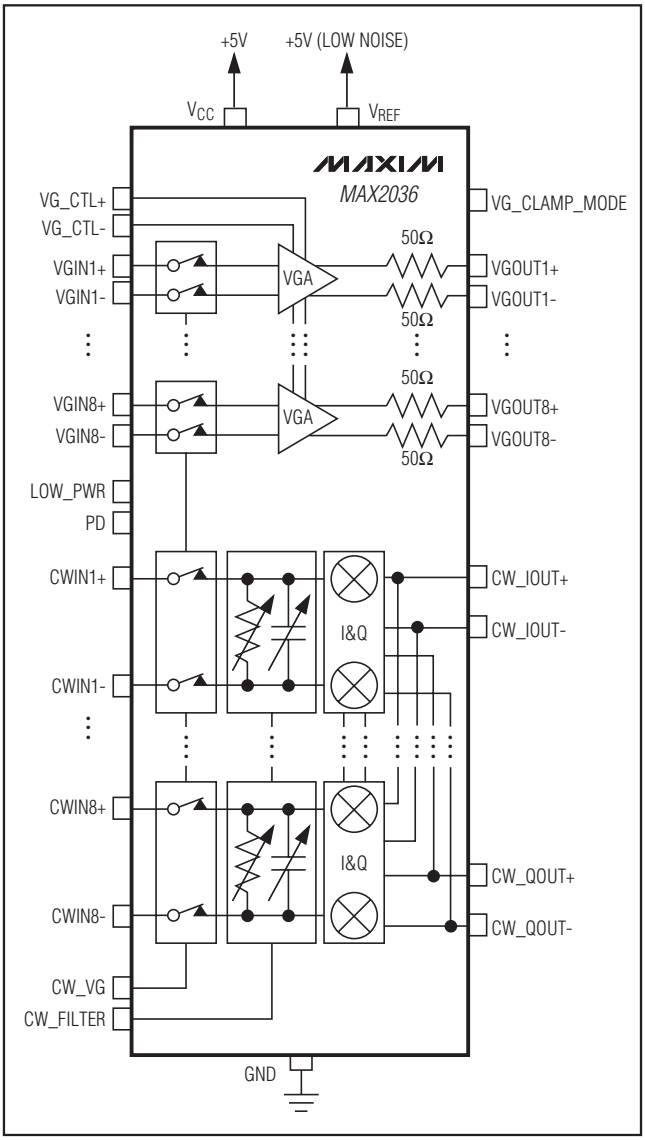
The MAX2036 is an 8-channel VGA integrated with a programmable octal quadrature mixer array designed for ultrasound imaging and Doppler applications. The device is optimized for efficient power consumption, high dynamic range, and exceptionally low-noise performance. The VGA path features differential inputs, analog variable gain control, differential outputs for direct ADC drive, and a selectable output voltage clamp to avoid ADC overdrive. The integrated octal quadrature mixer array includes serial-programmable LO phase generators for CWD beamforming applications. The LO phase dividers can be programmed for 4, 8, or 16 quadrature phases. Lowpass filters are integrated at the input paths of each CW mixer. The outputs for the mixers are summed into single I/Q differential current outputs.

The MAX2036 also integrates an octal quadrature mixer array and programmable LO phase generators for a complete continuous wave (CW) Doppler beamforming solution. The LO phase selection for each channel is programmed using a digital serial interface and a single high-frequency clock, or the LOs for each complex mixer pair can be directly driven using separate 4 x LO clocks. The serial interface is designed to allow multiple devices to be easily daisy chained in order to minimize program interface wiring. The LO phase dividers can be programmed to allow 4, 8, or 16 quadrature phases. The input path of each CW mixer consists of a selectable lowpass filter for optimal CWD noise performance. The outputs of the mixers are summed into single I and Q differential current outputs. The mixers and LO generators are designed to have exceptionally low noise performance of -155dBc/Hz at 1kHz offset from a 1.25MHz carrier, measured with 900mV$_{P-P}$ differential clutter signal.

Variable Gain Amplifier (VGA)

The MAX2036's VGAs are optimized for high linearity, high dynamic range, and low output-noise performance, making this component ideal for ultrasound imaging applications. The VGA paths also exhibit a channel-to-channel crosstalk of -80dB at 10MHz and an absolute gain error of less than ±0.5dB for minimal channel-to-channel focusing error in an ultrasound system. Each VGA path includes circuitry for adjusting analog gain, an output buffer with differential output ports (VGOUT_+, VGOUT_-) for driving ADCs, and differential input ports (VGIN_+, VGIN_-), which are ideal for directly interfacing to the MAX2034 quad LNA. See the *High-Level Wave Mixer and Programmable Beamformer Functional Diagram* for details.

High-Level Wave Mixer and Programmable Beamformer Functional Diagram



The VGA has an adjustable gain range from -10.5dB to +39.5dB, achieving a total dynamic range of 50dB (typ). The VGA gain can be adjusted using the differential gain-control inputs VG_CTL+ and VG_CTL-. Set the differential gain-control input voltage at +2V for minimum gain and -2V for maximum gain. The differential analog control common-mode voltage is 3V (typ).

Ultrasound VGA Integrated with CW Octal Mixer

VGA Clamp

A clamp is provided to limit the VGA output signals to avoid overdriving the ADC or to prevent ADC saturation. Set VG_CLAMP_MODE low to clamp the VGA differential outputs at $2.2V_{P-P}$. Set the VG_CLAMP_MODE high to disable the clamp.

Power-Down

The device can also be powered down with PD. Set PD to logic-high for power-down mode. In power-down mode, the device draws a total supply current of 27mA. Set PD to a logic-low for normal operation

Overload Recovery

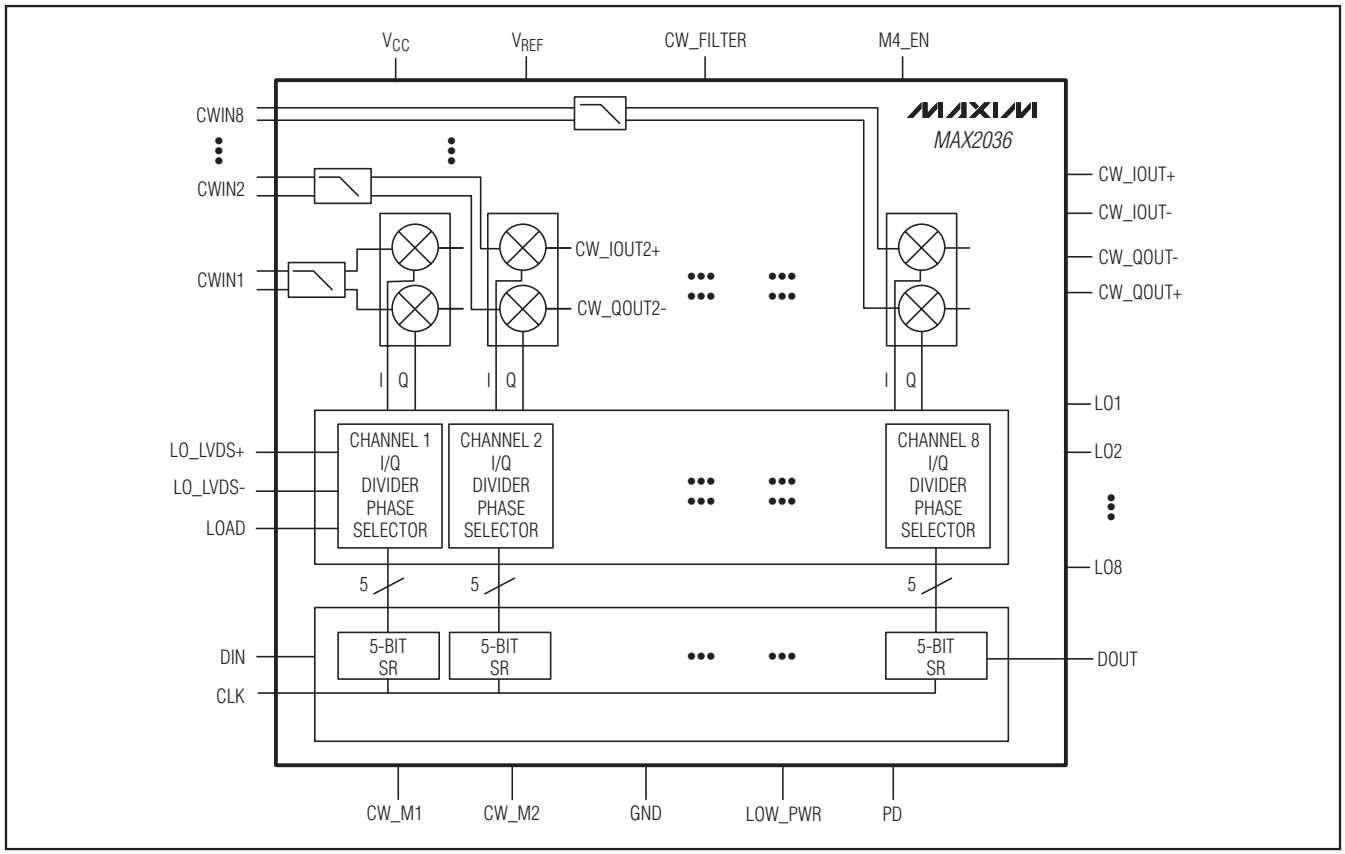
The device is also optimized for quick overload recovery for operation under the large input-signal conditions that are typically found in ultrasound input buffer imaging applications. See the *Typical Operating Characteristics* for an illustration of the rapid recovery time from a transmit-related overload.

Octal Continuous Wave (CW) Mixer

The MAX2036 CW mixers are designed using an active double-balanced topology. The mixers achieve high dynamic range and high-linearity performance, with exceptionally low noise, which is ideal for ultrasound CWD signal reception. The octal quadrature mixer array provides noise performance of -155dBc/Hz at 1kHz from a 1.25MHz carrier, and a two-tone, third-order, ultrasound-specific intermodulation product of typically -50dBc. See the *Ultrasound-Specific IMD3 Specification* in the *Applications Information* section.

The octal array exhibits quadrature and in-phase differential current outputs (CW_QOUT+, CW_QOUT-, CW_IOUT+, CW_IOUT-) to produce the total CWD beamformed signal. The maximum differential current output is typically $3mA_{P-P}$ and the mixer output-compliance voltage ranges from 4.75V to 12V.

High-Level CW Mixer and Programmable Beamformer Functional Diagram



Ultrasound VGA Integrated with CW Octal Mixer

CW Mixer Output Summation

The outputs from the octal mixer array are summed internally to produce the total CWD summed beamformed signal. The octal array produces eight differential quadrature (Q) outputs and eight differential in-phase (I) outputs. All quadrature and in-phase outputs are summed into single I and Q differential current outputs (CW_QOUT+, CW_QOUT-, CW_IOUT+, CW_IOUT-).

LO Phase Select

The LO phase dividers can be programmed through the shift registers to allow for 4, 8, or 16 quadrature phases for a complete CW beamforming solution.

CWD Beamforming Modes

There are four separate modes of operating the CWD beamformer. See Table 1 for a summary of the different modes of operation. The mode of operation can be selected by the CW_M1 and CW_M2 logic inputs. Phase generation is controlled through the serial interface. See the *Serial Interface* section in the *Applications Information* section for details on how to program for different quadrature phases.

Mode 1

For mode 1 operation, the LO_LVDS input frequency is typically 16 x f_{LO}. As the CWD LO frequency range is 1MHz to 7.5MHz, the input frequency ranges from 16MHz to 120MHz. This high LO clock frequency requires a differential LVDS input. The 16 x f_{LO} input is then divided by 16 to produce 16 phases. These 16 phases are generated for each of the 8 channels and programmed for the selected phase by a serial shift register. Each channel has a corresponding 5-bit shift register, which is used to program the output phase of the divide-by-16 circuit. The first 4 bits of the shift register are for programming the 16 phases; the fifth bit turns each channel on/off individually. For mode 1, set both CW_M1 and CW_M2 to a logic-low. See Table 2.

Table 2. Mode 1 Logic Table (B4 = 0: Channel On/B4 = 1 Channel Off)

MODE 1 CW_M1 = 0 CW_M2 = 0	MSB			LSB	SHUTDOWN
PHASE (DEG)	D	C	B	A	SD
	(B0)	(B1)	(B2)	(B3)	(B4)
0	0	0	0	0	0/1
22.5	0	0	0	1	0/1
45	0	0	1	0	0/1
67.5	0	0	1	1	0/1
90	0	1	0	0	0/1
112.5	0	1	0	1	0/1
135	0	1	1	0	0/1
157.5	0	1	1	1	0/1
180	1	0	0	0	0/1
202.5	1	0	0	1	0/1
225	1	0	1	0	0/1
247.5	1	0	1	1	0/1
270	1	1	0	0	0/1
292.5	1	1	0	1	0/1
315	1	1	1	0	0/1
337.5	1	1	1	1	0/1

Table 1. Summary of CWD Beamforming Methods

CW_M1	CW_M2	MODE	LO INPUT FREQUENCY	CLOCK INTERFACE	PHASE RESOLUTION	NO. OF CLOCK INPUTS PER CHIP	PROGRAM BY SERIAL SHIFT REGISTER (SSR)	NO. OF USEFUL BITS IN SSR	NO. OF DON'T-CARE BITS IN SSR
0	0	1	16 x	LVDS	16 phases	1	Yes	4	0
0	1	2	8 x	LVDS	8 phases	1	Yes	3	1 MSB
1	0	3	4 x	3V CMOS	4 phases	8	Yes	2	2 MSBs
1	1	4	4 x	3V CMOS	Quadrature provided	8	No	N/A	N/A

N/A = Not applicable.

Mode 2

The LO_LVDS input frequency is 8 x f_{LO} (typ) for mode 2 operation. The CWD LO frequency range is 1MHz to 7.5MHz, and the input frequency ranges from 8MHz to 60MHz. This high LO clock frequency requires a differential LVDS input. The 8 x f_{LO} input is then divided by 8 to produce 8 phases. These 8 phases are generated for each of the 8 channels and programmed for the selected phase by the serial shift register. Note that the serial shift register is common to modes 1, 2, and 3, where each channel has a corresponding 5-bit shift register, which is used to program the output phase. However, since mode 2 generates 8 phases only, 3 of the 4 phase-programming bits are used; 5 bits are still loaded per channel using the serial shift register, but the phase-programming MSB is a don't-care bit. The fifth bit in the shift register always turns each channel on/off individually. For mode 2, set CW_M1 to a logic-low and set CW_M2 to a logic-high. See Table 3.

Table 3. Mode 2 Logic Table (DC = Don't Care, B4 = 0: Channel On/B4 = 1: Channel Off)

MODE 2 CW_M1 = 0 CW_M2 = 1					SHUTDOWN
PHASE (DEG)	D	C	B	A	SD
	(B0)	(B1)	(B2)	(B3)	(B4)
0	DC	0	0	0	0/1
45	DC	0	0	1	0/1
90	DC	0	1	0	0/1
135	DC	0	1	1	0/1
180	DC	1	0	0	0/1
225	DC	1	0	1	0/1
270	DC	1	1	0	0/1
315	DC	1	1	1	0/1

Mode 3

The LO_LVDS input is not used in this mode. Separate 4 x f_{LO} clock inputs are provided using LO1–LO8 for each channel. The CWD LO frequency range is 1MHz to 7.5MHz, and the input frequency provides ranges from 4MHz to 30MHz. Note that the LO clock frequency can utilize 3V CMOS inputs. The 4 x f_{LO} LO1–LO8 inputs are divided by 4 to produce 4 phases. These 4 phases are generated for each of the 8 channels and programmed for the selected phase by the serial shift register. For mode 3, 4 phases are generated, and only 2 of the 4 phase-programming bits are required where the 2-phase programming MSBs are don't-care bits. For mode 3, set CW_M1 to a logic-high and set CW_M2 to a logic-low. See Table 4.

Table 4. Mode 3 Logic Table (DC = Don't Care, B4 = 0: Channel On/B4 = 1: Channel Off)

MODE 3 CW_M1 = 1 CW_M2 = 0					SHUTDOWN
PHASE (DEG)	D	C	B	A	SD
	(B0)	(B1)	(B2)	(B3)	(B4)
0	DC	DC	0	0	0/1
90	DC	DC	0	1	0/1
180	DC	DC	1	0	0/1
270	DC	DC	1	1	0/1

Mode 4

The LO_LVDS input is not used in this mode. The appropriate phases are externally provided using separate 4 x f_{LO} LO1–LO8 inputs for each channel. A 4 x f_{LO} input is required so the device can internally generate accurate duty-cycle independent quadrature LO drives. Note that the serial shift register is not used in this mode. The CWD LO frequency range is 1MHz to 7.5MHz and the input frequency ranges from 4MHz to 30MHz. The appropriate inputs are provided at LO1 to LO8. A reset line is provided to the customer so that all the CWD channels can be synchronized. The reset line is implemented through the RESET. For mode 4, set both CW_M1 and CW_M2 to logic-high. See Table 5.

Table 5. Mode 4 Logic Table

MODE 4 CW_M1 = 1 CW_M2 = 1					SHUTDOWN
PHASE (DEG)	D	C	B	A	SD
	(B0)	(B1)	(B2)	(B3)	(B4)
Serial bus not used in mode 4	N/A	N/A	N/A	N/A	N/A

N/A = Not applicable.

Ultrasound VGA Integrated with CW Octal Mixer

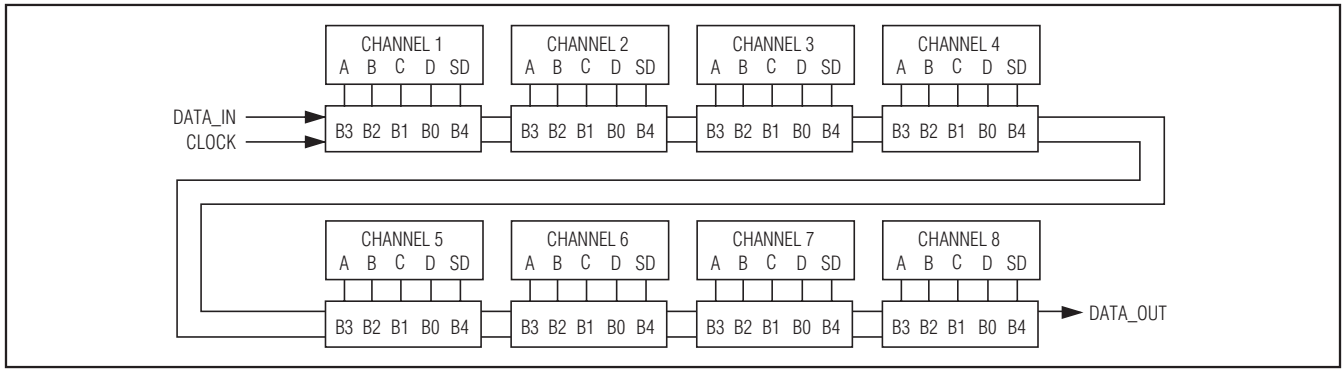


Figure 1. Data Flow of Serial Shift Register

Synchronization

Figure 1 illustrates the serial programming of the 8 individual channels through the serial data port. Note that the serial data can be daisy chained from one part to another, allowing a single data line to be used to program multiple chips in the system.

CW Lowpass Filter

The MAX2036 also includes selectable lowpass filters between each CW differential input pair and corresponding mixer input. Shunt capacitors and resistors are integrated on chip for high band and low band. The parallel capacitor/resistor networks, which appear differentially across each of the CW differential inputs, are selectable through the CW_FILTER. Drive CW_FILTER high to set the corner frequency of the filter to be f_C = 9.5MHz. Drive CW_FILTER low to set the corner frequency equal to f_C = 4.5MHz. The CW_VG allows the filter inputs to be disconnected from input nodes (internal to chip) to prevent overloading the LNA output and to not change the VGA input common-mode voltage.

VGA and CW Mixer Operation

During normal operation, the MAX2036 is configured such that either the VGA path is enabled while the mixer array is powered down (VGA mode), or the quadrature mixer array is enabled while the VGA path is powered down (CW mode). During VGA mode, besides powering down the CW mixer array, the differential inputs to the lowpass filters and CW mixers also are internally disconnected from the input nodes, making the CW differential inputs (CWIN_+, CWIN_-) high impedance. The CW mode disconnects the VGA inputs internally from the input ports of the device. For VGA mode, set CW_VG to a logic-high, while for CW mode, set CW_VG to a logic-low.

Power-Down and Low-Power Modes

During device power-down, both the VGA and CW mixer are disabled regardless of the logic set at CW_VG. Both the VGA and CW mixer inputs are high impedance since the internal switches to the inputs are all disconnected. The total supply current of the device reduces to 27mA. Set PD to a logic-high for device power-down.

A low-power mode is available to lower the required power for CWD operation. When selected, the complex mixers operate at lower quiescent currents and the total per-channel current is lowered to 53mA. Note that operation in this mode slightly reduces the dynamic performance of the device. Table 6 shows the logic function of standard operating modes.

Table 6. Logic Function of Standard Operating Modes

PD INPUT	CW_VG INPUT	LOW_PWR	VGA	CW MIXER	INTERNAL SWITCH TO VGA	INTERNAL SWITCH TO LPF AND CW	5V V_{CC} CURRENT CONSUMPTION (mA)	11V V_{MIX} CURRENT CONSUMPTION (mA)
1	1	N/A	Off	Off	Off	Off	27	0
1	0	N/A	Off	Off	Off	Off	27	0
0	0	0	Off	On	Off	On	245	106
0	0	1	Off	On	Off	On	245	53
0	1	N/A	On	Off	On	Off	204	0

N/A = Not applicable.

Applications Information

Mode Select Response Time

The mode select response time is the time that the device takes to switch between CW and VGA modes. One possible approach to interfacing the CW outputs to an instrumentation amplifier used to drive an ADC is shown in Figure 2. In this implementation, there are four large-value (in the range of 470nF to 1µF) capacitors between each of the CW_IOUT+, CW_IOUT-, CW_QOUT+, CW_QOUT- outputs and the circuitry they are driving. The output of the CW mixer usually drives the input of an instrumentation amplifier made up of op amps whose input impedance is set by common-mode setting resistors.

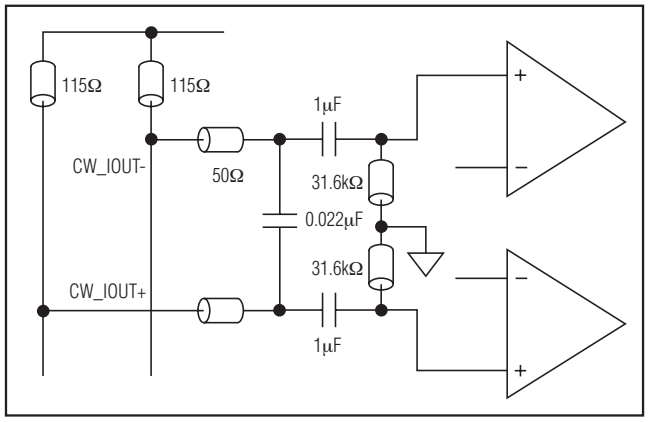


Figure 2. Typical Example of a CW Mixer's Output Circuit

There are clearly both a highpass corner and a lowpass corner present in this output network. The lowpass corner is set primarily by the 115Ω mixer pullup resistors, the series 50Ω resistors, and the shunt 0.022µF capacitor. This lowpass corner is used to filter a combination of LO leakage and upper sideband. The highpass corner, however, is of a larger concern due to the fact that it is dominated by the combination of a 1µF DC blocking capacitor and the pair of shunt 31.6kΩ resistors.

If drawn, the simplified dominant highpass network would look like Figure 3.

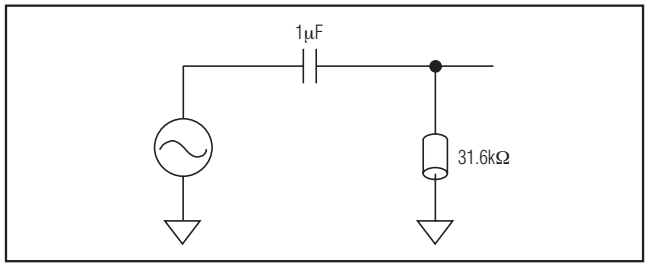


Figure 3. Simplified Circuit of Highpass Pole

The highpass pole in this case is at f_P = 1/(2 x pi x RC) ~ 5Hz. Note that this low highpass corner frequency is required in order to filter the downconverted clutter tone, which appears at DC, but not interfere with CWD imaging at frequencies as low as 400Hz. For example, if one wanted to use CWD down to 400Hz, then a good choice for the highpass pole would be at least a decade below this (< 40Hz) as not to incur rolloff due to pole. Remember, if the highpass pole is set to 400Hz, the response is 3dB down at that corner frequency. The placement of the highpass pole at 5Hz in the above example is between the DC and 40Hz limitations just discussed.

The bottom line is that any reasonably sized DC block between the output of the mixer and the instrumentation amplifier pose a significant time constant that slows the mode select switching speed.

An alternative solution to the approach in Figure 2, which enables faster mode select response time, is shown in Figure 4.

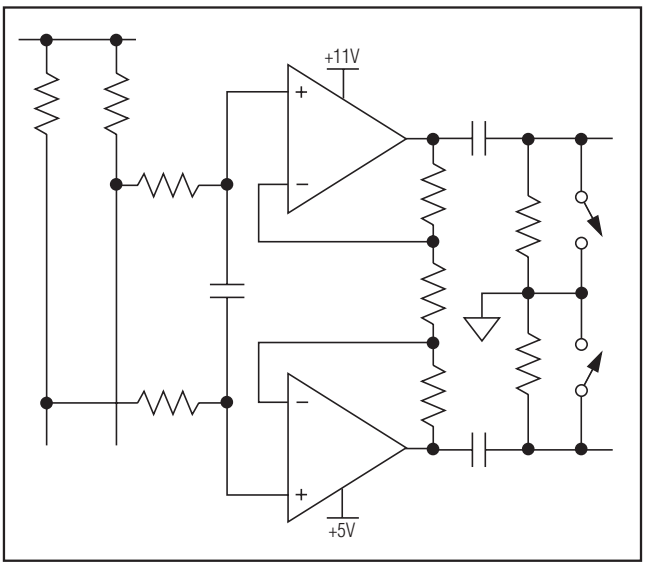


Figure 4. Improved Mode Select Response Time Achieved with DC-Coupled Input to Instrumentation Amplifier

In Figure 4, the outputs of the CWD mixers are DC-coupled into the inputs of the instrumentation amplifiers. Therefore, the op amps must be able to accommodate the full compliance range of the mixer outputs, which is a maximum of +11V when the mixers are disabled, down to the +5V supply of the MAX2036 when the mixers are enabled. The op amps can be powered from +11V for the high rail and +5V for the low rail, requiring a 6V op amp.

Ultrasound VGA Integrated with CW Octal Mixer

Serial Interface

The serial interface of the MAX2036 programs the LO for 16, 8, or 4 quadrature phases using a serial shift register implementation. Data is shifted into the device on DIN. The serial shift register clock is applied to the CLK input. The serial shift register has 5 bits per channel. The first 4 bits are for phase programming, and the fifth bit enables or disables each channel of the mixer array.

Each mixer can be programmed to 1 of 16 phases; therefore, 4 bits are required for each channel for programming. The master high-frequency mixer clock is applied to differential inputs LO_LVDS+ and LO_LVDS- (for modes 1 and 2) and LO_ (for modes 3 and 4). The LOAD input is provided to allow the user to load the phase counters with the programming values to generate the correct LO phases. The input signals for mixing are applied to the eight differential inputs, CWIN_+ and CWIN_-. The summed I/Q baseband differential outputs are provided on CW_IOUT+/- and CW_QOUT+/-. CW_M1 and CW_M2 are used to select one of the four possible modes of operation. See Table 1.

The serial interface is designed to allow multiple devices to be easily daisy chained in order to minimize program interface wiring. DOUT is available for this daisy-chain function.

Programming the Beamformer

During normal CWD operation, the mixer clock at LO_ or LO_LVDS± is on and the programming signals on DIN, CLK, and LOAD are off. (LOAD = high, CLK = low, and DIN = don't care, but fixed to a high or low). To start the programming sequence, turn off the mixer clock. Data is shifted into the shift register at a recommended 10MHz programming rate or 100ns minimum data clock period/time. See Figure 5 for timing details.

After the shift registers are programmed, pull the LOAD bus to logic-low and then back to logic-high to load the internal counters into I/Q phase divider/selectors with the proper values. LOAD must remain low for a minimum time of t_{CLH}. The user turns on the mixer clock to start beamforming. The clock must turn on such that it starts at the beginning of a mixer clock cycle.

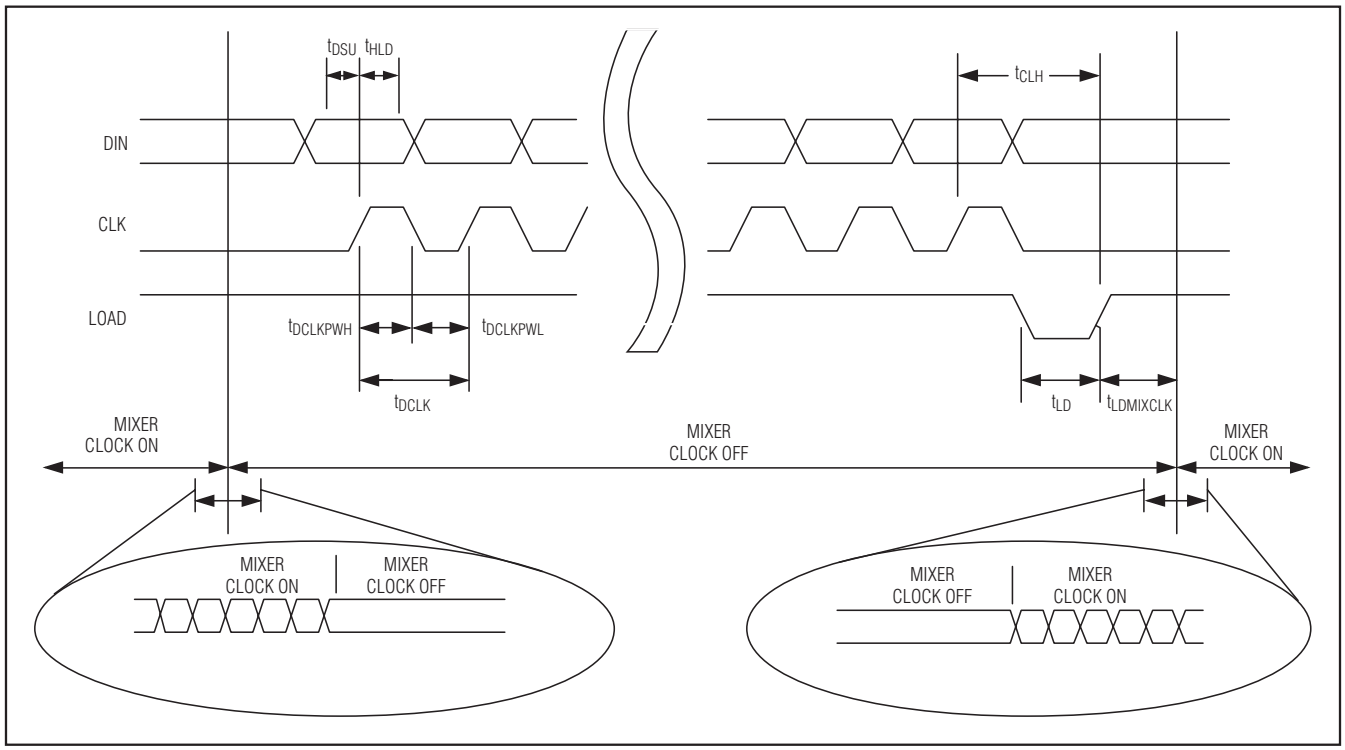


Figure 5. Shift Register Timing Diagram

CW Mixer Output Summation

The maximum differential current output is typically $3mA_{P-P}$ and the mixer output compliance voltage ranges from 4.75V to 12V per mixer channel. The mixer common-mode current in each of the differential mixer outputs is typically 3.25mA. The total summed current would equal N x 3.25mA in each of the 115Ω load resistors (where N = number of channels). In this case, the quiescent output voltage at $+V_{SUM}$ and $-V_{SUM}$ outputs would be +11V - (N x 3.25mA x 115) = +11V - (8 x 3.25mA x 115) = 8.05V. The voltage swing at each output, with one channel driven at max output current (differential $3mA_{P-P}$) while the other channels are not driven, would be $1.5mA_{P-P}$ x 115Ω or $174mV_{P-P}$ and the differential voltage would be $348mV_{P-P}$. The voltage compliance range is defined as the valid range for $+V_{SUM}$ and $-V_{SUM}$ in this example.

External Compensation

External compensation is required for bypassing internal biasing circuitry. Connect, as close as possible, individual 4.7µF capacitors from each pin EXT_C1, EXT_C2, and EXT_C3 (pins 13, 14, 15) to ground.

External Bias Resistor

An external resistor at EXT_RES is required to set the bias for the internal biasing circuitry. Connect, as close as possible, a 7.5kΩ (0.1%) resistor from EXT_RES (pin 38) to ground.

Analog Input and Output Coupling

In typical applications, the MAX2036 is being driven from a low-noise amplifier (such as the MAX2034) and the VGA is typically driving a discrete differential antialias filter into an ADC (such as the MAX1436 octal ADC). The differential input impedance of the MAX2036 is typically 240Ω. The differential outputs of the VGA are capable of driving a differential load capacitance to GND at each of the VGA differential outputs of 60pF, and differential capacitance across the VGA outputs is 10pF, R_L = 1kΩ. The differential outputs have a common-mode bias of approximately 3.75V. AC-couple these differential outputs if the next stage has a different common-mode input range.

Ultrasound-Specific IMD3 Specification

Unlike typical communications specs, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, f_1 represents reflections from tissue and f_2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude, and hence the measurement is defined with one input tone 25dB lower than the other. The IMD3 product of interest ($f_1 - (f_2 - f_1)$) presents itself as an undesired Doppler error signal in ultrasound applications. See Figure 6.

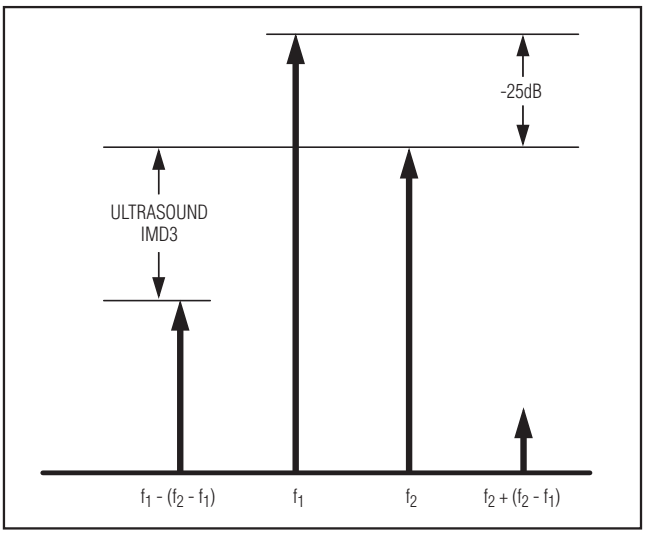


Figure 6. Ultrasound IMD3 Measurement Technique

PCB Layout

The pin configuration of the MAX2036 is optimized to facilitate a very compact physical layout of the device and its associated discrete components. A typical application for this device might incorporate several devices in close proximity to handle multiple channels of signal processing.

The exposed pad (EP) of the MAX2036's TQFP-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX2036 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Ultrasound VGA Integrated with CW Octal Mixer

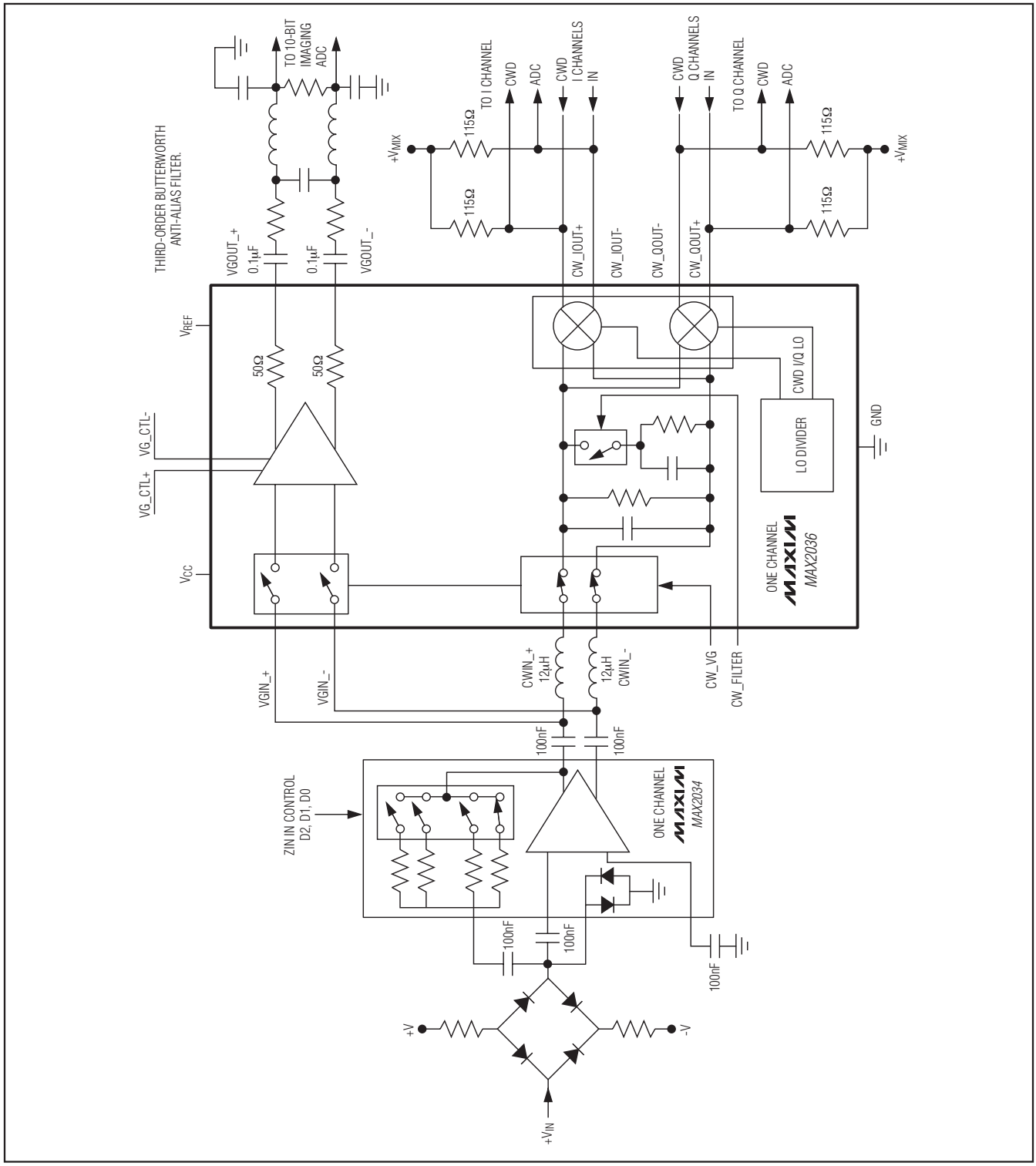
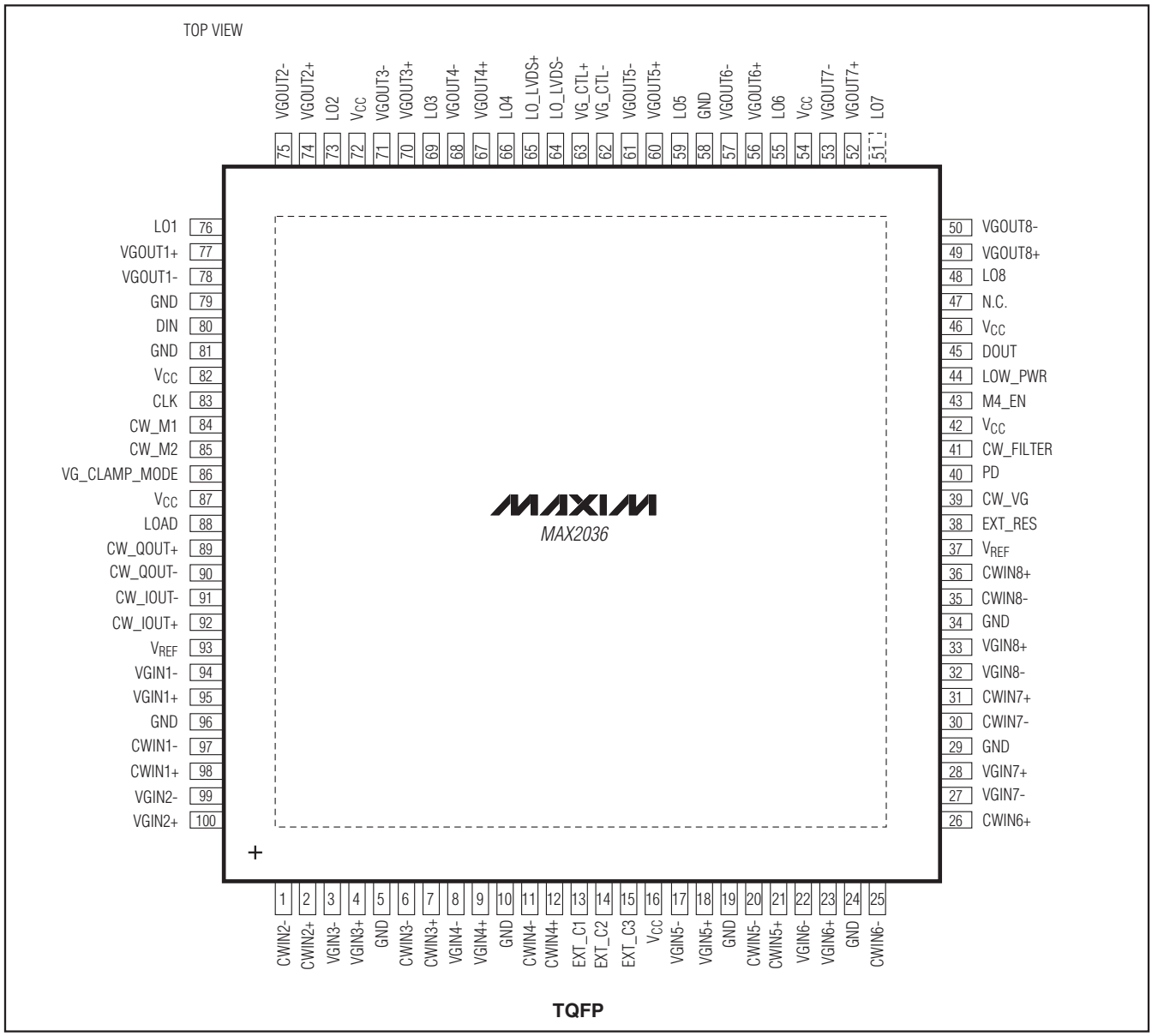


Figure 7. Typical per-Channel Ultrasound Imaging Application

Pin Configuration



TQFP

Ultrasound VGA Integrated with CW Octal Mixer

Chip Information

PROCESS: Silicon Complementary Bipolar

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
100 TQFP-EP	C100E+3	**21-0116**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/09	Initial release	—
1	6/09	Corrected pin name inconsistencies	1–6, 10, 12, 13, 18, 20

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